

FEATURES

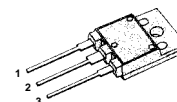
- ❑ Logic-Level Gate Drive
- ❑ Avalanche Rugged Technology
- ❑ Rugged Gate Oxide Technology
- ❑ Lower Input Capacitances
- ❑ Improved Gate Charge
- ❑ Extended Safe Operating Area
- ❑ Lower Leakage Current : 10uA (Max.) @ $V_{DS}=-200V$
- ❑ Lower $R_{DS(ON)}$: 0.175 Ω (Typ.)

$$BV_{DSS} = -200 V$$

$$R_{DS(on)} = 0.23 \Omega$$

$$I_D = -12.6 A$$

TO-3PF



1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	-200	V
I_D	Continuous Drain Current ($T_C=25^\circ C$)	-12.6	A
	Continuous Drain Current ($T_C=100^\circ C$)	-7.9	
I_{DM}	Drain Current-Pulsed ^①	-50.4	A
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy ^②	990	mJ
I_{AR}	Avalanche Current ^①	-12.6	A
E_{AR}	Repetitive Avalanche Energy ^①	20.4	mJ
dv/dt	Peak Diode Recovery dv/dt ^③	-5.0	V/ns
P_D	Total Power Dissipation ($T_C=25^\circ C$)	90	W
	Linear Derating Factor	0.72	
T_J, T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	0.61	$^\circ C / W$
$R_{\theta JA}$	Junction-to-Ambient	--	40	

Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV _{DSS}	Drain-Source Breakdown Voltage	-200	--	--	V	V _{GS} =0V, I _D =-250μA
ΔBV/ΔT _J	Breakdown Voltage Temp. Coeff.	--	-0.17	--	V/°C	I _D =-250μA See Fig 7
V _{GS(th)}	Gate Threshold Voltage	-1.0	--	-2.0	V	V _{DS} =-5V, I _D =-250μA
I _{GSS}	Gate-Source Leakage, Forward	--	--	100	nA	V _{GS} =-20V
	Gate-Source Leakage, Reverse	--	--	-100		V _{GS} =20V
I _{DSS}	Drain-to-Source Leakage Current	--	--	10	μA	V _{DS} =-200V
		--	--	100		V _{DS} =-160V, T _C =125 °C
R _{DS(on)}	Static Drain-Source On-State Resistance	--	.175	0.23	Ω	V _{GS} =-5V, I _D =-6.3A ④
g _{fs}	Forward Transconductance	--	13	--	S	V _{DS} =-40V, I _D =-6.3A ④
C _{iss}	Input Capacitance	--	2500	3250	pF	V _{GS} =0V, V _{DS} =-25V, f=1MHz See Fig 5
C _{oss}	Output Capacitance	--	400	520		
C _{rss}	Reverse Transfer Capacitance	--	210	270		
t _{d(on)}	Turn-On Delay Time	--	20	50	ns	V _{DD} =-100V, I _D =-12.6A, R _G =6.2Ω See Fig 13 ④ ⑤
t _r	Rise Time	--	150	310		
t _{d(off)}	Turn-Off Delay Time	--	100	210		
t _f	Fall Time	--	65	140		
Q _g	Total Gate Charge	--	90	120	nC	V _{DS} =-160V, V _{GS} =-5V, I _D =-12.6A See Fig 6 & Fig 12 ④ ⑤
Q _{gs}	Gate-Source Charge	--	12	--		
Q _{gd}	Gate-Drain(Miller) Charge	--	54	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I _S	Continuous Source Current	--	--	-12.6	A	Integral reverse pn-diode in the MOSFET
I _{SM}	Pulsed-Source Current ①	--	--	-50.4		
V _{SD}	Diode Forward Voltage ④	--	--	-1.5	V	T _J =25 °C, I _S =-12.6A, V _{GS} =0V
t _{rr}	Reverse Recovery Time	--	260	--	ns	T _J =25 °C, I _F =-19.5A, V _{DD} =-160V
Q _{rr}	Reverse Recovery Charge	--	2.8	--	μC	di _F /dt=100A/μs ④

Notes ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② L=3.9mH, I_{AS}=-19.5A, V_{DD}=-50V, R_G=27Ω, Starting T_J=25 °C
- ③ I_{SD}≤-19.5A, di/dt≤500A/μs, V_{DD}≤BV_{DSS}, Starting T_J=25 °C
- ④ Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%
- ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

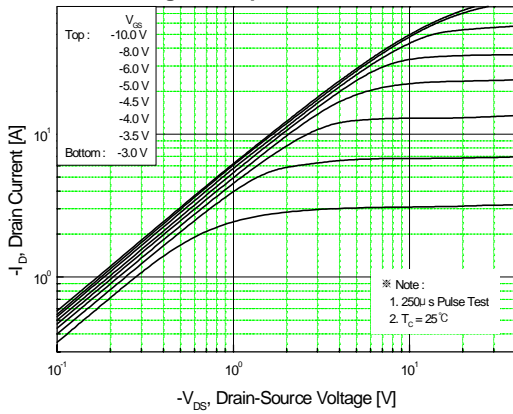


Fig 2. Transfer Characteristics

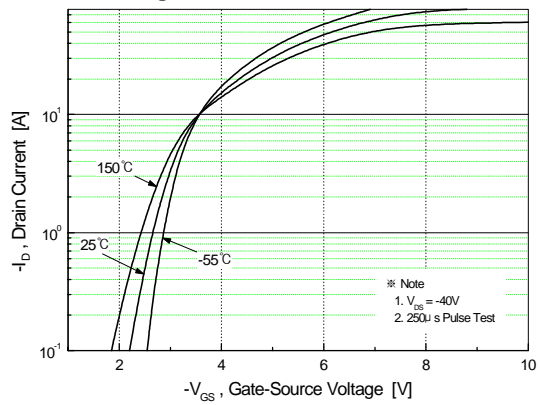


Fig 3. On-Resistance vs. Drain Current

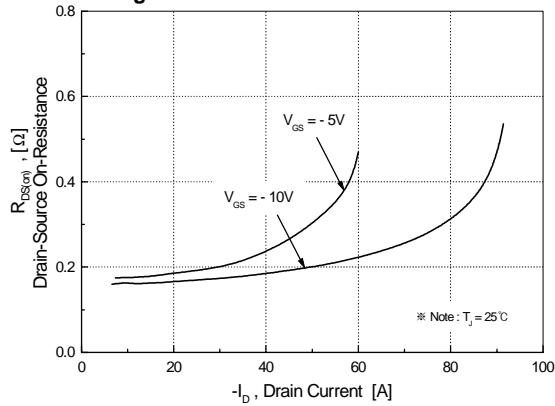


Fig 4. Source-Drain Diode Forward Voltage

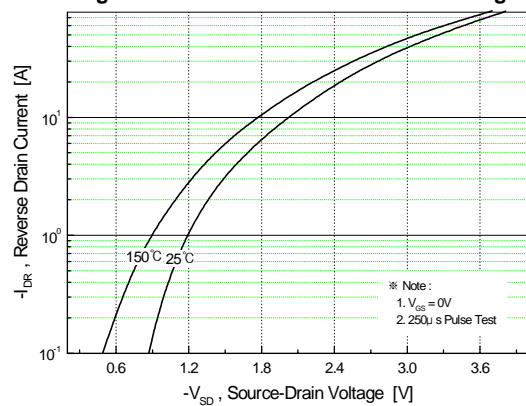


Fig 5. Capacitance vs. Drain-Source Voltage

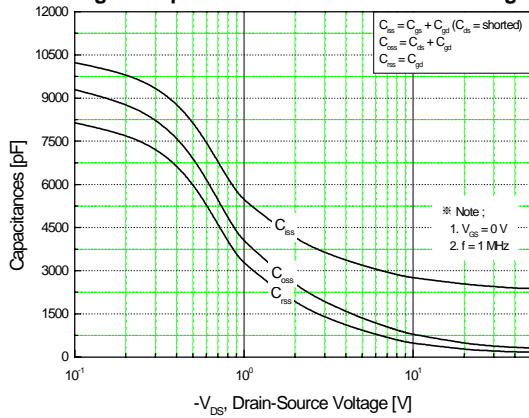


Fig 6. Gate Charge vs. Gate-Source Voltage

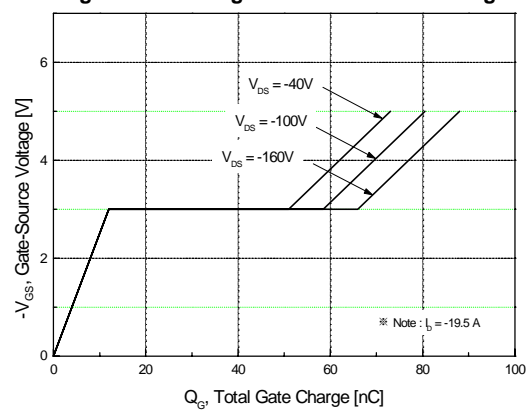


Fig 7. Breakdown Voltage vs. Temperature

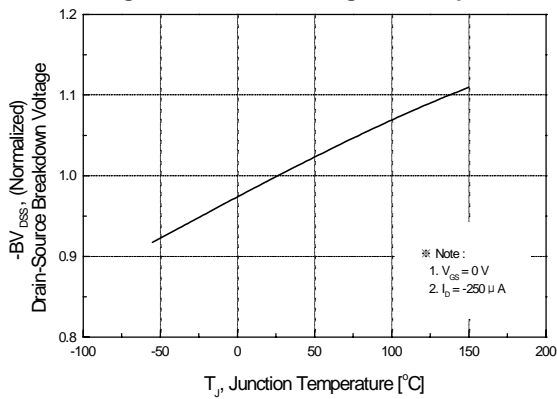


Fig 8. On-Resistance vs. Temperature

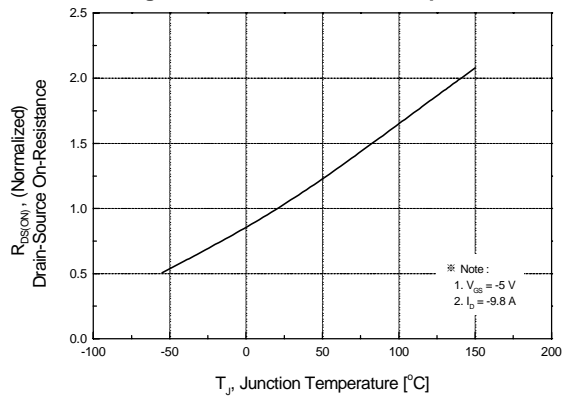


Fig 9. Max. Safe Operating Area

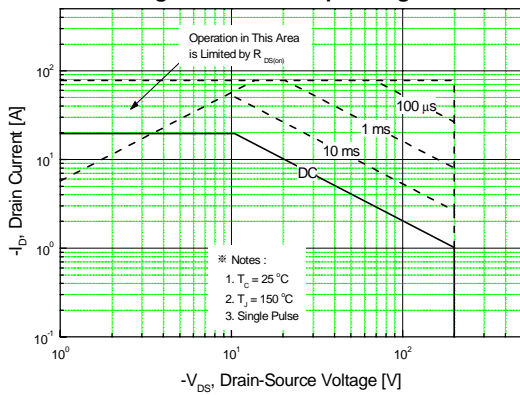


Fig 10. Max. Drain Current vs. Case Temperature

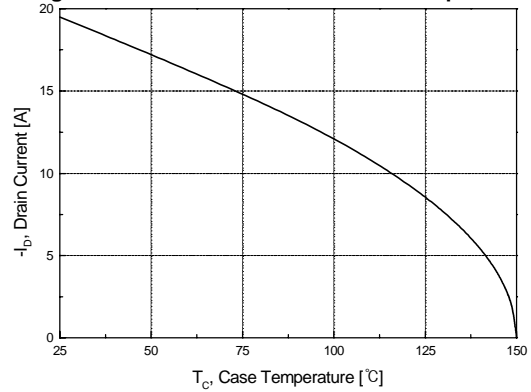


Fig 11. Thermal Response

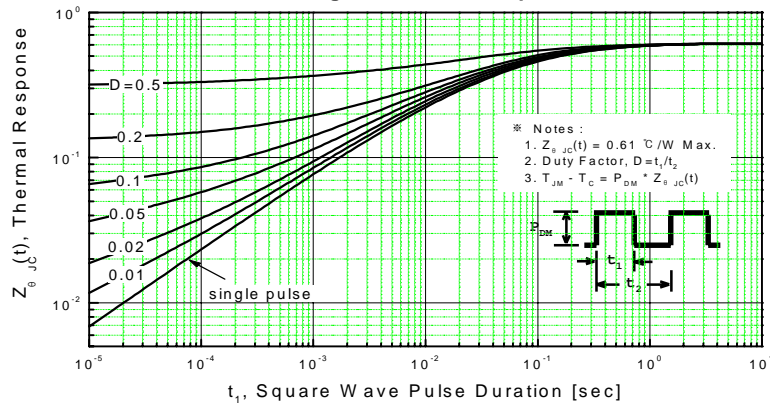


Fig 12. Gate Charge Test Circuit & Waveform

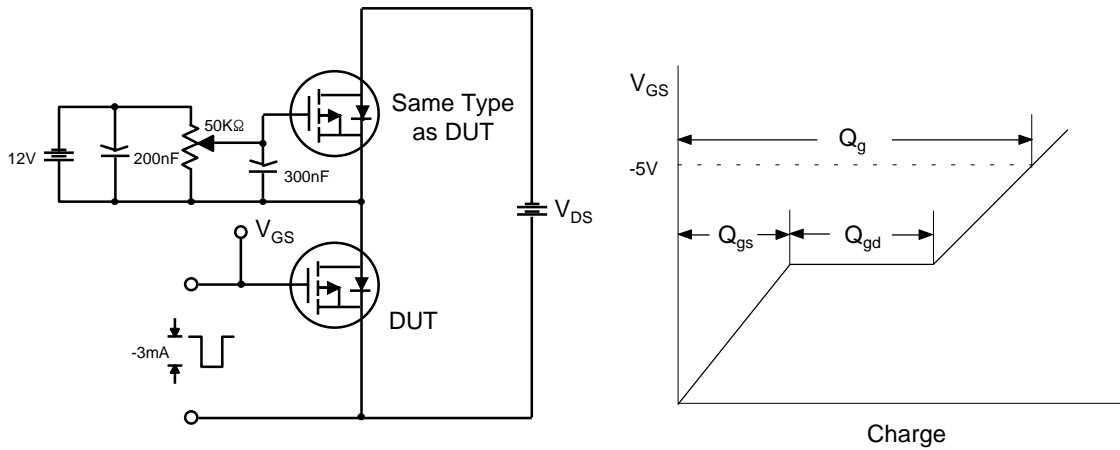


Fig 13. Resistive Switching Test Circuit & Waveforms

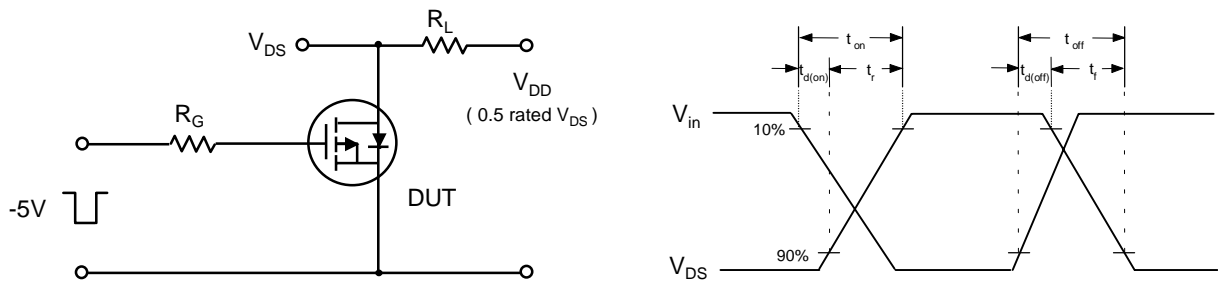


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

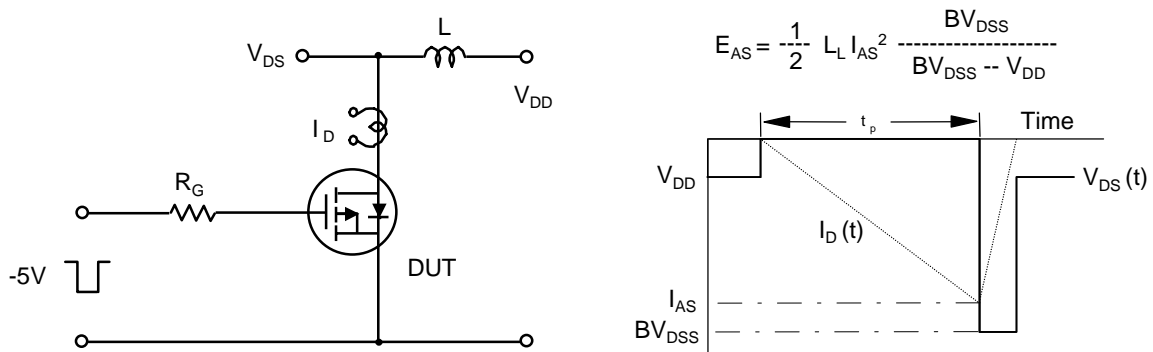
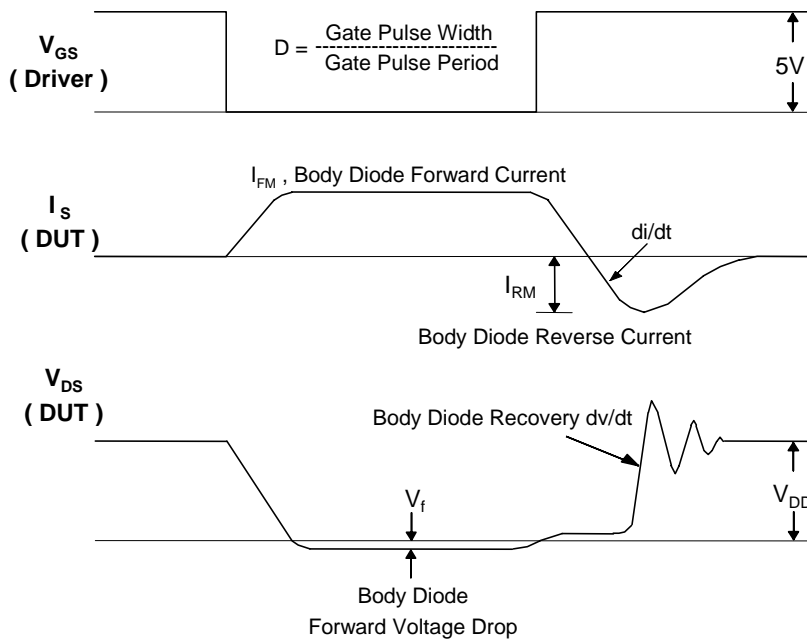
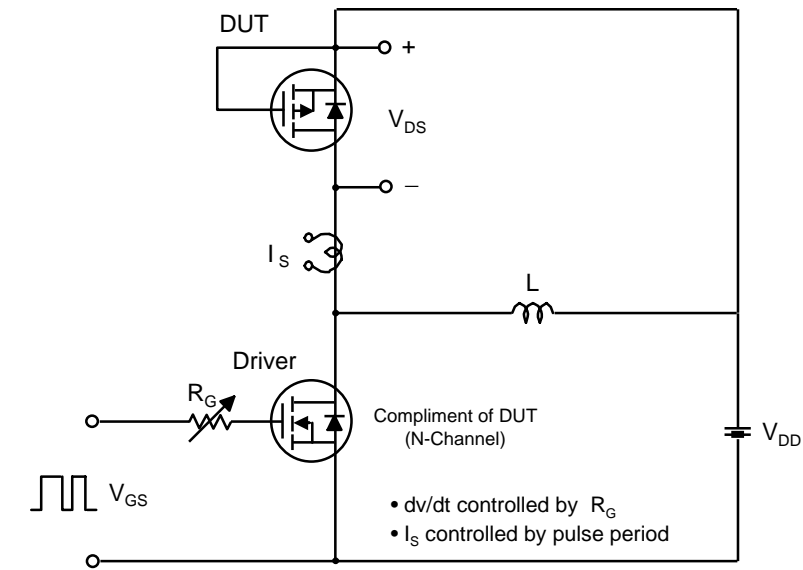


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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