EVB72013

433MHz FSK/ASK Transmitter

Evaluation Board Description

1. Features

- Frequency range from 425 MHz to 445 MHz
- Fully integrated PLL-stabilized VCO
- Single-ended RF output
- FSK via crystal pulling
- Wideband FSK deviation possible
- ASK/OOK via power amplifier modulation
- Wide power supply range from 1.95 V to 5.5 V
- Very low standby current
- Low voltage detector
- High over-all frequency accuracy
- FSK deviation and center frequency independently adjustable
- Data rates from DC to 40 kbps
- Adjustable output power range from -14 dBm to +11 dBm
- Adjustable current consumption from 3.8 mA to 16.8 mA
- Conforms to EN 300 220 and similar standards
- 8-pin Small Outline Integrated Circuit (SOIC)

2. Application Examples

- RF remote controls
- Automatic meter reading (AMR)
- Tire pressure monitoring systems (TPMS)
- Remote keyless entry (RKE)
- Alarm and security systems
- Garage door openers
- Home automation

3. Evaluation board example

4. Ordering information

Part No. (see paragraph 5)

EVB72013-433-FSK-C

Note: EVB default population is FSK, ASK modification according to section 3.1.

5. General Description

The MLX72013 evaluation board is designed to demonstrate the performance of the transmitter IC for conductive measurements. The power amplifier is matched to 50 Ohms by means of a π-matching network to operate at a resonant frequency of 433 MHz.

6. Contents

7. Theory of Operation

7.1. General

As depicted in Fig.1, the MLX72013 transmitter consists of a fully integrated voltage-controlled oscillator (VCO), a divide-by-16 divider (div16), a phase-frequency detector (PFD) and a charge pump (CP). An internal loop filter determines the dynamic behavior of the PLL and suppresses reference spurious signals. A Colpitts crystal oscillator (XOSC) is used as the reference oscillator of a phase-locked loop (PLL) synthesizer. The VCO's output signal feeds the power amplifier (PA). The RF signal power P_{out} can be adjusted in four steps from P_{out} = –14 dBm to +11 dBm, either by changing the value of resistor RPS or by varying the voltage V_{PS} at pin PSEL. The open-collector output (OUT) can be used either to directly drive a loop antenna or to be matched to a 50Ohm load. Bandgap biasing ensures stable operation of the IC at a power supply range of 1.95 V to 5.5 V.

7.2. Block Diagram

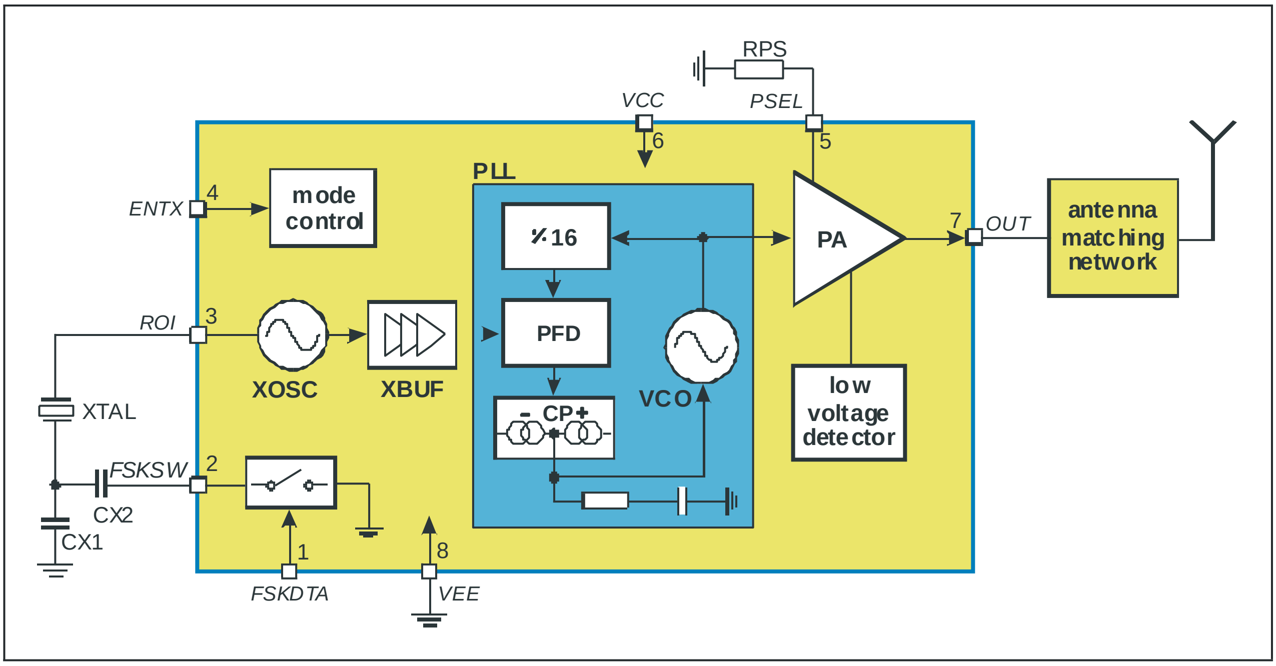


Fig. 1: Block diagram with external components

8. Functional Description

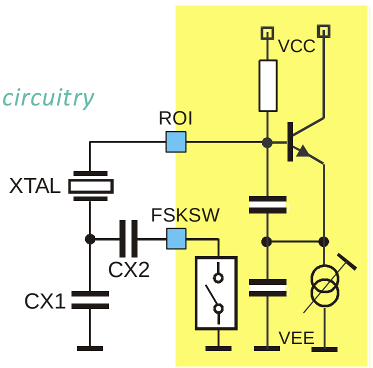
8.1. Crystal Oscillator

A Colpitts crystal oscillator with integrated functional capacitors is used as the reference oscillator for the PLL synthesizer. The equivalent input capacitance CRO offered by the crystal oscillator input pin ROI is about 18pF. The crystal oscillator is provided with an amplitude control loop in order to have a very stable frequency over the specified supply voltage and temperature range in combination with a short start-up time.

8.2. FSK Modulation

FSK modulation can be achieved by pulling the crystal oscillator frequency. A CMOS-compatible data stream applied at the pin FSKDTA digitally modulates the XOSC via an integrated NMOS switch. Two external pulling capacitors CX1 and CX2 allow the FSK deviation Δf and the center frequency f_c to be adjusted independently. At FSKDTA = 0, CX2 is connected in parallel to CX1 leading to the low-frequency component of the FSK spectrum (f_{min}); while at FSKDTA = 1, CX2 is deactivated and the XOSC is set to its high frequency f_{max}.
An external reference signal can be directly AC-coupled to the reference oscillator input pin ROI. Then the transmitter is used without a crystal. Now the reference signal sets the carrier frequency and may also contain the FSK (or FM) modulation.

Fig. 2: Crystal pulling circuitry



FSKDTA	Description
0	$f_{min} = f_c - \Delta f$ (FSK switch is closed)
1	$f_{max} = f_c + \Delta f$ (FSK switch is open)

8.3. Crystal Pulling

A crystal is tuned by the manufacturer to the required oscillation frequency f_0 at a given load capacitance CL and within the specified calibration tolerance. The only way to pull the oscillation frequency is to vary the effective load capacitance CL_{eff} seen by the crystal.
Figure 3 shows the oscillation frequency of a crystal as a function of the effective load capacitance. This capacitance changes in accordance with the logic level of FSKDTA around the specified load capacitance. The figure illustrates the relationship between the external pulling capacitors and the frequency deviation.
It can also be seen that the pulling sensitivity increases with the reduction of CL. Therefore, applications with a high frequency deviation require a low load capacitance. For narrow band FSK applications, a higher load capacitance could be chosen in order to reduce the frequency drift caused by the tolerances of the chip and the external pulling capacitors.

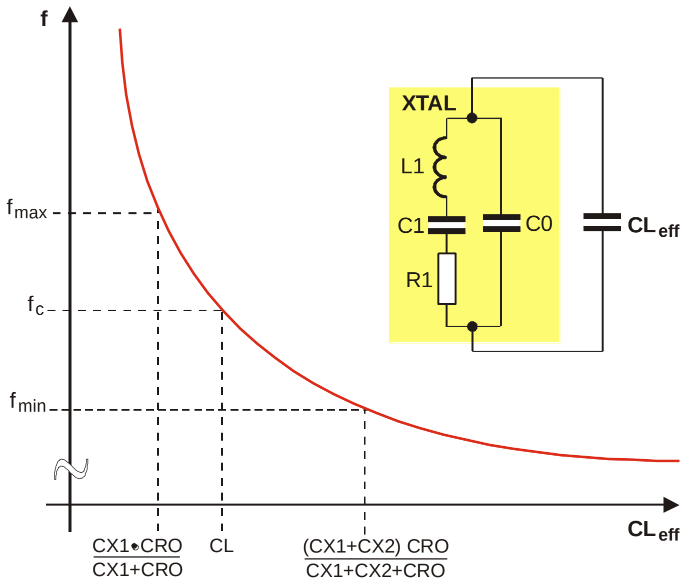


Fig. 3: Crystal pulling characteristic

8.4. ASK Modulation

The MLX72013 can be ASK-modulated by applying data directly at pin PSEL. This turns the PA on and off and therefore leads to an ASK signal at the output.

8.5. Output Power Selection

The transmitter is provided with an output power selection feature. There are four predefined output power steps and one off-step accessible via the power selection pin PSEL. A digital power step adjustment was chosen because of its high accuracy and stability. The number of steps and the step sizes as well as the corresponding power levels are selected to cover a wide spectrum of different applications.

The implementation of the output power control logic is shown in figure 4. There are two matched current sources with an amount of about 8 µA. One current source is directly applied to the PSEL pin. The other current source is used for the generation of reference voltages with a resistor ladder. These reference voltages are defining the thresholds between the power steps. The four comparators deliver thermometer-coded control signals depending on the voltage level at the pin PSEL. In order to have a certain amount of ripple tolerance in a noisy environment the comparators are provided with a little hysteresis of about 20 mV. With these control signals, weighted current sources of the power amplifier are switched on or off to set the desired output power level (Digitally Controlled Current Source). The LOCK signal and the output of the low voltage detector are gating this current source.

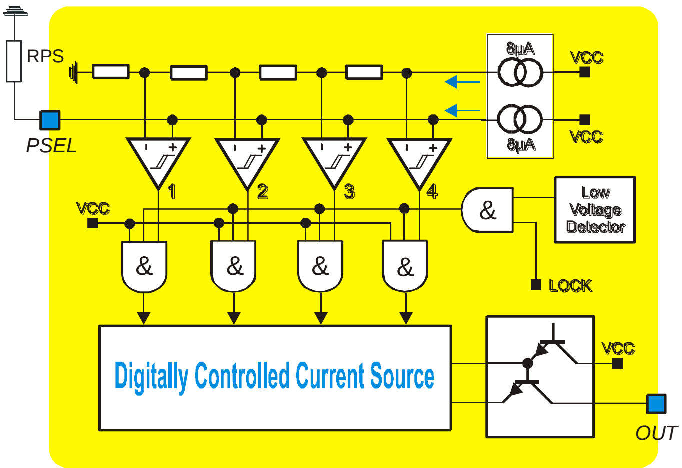


Fig. 4: Block diagram of output power control circuitry

There are two ways to select the desired output power step. First by applying a DC voltage at the pin PSEL, then this voltage directly selects the desired output power step. This kind of power selection can be used if the transmission power must be changed during operation. For a fixed-power application a resistor can be used which is connected from the PSEL pin to ground. The voltage drop across this resistor selects the desired output power level. For fixed-power applications at the highest power step this resistor can be omitted. The pin PSEL is in a high impedance state during the "TX standby" mode.

8.6. Lock Detection

The lock detection circuitry turns on the power amplifier only after PLL lock. This prevents from unwanted emission of the transmitter if the PLL is unlocked.

8.7. Low Voltage Detection

The supply voltage is sensed by a low voltage detect circuitry. The power amplifier is turned off if the supply voltage drops below a value of about 1.85 V. This is done in order to prevent unwanted emission of the transmitter if the supply voltage is too low.

8.8. Mode Control Logic

The mode control logic allows two different modes of operation as listed in the following table. The mode control pin ENTX is pulled-down internally. This guarantees that the whole circuit is shut down if this pin is left floating.

ENTX	Mode	Description
0	TX standby	TX disabled
1	TX active	TX enable

8.9. Timing Diagrams

After enabling the transmitter by the ENTX signal, the power amplifier remains inactive for the time t_{on}, the transmitter start-up time. The crystal oscillator starts oscillation and the PLL locks to the desired output frequency within the time duration t_{on}. After successful PLL lock, the LOCK signal turns on the power amplifier, and then the RF carrier can be FSK modulated.

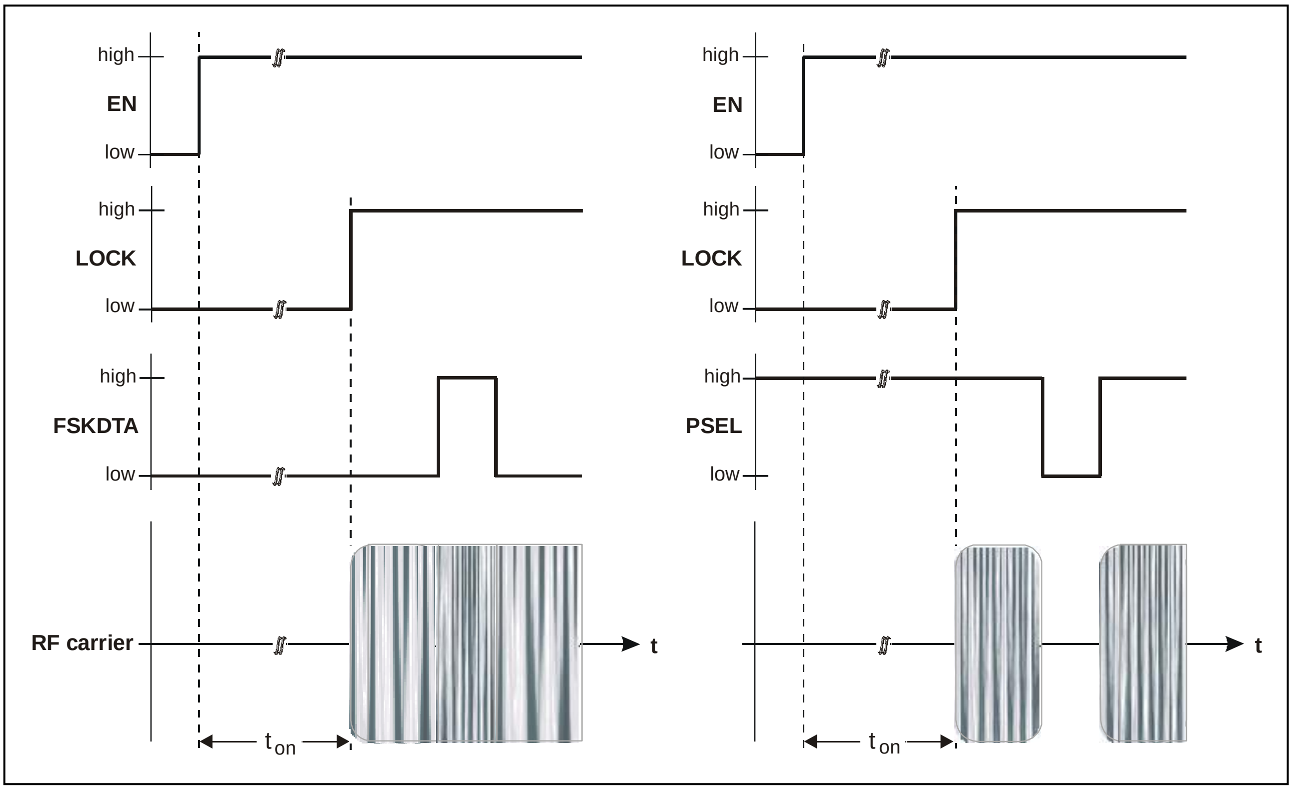


Fig. 5: Timing diagram for FSK modulation

For more detailed information, please refer to the latest MLX72013 data sheet revision.

9. 50Ω Connector Board Circuit Diagram

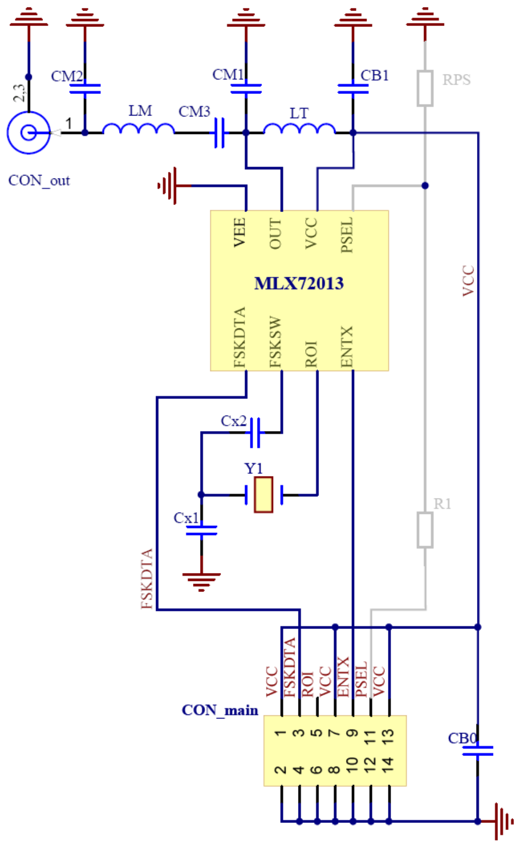


Fig. 6: Circuit diagram with 50 Ω matching network

9.1. Board Component Values to Fig. 7

Part	Size	Value @ 433.92 MHz	Tolerance	Description
CM1	0805	8.2 pF	±2%	impedance matching capacitor
CM2	0805	15 pF	±2%	impedance matching capacitor
CM3	0805	82 pF	±2%	impedance matching capacitor
LM	0805	22 nH	±5%	impedance matching inductor, **note 2**
LT	0805	27 nH	±5%	output tank inductor, **note 2**
CX1	0805	10 pF	±2%	XOSC capacitor (Δf = ±20 kHz) , **note 1**
CX2	0805	12 pF	±2%	XOSC capacitor (Δf = ±20 kHz) , **note 1**
RPS	0805	NIP	±5%	power-select resistor, see data sheet, sec 4.6 and 4.7
R1	0805	NIP	±5%	ASK mode: 0Ω jumper (ASK data can be applied at input PSEL), see data sheet, sec 4.7
CB0	0805	220 nF	±20%	de-coupling capacitor
CB1	0805	330 pF	±10%	de-coupling capacitor
Y1	SMD 6x3.5	27.12000 MHz	±30ppm calibr. ±20ppm temp.	fundamental wave crystal (C3M2712000E10FSDHK01), C_L = 10 pF, C_0 = 3 pF, R_1 = 50 Ω

Note 1: depends on crystal parameters, other Δf values can be selected with other CX1, CX2 values
Note 2: for high-power applications high-Q wire-wound inductors should be used

- NIP – not in place, may be populated optionally

9.2. 50Ω Connector Board PCB Top View

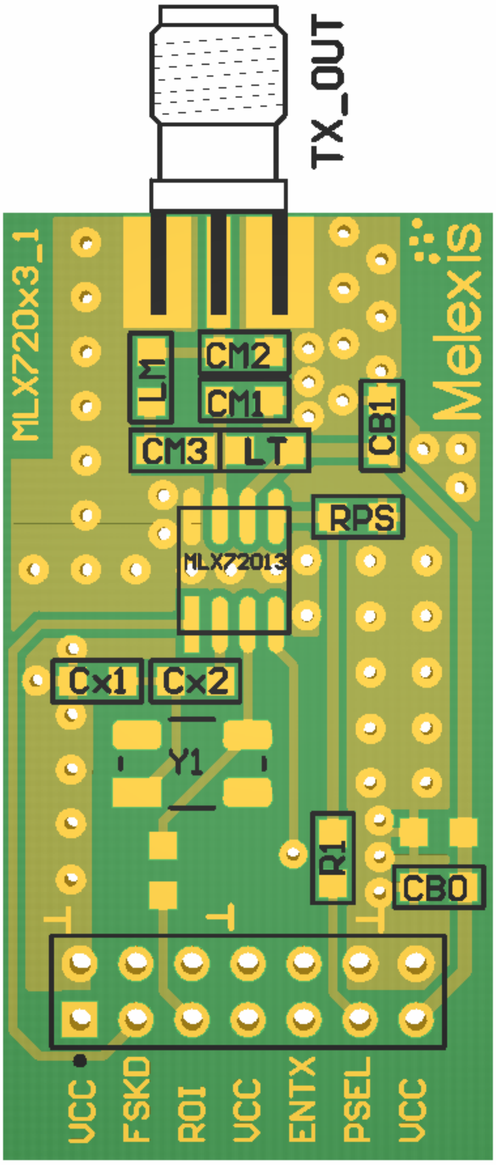


Fig. 7: PCB population

9.3. Board Connection

VCC	Power supply (1.9 V to 5.5 V)	**ROI**	External reference frequency input
FSKD	Input for FSK data (CMOS, see para. 2.2)	**ENTX**	Mode control pin
PSEL	Input for ASK data (R1 = 0Ω must be in place)	**⊥**	Several ground pins

9.4. Evaluation Board Layouts

Board layout data in Gerber format are available, board size is 22mm x 43mm x 1mm FR4.

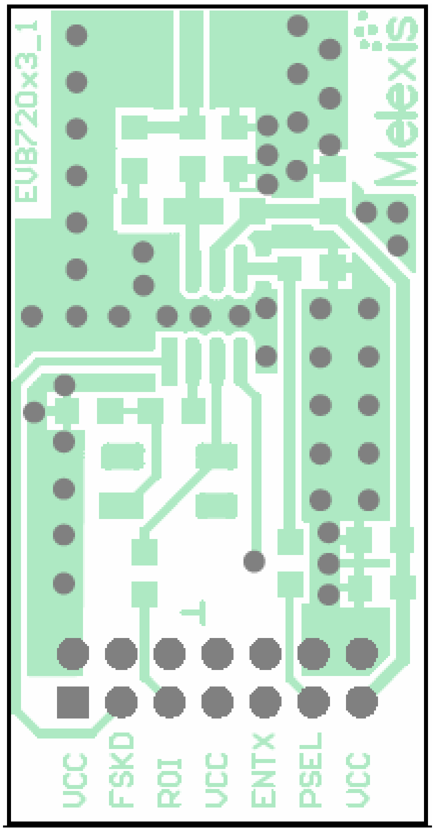


Fig.8: PCB top view

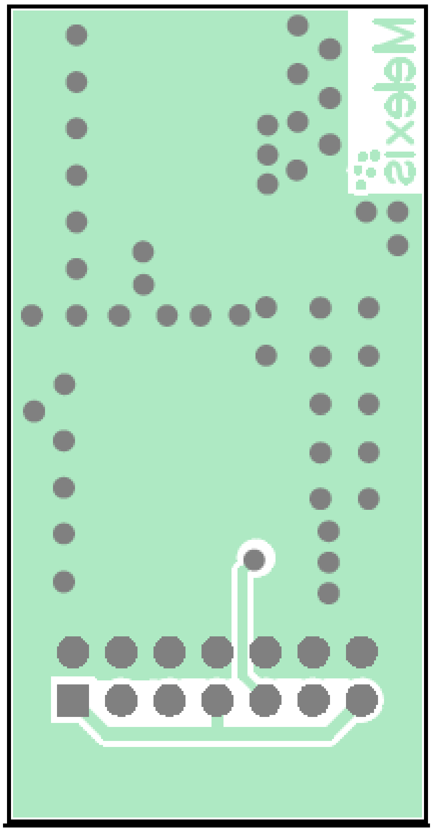


Fig 9: PCB bottom view

9.5. Board Variants

Type	Frequency/MHz		Modulation		Board Execution	
EVB72013	**–315**		**–FSK**		**–A**	antenna version
	–433		**–ASK**	according to section 3.1	**–C**	connector version
	–868		**–FM**			
	–915					

Note: **available EVB setups**

10. Package Description

- The device MLX72013 is RoHS compliant.

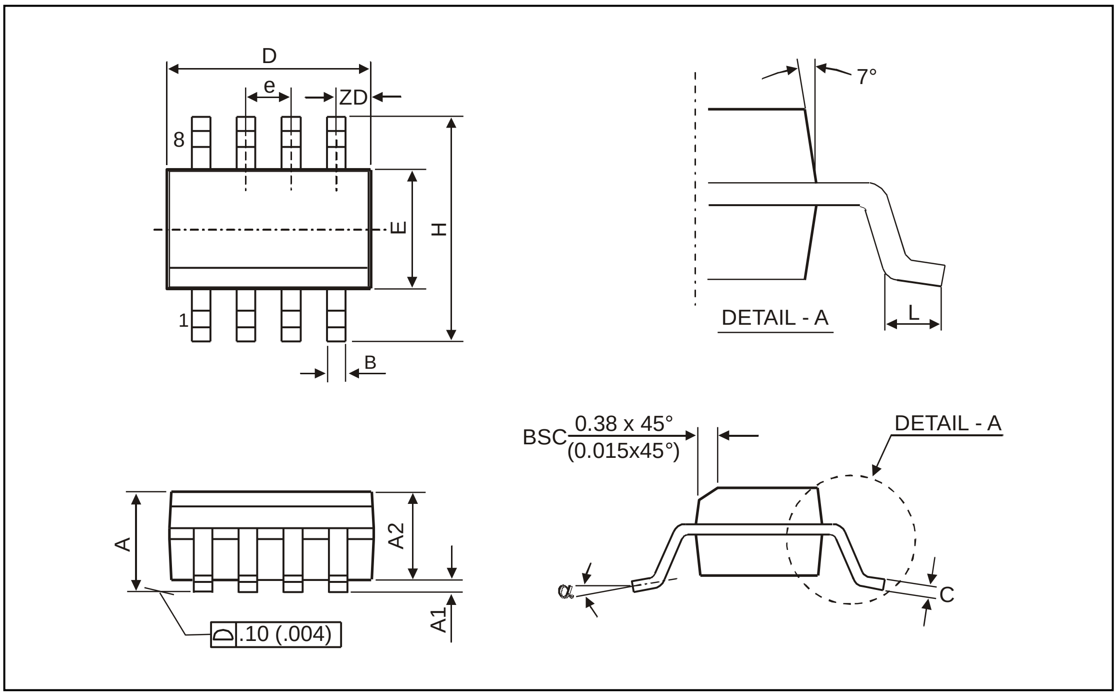


Fig. 10: SOIC8

all Dimension in mm, coplanarity < 0.1mm												
	D	**E**	**H**	**A**	**A1**	**A2**	**e**	**B**	**ZD**	**C**	**L**	**α**
min	4.80	3.81	5.80	1.52	0.10	1.37	1.27	0.36	0.53	0.19	0.41	0°
max	4.98	3.99	6.20	1.72	0.25	1.57		0.46		0.25	1.27	8°
all Dimension in inch, coplanarity < 0.004”												
min	0.189	0.150	0.2284	0.060	0.0040	0.054	0.050	0.014	0.021	0.075	0.016	0°
max	0.196	0.157	0.2440	0.068	0.0098	0.062		0.018		0.098	0.050	8°

10.1. Soldering Information

- The device MLX72013 is qualified for MSL1 with soldering peak temperature 260 deg C according to JEDEC J-STD-20.

11. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis recommends reviewing on our web site the General Guidelines soldering recommendation (http://www.melexis.com/Quality_soldering.aspx) as well as trim&form recommendations (http://www.melexis.com/Assets/Trim-and-form-recommendations-5565.aspx).

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/quality.aspx

12. ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

13. Your Notes

14. Contact

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