CS51411, CS51412, CS51413, CS51414

1.5 A, 260 kHz and 520 kHz, Low Voltage Buck Regulators with External Bias or Synchronization Capability

The CS5141X products are 1.5 A buck regulator ICs. These devices are fixed−frequency operating at 260 kHz and 520 kHz. The regulators use the V^{2TM} control architecture to provide unmatched transient response, the best overall regulation and the simplest loop compensation for today's high−speed logic. These products accommodate input voltages from 4.5 V to 40 V.

The CS51411 and CS51413 contain synchronization circuitry. The CS51412 and CS51414 have the option of powering the controller from an external 3.3 V to 6.0 V supply in order to improve efficiency, especially in high input voltage, light load conditions.

The on−chip NPN transistor is capable of providing a minimum of 1.5 A of output current, and is biased by an external "boost" capacitor to ensure saturation, thus minimizing on−chip power dissipation. Protection circuitry includes thermal shutdown, cycle−by−cycle current limiting and frequency foldback. The CS51411 and CS51413 are functionally pin−compatible with the LT1375. The CS51412 and CS51414 are functionally pin−compatible with the LT1376.

Features

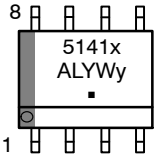
- V^2 Architecture Provides Ultrafast Transient Response, Improved Regulation and Simplified Design
- 2.0% Error Amp Reference Voltage Tolerance
- Switch Frequency Decrease of 4:1 in Short Circuit Conditions Reduces Short Circuit Power Dissipation
- BOOST Pin Allows "Bootstrapped" Operation to Maximize Efficiency
- Sync Function for Parallel Supply Operation or Noise Minimization
- Shutdown Lead Provides Power−Down Option
- 85 μA Quiescent Current During Power−Down
- Thermal Shutdown
- Soft−Start
- Pin−Compatible with LT1375 and LT1376
- These Devices are Pb−Free and are RoHS Compliant

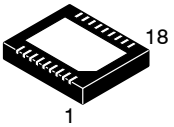
ON Semiconductor®

http://onsemi.com

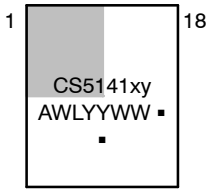
MARKING DIAGRAMS

SOIC−8
D SUFFIX
CASE 751





18−LEAD DFN
MN SUFFIX
CASE 505

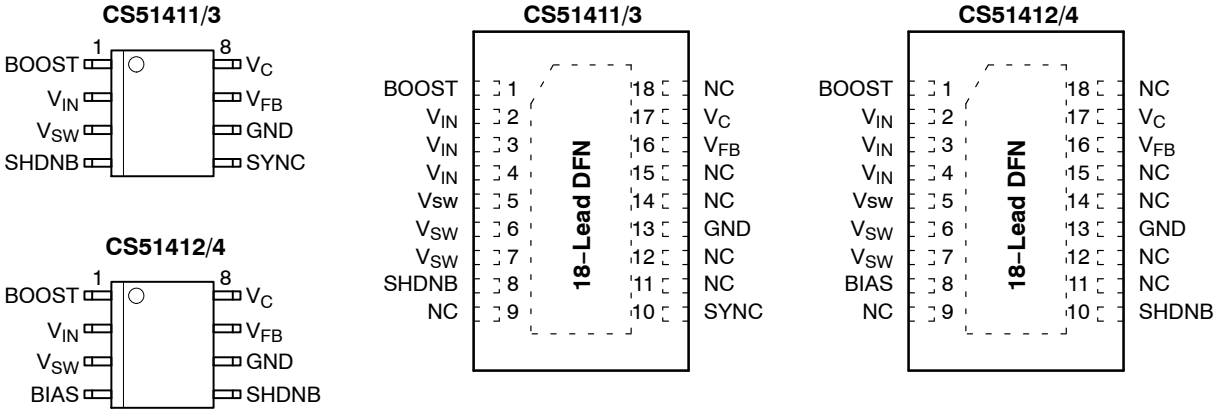


5141x = Device Code
x = 1, 2, 3 or 4
A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
y = E or G
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 18 of this data sheet.

PIN CONNECTIONS



PACKAGE PIN DESCRIPTION

SOIC−8 Package Pin #	DFN18 Package Pin #	Pin Symbol	Function
1	1	BOOST	The BOOST pin provides additional drive voltage to the on−chip NPN power transistor. The resulting decrease in switch on voltage increases efficiency.
2	2, 3, 4	V_{IN}	This pin is the main power input to the IC.
3	5, 6, 7	V_{SW}	This is the connection to the emitter of the on−chip NPN power transistor and serves as the switch output to the inductor. This pin may be subjected to negative voltages during switch off−time. A catch diode is required to clamp the pin voltage in normal operation. This node can stand −1.0 V for less than 50 ns during switch node flyback.
4 (CS51412/CS51414)	8	BIAS	The BIAS pin connects to the on−chip power rail and allows the IC to run most of its internal circuitry from the regulated output or another low voltage supply to improve efficiency. The BIAS pin is left floating if this feature is not used.
5 (CS51411/CS51413)	10	SYNC	This pin provides the synchronization input.
5 (CS51412/CS51414) 4 (CS51411/CS51413)	10 (CS51412/CS51414) 8 (CS51411/CS51413)	SHDNB	Shutdown_bar input. This is an active−low logical input, TTL compatible, with an internal pull−up current source. The IC goes into sleep mode, drawing less than 85 μA when the pin voltage is pulled below 1.0 V. This pin may be left floating in applications where a shutdown function is not required.
6	13	GND	Power return connection for the IC.
7	16	V_{FB}	The FB pin provides input to the inverting input of the error amplifier. If V_{FB} is lower than 0.29 V, the oscillator frequency is divided by four, and current limit folds back to about 1 A. These features protect the IC under severe overcurrent or short circuit conditions.
8	17	V_C	The V_C pin provides a connection point to the output of the error amplifier and input to the PWM comparator. Driving of this pin should be avoided because on−chip test circuitry becomes active whenever current exceeding 0.5 mA is forced into the IC.
−	9, 11, 12, 14, 15, 18	NC	No Connection

PRODUCT SELECTION GUIDE

Part Number	Frequency	Temperature Range	Bias/Sync
CS51411E	260 kHz	−40°C to 85°C	Sync
CS51411G	260 kHz	0°C to 70°C	Sync
CS51412E	260 kHz	−40°C to 85°C	Bias
CS51412G	260 kHz	0°C to 70°C	Bias
CS51413E	520 kHz	−40°C to 85°C	Sync
CS51413G	520 kHz	0°C to 70°C	Sync
CS51414E	520 kHz	−40°C to 85°C	Bias
CS51414G	520 kHz	0°C to 70°C	Bias

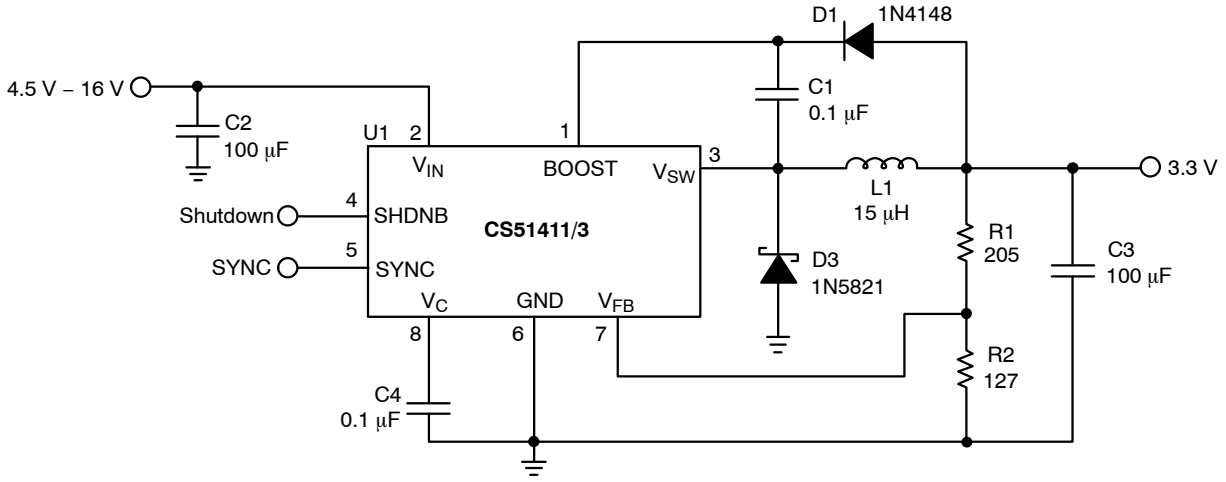


Figure 1. Application Diagram, 4.5 V – 16 V to 3.3 V @ 1.0 A Converter

MAXIMUM RATINGS

Rating		Value	Unit
Operating Junction Temperature Range, T_J		−40 to 150	°C
Lead Temperature Soldering:	Reflow for Leaded: (SMD styles only) (Note 1) Reflow for Pb−Free: (SMD styles only) (Note 2)	230 peak 260 peak (Note 3)	°C
Storage Temperature Range, T_S		−65 to +150	°C
ESD Damage Threshold (Human Body Model)		2.0	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 60−150 second above 183°C, 30 second maximum at peak.
2. 60−150 second above 217°C, 40 second maximum at peak.
3. +5°C/0°C allowable conditions, applies to both Pb and Pb−Free Devices.

MAXIMUM RATINGS

Pin Name	V_{Max}	V_{MIN}	I_{SOURCE}	I_{SINK}
V_{IN}	40 V	−0.3 V	N/A	4.0 A
BOOST	40 V	−0.3 V	N/A	100 mA
V_{SW}	40 V	−0.6 V/−1.0 V, t < 50 ns	4.0 A	10 mA
V_C	7.0 V	−0.3 V	1.0 mA	1.0 mA
SHDNB	7.0 V	−0.3 V	1.0 mA	1.0 mA
SYNC	7.0 V	−0.3 V	1.0 mA	1.0 mA
BIAS	7.0 V	−0.3 V	1.0 mA	50 mA
V_{FB}	7.0 V	−0.3 V	1.0 mA	1.0 mA
GND	7.0 V	−0.3 V	50 mA	1.0 mA

ELECTRICAL CHARACTERISTICS (−40°C < T_J < 125°C (CS51411E/2E/3E/4E); −40°C < T_A < 85°C (CS51411E/2E/3E/4E); 0°C < T_A < 70°C (CS51411G/2G/3G/4G), 4.5 V< V_{IN} < 40 V; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Oscillator					
Operating Frequency	CS51411/CS51412	224	260	296	kHz
Operating Frequency	CS51413/CS51414	446	520	594	kHz
Frequency Line Regulation	–	–	0.05	0.15	%/V
Maximum Duty Cycle	–	85	90	95	%
V_{FB} Frequency Foldback Threshold	–	0.29	0.32	0.36	V
PWM Comparator					
Slope Compensation Voltage	CS51411/CS51412, Fix V_{FB}, $\Delta V_C/\Delta T_{ON}$ CS51413/CS51414	8.0 25	17 50	26 75	mV/μs mV/μs
Minimum Output Pulse Width	CS51411/CS51412, V_{FB} to V_{SW} CS51413/CS51414, V_{FB} to V_{SW}	– –	150 –	300 230	ns ns
Power Switch					
Current Limit	V_{FB} > 0.36 V	1.6	2.3	3.0	A
Foldback Current	V_{FB} < 0.29 V	0.9	1.5	2.1	A
Saturation Voltage	I_{OUT} = 1.5 A, V_{BOOST} = V_{IN} + 2.5 V	0.4	0.7	1.0	V
Current Limit Delay	(Note 4)	–	120	160	ns
Error Amplifier					
Internal Reference Voltage	–	1.244	1.270	1.296	V
Reference PSRR	(Note 4)	–	40	–	dB
FB Input Bias Current	–	–	0.02	0.1	μA
Output Source Current	V_C = 1.270 V, V_{FB} = 1.0 V	15	25	35	μA
Output Sink Current	V_C = 1.270 V, V_{FB} = 2.0 V	15	25	35	μA
Output High Voltage	V_{FB} = 1.0 V	1.39	1.46	1.53	V
Output Low Voltage	V_{FB} = 2.0 V	5.0	20	60	mV
Unity Gain Bandwidth	(Note 4)	–	500	–	kHz
Open Loop Amplifier Gain	(Note 4)	–	70	–	dB
Amplifier Transconductance	(Note 4)	–	6.4	–	mA/V

4. Guaranteed by design, not 100% tested in production.

ELECTRICAL CHARACTERISTICS (–40°C < T_J < 125°C (CS51411E/2E/3E/4E); –40°C < T_A < 85°C (CS51411E/2E/3E/4E); 0°C < T_A < 70°C (CS51411G/2G/3G/4G), 4.5 V< V_{IN} < 40 V; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Sync					
Sync Frequency Range	CS51411/CS51412	305	–	470	kHz
Sync Frequency Range	CS51413/CS51414	575	–	880	kHz
Sync Pin Bias Current	V_{SYNC} = 0 V V_{SYNC} = 5.0 V	– 250	0.1 360	0.2 460	μA μA
Sync Threshold Voltage	–	1.0	1.5	1.9	V
Shutdown					
Shutdown Threshold Voltage	I_{CC} = 2 mA	1.0	1.3	1.6	V
Shutdown Pin Bias Current	V_{SHDNB} = 0 V	0.14	5.00	35	μA
Thermal Shutdown					
Overtemperature Trip Point	(Note 5)	175	185	195	°C
Thermal Shutdown Hysteresis	(Note 5)	–	42	–	°C
General					
Quiescent Current	I_{SW} = 0 A	–	–	6.25	mA
Shutdown Quiescent Current	V_{SHDNB} = 0 V	–	20	85	μA
Boost Operating Current	V_{BOOST} – V_{SW} = 2.5 V	6.0	15	40	mA/A
Minimum Boost Voltage	(Note 5)	–	–	2.5	V
Startup Voltage	–	2.2	3.3	4.4	V
Minimum Output Current	–	–	7.0	12	mA

5. Guaranteed by design, not 100% tested in production.

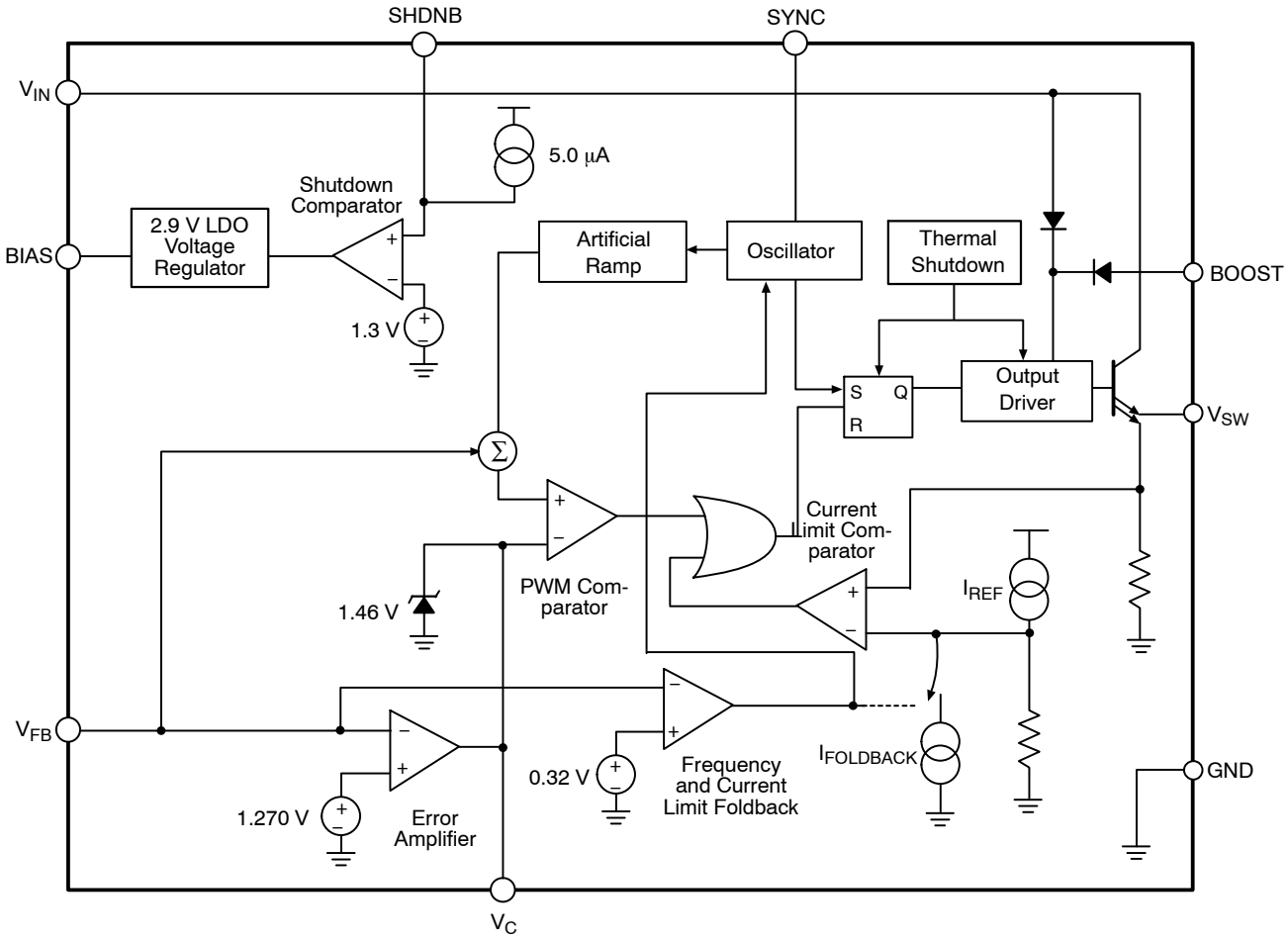


Figure 2. Block Diagram

APPLICATIONS INFORMATION

THEORY OF OPERATION

V² Control

The CS5141X family of buck regulators utilizes a V2 control technique and provides a high level of integration to enable high power density design optimization.

Every pulse width modulated controller configures basic control elements such that when connected to the feedback signal of a power converter, sufficient loop gain and bandwidth is available to regulate the voltage set point against line and load variations. The arrangement of these elements differentiates a voltage mode, or a current mode controller from a V2 device.

Figure 3 illustrates the basic architecture of a V2 controller.

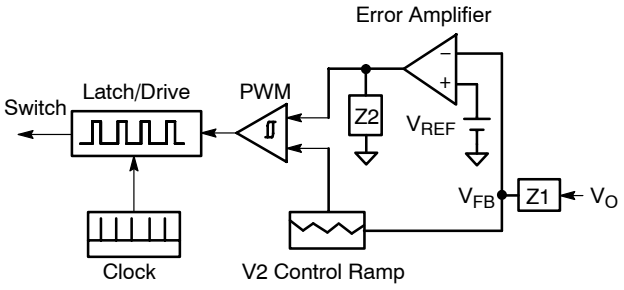


Figure 3. V2 Control

In common with V mode or I mode, the feedback signal is compared with a reference voltage to develop an error signal which is fed to one input of the PWM. The second input to the PWM, however, is neither a fixed voltage ramp nor the switch current, but rather the feedback signal from the output of the converter. This feedback signal provides both DC information as well as AC information (the control ramp) for the converter to regulate its set point. The control architecture is known as V2 since both PWM inputs are derived from the converter's output voltage. This is a little misleading because the control ramp is typically generated from current information present in the converter.

The feedback signal from the buck converter shown in Figure 4 is processed in one of two ways before being routed to the inputs of the PWM comparator. The Fast Feedback path (FFB) adds slope compensation to the feedback signal before passing it to one input of the PWM. The Slow Feedback path (SFB) compares the original feedback signal against a DC reference. The error signal generated at the output of the error amplifier VC is filtered by a low frequency pole before being routed to the second input of the PWM. Each switch cycle is initiated (S1 on), when the output latch is set by the oscillator. Each switch cycle terminates (S1 off), when the FFB signal (AC plus output DC) exceeds SFB (error DC), and the output latch is reset. In the event of a load transient, the FFB signal changes faster, in relation to the filtered SFB signal, causing duty cycle modulation to occur. Actual oscilloscope waveforms taken from the converter show the switch node V_{SWITCH}, the error signal V_C and the feedback signal V_{FB} (AC component only) are shown in Figure 5.

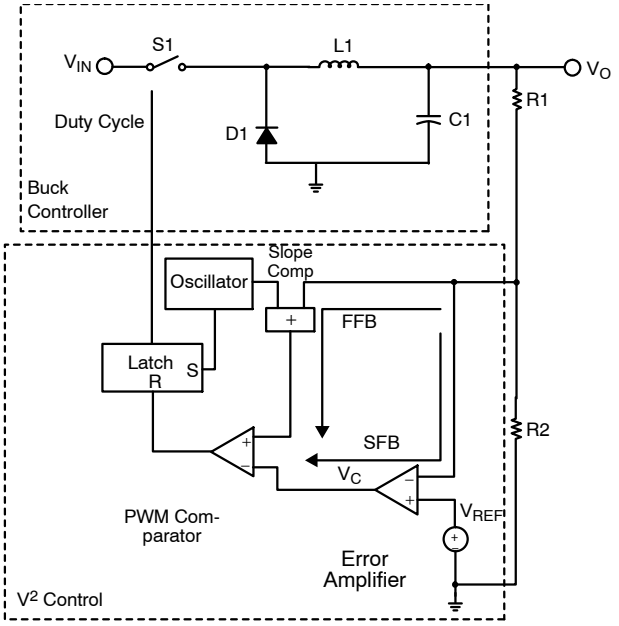


Figure 4. Buck Converter with V2 Control

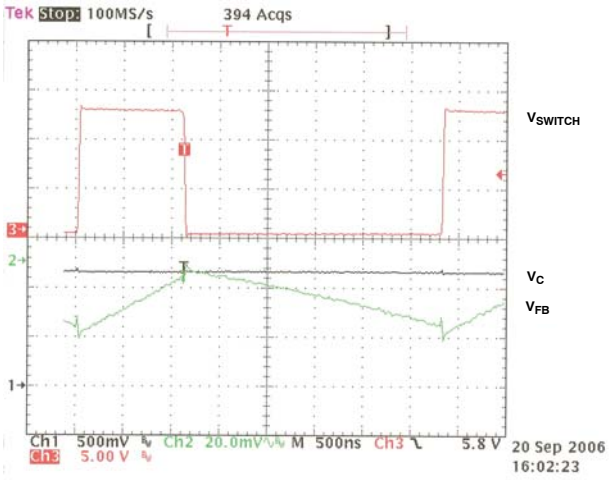


Figure 5.

In the event of a load transient, the FFB signal changes faster, in relation to the filtered SFB signal, causing duty cycle modulation to occur. By this means the converter's transient response time is independent of the error amplifier bandwidth. The error amplifier is used here to ensure excellent DC accuracy.

In order for the controller to operate optimally, a stable ramp is required at the feedback pin.

Control Ramp Generation

In original V2 designs, the control ramp VCR was generated from the converter's output ripple. Using a current derived ramp provides the same benefits as current mode, namely input feed forward, single pole output filter compensation and fast feedback following output load transients. Typically a tantalum or organic polymer capacitor is selected having a sufficiently large ESR component, relative to its capacitive and ESL ripple contributions, to ensure the control ramp was sensing inductor current and its amplitude was sufficient to maintain loop stability. This technique is illustrated in Figure 6.

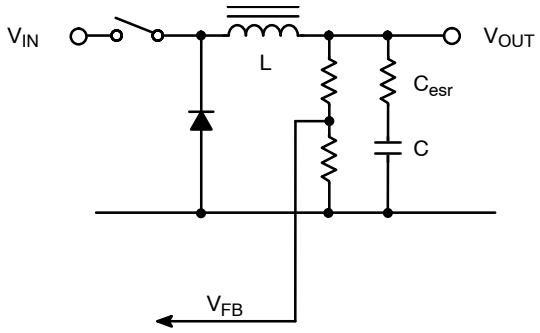


Figure 6. Control Ramp Generated from Output

Advances in multilayer ceramic capacitor technology are such that MLCC's can provide a cost effective filter solution for low voltage (< 12 V), high frequency converters (>200 kHz). For example, a 10 μF MLCC 16 V in a 805 SMT package has an ESR of 2 mΩ and an ESL of 100 nH. Using several MLCC's in parallel, connected to power and ground planes on a PCB with multiple vias, can provide a "near perfect" capacitor. Using this technique, output switching ripple below 10 mV can be readily obtained since parasitic ESR and ESL ripple contributions are nil. In this case, the control ramp is generated elsewhere in the circuit.

Ramp generation using dcr inductor current sensing, where the L/DCR time constant of the output inductor is matched with the CR time constant of the integrating network, is shown in Figure 7. The converter's transient response following a 1 A step load is shown in Figure 8. This transient response is indicative of a closed loop in excess of 10 kHz having good gain and phase margin in the frequency domain. Also note the amplitude of output switching ripple provided by just two 10 μF MLCC's.

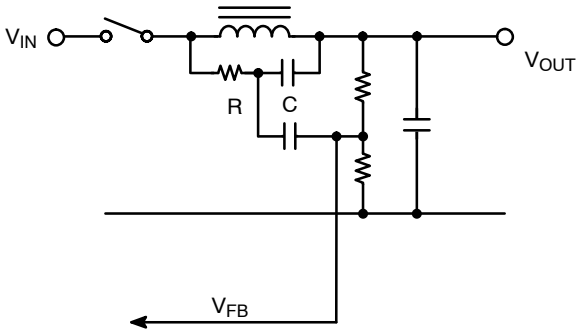


Figure 7. Control Ramp Generated from DCR Inductor Sensing

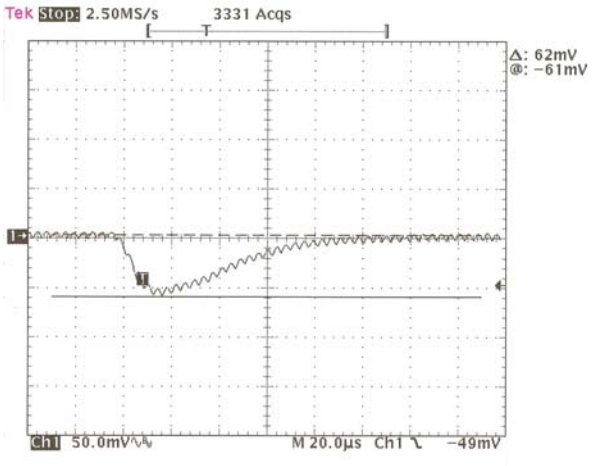


Figure 8.

Ramp generation using a voltage feed forward technique is illustrated in Figure 9.

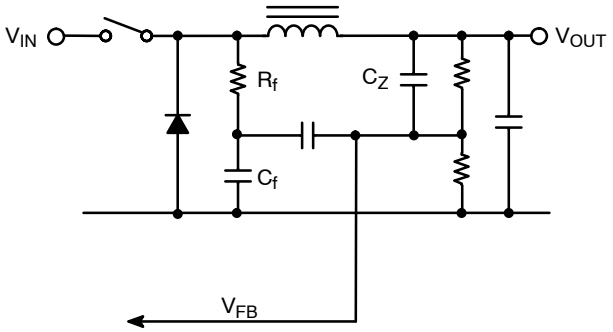


Figure 9. Control Ramp from Voltage Feed Forward

Some representative efficiency data is shown in Figure 10.

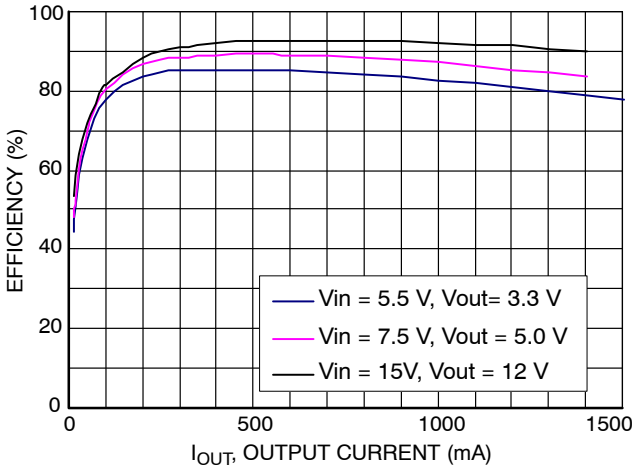


Figure 10. Efficiency versus Output Current

More detailed information is available in the ON Semiconductor application note AND8276/D on V2 and the CS5141x demonstration board number.

Error Amplifier

The CS5141X has a transconductance error amplifier, whose noninverting input is connected to an Internal Reference Voltage generated from the on−chip regulator. The inverting input connects to the V_{FB} pin. The output of the error amplifier is made available at the V_C pin. A typical frequency compensation requires only a 0.1 μF capacitor connected between the V_C pin and ground, as shown in Figure 1. This capacitor and error amplifier's output resistance (approximately 8.0 MΩ) create a low frequency pole to limit the bandwidth. Since V2 control does not require a high bandwidth error amplifier, the frequency compensation is greatly simplified.

The V_C pin is clamped below Output High Voltage. This allows the regulator to recover quickly from overcurrent or short circuit conditions.

Oscillator and Sync Feature (CS51411 and CS51413 only)

The on−chip oscillator is trimmed at the factory and requires no external components for frequency control. The high switching frequency allows smaller external components to be used, resulting in a board area and cost savings. The tight frequency tolerance simplifies magnetic components election. The switching frequency is reduced to 25% of the nominal value when the V_{FB} pin voltage is below Frequency Foldback Threshold. In short circuit or overload conditions, this reduces the power dissipation of the IC and external components.

An external clock signal can sync CS51411/CS51414 to a higher frequency. The rising edge of the sync pulse turns on the power switch to start a new switching cycle, as shown in Figure 11. There is approximately 0.5 μs delay between the rising edge of the sync pulse and rising edge of the V_{SW} pin voltage. The sync threshold is TTL logic compatible, and duty cycle of the sync pulses can vary from 10% to 90%. The frequency foldback feature is disabled during the sync mode.

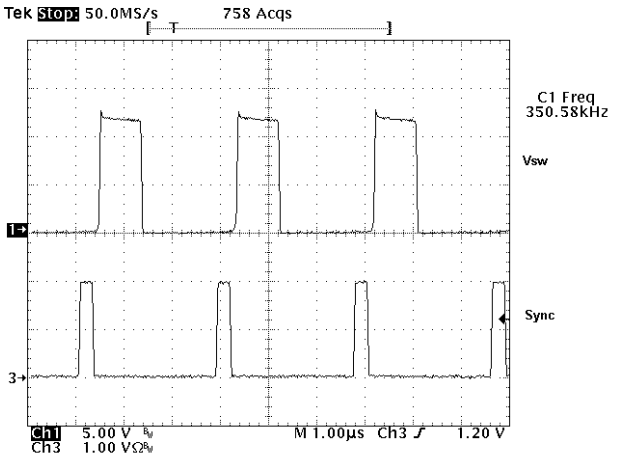


Figure 11. A CS51411 Buck Regulator is Synced by an External 350 kHz Pulse Signal

Power Switch and Current Limit

The collector of the built−in NPN power switch is connected to the V_{IN} pin, and the emitter to the V_{SW} pin. When the switch turns on, the V_{SW} voltage is equal to the V_{IN} minus switch Saturation Voltage. In the buck regulator, the V_{SW} voltage swings to one diode drop below ground when the power switch turns off, and the inductor current is commutated to the catch diode. Due to the presence of high pulsed current, the traces connecting the V_{SW} pin, inductor and diode should be kept as short as possible to minimize the noise and radiation. For the same reason, the input capacitor should be placed close to the V_{IN} pin and the anode of the diode.

The saturation voltage of the power switch is dependent on the switching current, as shown in Figure 12.

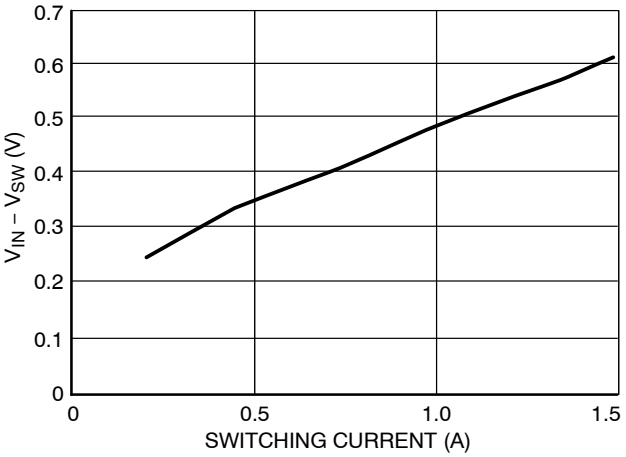


Figure 12. The Saturation Voltage of the Power Switch Increases with the Conducting Current

Members of the CS5141X family contain pulse−by−pulse current limiting to protect the power switch and external components. When the peak of the switching current reaches the Current Limit, the power switch turns off after the Current Limit Delay. The switch will not turn on until the next switching cycle. The current limit threshold is

independent of switching duty cycle. The maximum load current, given by the following formula under continuous conduction mode, is less than the Current Limit due to the ripple current.

$$I_{O(MAX)} = I_{LIM} - \frac{V_O(V_{IN} - V_O)}{2(L)(V_{IN})(f_S)}$$

where:

f_S = switching frequency,

I_{LIM} = current limit threshold,

V_O = output voltage,

V_{IN} = input voltage,

L = inductor value.

When the regulator runs undercurrent limit, the subharmonic oscillation may cause low frequency oscillation, as shown in Figure 13. Similar to current mode control, this oscillation occurs at the duty cycle greater than 50% and can be alleviated by using a larger inductor value. The current limit threshold is reduced to Foldback Current when the FB pin falls below Foldback Threshold. This feature protects the IC and external components under the power up or overload conditions.

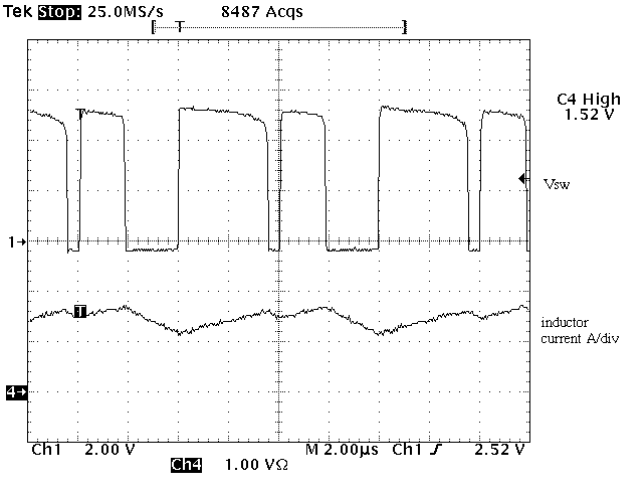


Figure 13. The Regulator in Current Limit

BOOST Pin

The BOOST pin provides base driving current for the power switch. A voltage higher than V_{IN} provides required headroom to turn on the power switch. This in turn reduces IC power dissipation and improves overall system efficiency. The BOOST pin can be connected to an external boost–strapping circuit which typically uses a 0.1 μF capacitor and a 1N914 or 1N4148 diode, as shown in Figure 1. When the power switch is turned on, the voltage on the BOOST pin is equal to

$$V_{BOOST} = V_{IN} + V_O - V_F$$

where:

V_F = diode forward voltage.

The anode of the diode can be connected to any DC voltage other than the regulated output voltage. However, the maximum voltage on the BOOST pin shall not exceed 40 V.

As shown in Figure 14, the BOOST pin current includes a constant 7.0 mA predriver current and base current proportional to switch conducting current. A detailed discussion of this current is conducted in Thermal Consideration section. A 0.1 μF capacitor is usually adequate for maintaining the Boost pin voltage during the on time.

BIAS Pin (CS51412 and CS51414 Only)

The BIAS pin allows a secondary power supply to bias the control circuitry of the IC. The BIAS pin voltage should be between 3.3 V and 6.0 V. If the BIAS pin voltage falls below that range, use a diode to prevent current drain from the BIAS pin. Powering the IC with a voltage lower than the regulator's input voltage reduces the IC power dissipation and improves energy transfer efficiency.

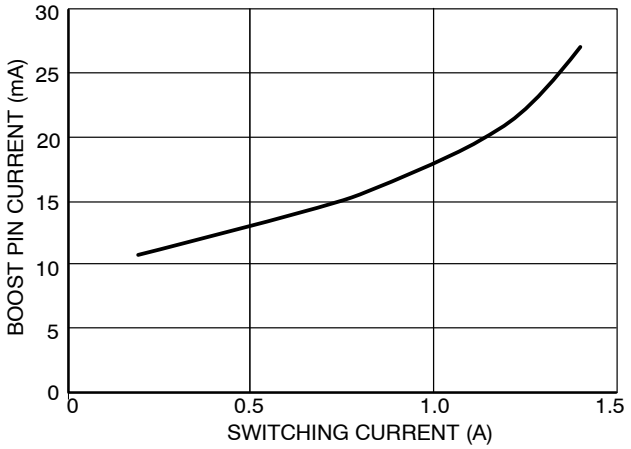


Figure 14. The Boost Pin Current Includes 7.0 mA Predriver Current and Base Current when the Switch is Turned On. The Beta Decline of the Power Switch Further Increases the Base Current at High Switching Current

Shutdown

The internal power switch will not turn on until the V_{IN} pin rises above the Startup Voltage. This ensures no switching until adequate supply voltage is provided to the IC. The IC transitions to sleep mode when the SHDNB pin is pulled low. In sleep mode, the internal power switch transistor remains off and supply current is reduced to the Shutdown Quiescent Current value (20 μA typical). This pin has an internal pull-up current source, so defaults to high (enabled) state when not connected.

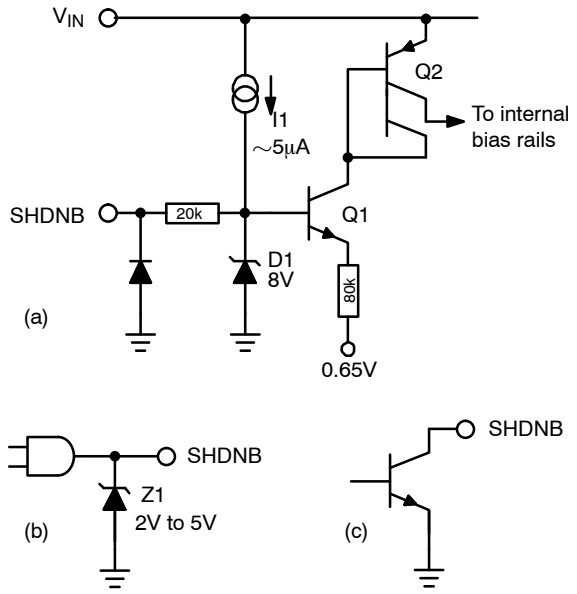


Figure 15. SHDNB pin equivalent internal circuit (a) and practical interface examples (b), (c).

Figure 15(a) depicts the SHDNB pin equivalent internal circuit. If the pin is open, current source I1 flows into the base of Q1, turning both Q1 and Q2 on. In turn, Q2 collector current enables the various internal power rails. In Figure 15(b), a standard logic gate is used to pull the pin low by shunting I1 to ground, which places the IC in sleep (shutdown) mode. Note that, when the gate output is logical high, the voltage at the SHDNB pin will rise to the internal clamp voltage of 8 V. This level exceeds the maximum output rating for most common logic families. Protection Zener diode Z1 permits the pin voltage to rise high enough to enable the IC, but remain less than the gate output voltage rating. In Figure 15(c), a single open-collector general-purpose NPN transistor is used to pull the pin low. Since transistors generally have a maximum collector voltage rating in excess of 8 V, the protection Zener diode in Figure 15(b) is not required.

Startup

During power up, the regulator tends to quickly charge up the output capacitors to reach voltage regulation. This gives rise to an excessive in−rush current which can be detrimental to the inductor, IC and catch diode. In V^2 control, the compensation capacitor provides Soft−Start with no need for extra pin or circuitry. During the power up, the Output Source Current of the error amplifier charges the compensation capacitor which forces V_C pin and thus output voltage ramp up gradually.

The Soft−Start duration can be calculated by

$$T_{SS} = \frac{V_C \times C_{COMP}}{I_{SOURCE}}$$

where:

V_C = V_C pin steady−state voltage, which is approximately equal to error amplifier's reference voltage.

C_{COMP} = Compensation capacitor connected to the V_C pin

I_{SOURCE} = Output Source Current of the error amplifier.

Using a 0.1 μF C_{COMP}, the calculation shows a T_{SS} over 5.0 ms which is adequate to avoid any current stresses. Figure 16 shows the gradual rise of the V_C, V_O and envelope of the V_{SW} during power up. There is no voltage overshoot after the output voltage reaches the regulation. If the supply voltage rises slower than the V_C pin, output voltage may overshoot.

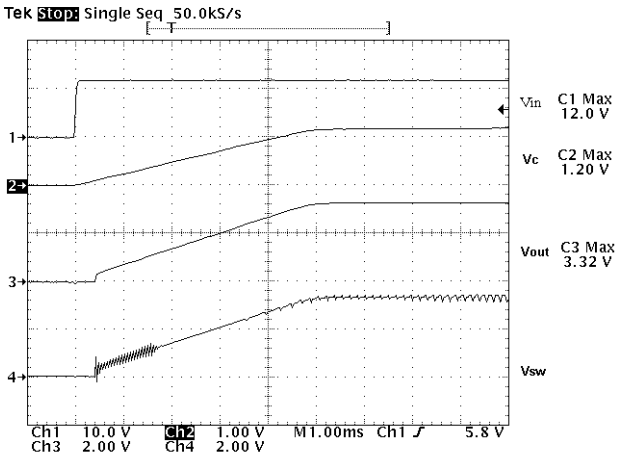


Figure 16. The Power Up Transition of CS5141X Regulator

Short Circuit

When the V_{FB} pin voltage drops below Foldback Threshold, the regulator reduces the peak current limit by 40% and switching frequency to 1/4 of the nominal frequency. These features are designed to protect the IC and external components during overload or short circuit conditions. In those conditions, peak switching current is clamped to the current limit threshold. The reduced switching frequency significantly increases the ripple current, and thus lowers the DC current. The short circuit can cause the minimum duty cycle to be limited by Minimum Output Pulse Width. The foldback frequency reduces the minimum duty cycle by extending the switching cycle. This protects the IC from overheating, and also limits the power that can be transferred to the output. The current limit foldback effectively reduces the current stress on the inductor and diode. When the output is shorted, the DC current of the inductor and diode can approach the current limit threshold. Therefore, reducing the current limit by 40% can result in an equal percentage drop of the inductor and diode current. The short circuit waveforms are captured in

Figure 17, and the benefit of the foldback frequency and current limit is self−evident.

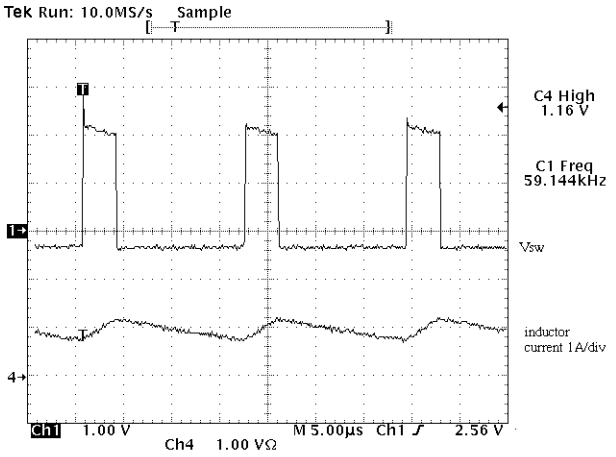


Figure 17. In Short Circuit, the Foldback Current and Foldback Frequency Limit the Switching Current to Protect the IC, Inductor and Catch Diode

Thermal Considerations

A calculation of the power dissipation of the IC is always necessary prior to the adoption of the regulator. The current drawn by the IC includes quiescent current, predriver current, and power switch base current. The quiescent current drives the low power circuits in the IC, which include comparators, error amplifier and other logic blocks. Therefore, this current is independent of the switching current and generates power equal to

$$W_Q = V_{IN} \times I_Q$$

where:

I_Q = quiescent current.

The predriver current is used to turn on/off the power switch and is approximately equal to 12 mA in worst case. During steady state operation, the IC draws this current from the Boost pin when the power switch is on and then receives it from the V_{IN} pin when the switch is off. The predriver current always returns to the V_{SW} pin. Since the predriver current goes out to the regulator's output even when the power switch is turned off, a minimum load is required to prevent overvoltage in light load conditions. If the Boost pin voltage is equal to $V_{IN} + V_O$ when the switch is on, the power dissipation due to predriver current can be calculated by

$$W_{DRV} = 12\ mA \times (V_{IN} - V_O + \frac{V_O^2}{V_{IN}})$$

The base current of a bipolar transistor is equal to collector current divided by beta of the device. Beta of 60 is used here to estimate the base current. The Boost pin provides the base current when the transistor needs to be on.

The power dissipated by the IC due to this current is

$$W_{BASE} = \frac{V_O^2}{V_{IN}} \times \frac{I_S}{60}$$

where:

I_S = DC switching current.

When the power switch turns on, the saturation voltage and conduction current contribute to the power loss of a non−ideal switch. The power loss can be quantified as

$$W_{SAT} = \frac{V_O}{V_{IN}} \times I_S \times V_{SAT}$$

where:

V_{SAT} = saturation voltage of the power switch which is shown in Figure 12.

The switching loss occurs when the switch experiences both high current and voltage during each switch transition. This regulator has a 30 ns turn−off time and associated power loss is equal to

$$W_S = \frac{I_S \times V_{IN}}{2} \times 30\ ns \times f_S$$

The turn−on time is much shorter and thus turn−on loss is not considered here.

The total power dissipated by the IC is sum of all the above

$$W_{IC} = W_Q + W_{DRV} + W_{BASE} + W_{SAT} + W_S$$

The IC junction temperature can be calculated from the ambient temperature, IC power dissipation and thermal resistance of the package. The equation is shown as follows,

$$T_J = W_{IC} \times R_{\theta JA} + T_A$$

The maximum IC junction temperature shall not exceed 125°C to guarantee proper operation and avoid any damages to the IC.

Using the BIAS Pin

The efficiency savings in using the BIAS pin is most notable at low load and high input voltage as will be explained below.

Figure 18 will help to understand the increase in efficiency when the BIAS pin is used. The circuitry shown is not the actual implementation, but is useful in the explanation.

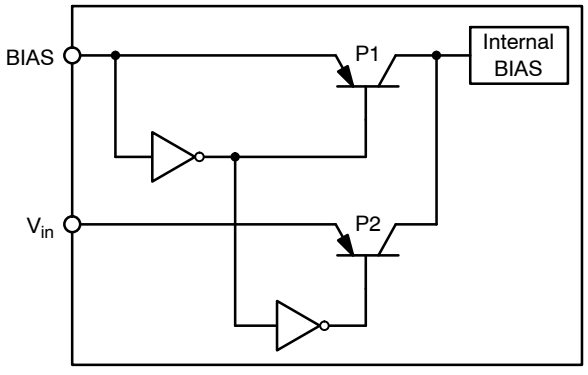


Figure 18.

Internal bias to the IC can be supplied via the V_{in} pin or the BIAS pin. When the BIAS pin is low, the logic turns P2 on and current is routed to the internal bias circuitry from the V_{in} pin. Conversely, when the BIAS pin is high, the logic

turns P1 on and current is routed to the internal bias circuitry from the BIAS pin.

Here is an example of the power savings:
The input voltage range for V_{in} is 4.5 V to 40 V. The input voltage range for BIAS is 3.3 V to 6 V. The quiescent current specification is 3 mA (min), 4 mA (typ), and 6.25 mA (max).

Using a typical battery voltage of 14 V and the typical quiescent current number of 4 mA, the power would be:

$$P = V \times I = 14 \times 4e{-}3 = 56\ mW$$

We'll assume the BIAS pin is connected to an external regulator at 5 V instead of the output voltage. The BIAS pin would normally be connected to the output voltage, but adding an added switching regulator efficiency number here would cloud this example. Now the internal BIAS circuitry is being powered via 5 V. The resulting on chip power being dissipated is:

$$P = V \times I = 5 \times 4e{-}3 = 21\ mW$$

The power savings is 35 mW.

Now, to demonstrate more notable savings using the maximum battery input voltage of 40 V, the maximum quiescent current of 6.25 mA, and the lowest allowed BIAS voltage for proper operation of 3.3 V;

Powered from V_{in}:

$$P = 40 \times 6.25e{-}3 = 250\ mW$$

Powered from the BIAS pin:

$$P = 3.3 \times 6.25e{-}3 = 21\ mW$$

The power savings is 229 mW.

Minimum Load Requirement

As pointed out in the previous section, a minimum load is required for this regulator due to the predriver current feeding the output. Placing a resistor equal to V_O divided by 12 mA should prevent any voltage overshoot at light load conditions. Alternatively, the feedback resistors can be valued properly to consume 12 mA current.

COMPONENT SELECTION

Input Capacitor

In a buck converter, the input capacitor witnesses pulsed current with an amplitude equal to the load current. This pulsed current and the ESR of the input capacitors determine the V_{IN} ripple voltage, which is shown in Figure 19. For V_{IN} ripple, low ESR is a critical requirement for the input capacitor selection. The pulsed input current possesses a significant AC component, which is absorbed by the input capacitors.

The RMS current of the input capacitor can be calculated using:

$$I_{RMS} = I_O \sqrt{D(1 - D)}$$

where:

D = switching duty cycle which is equal to V_O/V_{IN}.

I_O = load current.

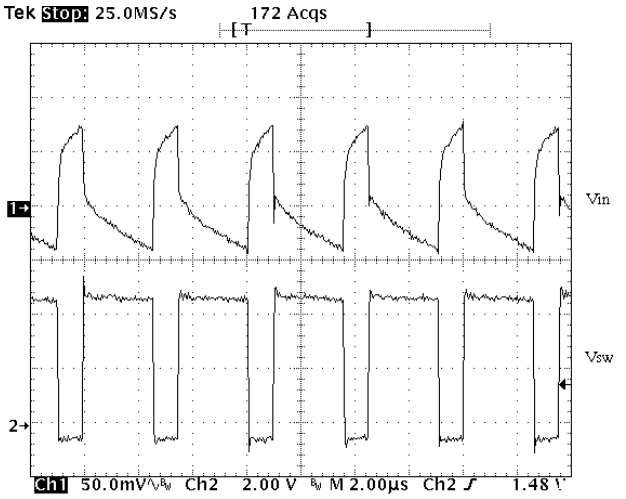


Figure 19. Input Voltage Ripple in a Buck Converter

To calculate the RMS current, multiply the load current with the constant given by Figure 20 at each duty cycle. It is a common practice to select the input capacitor with an RMS current rating more than half the maximum load current. If multiple capacitors are paralleled, the RMS current for each capacitor should be the total current divided by the number of capacitors.

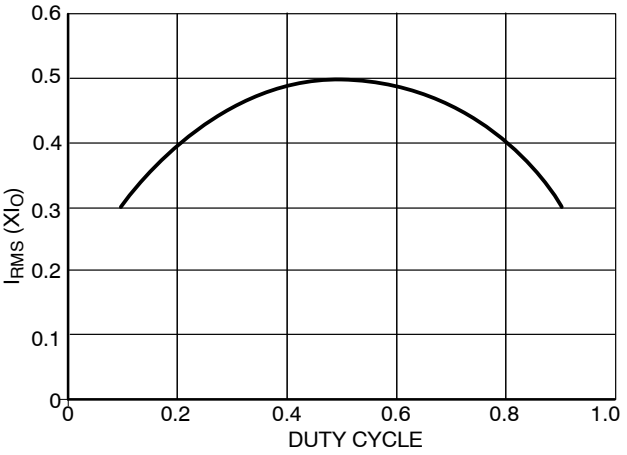


Figure 20. Input Capacitor RMS Current can be Calculated by Multiplying Y Value with Maximum Load Current at any Duty Cycle

Selecting the capacitor type is determined by each design's constraint and emphasis. The aluminum electrolytic capacitors are widely available at lowest cost. Their ESR and Equivalent Series Inductor (ESL) are relatively high. Multiple capacitors are usually paralleled to achieve lower ESR. In addition, electrolytic capacitors usually need to be paralleled with a ceramic capacitor for filtering high frequency noises. The OS−CON are solid aluminum electrolytic capacitors, and therefore has a much lower ESR. Recently, the price of the OS−CON capacitors has dropped significantly so that it is now feasible to use them for some low cost designs. Electrolytic capacitors are

physically large, and not used in applications where the size, and especially height is the major concern.

Ceramic capacitors are now available in values over 10 μF. Since the ceramic capacitor has low ESR and ESL, a single ceramic capacitor can be adequate for both low frequency and high frequency noises. The disadvantage of ceramic capacitors are their high cost. Solid tantalum capacitors can have low ESR and small size. However, the reliability of the tantalum capacitor is always a concern in the application where the capacitor may experience surge current.

Output Capacitor

In a buck converter, the requirements on the output capacitor are not as critical as those on the input capacitor. The current to the output capacitor comes from the inductor and thus is triangular. In most applications, this makes the RMS ripple current not an issue in selecting output capacitors.

The output ripple voltage is the sum of a triangular wave caused by ripple current flowing through ESR, and a square wave due to ESL. Capacitive reactance is assumed to be small compared to ESR and ESL. The peak−to−peak ripple current of the inductor is:

$$I_{P-P} = \frac{V_O(V_{IN} - V_O)}{(V_{IN})(L)(f_S)}$$

$V_{RIPPLE(ESR)}$, the output ripple due to the ESR, is equal to the product of I_{P-P} and ESR. The voltage developed across the ESL is proportional to the di/dt of the output capacitor. It is realized that the di/dt of the output capacitor is the same as the di/dt of the inductor current. Therefore, when the switch turns on, the di/dt is equal to $(V_{IN} - V_O)/L$, and it becomes V_O/L when the switch turns off. The total ripple voltage induced by ESL can then be derived from

$$V_{RIPPLE(ESL)} = ESL(\frac{V_{IN}}{L}) + ESL(\frac{V_{IN} - V_O}{L}) = ESL(\frac{V_{IN}}{L})$$

The total output ripple is the sum of the $V_{RIPPLE(ESR)}$ and $V_{RIPPLE(ESR)}$.

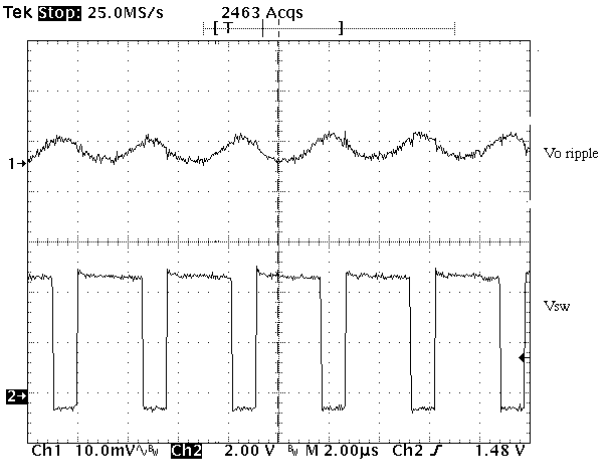


Figure 21. The Output Voltage Ripple Using Two 10 μF Ceramic Capacitors in Parallel

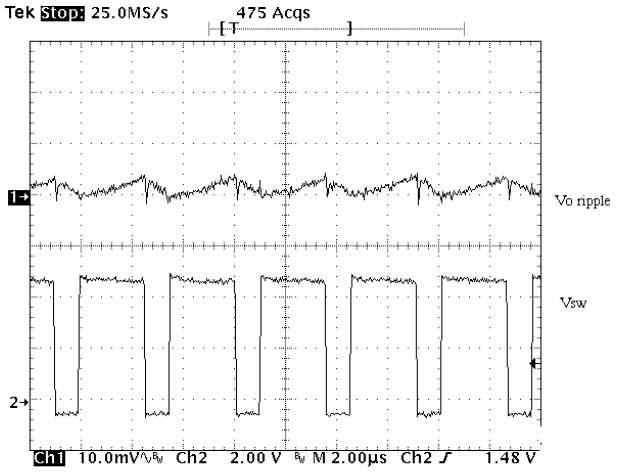


Figure 22. The Output Voltage Ripple Using One 100 μF POSCAP Capacitor

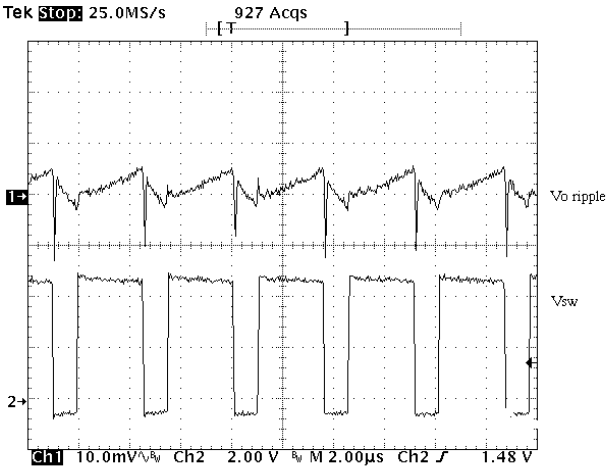


Figure 23. The Output Voltage Ripple Using One 100 μF OS−CON

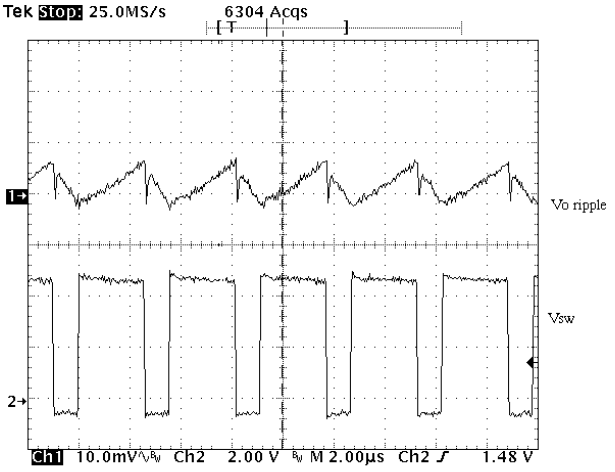


Figure 24. The Output Voltage Ripple Using One 100 μF Tantalum Capacitor

Figure 21 to Figure 24 show the output ripple of a 5.0 V to 3.3 V/500 mA regulator using 22 μH inductor and various capacitor types. At the switching frequency, the low ESR and ESL make the ceramic capacitors behave capacitively as shown in Figure 21. Additional paralleled ceramic capacitors will further reduce the ripple voltage, but inevitably increase the cost. “POSCAP”, manufactured by SANYO, is a solid electrolytic capacitor. The anode is sintered tantalum and the cathode is a highly conductive polymerized organic semiconductor. TPC series, featuring low ESR and low profile, is used in the measurement of Figure 22. It is shown that POSCAP presents a good balance of capacitance and ESR, compared with a ceramic capacitor. In this application, the low ESR generates less than 5.0 mV of ripple and the ESL is almost unnoticeable. The ESL of the through−hole OS−CON capacitor give rise to the inductive impedance. It is evident from Figure 23 which shows the step rise of the output ripple on the switch turn−on and large spike on the switch turn−off. The ESL prevents the output capacitor from quickly charging up the parasitic capacitor of the inductor when the switch node is pulled below ground through the catch diode conduction. This results in the spike associated with the falling edge of the switch node. The D package tantalum capacitor used in Figure 24 has the same footprint as the POSCAP, but doubles the height. The ESR of the tantalum capacitor is apparently higher than the POSCAP. The electrolytic and tantalum capacitors provide a low−cost solution with compromised performance. The reliability of the tantalum capacitor is not a serious concern for output filtering because the output capacitor is usually free of surge current and voltage.

Diode Selection

The diode in the buck converter provides the inductor current path when the power switch turns off. The peak reverse voltage is equal to the maximum input voltage. The peak conducting current is clamped by the current limit of the IC. The average current can be calculated from:

$$I_{D(AVG)} = \frac{I_O(V_{IN} - V_O)}{V_{IN}}$$

The worse case of the diode average current occurs during maximum load current and maximum input voltage. For the diode to survive the short circuit condition, the current rating of the diode should be equal to the Foldback Current Limit. See Table 1 for Schottky diodes from ON Semiconductor which are suggested for CS5141X regulator.

Inductor Selection

When choosing inductors, one might have to consider maximum load current, core and copper losses, component height, output ripple, EMI, saturation and cost. Lower inductor values are chosen to reduce the physical size of the inductor. Higher value cuts down the ripple current, core losses and allows more output current. For most applications, the inductor value falls in the range between 2.2 μH and 22 μH. The saturation current ratings of the inductor shall not exceed the $I_{L(PK)}$, calculated according to

$$I_{L(PK)} = I_O + \frac{V_O(V_{IN} - V_O)}{2(f_S)(L)(V_{IN})}$$

The DC current through the inductor is equal to the load current. The worse case occurs during maximum load current. Check the vendor’s spec to adjust the inductor value undercurrent loading. Inductors can lose over 50% of inductance when it nears saturation.

The core materials have a significant effect on inductor performance. The ferrite core has benefits of small physical size, and very low power dissipation. But be careful not to operate these inductors too far beyond their maximum ratings for peak current, as this will saturate the core. Powered Iron cores are low cost and have a more gradual saturation curve. The cores with an open magnetic path, such as rod or barrel, tend to generate high magnetic field radiation. However, they are usually cheap and small. The cores providing a close magnetic loop, such as pot−core and toroid, generate low electro−magnetic interference (EMI).

There are many magnetic component vendors providing standard product lines suitable for CS5141X. Table 2 lists three vendors, their products and contact information.

Table 1.

Part Number	$V_{BREAKDOWN}$ (V)	$I_{AVERAGE}$ (A)	$V_{(F)}$ (V) @ $I_{AVERAGE}$	Package
1N5817	20	1.0	0.45	Axial Lead
1N5818	30	1.0	0.55	Axial Lead
1N5819	40	1.0	0.6	Axial Lead
MBR0520	20	0.5	0.385	SOD−123
MBR0530	30	0.5	0.43	SOD−123
MBR0540	40	0.5	0.53	SOD−123
MBRS120	20	1.0	0.55	SMB
MBRS130	30	1.0	0.395	SMB
MBRS140	40	1.0	0.6	SMB

Table 2.

Vendor	Product Family	Web Site	Telephone
Coiltronics	UNI−Pac1/2: SMT, barrel THIN−PAC: SMT, toroid, low profile CTX: Leaded, toroid	www.coiltronics.com	(516) 241−7876
Coilcraft	DO1608: SMT, barrel DS/DT 1608: SMT, barrel, magnetically shielded DO3316: SMT, barrel DS/DT 3316: SMT, barrel, magnetically shielded DO3308: SMT, barrel, low profile	www.coilcraft.com	(800) 322−2645
Pulse	−	www.pulseeng.com	(619) 674−8100

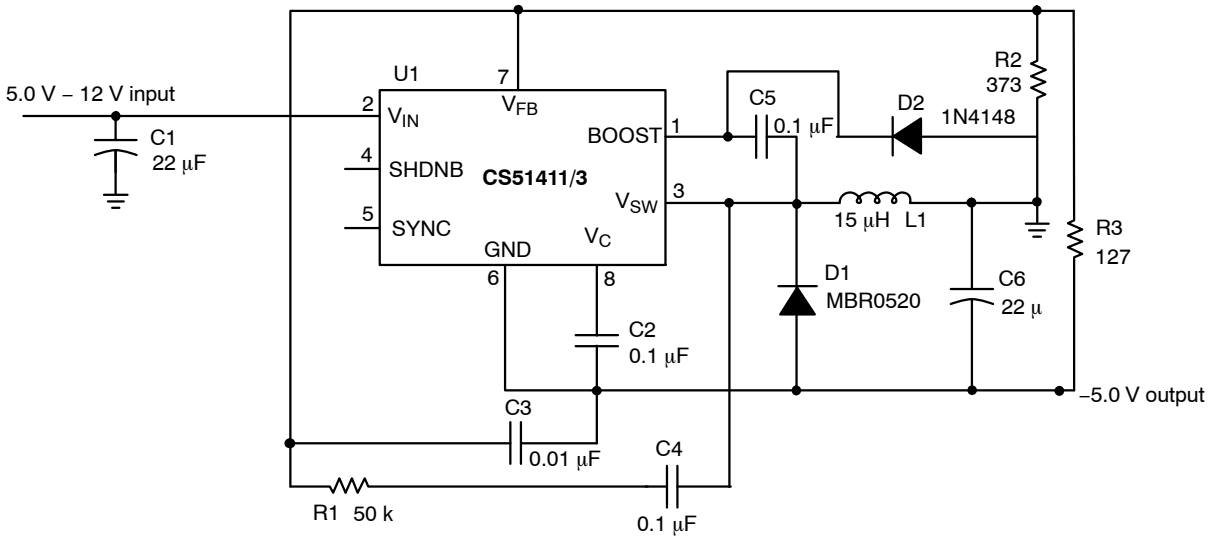


Figure 25. Additional Application Diagram, 5.0 V – 12 V to –5.0 V/400 mA Inverting Converter

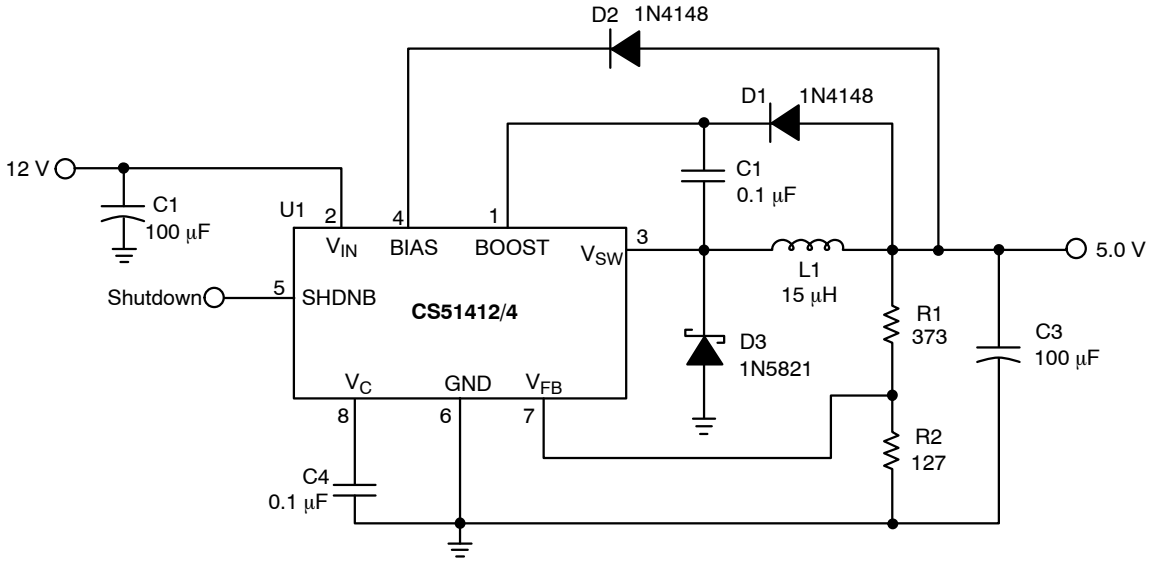


Figure 26. Additional Application Diagram, 12 V to 5.0 V/1.0 A Buck Converter using the BIAS Pin

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
CS51411ED8G	−40°C < T_A < 85°C	SOIC−8 (Pb−Free)	98 Units/Rail
CS51411EDR8G		SOIC−8 (Pb−Free)	2500 Tape & Reel
CS51411EMNR2G		DFN18 (Pb−Free)	2500 Tape & Reel
CS51412ED8G		SOIC−8 (Pb−Free)	98 Units/Rail
CS51412EDR8G		SOIC−8 (Pb−Free)	2500 Tape & Reel
CS51412EMNR2G		DFN18 (Pb−Free)	2500 Tape & Reel
CS51413ED8G		SOIC−8 (Pb−Free)	98 Units/Rail
CS51413EDR8G		SOIC−8 (Pb−Free)	2500 Tape & Reel
CS51413EMNR2G		DFN18 (Pb−Free)	2500 Tape & Reel
CS51414ED8G		SOIC−8 (Pb−Free)	98 Units/Rail
CS51414EDR8G		SOIC−8 (Pb−Free)	2500 Tape & Reel
CS51414EMNR2G		DFN18 (Pb−Free)	2500 Tape & Reel
CS51411GD8G	0°C < T_A < 70°C	SOIC−8 (Pb−Free)	98 Units/Rail
CS51411GDR8G		SOIC−8 (Pb−Free)	2500 Tape & Reel
CS51411GMNR2G		DFN18 (Pb−Free)	2500 Tape & Reel
CS51412GD8G		SOIC−8 (Pb−Free)	98 Units/Rail
CS51412GDR8G		SOIC−8 (Pb−Free)	2500 Tape & Reel
CS51412GMNR2G		DFN18 (Pb−Free)	2500 Tape & Reel
CS51413GD8G		SOIC−8 (Pb−Free)	98 Units/Rail
CS51413GDR8G		SOIC−8 (Pb−Free)	2500 Tape & Reel
CS51413GMNR2G		DFN18 (Pb−Free)	2500 Tape & Reel
CS51414GD8G		SOIC−8 (Pb−Free)	98 Units/Rail
CS51414GDR8G		SOIC−8 (Pb−Free)	2500 Tape & Reel
CS51414GMNR2G		DFN18 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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CASE 505−01
ISSUE D

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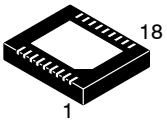
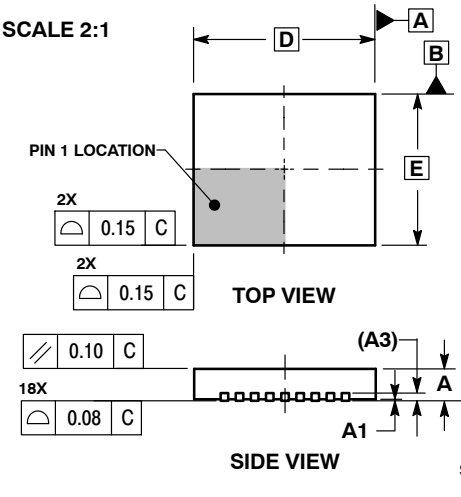
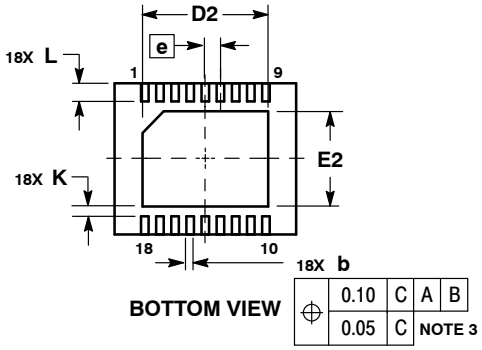
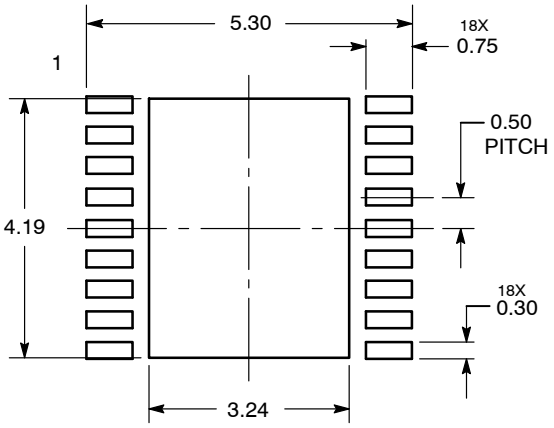


SCALE 2:1





SOLDERING FOOTPRINT

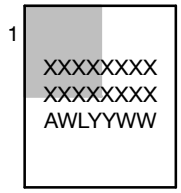


DIMENSIONS: MILLIMETERS

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	3.98	4.28
E	5.00 BSC	
E2	2.98	3.28
e	0.50 BSC	
K	0.20	−−−
L	0.45	0.65

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**18 PIN DFN, 6X5 MM. 0.5 MM PITCH**	**PAGE 1 OF 1**

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SCALE 1:1

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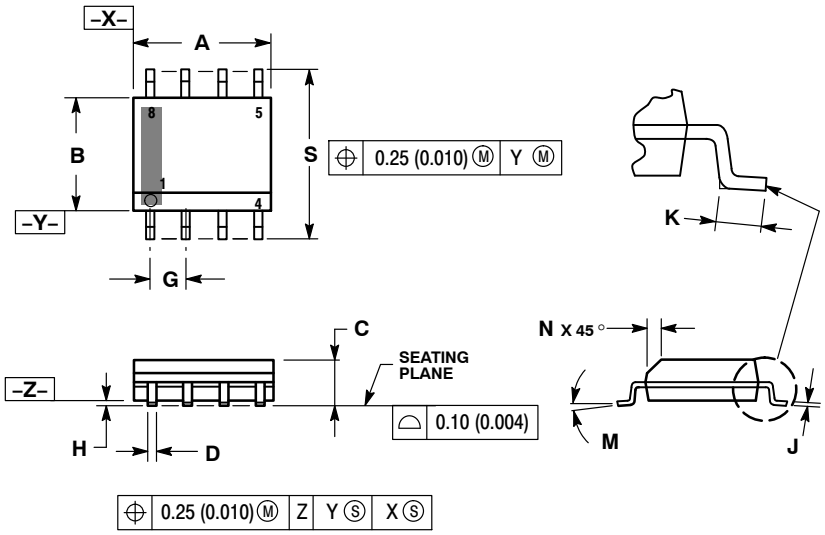
ISSUE AK

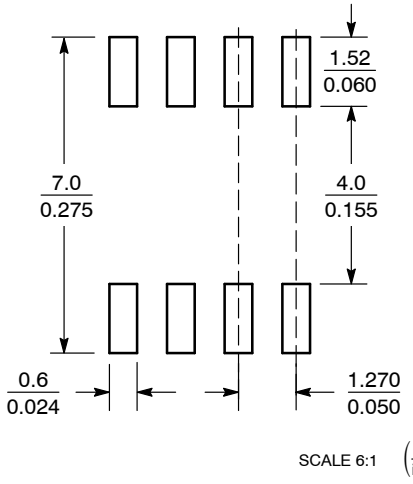
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

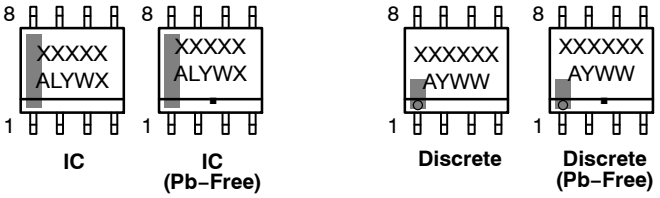
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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