

Sample &

Buy



SN65LVDS100, SN65LVDT100, SN65LVDS101, SN65LVDT101

29

SLLS516E - AUGUST 2002 - REVISED JULY 2015

Reference

Design

# SN65LVDx10x Differential Translator/Repeater

Technical

Documents

#### 1 Features

- Designed for Signaling Rates ≥ 2 Gbps
- Total Jitter < 65 ps
- Low-Power Alternative for the MC100EP16
- Low 100-ps (Maximum) Part-to-Part Skew
- 25 mV of Receiver Input Threshold Hysteresis Over 0-V to 4-V Input Voltage Range
- Inputs Electrically Compatible With LVPECL, CML, and LVDS Signal Levels
- 3.3-V Supply Operation
- LVDT Integrates 110-Ω Terminating Resistor .
- Offered in SOIC and MSOP

#### Applications 2

V<sub>CC</sub>

Δ

Δ

- Wireless Infrastructure
- **Telecom Infrastructure**
- Printers

# 3 Description

Tools &

Software

The SN65LVDS100, SN65LVDT100, SN65LVDS101, and SN65LVDT101 are high-speed differential receivers and drivers connected as repeaters. The receiver accepts low-voltage differential signaling (LVDS), positive-emitter-coupled logic (PECL), or current-mode logic (CML) input signals at rates up to 2 Gbps and repeats it as either an LVDS or PECL output signal. The signal path through the device is differential for low radiated emissions and minimal added jitter.

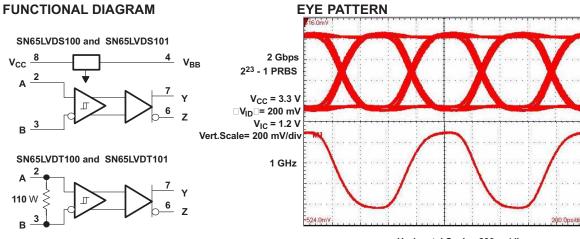
Support &

Community

### Device Information<sup>(1)</sup>

| PART NUMBER  | PACKAGE   | BODY SIZE (NOM)   |
|--------------|-----------|-------------------|
|              | SOIC (8)  | 4.90 mm × 3.91 mm |
| SN65LVDS100  | VSSOP (8) | 3.00 mm × 3.00 mm |
| SN65LVDT100  | SOIC (8)  | 4.90 mm × 3.91 mm |
|              | VSSOP (8) | 3.00 mm × 3.00 mm |
| SN65LVDS101  | SOIC (8)  | 4.90 mm × 3.91 mm |
| SIN05LVD5101 | VSSOP (8) | 3.00 mm × 3.00 mm |
| SN65LVDT101  | SOIC (8)  | 4.90 mm × 3.91 mm |
|              | VSSOP (8) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



# **Dual Eye Diagram**

Horizontal Scale= 200 ps/div





10.2 Functional Block Diagram ...... 15

14.3 Trademarks ...... 33 

Mechanical, Packaging, and Orderable

11 Application and Implementation...... 21 11.2 Typical Application ..... 22 13.1 Layout Guidelines ...... 30 13.2 Layout Example ...... 32 14 Device and Documentation Support ...... 33 14.1 Related Links ...... 33 

Feature Description..... 15 

www.ti.com

# Table of Contents

10.3

10.4

14.2

15

| 1  | Feat | tures 1                            |
|----|------|------------------------------------|
| 2  | Арр  | lications 1                        |
| 3  | Des  | cription 1                         |
| 4  | Rev  | ision History 2                    |
| 5  | Des  | cription (Continued) 3             |
| 6  | Dev  | ice Options 3                      |
| 7  | Pin  | Configuration and Functions 3      |
| 8  | Spe  | cifications 4                      |
|    | 8.1  | Absolute Maximum Ratings 4         |
|    | 8.2  | ESD Ratings 4                      |
|    | 8.3  | Recommended Operating Conditions 4 |
|    | 8.4  | Thermal Information 5              |
|    | 8.5  | Electrical Characteristics 5       |
|    | 8.6  | Switching Characteristics 6        |
|    | 8.7  | Typical Characteristics 7          |
| 9  | Para | ameter Measurement Information 12  |
| 10 | Deta | ailed Description 15               |
|    | 10.1 | Overview                           |
|    |      |                                    |

# **4** Revision History

2

| CI | hanges from Revision D (December 2014) to Revision E   | Page |
|----|--|------|
| •  | Changed Features From: "Over 0-V to 4-V Common-Mode Range" To: "Over 0-V to 4-V Input Voltage Range" | 1    |
|    |  |      |

#### Changes from Revision C (June 2004) to Revision D

Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device 

Page



# 5 Description (Continued)

The outputs of the SN65LVDS100 and SN65LVDT100 are LVDS levels as defined by TIA/EIA-644-A. The outputs of the SN65LVDS101 and SN65LVDT101 are compatible with 3.3-V PECL levels. Both drive differential transmission lines with nominally  $100-\Omega$  characteristic impedance.

The SN65LVDT100 and SN65LVDT101 include a 110- $\Omega$  differential line termination resistor for less board space, fewer components, and the shortest stub length possible. They do not include the V<sub>BB</sub> voltage reference found in the SN65LVDS100 and SN65LVDS101. V<sub>BB</sub> provides a voltage reference of typically 1.35 V below V<sub>CC</sub> for use in receiving single-ended input signals and is particularly useful with single-ended 3.3-V PECL inputs. When V<sub>BB</sub> is not used, it should be unconnected or open.

All devices are characterized for operation from -40°C to 85°C.

#### 6 **Device Options**

| ORDERABLE PART NUMBER | OUTPUT | TERMINATION RESISTOR | V <sub>BB</sub> |
|-----------------------|--------|----------------------|-----------------|
| SN65LVDS100D          | LVDS   | No                   | Yes             |
| SN65LVDS100DGK        | LVDS   | No                   | Yes             |
| SN65LVDT100D          | LVDS   | Yes                  | No              |
| SN65LVDT100DGK        | LVDS   | Yes                  | No              |
| SN65LVDS101D          | LVPECL | No                   | Yes             |
| SN65LVDS101DGK        | LVPECL | No                   | Yes             |
| SN65LVDT101D          | LVPECL | Yes                  | No              |
| SN65LVDT101DGK        | LVPECL | Yes                  | No              |

# 7 Pin Configuration and Functions

NC [

R

VBBE



1

2

3

4

8

7

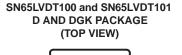
6

5

\_Υ

Ζ Ζ

🗀 GND





NC = Not Connected

#### **Pin Functions**

|                 | PIN                         |                             |     |                                   |
|-----------------|-----------------------------|-----------------------------|-----|-----------------------------------|
| NAME            | SN65LVDS100,<br>SN65LVDS101 | SN65LVDT100,<br>SN65LVDT101 | I/O | DESCRIPTION                       |
| А               | 2                           | 2                           | I   | Differential non-inverting input  |
| В               | 3                           | 3                           | I   | Differential inverting input      |
| GND             | 5                           | 5                           | _   | Ground                            |
| NC              | 1                           | 1, 4                        | _   | No connect                        |
| V <sub>BB</sub> | 4                           | —                           | 0   | Voltage reference                 |
| V <sub>CC</sub> | 8                           | 8                           | _   | Supply voltage                    |
| Y               | 7                           | 7                           | 0   | Differential non-inverting output |
| Z               | 6                           | 6                           | 0   | Differential inverting output     |

Copyright © 2002–2015, Texas Instruments Incorporated

# 8 Specifications

# 8.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range unless otherwise noted

|                 |  | MIN  | MAX | UNIT |
|-----------------|--|------|-----|------|
| V <sub>CC</sub> | Supply voltage range <sup>(2)</sup>                              | -0.5 | 4   | V    |
| I <sub>BB</sub> | V <sub>BB</sub> output current                                   | -0.5 | 0.5 | mA   |
| VI              | Veltage range (A. P. V. 7)                                       | 0    | 4.3 | V    |
| Vo              | Voltage range, (A, B, Y, Z)                                      | 0    | 4.3 | v    |
| V <sub>ID</sub> | Differential voltage, $ V_A - V_B $ ('LVDT100 and 'LVDT101 only) |      | 1   | V    |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

#### 8.2 ESD Ratings

|                    |                         |                                       |  | VALUE | UNIT |
|--------------------|-------------------------|---------------------------------------|--|-------|------|
|                    |                         | Human body model (HBM), per           | Pins 2, 3, 5, 6, 7                           | ±5000 | V    |
| V <sub>(ESD)</sub> | Electrostatic discharge | ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup> | All pins except 2, 3, 5, 6, 7                | ±2000 | V    |
|                    |                         | Charged-device model (CDM), per JE    | DEC specification JESD22-C101 <sup>(2)</sup> | ±1500 | V    |

(1) Tested in accordance with JEDEC Standard 22, Test Method A114-A.7.

(2) Tested in accordance with JEDEC Standard 22, Test Method C101.

#### 8.3 Recommended Operating Conditions

|   |                      | MIN                 | NOM | MAX | UNIT |
|---|----------------------|---------------------|-----|-----|------|
| Supply voltage, V <sub>CC</sub>   |                      | 3                   | 3.3 | 3.6 | V    |
| Magnitude of differential input values a 1)/                                    | 'LVDS100 or 'LVDS101 | 0.1                 |     | 1   | N/   |
| Magnitude of differential input voltage  V <sub>ID</sub>                        | 'LVDT100 or 'LVDT101 | 0.1                 |     | 0.8 | V    |
| Input voltage (any combination of common-mode or input signals), V <sub>I</sub> |                      | 0                   |     | 4   | V    |
| V <sub>BB</sub> output current, I <sub>O(VBB)</sub>                             |                      | -400 <sup>(1)</sup> |     | 12  | μA   |
| Operating free-air temperature, T <sub>A</sub>                                  |                      |                     |     | 85  | °C   |

(1) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet.

4



# 8.4 Thermal Information

|                |   |        | SN65LVDS100, SN65LVDT100, SN65LVDS101,<br>SN65LVDT101 |      |  |  |
|----------------|---|--------|---|------|--|--|
|                | THERMAL METRIC <sup>(1)</sup>                   | D      | DGK   | UNIT |  |  |
|                |   | 8 PINS | 8 PINS  |      |  |  |
| $R_{\thetaJA}$ | Junction-to-ambient thermal resistance          | 208    | 263   | °C/W |  |  |
|                | Power dissipation rating: $T_A \le 25^{\circ}C$ | 151    | 377   |      |  |  |
|                | Power dissipation rating: $T_A \le 85^{\circ}C$ | 192    | 481   | mW   |  |  |

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

# 8.5 Electrical Characteristics

over recommended operating conditions (unless otherwise specified)

|                     | PARAMETER   | TEST CONDITIONS  | MIN                   | TYP <sup>(1)</sup>     | MAX                   | UNIT |  |
|---------------------|---|--|-----------------------|------------------------|-----------------------|------|--|
|                     | Supply current, 'LVDx100                                    | No load or input   |                       | 25                     | 30                    |      |  |
| ICC                 | Supply current, 'LVDx101                                    | $R_L = 50 \Omega$ to 1 V, No input   |                       | 50                     | 61                    | mA   |  |
|                     | Device power dissipation, 'LVDx100                          | $R_L$ = 100 Ω, No input  |                       |                        | 110                   |      |  |
| P <sub>D</sub>      | Device power dissipation, 'LVDx101                          | Y and Z to $V_{CC}$ – 2 V through 50 $\Omega$ No input   |                       | 116                    | 142                   | mW   |  |
| $V_{BB}$            | Reference voltage output, 'LVDS100 or 'LVDS101              | I <sub>O</sub> = -400 μA or 12 μA  | V <sub>CC</sub> – 1.4 | V <sub>CC</sub> – 1.35 | V <sub>CC</sub> – 1.3 | mV   |  |
| SN65LV              | DS100 and SN65LVDS101 INPUT CHAR                            | ACTERISTICS (see Figure 30)  |                       |                        |                       |      |  |
| V <sub>IT+</sub>    | Positive-going differential input voltage threshold         | Coo Figure 20 and Table 4  |                       |                        | 100                   |      |  |
| V <sub>IT-</sub>    | Negative-going differential input voltage threshold         | See Figure 30 and Table 1  | -100                  |                        |                       | mV   |  |
| I,                  | Input current   | V <sub>I</sub> = 0 V or 2.4 V<br>Second input at 1.2 V   | -20                   |                        | 20                    | μA   |  |
|                     |   | V <sub>I</sub> = 4 V, Second input at 1.2 V  |                       |                        | 33                    | μA   |  |
|                     | Power off input current                                     | $V_{CC} = 1.5 \text{ V}, \text{ V}_{I} = 0 \text{ V} \text{ or } 2.4 \text{ V}$<br>Second input at 1.2 V | -20                   |                        | 20                    | μA   |  |
| I <sub>I(OFF)</sub> |   | $V_{CC} = 1.5 \text{ V}, V_I = 4 \text{ V}$<br>Second input at 1.2 V                                     |                       |                        | 33                    |      |  |
| I <sub>IO</sub>     | Input offset current ( I <sub>IA</sub> - I <sub>IB</sub>  ) | $V_{IA} = V_{IB}, 0 \le V_{IA} \le 4 V$  | -6                    |                        | 6                     | μA   |  |
| Ci                  | Small-signal input capacitance to GND                       | V <sub>1</sub> = 1.2 V   |                       | 0.6                    |                       | pF   |  |
| SN65LV              | DT100 and SN65LVDT101 INPUT CHAR                            | ACTERISTICS (see Figure 30)  |                       |                        |                       |      |  |
| V <sub>IT+</sub>    | Positive-going differential input voltage threshold         | Cas Figure 20 and Table 4  |                       |                        | 100                   |      |  |
| V <sub>IT-</sub>    | Negative-going differential input voltage threshold         | See Figure 30 and Table 1  | -100                  |                        |                       | mV   |  |
|                     | logut ourroat   | $V_I = 0 V \text{ or } 2.4 V$ , Other input open   | -40                   |                        | 40                    | ۵    |  |
| I <sub>I</sub>      | Input current   | V <sub>I</sub> = 4 V, Other input open   |                       |                        | 66                    | μA   |  |
|                     | Device off inside overage                                   | $V_{CC}$ = 1.5 V, V <sub>I</sub> = 0 V or 2.4 V<br>Other input open                                      | -40                   |                        | 40                    |      |  |
| I <sub>I(OFF)</sub> | Power off input current                                     | $V_{CC} = 1.5 \text{ V}, \text{ V}_{I} = 4 \text{ V}$<br>Other input open                                |                       |                        | 66                    | μA   |  |
| D                   |   | V <sub>ID</sub> = 300 mV or 500 mV<br>V <sub>IC</sub> = 0 V or 2.4 V                                     | 90                    | 110                    | 132                   | 0    |  |
| R <sub>(T)</sub>    | Differential input resistance                               | $V_{CC} = 0 V, V_{ID} = 300 mV \text{ or } 500 mV$<br>$V_{IC} = 0 V \text{ or } 2.4 V$                   | 90                    | 110                    | 132                   | Ω    |  |
| C <sub>i</sub>      | Small-signal differential input capacitance                 | V <sub>I</sub> = 1.2 V   |                       | 0.6                    |                       | pF   |  |

(1) Typical values are with a 3.3-V supply voltage and room temperature

#### **EXAS ISTRUMENTS**

# SN65LVDS100, SN65LVDT100, SN65LVDS101, SN65LVDT101

SLLS516E - AUGUST 2002 - REVISED JULY 2015

www.ti.com

# Electrical Characteristics (continued)

| over recommended | operating | conditions | (unless  | otherwise  | specified) |
|------------------|-----------|------------|----------|------------|------------|
|                  | oporating | oonaniono  | (0110000 | 0110110100 | opcomoa,   |

|                     | PARAMETER   | TEST CONDITIONS   | MIN                    | TYP <sup>(1)</sup>     | MAX                    | UNIT |
|---------------------|---|---|------------------------|------------------------|------------------------|------|
| SN65LVD             | 6100 and SN65LVDT100 OUTPUT CH  | ARACTERISTICS (see Figure 30)                             |                        |                        | P                      |      |
| V <sub>OD</sub>     | Differential output voltage magnitude   |   | 247                    | 340                    | 454                    |      |
| Δ V <sub>OD</sub>   | Change in differential output voltage magnitude between logic states          | See Figure 31   | -50                    |                        | 50                     | mV   |
| V <sub>OC(SS)</sub> | Steady-state common-mode output voltage                                       |   | 1.125                  |                        | 1.375                  | V    |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-<br>mode output voltage between logic<br>states | See Figure 32   | -50                    |                        | 50                     | mV   |
| V <sub>OC(PP)</sub> | Peak-to-peak common-mode output voltage                                       |   |                        | 50                     | 150                    | mV   |
| l <sub>os</sub>     | Short-circuit output current  | $V_{O(Y)}$ or $V_{O(Z)} = 0$ V                            | -24                    |                        | 24                     | mA   |
| I <sub>OS(D)</sub>  | Differential short-circuit output<br>current                                  | $V_{OD} = 0 V$  | -12                    |                        | 12                     | mA   |
| SN65LVD             | S101 and SN65LVDT101 OUTPUT CH  | ARACTERISTICS (see Figure 30)                             |                        |                        |                        |      |
| V                   |   | 50 $\Omega$ to V <sub>CC</sub> – 2 V, See Figure 39       | V <sub>CC</sub> – 1.25 | V <sub>CC</sub> – 1.02 | V <sub>CC</sub> – 0.9  | V    |
| V <sub>OH</sub>     | High-level output voltage   | $V_{CC}$ = 3.3 V, 50- $\Omega$ load to 2.3 V              | 2055                   | 2280                   | 2405                   | mV   |
| V                   |   | 50 $\Omega$ to V <sub>CC</sub> – 2 V, See Figure 39       | V <sub>CC</sub> – 1.83 | V <sub>CC</sub> – 1.61 | V <sub>CC</sub> – 1.53 | V    |
| V <sub>OL</sub>     | Low-level output voltage  | $V_{CC}$ = 3.3 V, 50- $\Omega$ load to 2.3 V              | 1475                   | 1690                   | 1775                   | mV   |
| V <sub>od</sub>     | Differential output voltage magnitude   | 50- $\Omega$ load to V <sub>CC</sub> – 2 V, See Figure 39 | 475                    | 575                    | 750                    | mV   |

# 8.6 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER             |  | TEST CONDITIONS           | MIN   | TYP <sup>(1)</sup> | MAX | UNIT |    |
|-----------------------|--|---------------------------|---|--------------------|-----|------|----|
|                       | Propagation delay time,                          | 'LVDx100                  |   | 300                | 470 | 800  | 20 |
| t <sub>PLH</sub>      | low-to-high-level output                         | 'LVDx101                  |   | 400                | 630 | 900  | ps |
| +                     | Propagation delay time,                          | 'LVDx100                  |   | 300                | 470 | 800  | 20 |
| t <sub>PHL</sub>      | high-to-low-level output                         | 'LVDx100                  |   | 400                | 630 | 900  | ps |
| t <sub>r</sub>        | Differential output signal (20% to 80%)          | rise time                 | See Figure 33   |                    |     | 220  | ps |
| t <sub>f</sub>        | Differential output signal (20% to 80%)          | fall time                 |   |                    |     | 220  | ps |
| t <sub>sk(p)</sub>    | Pulse skew ( t <sub>PHL</sub> – t <sub>PLH</sub> | ) <sup>(2)</sup>          |   |                    | 5   | 50   | ps |
| t <sub>sk(pp)</sub>   | Part-to-part skew <sup>(3)</sup>                 |                           | V <sub>ID</sub> = 0.2 V, See Figure 33  |                    |     | 100  | ps |
| t <sub>jit(per)</sub> | RMS period jitter <sup>(4)</sup>                 |                           | 1 GHz 50% duty-cycle square-wave  |                    | 1   | 3.7  | ps |
| t <sub>jit(cc)</sub>  | Peak cycle-to-cycle jitter                       | (5)                       | input<br>V <sub>ID</sub> = 200 mV, V <sub>IC</sub> = 1.2 V<br>See Figure 34                               |                    | 6   | 23   | ps |
| t <sub>jit(pp)</sub>  | Peak-to-peak jitter                              |                           | 2 GHz PRBS, $2^{23}$ – 1 run length<br>V <sub>ID</sub> = 200 mV, V <sub>IC</sub> = 1.2 V<br>See Figure 34 |                    | 28  | 65   | ps |
| t <sub>jit(det)</sub> | Peak-to-peak determinis                          | tic jitter <sup>(6)</sup> | 2 GHz PRBS, $2^7 - 1$ run length<br>V <sub>ID</sub> = 200 mV, V <sub>IC</sub> = 1.2 V<br>See Figure 34    |                    | 17  | 48   | ps |

(1) All typical values are at 25°C and with a 3.3-V supply.

 $t_{sk(p)}$  is the magnitude of the time difference between the  $t_{PLH}$  and  $t_{PHL}$  of any output of a single device.  $t_{sk(pp)}$  is the magnitude of the time difference in propagation delay time between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits. Period jitter is the deviation in cycle time of a signal with respect to the ideal period over a random sample of 1,000,000 cycles. (3)

(4)

(5) Cycle-to-cycle jitter is the variation in cycle time of a signal between adjacent cycles, over a random sample of 1,000 adjacent cycle pairs.

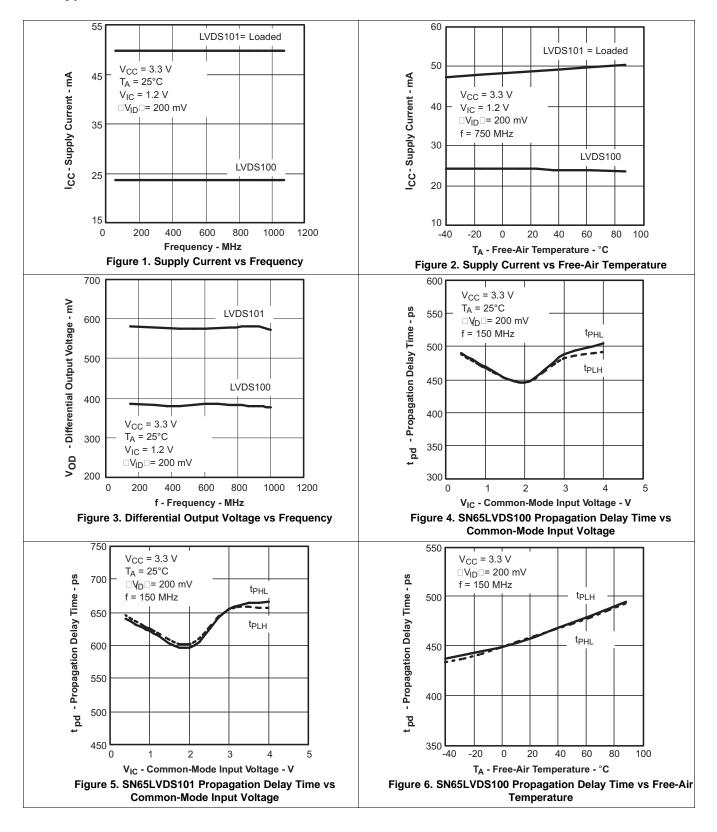
(6) Deterministic jitter is the sum of pattern-dependent jitter and pulse-width distortion.

6 Submit Documentation Feedback

<sup>(2)</sup> 



### 8.7 Typical Characteristics



Copyright © 2002–2015, Texas Instruments Incorporated

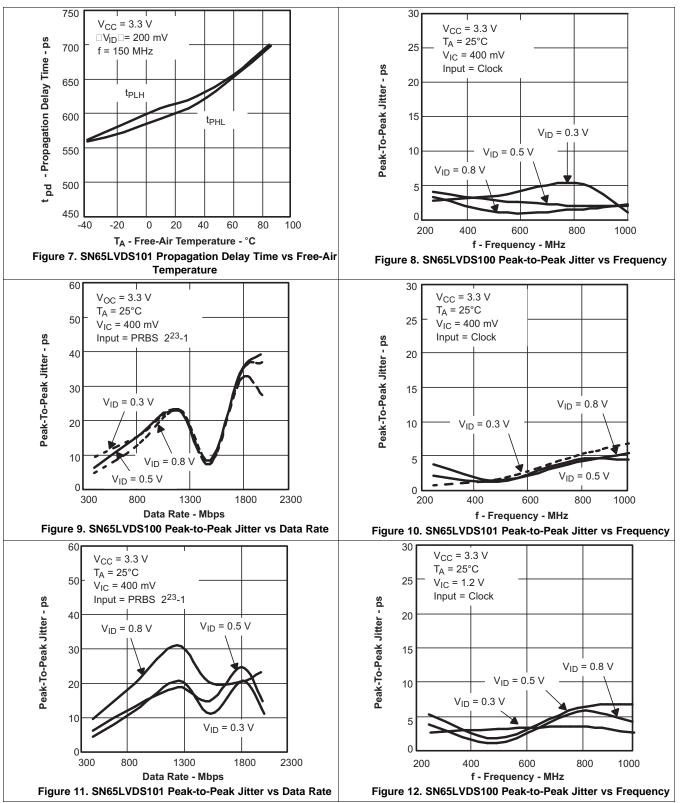


# SN65LVDS100, SN65LVDT100, SN65LVDS101, SN65LVDT101

SLLS516E - AUGUST 2002 - REVISED JULY 2015

www.ti.com

#### **Typical Characteristics (continued)**



Submit Documentation Feedback

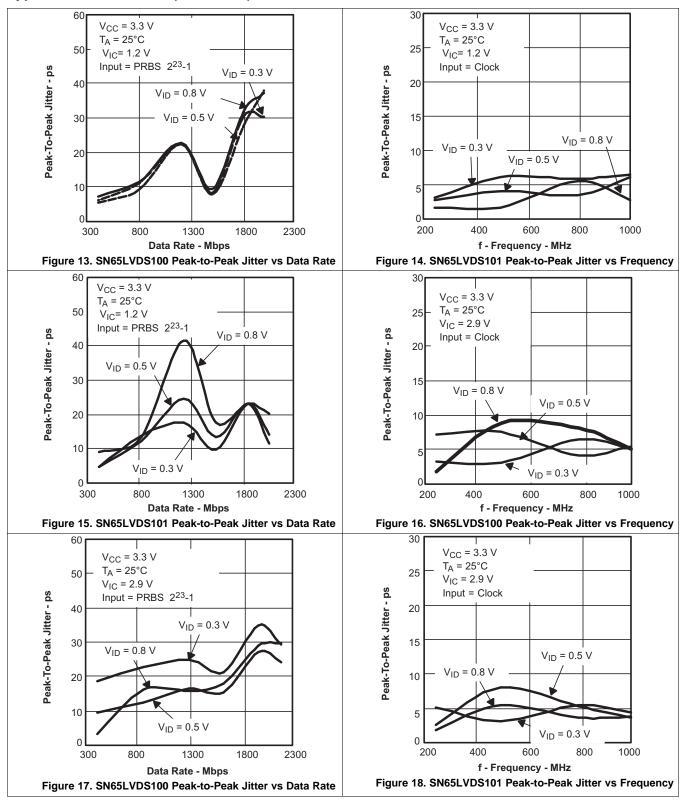
8

Copyright © 2002–2015, Texas Instruments Incorporated

Product Folder Links: SN65LVDS100 SN65LVDT100 SN65LVDS101 SN65LVDT101



#### **Typical Characteristics (continued)**

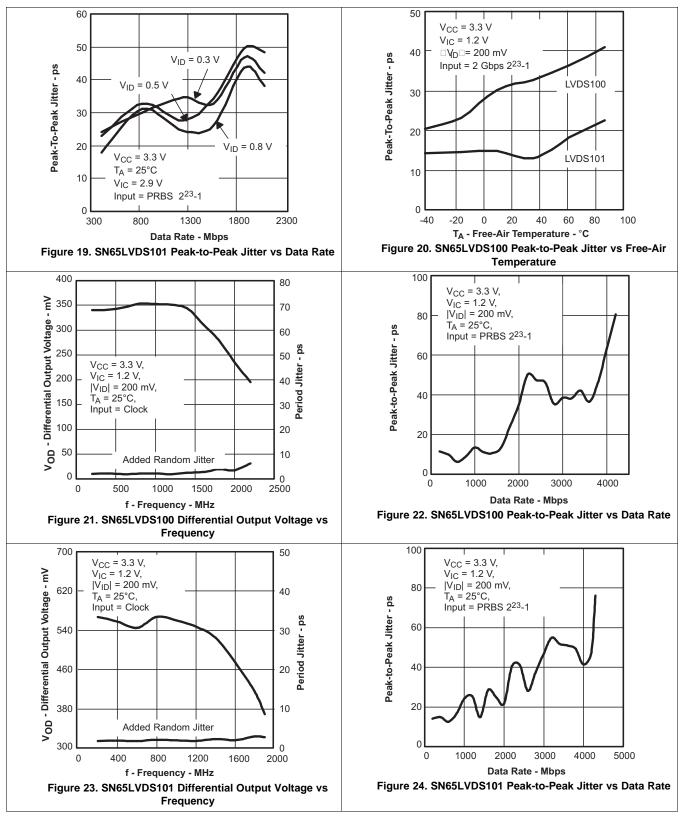




#### SN65LVDS100, SN65LVDT100, SN65LVDS101, SN65LVDT101 SLLS516E – AUGUST 2002 – REVISED JULY 2015

www.ti.com

### **Typical Characteristics (continued)**

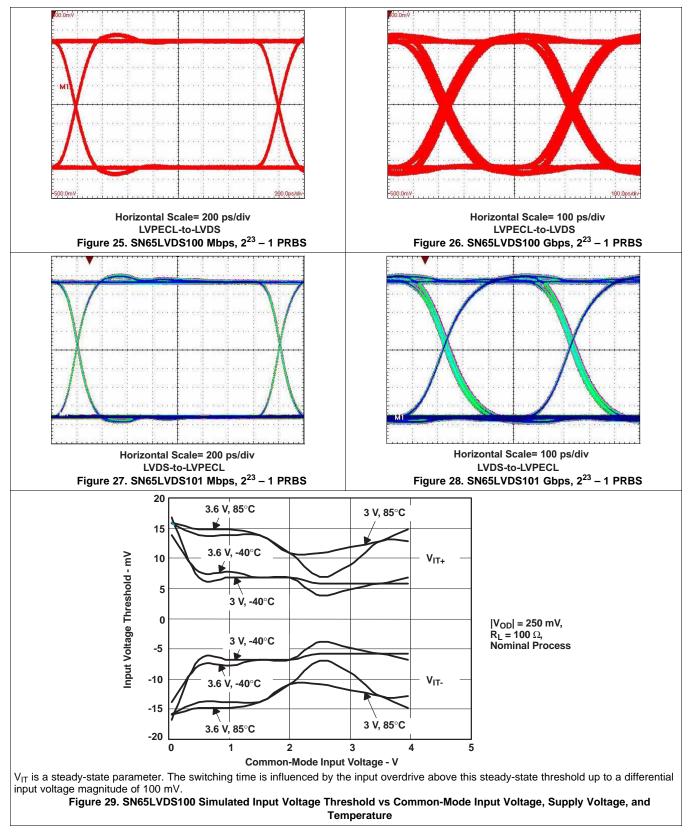


Copyright © 2002–2015, Texas Instruments Incorporated

Product Folder Links: SN65LVDS100 SN65LVDT100 SN65LVDS101 SN65LVDT101



### **Typical Characteristics (continued)**



# 9 Parameter Measurement Information

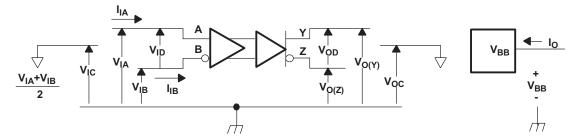


Figure 30. Voltage and Current Definitions

| APPLIED VOLTAGES |                 | RESULTING DIFFERENTIAL<br>INPUT VOLTAGE | RESULTING COMMON-<br>MODE INPUT VOLTAGE | OUTPUT <sup>(1)</sup> |
|------------------|-----------------|---|---|-----------------------|
| VIA              | V <sub>IB</sub> | V <sub>ID</sub>                         | VIC                                     |                       |
| 1.25 V           | 1.15 V          | 100 mV                                  | 1.2 V                                   | Н                     |
| 1.15 V           | 1.25 V          | –100 mV                                 | 1.2 V                                   | L                     |
| 4.0 V            | 3.9 V           | 100 mV                                  | 3.95 V                                  | Н                     |
| 3.9 V            | 4. 0 V          | –100 mV                                 | 3.95 V                                  | L                     |
| 0.1 V            | 0.0 V           | 100 mV                                  | 0.05 V                                  | Н                     |
| 0.0 V            | 0.1 V           | –100 mV                                 | 0.05 V                                  | L                     |
| 1.7 V            | 0.7 V           | 1000 mV                                 | 1.2 V                                   | Н                     |
| 0.7 V            | 1.7 V           | –1000 mV                                | 1.2 V                                   | L                     |
| 4.0 V            | 3.0 V           | 1000 mV                                 | 3.5 V                                   | Н                     |
| 3.0 V            | 4.0 V           | –1000 mV                                | 3.5 V                                   | L                     |
| 1.0 V            | 0.0 V           | 1000 mV                                 | 0.5 V                                   | н                     |
| 0.0 V            | 1.0 V           | –1000 mV                                | 0.5 V                                   | L                     |

(1) H = high level, L = low level

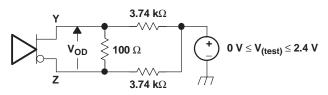
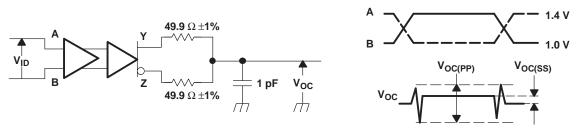


Figure 31. SN65LVDx100 Differential Output Voltage (V<sub>OD</sub>) Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t<sub>r</sub> or t<sub>f</sub> ≤ 0.25 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C<sub>L</sub> includes instrumentation and fixture capacitance within 0.06 mm of the device under test. The measurement of V<sub>OC(PP)</sub> is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

# Figure 32. Test Circuit and Definitions for the SN65LVDx100 Driver Common-Mode Output Voltage

Submit Documentation Feedback

12

Product Folder Links: SN65LVDS100 SN65LVDT100 SN65LVDS101 SN65LVDT101

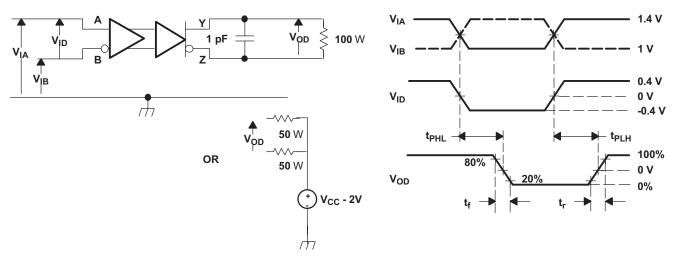


# SN65LVDS100, SN65LVDT100, SN65LVDS101, SN65LVDT101

www.ti.com

SLLS516E - AUGUST 2002 - REVISED JULY 2015

13



NOTE: All input pulses are supplied by a generator having the following characteristics: t<sub>r</sub> or t<sub>f</sub> ≤ 0.25 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C<sub>L</sub> includes instrumentation and fixture capacitance within 0.06 mm of the device under test. Measurement equipment provides a bandwidth of 5 GHz minimum.



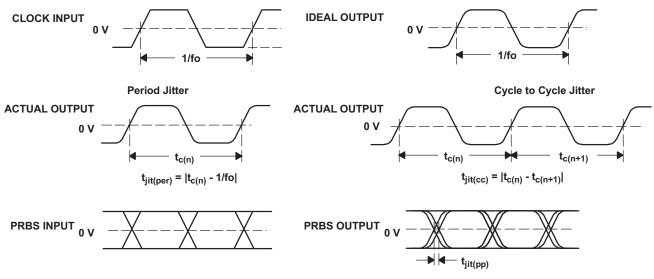
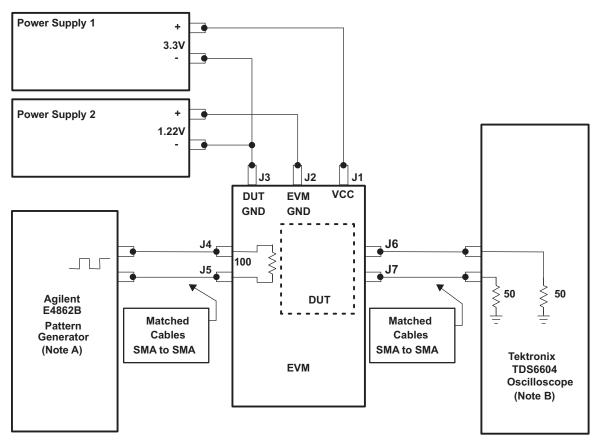


Figure 34. Driver Jitter Measurement Waveforms





- A. Source jitter is subtracted from the measured values.
- B. TDS JIT3 jitter analysis software installed

# Figure 35. Jitter Setup Connections for SN65LVDS100 and SN65LVDS101



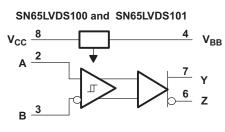
# **10** Detailed Description

### 10.1 Overview

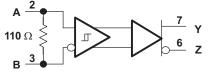
The SN65LVDx10x family of devices are fully differential, high-speed translators/repeaters. All devices in the family include a wide common-mode range receiver that accepts low-voltage differential signals covering a variety of standards. A receiver with an input sensitivity of  $\pm 100$  mV and 25 mV of hysteresis is incorporated. The SN65LVDx100 devices include an output driver that meets all the specifications of the LVDS standard (TIA/EIA-644A). The SN65LVDx101 devices include an output driver that is compatible with 3.3-V PECL levels.

The SN65LVDx10x family is intended to drive a 100- $\Omega$  transmission line. This transmission line may be a printedcircuit board (PCB) or cabled interconnect. With transmission lines, optimum signal quality and power delivery is reached when a transmission line is terminated with a load equal to the characteristic impedance of the interconnecting media. Likewise, the driven 100- $\Omega$  transmission line should be terminated with a matched resistance.

# **10.2** Functional Block Diagram



SN65LVDT100 and SN65LVDT101



# **10.3 Feature Description**

#### 10.3.1 Receiver Features

#### 10.3.1.1 Voltage Range and Common-Mode Range

The receiver circuit incorporated into the SN65LVDx10x family supports receiving most low-voltage differential signals. This wide common-mode range receiver can accept any input signal between 0 and 4 V. Without referencing any specific standard, we can analyze the range of signals that can be input to this family of devices. Assuming an input signal has a 400-mV differential input voltage  $|(V^+ - V^-)|$ , the maximum recommended input voltage is 4 V. The absolute value of the most positive signal of a differential input would be  $V_{MAX}$ :

 $V_{MAX} = V_{CM} + \frac{1}{2} (V_{DIFF})$ 

where

- V<sub>CM</sub> = common-mode voltage
- V<sub>DIFF</sub> = differential voltage

(1)

Therefore, using our  $V_{MAX}$  of 4 V and  $V_{DIFF}$  of 400 mV, we see that we can simultaneously support a differential voltage of 400 mV and a common-mode voltage of 3.8 V. As is obvious from Equation 1, the common-mode and differential voltages are coupled: as the differential voltage increases in magnitude, the maximum common-mode voltage supported decreases.

Using a similar analysis, and considering the 0-V minimum input voltage, we can see that we could simultaneously support a differential voltage of 400 mV and a common-mode voltage of 0.2 V. Thus, we have a receiver that can support common-mode voltages in the approximate range of 0.2 V to 3.8 V.

Copyright © 2002–2015, Texas Instruments Incorporated

SLLS516E - AUGUST 2002 - REVISED JULY 2015

# Feature Description (continued)

The 400-mV example alluded to above is a reasonable maximum differential input voltage across a wide variety of standards (LVDS, M-LVDS, CML, LVPECL, and so on). We can use the specifications for any of these standards to understand the value of this wide input range receiver.

A standard compliant LVDS driver generates a 350-mV differential signal with a common-mode voltage of 1.2 V. The noninverting output thus resides at 1.375 V, while the inverting signal is at a voltage of 1.025 V. Because the SN65LVDx10x family receiver operates over a range of 0 V to 4 V, the wide common-mode receiver then can accept signals that are common-mode shifted by –1.025 V to 2.625 V. Similar analysis can be performed for any other input signal.

# 10.3.1.2 Sensitivity

Table 2 provides a truth table for the SN65LVDx10x family. Again, the same receiver circuitry is used on each of the devices in this family; therefore, the truth table is the same for all family devices. When the differential input voltage is greater than 100 mV, the receiver outputs a HI level. If the differential input voltage is less than -100 mV, the receiver outputs a LO level.

Between these two thresholds the receiver output is indeterminate. When the input signal falls in this  $-100 \text{ mV} < V_{\text{ID}} < 100 \text{ mV}$  range, the receiver output state cannot be determined unambiguously. Having said that, it is important to note that the SN65LVDx10x family receivers include 25 mV of hysteresis. The hysteresis is incorporated into the design to prevent the output switching when the receiver input voltage is close to 0 V (for example, the receiver inputs are open-circuited, or the receiver is connected to a driver that is high-impedance). With the open-circuited input and when the magnitude of the differential noise voltage on the bus is low (approximately <  $\pm 10 \text{ mV}$ ), the hysteresis serves to hold the device output at the last known state. This feature helps prevent chattering on the device output.

Noticeably absent from this receiver is any integrated failsafe feature. External components may be added to the receiver circuit to provide failsafe. Such an implementation is covered below.

### 10.3.1.3 Failsafe Considerations

Failsafe, in regard to a line receiver, usually means that the output goes to a defined logical state with no input signal. To keep added jitter to an absolute minimum, the SN65LVDS100 does not include this feature. It does exhibit 25 mV of input voltage hysteresis to prevent oscillation and keep the output in the last state prior to input-signal loss (assuming the differential noise in the system is less than the hysteresis).

Should failsafe be required, it may be added externally with a 1.6-k $\Omega$  pullup resistor to the 3.3-V supply and a 1.6-k $\Omega$  pulldown resistor to ground as shown in Figure 36 The default output state is determined by which line is pulled up or down and is the user's choice. The location of the 1.6-k $\Omega$  resistors is not critical. However, the 100- $\Omega$  resistor should be located at the end of the transmission line.

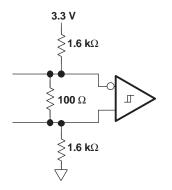


Figure 36. External Failsafe Circuit

Addition of this external failsafe will reduce the differential noise margin and add jitter to the output signal. The roughly 100-mV steady-state voltage generated across the  $100-\Omega$  resistor adds (or subtracts) from the signal generated by the upstream line driver. If the differential output of the line driver is symmetrical about zero volts, then the input at the receiver will appear asymmetrical with the external failsafe. Perhaps more important, is the extra time it takes for the input signal to overcome the added failsafe offset voltage.

16 Submit Documentation Feedback

Product Folder Links: SN65LVDS100 SN65LVDT100 SN65LVDS101 SN65LVDT101





#### Feature Description (continued)

In Figure 37 and using an external failsafe, the high-level differential voltage at the input of the SN65LVDS100 reaches 340 mV and the low-level –400 mV indicating a 60-mV differential offset induced by the external failsafe circuitry. The figure also reveals that the lowest peak-to-peak time jitter does not occur at zero-volt differential (the nominal input threshold of the receiver) but at –60 mV, the failsafe offset.

The added jitter from external failsafe increases as the signal transition times are slowed by cable effects. When a ten-meter CAT-5 UTP cable is introduced between the driver and receiver, the zero-crossing peak-to-peak jitter at the receiver output adds 250 ps when the external failsafe is added with this specific test set up. If external failsafe is used in conjunction with the SN65LVDS100, the noise margin and jitter effects should be budgeted.

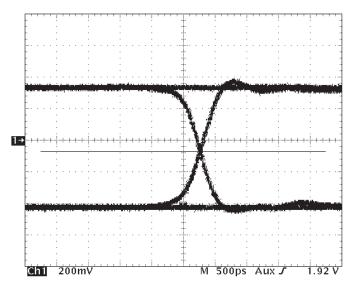


Figure 37. Receiver Input Eye Pattern with External Failsafe

#### 10.3.1.4 V<sub>BB</sub> Voltage Reference

Pin 4 ( $V_{BB}$ ) on the SN65LVDS10x devices acts a voltage reference. This is an output signal from the device, with a nominal value of  $V_{CC}$  – 1.35 V. This output can be used when receiving a single-ended input signal. This voltage reference would then be connected to the inverting input pin on the device (pin 3: B). The application where such a use makes sense is when the device is to receive a single-ended 3.3-V LVPECL signal. The common-mode voltage of a 3.3-V LVPECL signal is approximately 1.35 V below the device supply rail. While the value of  $V_{BB}$  is ideal for single-ended LVPECL signals, its use may be extended to other single-ended inputs as long as the active single-ended signal is conditioned to have a common-mode voltage close to the nominal value of  $V_{BB}$ .

Caution is in order when using the V<sub>BB</sub> signal. The expected application when using this signal is as a voltage reference to high-impedance input. The maximum current that can be sourced by this pin is 400  $\mu$ A, while the maximum current that can be sunk is 12  $\mu$ A. In cases where the SN65LVDS10x device is to be used without using V<sub>BB</sub> as a reference, the V<sub>BB</sub> pin should be left unconnected.

#### 10.3.1.5 Integrated Termination

The SN65LVDT10x devices are identical to the SN65LVDS10x devices in all regards, with the addition that the SN65LVDT10x devices incorporate an integrated termination resistor along with the receiver. This termination would take the place of the matched load-line termination mentioned above. The SN65LVDT10x can be used in a point-to-point system or in a multidrop system when it is the last receiver on the multidrop bus. The SN65LVDT10x should not be used at every node in a multidrop system as this would change the loaded bus impedance throughout the bus resulting in multiple reflections and signal distortion.

Copyright © 2002–2015, Texas Instruments Incorporated

SLLS516E - AUGUST 2002 - REVISED JULY 2015

### 10.3.1.6 Receiver Equivalent Schematic

The SN65LVDx10x equivalent input schematic diagram is shown in Figure 38. The receiver input is a highimpedance differential pair in the case of the SN65LVDS10x. The SN65LVDT10x devices include an internal termination resistor of 110  $\Omega$  across the input port. 7-V Zener diodes are included on each input to provide ESD protection.

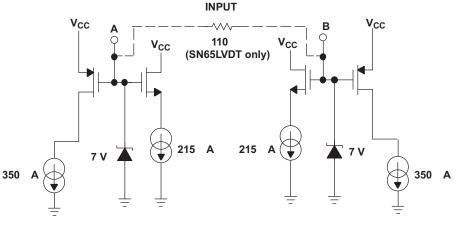


Figure 38. Receiver Equivalent Schematic

### 10.3.2 Driver Features

# 10.3.2.1 Signaling Rate, Edge Rate, and Added Jitter

The SN65LVDT10x family has been designed to provide uncompromising signal quality at signaling rates up to 2 Gbps, and beyond. Specifying a maximum signaling rate (the signaling rate is the same as the bit rate) for a device depends on the eye quality that can be achieved. This eye quality is driven by a number of factors, with two of the most critical parameters being the rise or fall time and added jitter.

The rise and fall times for a device are critical for an obvious reason: the time it takes for a device to change states will be a limiting factor in how fast a device can be operated. If a device is operated much faster than the speed at which it can change states, the vertical opening of the eye diagram will be decreased. In some cases this may be perfectly acceptable. As an example, assume an SN65LVDS100 is being using to receive a CML signal, and translate the CML signal into an LVDS signal. At speeds up to 2 Gbps (or 1 GHz for a clock signal because there are 2 bit times for each clock cycle), the LVDS output signal will have a differential output voltage of at least 247 mV, with a nominal value of 340 mV (see the *Electrical Characteristics* section for reference). If the input is at a higher speed, there is no circuitry within the SN65LVDS100 that would prevent the device from trying to output an LVDS signal. As the signaling rate is increased beyond 2 Gbps, the output signal would show a decrease in vertical eye opening. This decrease may not impact the utility of the device at the system level. Signal chain noise analysis would need to be performed to determine whether the overall system would be affected.

In a similar way, we can see the effect of added jitter, and how it can place upper limits on the useful operating rate. At the stated 2-Gbps signaling rate, the unit interval (UI) time, t<sub>UI</sub>, is the reciprocal of 2 Gbps, or 500 ps. As added jitter is introduced by a device such as the SN65LVDT10x family, it serves to close down the eye pattern horizontally (or in time). As the output eye diagram will eventually be used to recover the transmitted or encoded data, the jitter tolerance at the eventual consumer would determine if the eye closure introduced by a SN65LVDT10x is acceptable. The nominal total jitter for the SN65LVDT10x family devices is 28 ps, while the worst case jitter is 65 ps. The 28 ps represents less than 6% of the UI and the 65 ps represents 13% of the UI. Both values will generally be within the amount of added jitter that can be tolerated in a system.

# 10.3.2.2 SN65LVDx100 LVDS Output

#### 10.3.2.2.1 Driver Output Voltage

The SN65LVDx100 driver operates and meets all the specified performance requirements for supply voltages in the range of 3 V to 3.6 V. The driver output voltage has a nominal value of 340 mV, with maximum and minimum output voltages that meet the LVDS standard specifications of 247 mV and 454 mV, respectively.





#### 10.3.2.2.2 Driver Offset

An LVDS compliant driver is required to maintain the common-mode output voltage at 1.2 V (±75 mV). The SN65LVDx100 incorporates sense circuitry and a control loop to source common-mode current and keep the output signal within specified values. Further, the device maintains the output common-mode voltage at this set point over the full 3-V to 3.6-V supply range.

#### 10.3.2.3 SN65LVDx101 LVPECL Output

#### 10.3.2.3.1 Driver Voltage

The SN65LVDx101 driver is an LVPECL differential driver. Figure 40 shows an equivalent output schematic for the SN65LVDx101 driver. The differential signal output of the driver is simply the output of the differential pair, emitter-coupled to the device output. For an ECL class device such as this, the output base-emitter diodes must always be on. This need for the consistently active output stages helps explain the classical ECL load shown in Figure 39.

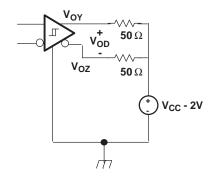


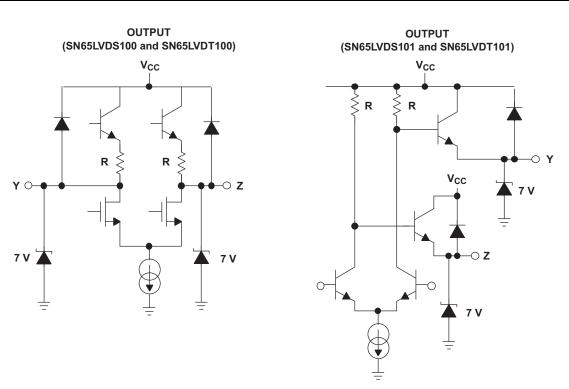
Figure 39. Typical Termination for LVPECL Output Driver (SN65LVDx101)

Figure 39 shows that the SN65LVDx101 outputs drive  $50-\Omega$  loads terminated to a supply that is 2 V below the supply voltage of the SN65LVDx101 device. Driving a load that is referenced to a supply 2 V below the device supply assures that the final transistor stages in the output driver are always on. A common question for those new to ECL devices concerns the implementation of this output load. There is no need generally to have a regulated supply to support this. A Thevenin load is often used to create a  $50-\Omega$  effective termination, at a common-mode voltage 2 V below the local supply rail. Many other implementations have been used. The key to the specific load that is implemented lies in the understanding that the ECL driver output stage is a voltage driver, with the output voltage always referenced to the positive power rail for the device. The load that is driven must ensure that the final transistors on each output leg are in the active regions at all times.

#### 10.3.2.4 Driver Equivalent Schematics

The SN65LVDx10x equivalent output schematic diagrams are shown in Figure 40. The SN65LVDx10x output is represented by a differential pair with 7-V Zener diodes on each output leg. The Zener diodes provide ESD protection. The SN65LVDx10x1 LVPECL output is represented by a differential pair, with follower stages, and with 7-V Zener diodes on each output leg for ESD protection.





#### Figure 40. Driver Equivalent Schematics

# **10.4 Device Functional Modes**

| DIFFERENTIAL INPUT                 | OUTPUTS <sup>(1)</sup> |   |  |
|------------------------------------|------------------------|---|--|
| $V_{ID} = V_A - V_B$               | Y                      | Z |  |
| V <sub>ID</sub> ≥ 100 mV           | н                      | L |  |
| –100 mV < V <sub>ID</sub> < 100 mV | ?                      | ? |  |
| $V_{ID} \le -100 \text{ mV}$       | L                      | Н |  |
| Open                               | ?                      | ? |  |

### Table 2. SN65LVDx10x Truth Table

(1) H = high level, L = low level, ? = indeterminate



# 11 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### **11.1** Application Information

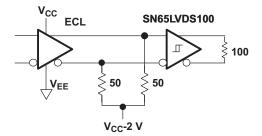
The SN65LVDx10x are single-channel repeaters/translators. The functionality of these devices is simple, yet extremely flexible, leading to their use in designs ranging from wireless base stations to desktop computers. SN65LVDx10x devices are often used as buffers to regenerate or repeat the signal at their port. The devices in this family can accept any differential signal that meets the input port requirements specified herein. The input signal does not need to comply with any particular standard to be repeated: it just needs to fall within the common-mode input range of these devices, and have a differential input signal of at least 100 mV in magnitude. With such an input the designer can use a SN65LVDx100 device to repeat the digital input signal, and generate an output signal that carries the information at its input port, and complies with all the requirements of the LVDS standard. Similarly, an SN65LVDx101 device is a general-purpose differential receiver that repeats the input data at its output port, while complying with LVPECL output specifications.

Translating from one signaling standard to a different signaling standard is a common application issue. Two ICs that use different signaling standards may need to communicate with each other. An FPGA may output an LVDS signal and an ASIC may be designed to receive LVPECL inputs. Directly connecting the two devices would end up with communication errors. In such a case an SN65LVDS101 can be used to translate between the incompatible standards. The common application issue of converting from one standard to another are covered in *Typical Application*.



### 11.2 Typical Application

### 11.2.1 PECL to LVDS Translation



### Figure 41. PECL to LVDS Translation

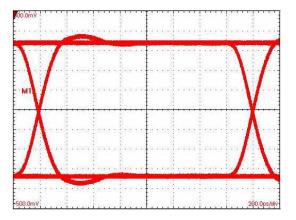
### 11.2.1.1 Design Requirements

| DESIGN PARAMETER                              | EXAMPLE VALUE   |
|---|---|
| PECL Source Supply Voltage (V <sub>CC</sub> ) | 3.3 V   |
| SN65LVDS100 Supply Voltage                    | 3.0 to 3.6 V  |
| Driver Signaling Rate                         | DC to 2000 Mbps   |
| Interconnect Characteristic Impedance         | 100 Ω   |
| Termination Resistance                        | 50 $\Omega$ to $V_{CC}$ – 2 V on each side of transmission line |

#### 11.2.1.2 Detailed Design Requirements

Translating an LVPECL signal to LVDS is straightforward using the SN65LVDS100. The common-mode output of an LVPECL driver is approximately 2 V, while the differential output voltage would be approximately 600 to 800 mV. 2 V is right in the middle of the common-mode range of the SN65LVDS100, while the differential voltage is more than enough signal for the high-sensitivity receiver. As shown in Figure 41, 50- $\Omega$  pulldown resistors to V<sub>CC</sub> – 2 V are needed, and the rationale for these have been discussed earlier.

#### 11.2.1.3 Application Curve



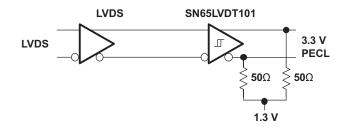
Horizontal Scale= 200 ps/div LVPECL-to-LVDS Figure 42. SN65LVDS100 Mbps, 2<sup>23</sup> – 1 PRBS

22 Submit Documentation Feedback

Product Folder Links: SN65LVDS100 SN65LVDT100 SN65LVDS101 SN65LVDT101



#### 11.2.2 LVDS to 3.3-V PECL Translation



#### Figure 43. LVDS to 3.3-V PECL Translation

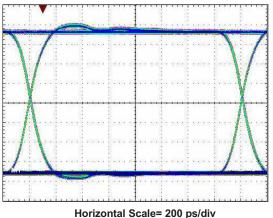
#### 11.2.2.1 Design Requirements

| DESIGN PARAMETER                              | EXAMPLE VALUE             |
|---|---------------------------|
| LVDS Source Supply Voltage (V <sub>CC</sub> ) | 3.3 V                     |
| SN65LVDT101 Supply Voltage                    | 3.0 to 3.6 V              |
| Driver Signaling Rate                         | DC to 2000 Mbps           |
| Interconnect Characteristic Impedance         | 100 Ω                     |
| Termination Resistance                        | Integrated in SN65LVDT101 |

#### 11.2.2.2 Detailed Design Requirements

Translating an LVDS signal to LVPECL is conveniently done using the SN65LVDT101. The common-mode output of an LVDS driver is 1.2 V, while the differential output voltage would be approximately 350 mV. 1.2 V is well within the common-mode range of the SN65LVDT101, while the differential voltage is more than enough signal for the high-sensitivity receiver. The integrated variant of the LVPECL translators is used here as it includes precisely the load required for operation of an LVDS driver. This circuit is shown in Figure 43.

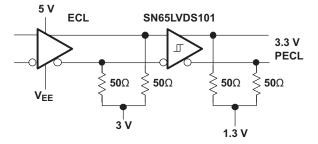
#### 11.2.2.3 Application Curve



LVDS-to-LVPECL Figure 44. SN65LVDS101 Mbps, 2<sup>23</sup> – 1 PRBS



#### 11.2.3 5-V PECL to 3.3-V PECL Translation



#### Figure 45. 5-V PECL to 3.3-V PECL Translation

#### 11.2.3.1 Design Requirements

| DESIGN PARAMETER                              | EXAMPLE VALUE   |  |
|---|---|--|
| PECL Source Supply Voltage (V <sub>CC</sub> ) | 5.0 V   |  |
| SN65LVDS101 Supply Voltage                    | 3.0 to 3.6 V  |  |
| Driver Signaling Rate                         | DC to 2000 Mbps   |  |
| Interconnect Characteristic Impedance         | 100 Ω   |  |
| Termination Resistance                        | 50 $\Omega$ to $V_{CC}$ – 2 V on each side of transmission line |  |

#### 11.2.3.2 Detailed Design Requirements

At times a 5-V PECL will need to be converted to a 3.3-V PECL signal. When the 5-V signal is encoded (8b10b for example), ac-coupling can be used. Figure 45 shows how to translate a 5-V PECL signal to 3.3-V PECL when a dc connection is needed.

The 50- $\Omega$  pulldown resistors to V<sub>CC</sub> – 2 V are familiar by now. The SN65LVDS101 provides the 3.3-V based LVPECL signal.

A level of care must be exercised with this solution. The absolute voltage levels at the input pins to the SN65LVDS101 must be less than or equal to 4 V. With a 5-V PECL signal, the non-inverting output will generally be just below 4 V. If the 5-V PECL supply goes much above 5 V, the input voltage at the SN65LVDS101 may violate the specifications. Ensure that the worst-case high-output voltage from the 5-V PECL driver will be within the range of the SN65LVDS101.

#### 11.2.3.3 Application Curve

Reference: Figure 44

www.ti.com



#### 11.2.4 CML to LVDS or 3.3-V PECL Translation

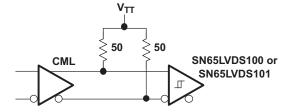


Figure 46. CML to LVDS or 3.3-V PECL Translation

#### 11.2.4.1 Design Requirements

| DESIGN PARAMETER                                  | EXAMPLE VALUE   |
|---|---|
| CML Termination Supply Voltage (V <sub>TT</sub> ) | 3.3 V   |
| SN65LVDS10x Supply Voltage                        | 3.0 to 3.6 V  |
| Driver Signaling Rate                             | DC to 2000 Mbps   |
| Interconnect Characteristic Impedance             | 100 Ω   |
| Termination Resistance                            | 50 $\Omega$ to $V_{TT}$ on each side of transmission line |

# 11.2.4.2 Detailed Design Requirements

Current-mode logic (CML) signals are designed to drive a  $100-\Omega$  transmission line with a load termination being two  $50-\Omega$  pullup resistors to a power supply. This circuit is shown in Figure 46. Common CML drivers include 16-mA current sources that serve to develop the differential output signal. Using this 16-mA current source and assuming a 3.3-V CML driver is being used, the common-mode output of the driver in Figure 46 is 2.9 V and the differential output voltage is 800 mV. Both values are well within the operational envelope of the SN65LVDx10x family receivers.

To convert from 3.3-V CML signals to LVDS signals, the driver and receiver are connected in a straightforward fashion. The SN65LVDS100 is used in this circuit to convert to an LVDS output, while the SN65LVDS101 is used to convert to LVPECL.

Again, the reader will notice that the integrated termination devices in the SN65LVDx10x family are not mentioned for this conversion. The 'LVDT devices incorporate a shunt  $100-\Omega$  termination which are not appropriate when a pullup termination is needed.

#### 11.2.4.3 Application Curve

Reference: Figure 44

25



#### 11.2.5 Single-Ended 3.3-V PECL to LVDS Translation

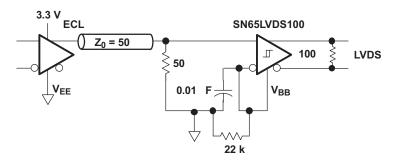


Figure 47. Single-Ended 3.3-V PECL to LVDS Translation

#### 11.2.5.1 Design Requirements

| DESIGN PARAMETER                      | EXAMPLE VALUE   |
|---------------------------------------|-----------------|
| ECL Supply Voltage                    | 3.3 V           |
| SN65LVDS100 Supply Voltage            | 3.0 to 3.6 V    |
| Driver Signaling Rate                 | DC to 2000 Mbps |
| Interconnect Characteristic Impedance | 50 Ω            |
| Termination Resistance                | 50 Ω to GND     |
| V <sub>BB</sub> Current to GND        | 91 µA           |

### 11.2.5.2 Detailed Design Requirements

The SN65LVDx10x family of devices provides the flexibility to translate single-ended input signals to differential outputs. The output can be either LVDS or LVPECL, depending on the choice of SN65LVDS10x that is used. Figure 47 demonstrates how to convert a single-ended LVPECL signal to an LVDS signal.

The common receiver used in this family will work with any pair of input signals that comply with its input requirements. In this example, let's assume the single-sided LVPECL signal has a high-level voltage of  $V_{CC} - 1 V = 2.3 V$ . Assume the low-level output voltage is  $V_{CC} - 1.6 V = 1.7 V$ . The common-mode of these two levels is 2 V, which happens to be  $V_{CC} - 1.3 V$ .

To use a single-ended signal with these receivers, we need to bias the unused input of the differential receiver. In this case we will bias the inverting input pin. With the high and low signal levels calculated above, we see the optimum bias point for the unused pin would be the common-mode or average signal level. The  $V_{BB}$  pin provides this needed voltage.  $V_{BB}$  has a nominal value of  $V_{CC}$  – 1.35 V.

The 22-k $\Omega$  resistor in the circuit serves to limit the dc current being sourced by V<sub>BB</sub>. This resistor setting will limit the current to less than 100  $\mu$ A, well within the recommended maximum value of 400  $\mu$ A.

The drawback of a single-ended to differential-converted shown here is that the unused pin is being set to a fixed value that will be close to the signal common-mode voltage. Any deviation from  $V_{BB}$  (in the actual signal common-mode) results in duty-cycle distortion at the differential output. Whether or not this is an issue is application dependent. If, for example, the input signal is a clock signal and clocking only happens on one edge, the distortion may be acceptable.

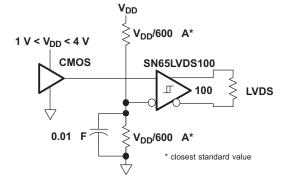
# 11.2.5.3 Application Curve

Reference: Figure 42

Product Folder Links: SN65LVDS100 SN65LVDT100 SN65LVDS101 SN65LVDT101



#### 11.2.6 Single-Ended CMOS to LVDS Translation



#### Figure 48. Single-Ended CMOS to LVDS Translation

#### 11.2.6.1 Design Requirements

| DESIGN PARAMETER                       | EXAMPLE VALUE                 |
|--|-------------------------------|
| CMOS Supply Voltage (V <sub>DD</sub> ) | 1 V < V <sub>DD</sub> < 4 V   |
| SN65LVDS100 Supply Voltage             | 3.0 to 3.6 V                  |
| Driver Signaling Rate                  | DC to 500 Mbps                |
| V <sub>BB</sub> Current to GND         | 91 µA (V <sub>DD</sub> = 4 V) |

#### 11.2.6.2 Detailed Design Requirements

The SN65LVDx10x family of devices can also translate a CMOS input signals to differential outputs. The output can be either LVDS or LVPECL, depending on the choice of SN65LVDS10x that is used. Figure 48 demonstrates how to convert a CMOS signal to an LVDS signal.

The CMOS signal in this case can be from any power rail up to 4 V (not a common rail, but the maximum allowable input at the receiver nonetheless). The unused or inverting signal in this case is biased to  $V_{DD}/2$  which will be equal to the common-mode of the CMOS input signal.

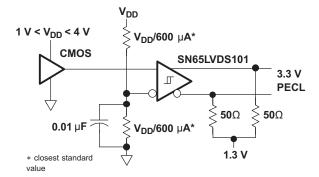
There is less concern with this circuit with regards to duty-cycle distortion, as we have assumed that the CMOS driver and the local voltage divider are referenced to the same rail. If different rails were used, the usual cautions on duty-cycle distortion would apply.

#### 11.2.6.3 Application Curve

Reference: Figure 42



#### 11.2.7 Single-Ended CMOS to 3.3-V PECL Translation



#### Figure 49. Single-Ended CMOS to 3.3-V PECL Translation

#### 11.2.7.1 Design Requirements

| DESIGN PARAMETER                       | EXAMPLE VALUE                 |
|--|-------------------------------|
| CMOS Supply Voltage (V <sub>DD</sub> ) | 1 V < V <sub>DD</sub> < 4 V   |
| SN65LVDS101 Supply Voltage             | 3.0 to 3.6 V                  |
| Driver Signaling Rate                  | DC to 500 Mbps                |
| V <sub>BB</sub> Current to GND         | 91 µA (V <sub>DD</sub> = 4 V) |

#### 11.2.7.2 Detailed Design Requirements

Figure 49 demonstrates how to implement a CMOS to LVPECL translation. The elements in this circuit are now familiar, so the reader is referred to the previous discussions.

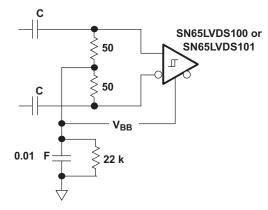
#### 11.2.7.3 Application Curve

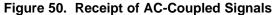
Reference: Figure 44

28 Submit Documentation Feedback Copyright © 2002–2015, Texas Instruments Incorporated Product Folder Links: SN65LVDS100 SN65LVDT100 SN65LVDS101 SN65LVDT101



#### 11.2.8 Receipt of AC-Coupled Signals





#### 11.2.8.1 Design Requirements

| DESIGN PARAMETER                  | EXAMPLE VALUE                 |
|-----------------------------------|-------------------------------|
| AC-coupling capacitor             | 10 nF                         |
| SN65LVDS100 Supply Voltage        | 3.0 to 3.6 V                  |
| Driver Signaling Rate             | Up to 500 Mbps                |
| V <sub>BB</sub> Current to GND    | 91 µA (V <sub>DD</sub> = 4 V) |
| Low-Frequency Cutoff of RC Filter | 318 kHz                       |

#### 11.2.8.2 Detailed Design Requirements

The general need to convert ac-coupled signals to either LVDS or LVPECL is shown in Figure 50. The transmission line is terminated with a center-tapped  $100-\Omega$  resistor network. The center tap is tied to the previously discussed V<sub>BB</sub> bias reference. The bias reference is current limited with the same 22-k $\Omega$  resistor to ground. The use of V<sub>BB</sub> is chosen for ease. This sets the common-mode at the receiver input approximately in the middle of the receiver input range (approximately 2 V).

The ac-coupling capacitors used on the input signal may be integrated into the source destination device, or may be discretely inserted on board. The capacitance value and the 50- $\Omega$  to ground terminations serve as a high-pass filter, blocking dc content. With a 10-nF capacitor the low-frequency zero is at 318 kHz. The reader needs to understand the frequency content of the incoming signal to determine whether this zero location is appropriate.

#### 11.2.8.3 Application Curve

Reference: Figure 42

# **12 Power Supply Recommendations**

The LVDS drivers in this data sheet are designed to operate from a single power supply, with supply voltages in the range of 3.0 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than  $|\pm 1 V|$ . Board level and local device level bypass capacitance should be used and have been covered.

# 13 Layout

# 13.1 Layout Guidelines

# 13.1.1 Microstrip vs. Stripline Topologies

As per SLLD009, modern printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 51.

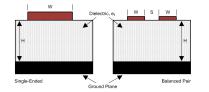


Figure 51. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems since the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines, if possible. The PCB traces allow designers to specify the necessary tolerances for  $Z_0$  based on the overall noise budget and reflection allowances. Footnotes 1, 2, and 3 provide formulas for  $Z_0$  and  $t_{PD}$  for differential and single-ended traces. (1) (2) (3)

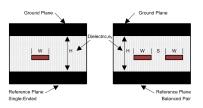


Figure 52. Stripline Topology

# 13.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers<sup>™</sup> 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 µm or 0.0003 in (minimum).
- Copper plating should be 25.4 µm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

30 Submit Documentation Feedback

<sup>(1)</sup> Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.

<sup>(2)</sup> Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.

<sup>(3)</sup> Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.



#### Layout Guidelines (continued)

#### 13.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you must decide how many levels to use in the stack. To reduce the TTL/CMOS-to-LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in Figure 53.

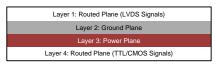


Figure 53. Four-Layer PCB Board

#### NOTE

The separation between layers 2 and 3 should be 127  $\mu$ m (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in Figure 54.



Figure 54. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, since it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

#### 13.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low-noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be  $100-\Omega$  differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broadside-coupled.

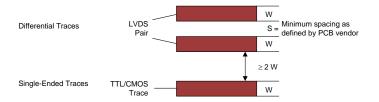


Figure 55. 3-W Rule for Single-Ended and Differential Traces (Top View)

Copyright © 2002–2015, Texas Instruments Incorporated



### Layout Guidelines (continued)

You should exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

#### 13.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path for high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

# 13.2 Layout Example

### See Layout Guidelines examples.

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 56.

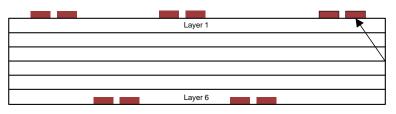


Figure 56. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 57. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

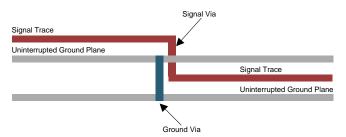


Figure 57. Ground Via Location (Side View)

Short and low-impedance connection of the device's ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

32 Submit Documentation Feedback

Product Folder Links: SN65LVDS100 SN65LVDT100 SN65LVDS101 SN65LVDT101



# 14 Device and Documentation Support

### 14.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

| PARTS       | PRODUCT FOLDER SAMPLE & BUY |            | TECHNICAL<br>DOCUMENTS | TOOLS &<br>SOFTWARE | SUPPORT & COMMUNITY |  |  |
|-------------|-----------------------------|------------|------------------------|---------------------|---------------------|--|--|
| SN65LVDS100 | Click here                  | Click here | Click here             | Click here          | Click here          |  |  |
| SN65LVDT100 | Click here                  | Click here | Click here             | Click here          | Click here          |  |  |
| SN65LVDS101 | Click here                  | Click here | Click here             | Click here          | Click here          |  |  |
| SN65LVDT101 | Click here                  | Click here | Click here             | Click here          | Click here          |  |  |

#### Table 3. Related Links

# 14.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E<sup>™</sup> Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

# 14.3 Trademarks

E2E is a trademark of Texas Instruments. Rogers is a trademark of Rogers Corporation. All other trademarks are the property of their respective owners.

# 14.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

# 14.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

# 15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



6-Feb-2020

# **PACKAGING INFORMATION**

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish  | MSL Peak Temp      | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------|--------------------|--------------|-------------------------|---------|
| SN65LVDS100D      | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | NIPDAU            | Level-1-260C-UNLIM | -40 to 85    | (4/3)<br>DL100          | Samples |
| SN65LVDS100DG4    | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | NIPDAU            | Level-1-260C-UNLIM | -40 to 85    | DL100                   | Samples |
| SN65LVDS100DGK    | ACTIVE        | VSSOP        | DGK                | 8    | 80             | Green (RoHS<br>& no Sb/Br) | NIPDAU            | Level-1-260C-UNLIM | -40 to 85    | AZK                     | Samples |
| SN65LVDS100DGKG4  | ACTIVE        | VSSOP        | DGK                | 8    | 80             | Green (RoHS<br>& no Sb/Br) | NIPDAU            | Level-1-260C-UNLIM | -40 to 85    | AZK                     | Samples |
| SN65LVDS100DGKR   | ACTIVE        | VSSOP        | DGK                | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU   NIPDAUAG | Level-1-260C-UNLIM | -40 to 85    | AZK                     | Samples |
| SN65LVDS100DR     | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU            | Level-1-260C-UNLIM | -40 to 85    | DL100                   | Samples |
| SN65LVDS100DRG4   | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU            | Level-1-260C-UNLIM | -40 to 85    | DL100                   | Samples |
| SN65LVDS101D      | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | NIPDAU            | Level-1-260C-UNLIM | -40 to 85    | DL101                   | Samples |
| SN65LVDS101DGK    | ACTIVE        | VSSOP        | DGK                | 8    | 80             | Green (RoHS<br>& no Sb/Br) | NIPDAU            | Level-1-260C-UNLIM | -40 to 85    | AZM                     | Samples |
| SN65LVDS101DGKR   | ACTIVE        | VSSOP        | DGK                | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU            | Level-1-260C-UNLIM | -40 to 85    | AZM                     | Samples |
| SN65LVDS101DGKRG4 | ACTIVE        | VSSOP        | DGK                | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU            | Level-1-260C-UNLIM | -40 to 85    | AZM                     | Samples |
| SN65LVDS101DR     | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU            | Level-1-260C-UNLIM | -40 to 85    | DL101                   | Samples |
| SN65LVDT100D      | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | NIPDAU            | Level-1-260C-UNLIM | -40 to 85    | DE100                   | Samples |
| SN65LVDT100DGK    | ACTIVE        | VSSOP        | DGK                | 8    | 80             | Green (RoHS<br>& no Sb/Br) | NIPDAU            | Level-1-260C-UNLIM | -40 to 85    | AZL                     | Samples |
| SN65LVDT100DGKG4  | ACTIVE        | VSSOP        | DGK                | 8    | 80             | Green (RoHS<br>& no Sb/Br) | NIPDAU            | Level-1-260C-UNLIM | -40 to 85    | AZL                     | Samples |
| SN65LVDT100DGKR   | ACTIVE        | VSSOP        | DGK                | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU            | Level-1-260C-UNLIM | -40 to 85    | AZL                     | Samples |
| SN65LVDT100DGKRG4 | ACTIVE        | VSSOP        | DGK                | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU            | Level-1-260C-UNLIM | -40 to 85    | AZL                     | Samples |



6-Feb-2020

| Orderable Device | Status | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp      | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|--------|--------------|--------------------|------|----------------|----------------------------|-------------------------|--------------------|--------------|-------------------------|---------|
| SN65LVDT100DR    | ACTIVE | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM | -40 to 85    | DE100                   | Samples |
| SN65LVDT101D     | ACTIVE | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM | -40 to 85    | DE101                   | Samples |
| SN65LVDT101DG4   | ACTIVE | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM | -40 to 85    | DE101                   | Samples |
| SN65LVDT101DGK   | ACTIVE | VSSOP        | DGK                | 8    | 80             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM | -40 to 85    | BAF                     | Samples |
| SN65LVDT101DGKR  | ACTIVE | VSSOP        | DGK                | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM | -40 to 85    | BAF                     | Samples |
| SN65LVDT101DR    | ACTIVE | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM | -40 to 85    | DE101                   | Samples |

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



6-Feb-2020

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

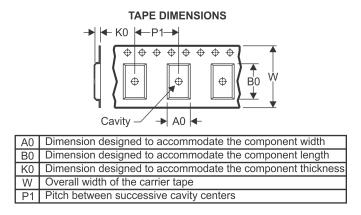
# PACKAGE MATERIALS INFORMATION

www.ti.com

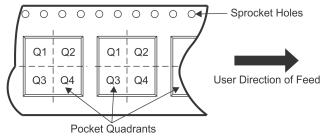
Texas Instruments

# TAPE AND REEL INFORMATION





# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



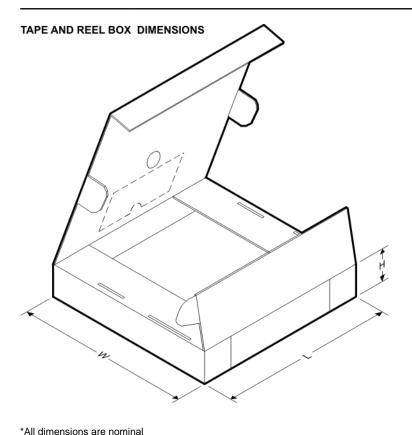
| *All dimensions are nominal |                 |                    |   |      |                          |                          |            |            |            |            |           |                  |
|-----------------------------|-----------------|--------------------|---|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| Device                      | Package<br>Type | Package<br>Drawing |   | SPQ  | Reel<br>Diameter<br>(mm) | Reel<br>Width<br>W1 (mm) | A0<br>(mm) | B0<br>(mm) | K0<br>(mm) | P1<br>(mm) | W<br>(mm) | Pin1<br>Quadrant |
| SN65LVDS100DGKR             | VSSOP           | DGK                | 8 | 2500 | 330.0                    | 12.4                     | 5.3        | 3.4        | 1.4        | 8.0        | 12.0      | Q1               |
| SN65LVDS100DR               | SOIC            | D                  | 8 | 2500 | 330.0                    | 12.4                     | 6.4        | 5.2        | 2.1        | 8.0        | 12.0      | Q1               |
| SN65LVDS101DGKR             | VSSOP           | DGK                | 8 | 2500 | 330.0                    | 12.4                     | 5.3        | 3.4        | 1.4        | 8.0        | 12.0      | Q1               |
| SN65LVDS101DR               | SOIC            | D                  | 8 | 2500 | 330.0                    | 12.4                     | 6.4        | 5.2        | 2.1        | 8.0        | 12.0      | Q1               |
| SN65LVDT100DGKR             | VSSOP           | DGK                | 8 | 2500 | 330.0                    | 12.4                     | 5.3        | 3.4        | 1.4        | 8.0        | 12.0      | Q1               |
| SN65LVDT100DR               | SOIC            | D                  | 8 | 2500 | 330.0                    | 12.4                     | 6.4        | 5.2        | 2.1        | 8.0        | 12.0      | Q1               |
| SN65LVDT101DGKR             | VSSOP           | DGK                | 8 | 2500 | 330.0                    | 12.4                     | 5.3        | 3.4        | 1.4        | 8.0        | 12.0      | Q1               |
| SN65LVDT101DR               | SOIC            | D                  | 8 | 2500 | 330.0                    | 12.4                     | 6.4        | 5.2        | 2.1        | 8.0        | 12.0      | Q1               |

Texas Instruments

www.ti.com

# PACKAGE MATERIALS INFORMATION

31-May-2019



| All dimensions are nominal |              |                 |      |      |             |            |             |
|----------------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| Device                     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
| SN65LVDS100DGKR            | VSSOP        | DGK             | 8    | 2500 | 358.0       | 335.0      | 35.0        |
| SN65LVDS100DR              | SOIC         | D               | 8    | 2500 | 350.0       | 350.0      | 43.0        |
| SN65LVDS101DGKR            | VSSOP        | DGK             | 8    | 2500 | 358.0       | 335.0      | 35.0        |
| SN65LVDS101DR              | SOIC         | D               | 8    | 2500 | 350.0       | 350.0      | 43.0        |
| SN65LVDT100DGKR            | VSSOP        | DGK             | 8    | 2500 | 358.0       | 335.0      | 35.0        |
| SN65LVDT100DR              | SOIC         | D               | 8    | 2500 | 350.0       | 350.0      | 43.0        |
| SN65LVDT101DGKR            | VSSOP        | DGK             | 8    | 2500 | 358.0       | 335.0      | 35.0        |
| SN65LVDT101DR              | SOIC         | D               | 8    | 2500 | 350.0       | 350.0      | 43.0        |

# D0008A



# **PACKAGE OUTLINE**

# SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



#### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.

- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



# D0008A

# **EXAMPLE BOARD LAYOUT**

# SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# D0008A

# **EXAMPLE STENCIL DESIGN**

# SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.



DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.



# DGK (S-PDSO-G8)

# PLASTIC SMALL OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



#### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2020, Texas Instruments Incorporated