LM2771 Low-Ripple 250mA Switched Capacitor Step-Down DC/DC Converter

Check for Samples: LM2771

FEATURES

- **Low-Noise Fixed Frequency Operation**
- **1.5V Output Voltage**
- **Li-Ion (3.6V) to 1.5V with 81% Efficiency**
- **1.7% Output Voltage Accuracy**
- **Very Low Output Ripple: 8mV @ 250mA**
- **Output Currents up to 250mA**
- **2.7V to 5.5V Input Range**
- **Shutdown Disconnects Load from V_{IN}**
- **1.1MHz Switching Frequency**
- **No Inductors…Small Solution Size**
- **Current Limit and Thermal Protection**
- **WSON-10 Package (3mm × 3mm × 0.8mm)**

APPLICATIONS

- **DSP, Memory, and Microprocessor Power Supplies**
- **Mobile Phones and Pagers**
- **Portable Electronic Devices**

DESCRIPTION

The LM2771 is a switched capacitor step-down regulator that produces a 1.5V output without the use of an inductor. It is capable of supplying loads up to 250mA. The LM2771 operates with an input voltage from 2.7V to 5.5V, and requires only 3 low-cost ceramic capacitors.

The LM2771 uses a regulated 0.5x charge pump to give power conversion efficiencies nearly twice as high as an LDO. Pre-regulated 1.1MHz fixed-frequency switching results in very low ripple and noise on both the input and the output. When output currents are low (<30mA typ.), the part automatically switches to a low-ripple PFM regulation mode to maintain high efficiency over the entire load range. At input voltages below 3.5V (Typ), the charge pump goes into pass mode, with efficiencies similar to an LDO.

Typical Application Circuit

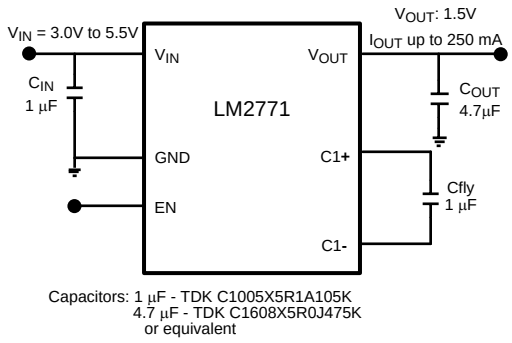


Figure 1.

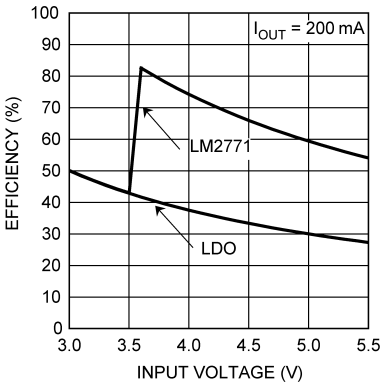
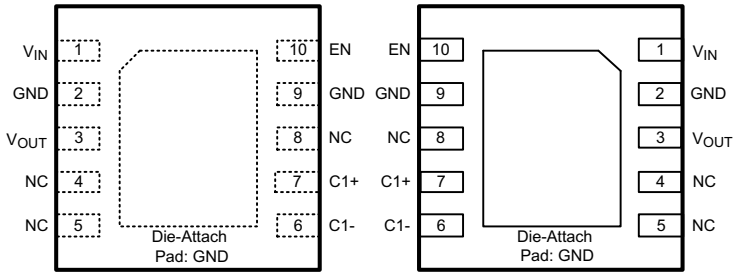


Figure 2. LM2771 Efficiency vs. Low-Dropout Linear Regulator (LDO) Efficiency

Connection Diagram

Figure 3. 10-Pin Non-Pullback Leadless Frame Package (WSON-10)
Package Number DSC0010A



Pin Descriptions

Pin #	Name	Description
1	V_{IN}	Input Voltage: Recommended V_{IN} operating range 3.0V to 5.5V.
2	GND	Ground
3	V_{OUT}	Output Voltage
4	NC	No Connect
5	NC	No Connect
6	C1-	Flying Capacitor 1: Negative Terminal
7	C1+	Flying Capacitor 1: Positive Terminal
8	NC	No Connect
9	GND	Ground
10	EN	Enable Pin Logic Input. Applying a logic HIGH voltage signal enables the part. A logic LOW voltage signal places the the device in shutdown.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

V_{IN} Pin Voltage		-0.3V to 6.0V
EN Pin Voltage		-0.3V to (V_{IN}+0.3V) w/ 6.0V max
Continuous Power Dissipation(4)		Internally Limited
Junction Temperature (T_{J-MAX})		150ºC
Storage Temperature Range		-65ºC to +150º C
Maximum Lead Temperature(5)		265ºC
ESD Rating(6)	Human Body Model	2.0kV
	Machine Model	200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply ensured performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) All voltages are with respect to the potential at the GND pins.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=150ºC (typ.) and disengages at T_J=140ºC (typ.).
(5) For detailed information on soldering requirements and recommendations, please refer to Texas Instruments' Application Note 1187 (Literature Number SNOA401): Leadless Leadframe Package (LLP).
(6) The Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Operating Ratings (1)(2)

Input Voltage Range	2.7V to 5.5V
Recommended Load Current Range	0mA to 250mA
Junction Temperature (T_J) Range	-30°C to +110°C
Ambient Temperature (T_A) Range (3)	-30°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply ensured performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins.
(3) Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 110ºC), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} - (\theta_{JA} \times P_{D\text{-}MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), WSON-10 Package (1)	55°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues.

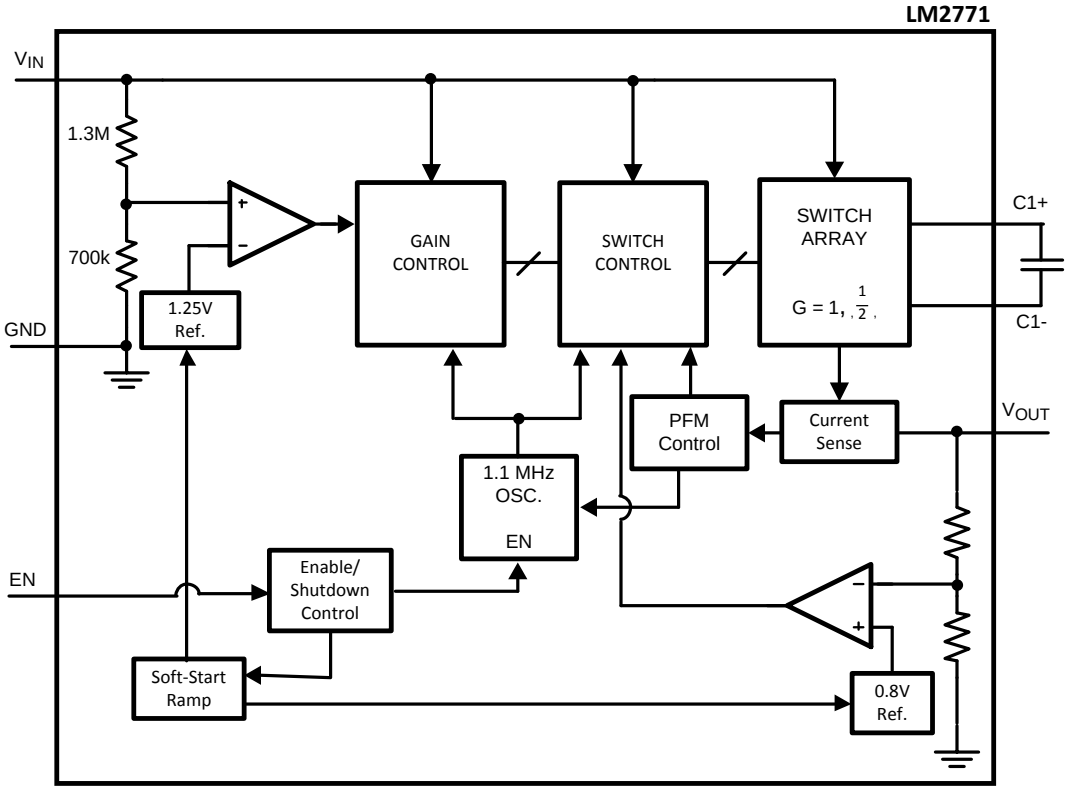
Electrical Characteristics (1)(2)

Limits in standard typeface are for T_J = 25ºC. Limits in **boldface** type apply over the full operating junction temperature range (-30°C ≤ T_J ≤ +110°C) . Unless otherwise noted, specifications apply to the LM2771 Typical Application Circuit (pg. 1) with: V_{IN} = 3.6V; V(EN) = 1.8V, C_{IN} = C_1 = 1.0µF, C_{OUT} = 4.7µF. (3)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	1.5V Output Voltage Regulation	3.0V ≤ V_{IN} ≤ 5.5V 0mA ≤ I_{OUT} ≤ 200mA	**1.455 (−3%)**	1.5	**1.545 (+3%)**	V
		3.0V ≤ V_{IN} ≤ 5.5V I_{OUT} = 150mA	**1.475 (−1.7%)**	1.5	**1.525 (+1.7%)**	
		3.0V < V_{IN} ≤ 5.5V, 0mA ≤ I_{OUT} ≤ 250mA	1.445 (−3.7%)	1.5	1.545 (+3%)	
V_{OUT}/I_{OUT}	Output Load Regulation	V_{OUT} = 1.5V 0mA ≤ I_{OUT} ≤ 250mA		0.17		mV/mA
V_{OUT}/V_{IN}	Output Line Regulation			0.1		%/V
E	Power Efficiency	I_{OUT} = 200mA		81		%
I_Q	Quiescent Supply Current	I_{OUT} = 0mA (4)		45	**50**	µA
V_R	Fixed Frequency Output Ripple	40mA ≤ I_{OUT} ≤ 250mA		8		mV
$V_{R–PFM}$	PFM–Mode Output Ripple	I_{OUT} < 40mA		12		mV
I_{SD}	Shutdown Current	V(EN) = 0V		0.1	**0.5**	µA
F_{SW}	Switching Frequency	3.2V ≤ V_{IN} ≤ 5.5V	**0.80**	1.1	**1.40**	MHz
R_{OL}	Open–Loop Output Resistance	I_{OUT} = 200mA (5)		1.0		Ω
I_{CL}	Output Current Limit	V_{IN} = 5.5V 0V ≤ V_{OUT} ≤ 0.2V (6)		500		mA
t_{ON}	Turn-on Time			150		µs
V_{IL}	Logic-low Input Voltage	3.0V ≤ V_{IN} ≤ 5.5V	**0**		**0.5**	V
V_{IH}	Logic-high Input Voltage	3.0V ≤ V_{IN} ≤ 5.5V	**0.95**		**V_{IN}**	V
I_{IH}	Logic-high Input Current	V(EN) = 1.8V (7)		5		µA
I_{IL}	Logic-low Input Current	Logic Input = 0V		0.1		µA

(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(3) C_{IN}, C_{OUT}, C_1: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
(4) V_{OUT} is set to 1.6V during this test.
(5) Open loop output resistance can be used to predict output voltage when, under low V_{IN} and high I_{OUT} conditions, V_{OUT} falls out of regulation. $V_{OUT} = V_{IN}/2 - (R_{OL} \times I_{OUT})$
(6) Maximum input current is equal to half the maximum output current for buck-mode switched capacitor converters.
(7) There is a 350kΩ pull-down resistor connected internally between the EN pin and GND.

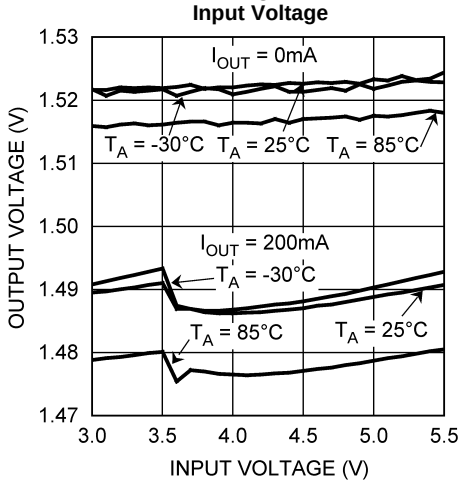
Block Diagram



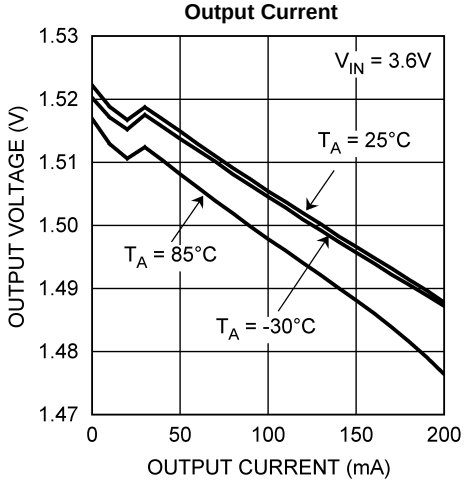
Typical Performance Characteristics

Unless otherwise specified: V_{IN} = 3.6V, C_{IN} = C_1 = 1.0µF, C_{OUT} = 4.7µF, T_A = 25ºC. Capacitors are low-ESR multi-layer ceramic capacitors (MLCC's).

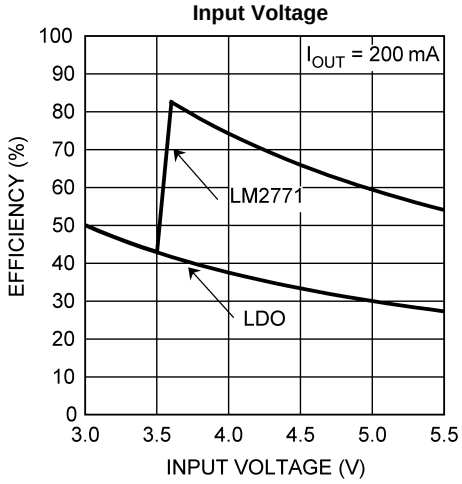
Output Voltage vs. Input Voltage



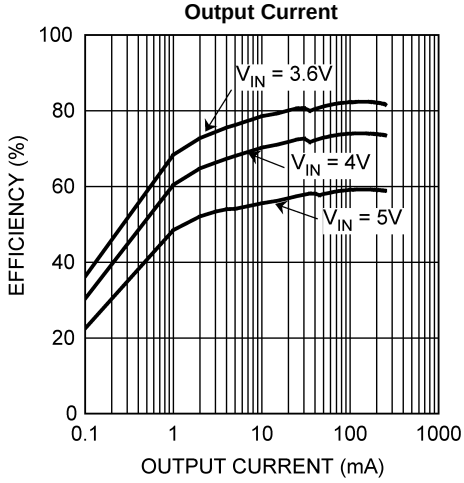
Output Voltage vs. Output Current



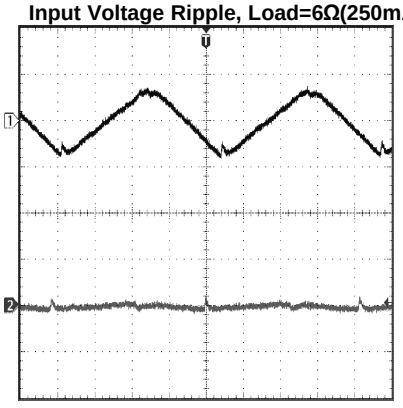
Efficiency vs. Input Voltage



Efficiency vs. Output Current

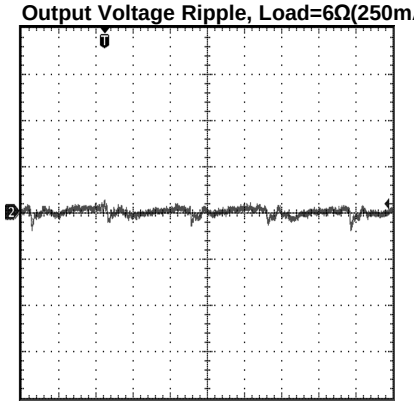


Input Voltage Ripple, Load=6Ω(250mA)



CH1: V_{IN}, C_{IN} = 1µF; Scale: 50mV/Div, AC Coupled
CH2: V_{IN}, C_{IN} = 10µF; Scale: 50mV/Div, AC Coupled
Time scale: 200ns/Div

Output Voltage Ripple, Load=6Ω(250mA)

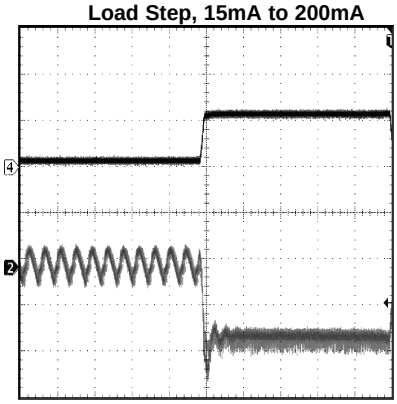


CH2: V_{OUT}, C_{OUT} = 4.7µF; Scale: 20mV/Div, AC Coupled
Time scale: 200ns/Div

Typical Performance Characteristics (continued)

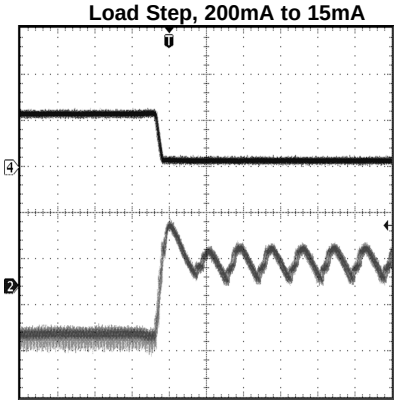
Unless otherwise specified: V_{IN} = 3.6V, C_{IN} = C_1 = 1.0µF, C_{OUT} = 4.7µF, T_A = 25ºC. Capacitors are low-ESR multi-layer ceramic capacitors (MLCC's).

Load Step, 15mA to 200mA



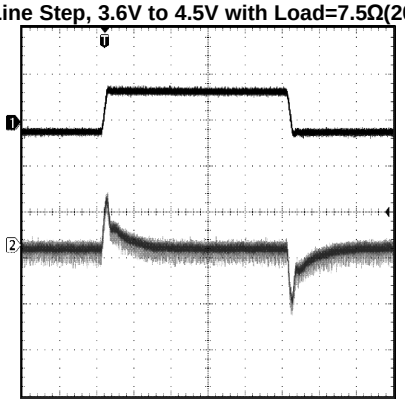
CH2: V_{OUT}; Scale: 20mV/Div, AC Coupled
CH4: I_{OUT}; Scale: 200mA/Div
Time scale: 20µs/Div

Load Step, 200mA to 15mA



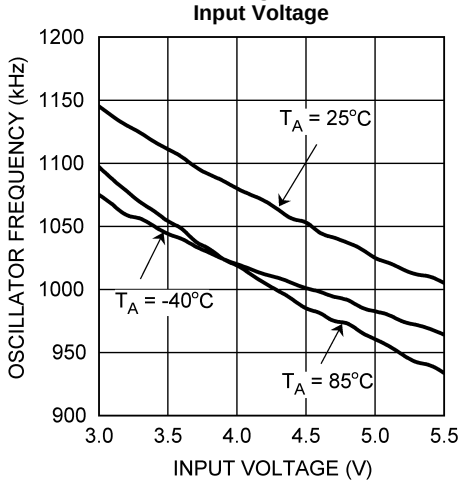
CH2: V_{OUT}; Scale: 20mV/Div, AC Coupled
CH4: I_{OUT}; Scale: 200mA/Div
Time scale: 10µs/Div

Line Step, 3.6V to 4.5V with Load=7.5Ω(200mA)

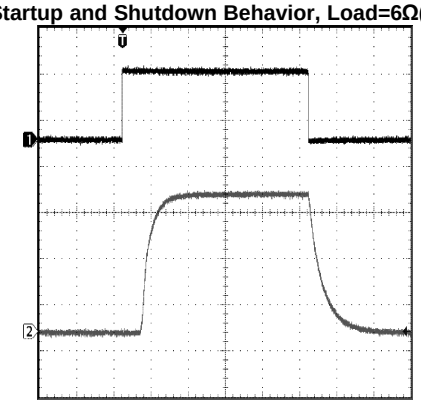


CH1: V_{IN}; Scale: 1V/Div, AC Coupled
CH2: V_{OUT}; Scale: 20mV/Div, AC Coupled
Time scale: 40µs/Div

Oscillator Frequency vs. Input Voltage



Startup and Shutdown Behavior, Load=6Ω(250mA)



CH1: V_{EN}; Scale: 2V/Div, DC Coupled
CH2: V_{OUT}; Scale: 500mV/Div, DC Coupled
Time scale: 100µs/Div

OPERATION DESCRIPTION

OVERVIEW

The LM2771 is a switched capacitor converter that produces a regulated, low voltage output. The core of the part is a highly efficient charge pump that utilizes fixed frequency pre-regulation and Pulse Frequency Modulation to minimize ripple and power losses over wide input voltage and output current ranges. A description of the principal operational characteristics of the LM2771 is detailed in the CIRCUIT DESCRIPTION, and EFFICIENCY PERFORMANCE sections. These sections refer to details in the Block Diagram.

CIRCUIT DESCRIPTION

The core of the LM2771 is a two-phase charge pump controlled by an internally generated non-overlapping clock. The charge pump operates by using an external flying capacitor, C1, to transfer charge from the input to the output. At input voltages below 3.5V (typ.) the LM2771 operates in a "pass mode", with the input current being equal to the load current. At input voltages above 3.5V (typ.) the part utilizes a gain of ½, resulting in an input current equal to half the load current.

The two phases of the switched capacitor switching cycle will be referred to as the "charge phase" and the "discharge phase". During the charge phase, the flying capacitor is charged by the input supply. After half of the switching cycle [$t = 1/(2\times F_{SW})$], the LM2771 switches to the discharge phase. In this configuration, the charge that was stored on the flying capacitor in the charge phase is transferred to the output.

The LM2771 uses fixed frequency pre-regulation to regulate the output voltage to 1.5V during moderate to high load currents. The input and output connections of the flying capacitor is made with internal MOS switches. Pre-regulation limits the gate drive of the MOS switch connected between the voltage input and the flying capacitor. Controlling the on resistance of this switch limits the amount of charge transferred into and out of the flying capacitor during the charge and discharge phases, and in turn helps to keep the output ripple very low.

When output currents are low (<30mA typ.), the LM2771 automatically switches to a low-ripple Pulse Frequency Modulation (PFM) form of regulation. In PFM mode, the flying capacitor stays in the discharge phase until the output voltage drops below a predetermined trip point. When this occurs, the flying capacitor switches back to the charge phase. After being charged, the flying capacitor repeats the process of staying in the discharge phase and switching to the charge phase when necessary.

EFFICIENCY PERFORMANCE

Charge-pump efficiency is derived in the following two ideal equations (supply current and other losses are neglected for simplicity):

$$I_{IN} = G \times I_{OUT}\ E = (V_{OUT} \times I_{OUT}) \div (V_{IN} \times I_{IN}) = V_{OUT} \div (G \times V_{IN}) \quad (1)$$

In the equations, G represents the charge pump gain. Efficiency is at its highest as $G\times V_{IN}$ approaches V_{OUT}. Refer to the efficiency graph in the Typical Performance Characteristics section for detailed efficiency data. The transition between Pass mode and the gain of ½ is clearly distinguished by the sharp discontinuity in the efficiency curve.

SHUTDOWN

The LM2771 is in shutdown mode when the voltage on the enable pin (EN) is logic-low. In shutdown, the LM2771 draws virtually no supply current. When in shutdown, the output of the LM2771 is completely disconnected from the input. The internal feedback resistors will pull the output voltage down to 0V.

SOFT-START

The LM2771 employs soft start circuitry to prevent excessive input inrush currents during startup. At startup, the output voltage gradually rises from 0V to the nominal output voltage. This occurs in 150µs (typ.). Soft-start is engaged when the part is enabled, including situations where voltage is established simultaneously on the V_{IN} and EN pins.

THERMAL SHUTDOWN

Protection from damage related to overheating is achieved with a thermal shutdown feature. When the junction temperature rises to 150ºC (typ.), the part switches into shutdown mode. The LM2771 disengages thermal shutdown when the junction temperature of the part is reduced to 140ºC (typ.). Due to the high efficiency of the LM2771, thermal shutdown and/or thermal cycling should not be encountered when the part is operated within specified input voltage, output current, and ambient temperature operating ratings. If thermal cycling is seen under these conditions, the most likely cause is an inadequate PCB layout that does not allow heat to be sufficiently dissipated out of the WSON package.

CURRENT LIMIT PROTECTION

The LM2771 charge pump contains current limit protection circuitry that protects the device during V_{OUT} fault conditions where excessive current is drawn. Output current is limited to 500mA (typ).

Application Information

RECOMMENDED CAPACITOR TYPES

The LM2771 requires 3 external capacitors for proper operation. Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive and have very low equivalent series resistance (ESR, ≤ 15mΩ typ.). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors generally are not recommended for use with the LM2771 due to their high ESR, as compared to ceramic capacitors.

For most applications, ceramic capacitors with an X7R or X5R temperature characteristic are preferred for use with the LM2771. These capacitors have tight capacitance tolerance (as good as ±10%) and hold their value over temperature (X7R: ±15% over -55ºC to 125ºC; X5R: ±15% over -55ºC to 85ºC).

Capacitors with a Y5V or Z5U temperature characteristic are generally not recommended for use with the LM2771. These types of capacitors typically have wide capacitance tolerance (+80%, -20%) and vary significantly over temperature (Y5V: +22%, -82% over -30ºC to +85ºC range; Z5U: +22%, -56% over +10ºC to +85ºC range). Under some conditions, a 1µF-rated Y5V or Z5U capacitor could have a capacitance as low as 0.1µF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM2771.

Net capacitance of a ceramic capacitor decreases with increased DC bias. This degradation can result in lower capacitance than expected on the input and/or output, resulting in higher ripple voltages and currents. Using capacitors at DC bias voltages significantly below the capacitor voltage rating will usually minimize DC bias effects. Consult capacitor manufacturers for information on capacitor DC bias characteristics.

Capacitance characteristics can vary quite dramatically with different application conditions, capacitor types, and capacitor manufacturers. It is strongly recommended that the LM2771 circuit be thoroughly evaluated early in the design-in process with the mass-production capacitors of choice. This will help ensure that any such variability in capacitance does not negatively impact circuit performance.

The table below lists some leading ceramic capacitor manufacturers.

Manufacturer	Contact Information
AVX	www.avx.com
Murata	www.murata.com
Taiyo-Yuden	www.t-yuden.com
TDK	www.component.tdk.com
Vishay-Vitramon	www.vishay.com

OUTPUT CAPACITOR AND OUTPUT VOLTAGE RIPPLE

The output capacitor in the LM2771 circuit (C_{OUT}) directly impacts the magnitude of output voltage ripple. Other prominent factors also affecting output voltage ripple include input voltage, output current and flying capacitance. Due to the complexity of the regulation topology, providing equations or models to approximate the magnitude of the ripple can not be easily accomplished. But one important generalization can be made: increasing (decreasing) the output capacitance will result in a proportional decrease (increase) in output voltage ripple.

In typical high-current applications, a 4.7µF low-ESR ceramic output capacitor is recommended. Different output capacitance values can be used to reduce ripple, shrink the solution size, and/or cut the cost of the solution. But changing the output capacitor may also require changing the flying capacitor and/or input capacitor to maintain good overall circuit performance. Performance of the LM2771 with different capacitor setups in discussed in the section RECOMMENDED CAPACITOR CONFIGURATIONS.

High ESR in the output capacitor increases output voltage ripple. If a ceramic capacitor is used at the output, this is usually not a concern because the ESR of a ceramic capacitor is typically very low and has only a minimal impact on ripple magnitudes. If a different capacitor type with higher ESR is used (tantalum, for example), the ESR could result in high ripple. To eliminate this effect, the net output ESR can be significantly reduced by placing a low-ESR ceramic capacitor in parallel with the primary output capacitor. The low ESR of the ceramic capacitor will be in parallel with the higher ESR, resulting in a low net ESR based on the principles of parallel resistance reduction.

INPUT CAPACITOR AND INPUT VOLTAGE RIPPLE

The input capacitor (C_{IN}) is a reservoir of charge that aids a quick transfer of charge from the supply to the flying capacitor during the charge phase of operation. The input capacitor helps to keep the input voltage from drooping at the start of the charge phase when the flying capacitor is connected to the input. It also filters noise on the input pin, keeping this noise out of sensitive internal analog circuitry that is biased off the input line.

Much like the relationship between the output capacitance and output voltage ripple, input capacitance has a dominant and first-order effect on input ripple magnitude. Increasing (decreasing) the input capacitance will result in a proportional decrease (increase) in input voltage ripple. Input voltage, output current, and flying capacitance also will affect input ripple levels to some degree.

In typical high-current applications, a 1µF low-ESR ceramic capacitor is recommended on the input. Different input capacitance values can be used to reduce ripple, shrink the solution size, and/or cut the cost of the solution. But changing the input capacitor may also require changing the flying capacitor and/or output capacitor to maintain good overall circuit performance. Performance of the LM2771 with different capacitor setups is discussed below in RECOMMENDED CAPACITOR CONFIGURATIONS.

FLYING CAPACITOR

The flying capacitor (C_1) transfers charge from the input to the output. Flying capacitance can impact both output current capability and ripple magnitudes. If flying capacitance is too small, the LM2771 may not be able to regulate the output voltage when load currents are high. On the other hand, if the flying capacitance is too large, the flying capacitor might overwhelm the input and output capacitors, resulting in increased input and output ripple.

Polarized capacitors (tantalum, aluminum electrolytic, etc.) must not be used for the flying capacitor, as they could become reverse-biased during LM2771 operation.

RECOMMENDED CAPACITOR CONFIGURATIONS

The data in Table 1 can be used to assist in the selection of a capacitor configuration that best balances solution size and cost with the electrical requirements of the application.

As previously discussed, input and output ripple voltages will vary with output current and input voltage. The numbers provided show expected ripple voltage when V_{IN} = 3.6V and load currents are between 10mA and 200mA. The table offers first look at approximate ripple levels and provides a comparison for the different capacitor configurations presented, but is not intended to ensure performance.

Table 1. LM2771 Performance with Different Capacitor Configurations (1)

CAPACITOR CONFIGURATION (V_{IN} = 3.6V)	TYPICAL INPUT RIPPLE	TYPICAL OUTPUT RIPPLE
C_{IN} = 1µF, C_{OUT} = 4.7µF, C_1 = 1µF	45mV	8mV
C_{IN} = 1µF, C_{OUT} = 2.2µF, C_1 = 1µF	94mV	19mV
C_{IN} = 0.47µF, C_{OUT} = 4.7µF, C_1 = 1µF	105mV	11mV
C_{IN} = 0.47µF, C_{OUT} = 3.3µF, C_1 = 1µF	102mV	16mV
C_{IN} = 0.47µF, C_{OUT} = 3.3µF, C_1 = 0.33µF	120mV	15mV

(1) Refer to the text in the Recommended Capacitor Configurations section for detailed information on the data in this table

Layout Guidelines

Proper board layout will help to ensure optimal performance of the LM2771 circuit. The following guidelines are recommended:

- Place capacitors as close to the LM2771 as possible, and preferably on the same side of the board as the IC.
- Use short, wide traces to connect the external capacitors to the LM2771 to minimize trace resistance and inductance.
- Use a low resistance connection between ground and the GND pin of the LM2771. Using wide traces and/or multiple vias to connect GND to a ground plane on the board is most advantageous.

REVISION HISTORY

Changes from Original (May 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2771SD/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-30 to 110	L2771	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

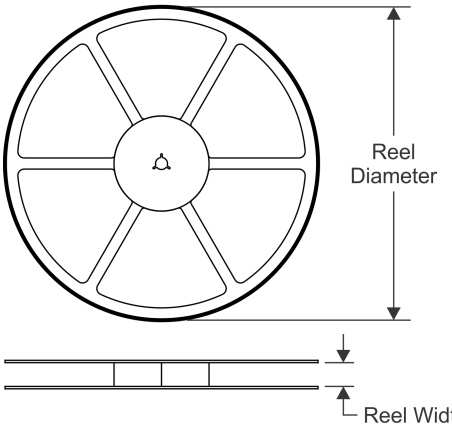
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

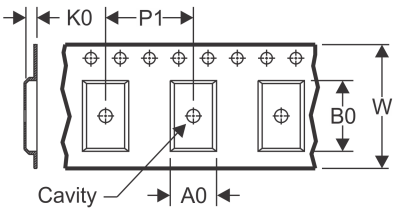
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

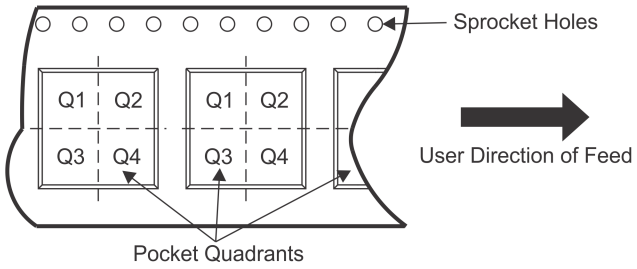


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

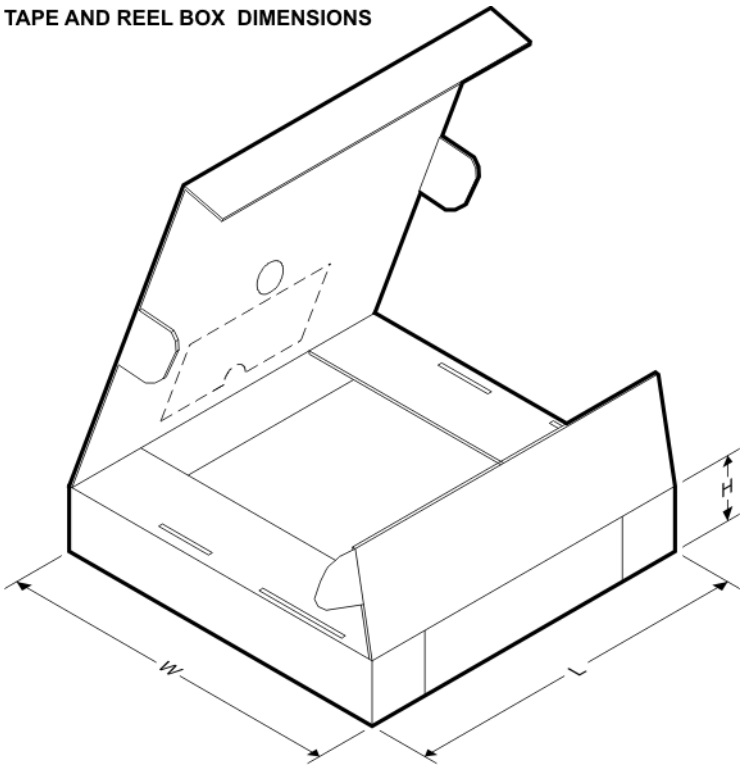
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2771SD/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

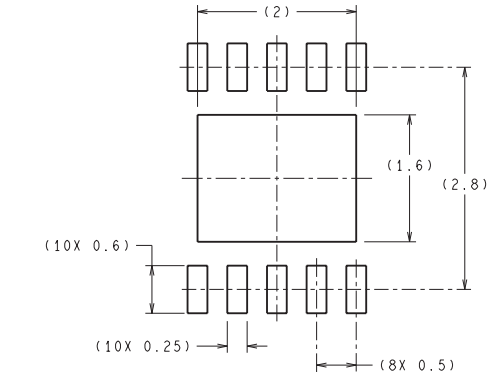
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

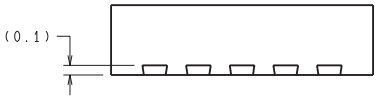
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2771SD/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0

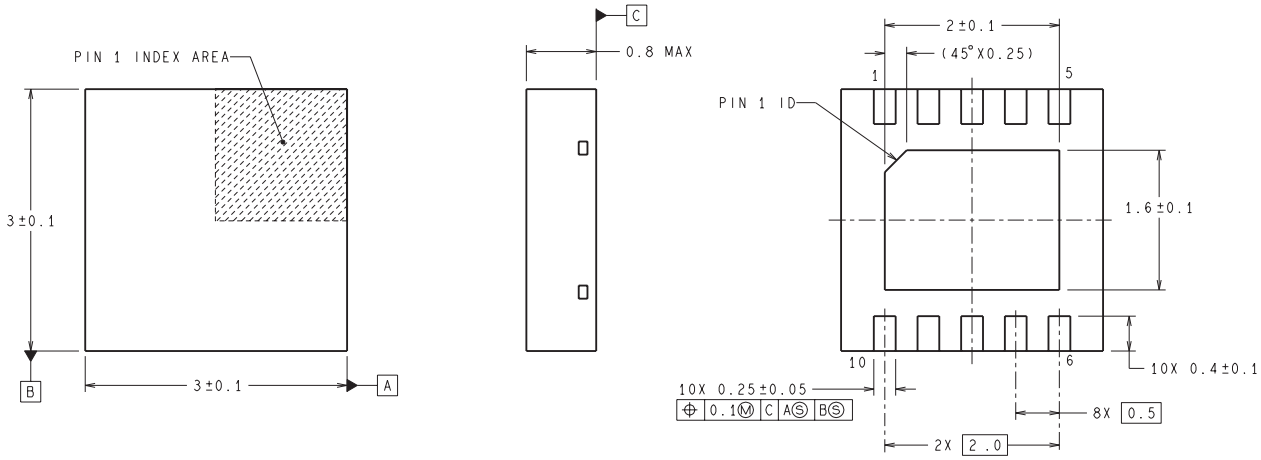
DSC0010A



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





SDA10A (Rev A)

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