

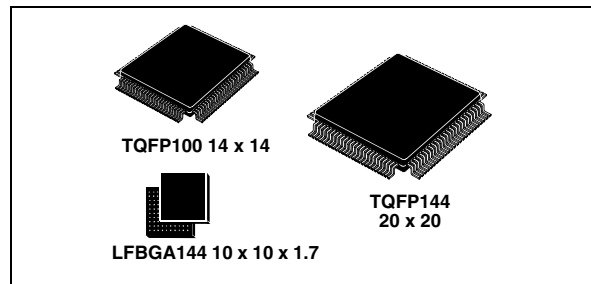


STR73xFxx

ARM7TDMI™ 32-bit MCU with Flash, 3x CAN, 4 UARTs, 20 timers, ADC, 12 comm. interfaces

Features

- **Core**
 - ARM7TDMI 32-bit RISC CPU
 - 32 MIPS @ 36 MHz
- **Memories**
 - Up to 256 Kbytes Flash program memory (10,000 cycles endurance, data retention 20 years @ 85° C)
 - 16 Kbytes RAM
- **Clock, reset and supply management**
 - 4.5 - 5.5 V application supply and I/Os
 - Embedded 1.8 V regulator for core supply
 - Embedded oscillator running from external 4-8 MHz crystal or ceramic resonator
 - Up to 36 MHz CPU frequency with internal PLL
 - 32 kHz or 2 MHz internal RC oscillator, software configurable for fast startup and backup clock
 - Real-time clock for clock-calendar function
 - Wake-up timer driven by internal RC for wake-up from STOP mode
 - 5 power saving modes: SLOW, WFI, LPWFI, STOP and HALT modes
- **Nested interrupt controller**
 - Fast interrupt handling with multiple vectors
 - 64 maskable IRQs with 64 vectors and 16 priority levels
 - 2 maskable FIQ sources
 - 16 external interrupts, up to 32 wake-up lines
- **Up to 112 I/O ports**
 - 72/112 multifunctional bidirectional I/Os



- **DMA**
 - 4 DMA controllers with 4 channels each
- **Timers**
 - 16-bit watchdog timer (WDG)
 - 6/10 16-bit timers (TIM) each with: 2 input captures, 2 output compares, PWM and pulse counter modes
 - 6 16-bit PWM modules (PWM)
 - 3 16-bit timebase timers with 8-bit prescalers
- **12 communications interfaces**
 - 2 I²C interfaces
 - 4 UART asynchronous serial interfaces
 - 3 BSPI synchronous serial interfaces
 - Up to 3 CAN interfaces (2.0B Active)
- **10-bit A/D converter**
 - 12/16 channels
 - Conversion time: min. 3 μs, range: 0 to 5V
- **Development tools support**
 - JTAG interface

Table 1. Device summary

| Reference | Part number |
|-----------|--|
| STR73xFxx | STR730FZ1, STR730FZ2, STR731FV0, STR731FV1, STR731FV2, STR735FZ1, STR735FZ2, STR736FV0, STR736FV1, STR736FV2 |

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1 Scope

This datasheet provides the STR73x ordering information, mechanical and electrical device characteristics.

For complete information on the STR73xF microcontroller memory, registers and peripherals, please refer to the STR73x reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash programming reference manual.

For information on the ARM7TDMI core please refer to the ARM7TDMI technical reference manual.

1.1 Description

ARM core with embedded Flash & RAM

STR73xF family combines the high performance ARM7TDMI™ CPU with an extensive range of peripheral functions and enhanced I/O capabilities. All devices have on-chip high-speed single voltage Flash memory and high-speed RAM. The STR73xF family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Extensive tools support

STMicroelectronics' 32-bit, ARM core-based microcontrollers are supported by a complete range of high-end and low-cost development tools to meet the needs of application developers. This extensive line of hardware/software tools includes starter kits and complete development packages all tailored for ST's ARM core-based MCUs.

The range of development packages includes third-party solutions that come complete with a graphical development environment and an in-circuit emulator/programmer featuring a JTAG application interface. These support a range of embedded operating systems (OS), while several royalty-free OSs are also available.

For more information, please refer to ST MCU site <http://www.st.com/mcu>

Figure 1 shows the general block diagram of the device family.



2 Overview

Table 2. Product overview

| Features | STR730FZx | | STR735FZx | | STR731FVx | | | STR736FVx | | |
|-----------------------|---|------|-----------|------|--|------|------|-----------|------|------|
| | 128K | 256K | 128K | 256K | 64K | 128K | 256K | 64K | 128K | 256K |
| Flash memory - bytes | 128K | 256K | 128K | 256K | 64K | 128K | 256K | 64K | 128K | 256K |
| RAM - bytes | 16 K | | | | 16 K | | | | | |
| Peripheral functions | 10 TIM timers, 112 I/Os, 32 wake-up lines, 16 ADC | | | | 6 TIM timers, 72 I/Os, 18 wake-up lines, 12 ADC channels | | | | | |
| CAN peripherals | 3 | | 0 | | 3 | | | 0 | | |
| Operating voltage | 4.5 to 5.5 V | | | | | | | | | |
| Operating temperature | -40 to +85°C/-40 to +105° C | | | | | | | | | |
| Packages | T=TQFP144 20 x 20 H=LFBGA144 10 x10 | | | | T=TQFP100 14x14 | | | | | |

Package choice: reduced pin-count TQFP100 or feature-rich 144-pin TQFP or LFBGA

The STR73xF family is available in 3 packages. The TQFP144 and LFBGA144 versions have the full set of all features. The 100-pin version has fewer timers, I/Os and ADC channels. Refer to the Device Summary on Page 1 for a comparison of the I/Os available on each package.

The family includes versions with and without CAN.

High speed Flash memory

The Flash program memory is organized in 32-bit wide memory cells which can be used for storing both code and data constants. It is accessed by CPU with zero wait states @ 36 MHz.

The STR7 embedded Flash memory can be programmed using in-circuit programming or in-application programming.

The Flash memory endurance is 10K write/erase cycles and the data retention is 20 years @ 85° C.

IAP (in-application programming): IAP is the ability to re-program the Flash memory of a microcontroller while the user program is running.

ICP (in-circuit programming): ICP is the ability to program the Flash memory of a microcontroller using JTAG protocol while the device is mounted on the user application board.

The Flash memory can be protected against different types of unwanted access (read/write/erase). There are two types of protection:

- Sector write protection
- Flash debug protection (locks JTAG access)

Flexible power management

To minimize power consumption, you can program the STR73xF to switch to SLOW, WFI LPWFI, STOP or HALT modes depending on the current system activity in the application.

Flexible clock control

Two clock sources are used to drive the microcontroller, a main clock driven by an external crystal or ceramic resonator and an internal backup RC oscillator that operates at 2 MHz or 32 kHz. The embedded PLL can be configured to generate an internal system clock of up to 36 MHz. The PLL output frequency can be programmed using a wide selection of multipliers and dividers.

Voltage regulators

The STR73xF requires an external 4.5 to 5.5 V power supply. There are two internal Voltage Regulators for generating the 1.8 V power supply needed by the core and peripherals. The main VR is switched off and the Low Power VR switched on when the application puts the STR73xF in Low Power Wait for Interrupt (LPWFI) mode.

Low voltage detectors

The voltage regulator and Flash modules each have an embedded LVD that monitors the internal 1.8 V supply. If the voltage drops below a certain threshold, the LVD will reset the STR73xF.

Note: An external power-on reset must be provided ensure the microcontroller starts-up correctly.

2.1 On-chip peripherals

CAN interfaces

The three CAN modules are compliant with the CAN specification V2.0 part B (active). The bit rate can be programmed up to 1 Mbaud. These are not available in the STR735 and STR736.

DMA

4 DMA controllers, each with 4 data streams manage memory to memory, peripheral to peripheral, peripheral to memory and memory to peripheral transfers. The DMA requests are connected to TIM timers, BSPI0, BSPI1, BSPI2 and ADC. One of the streams can be configured to be triggered by a software request, independently from any peripheral activity.

16-bit timers (TIM)

Each of the ten timers (six in 100-pin devices) have a 16-bit free-running counter with 7-bit prescaler, up to two input capture/output compare functions, a pulse counter function, and a PWM channel with selectable frequency. This provides a total of 16 independent PWMs (12 in 100-pin devices) when added with the PWM modules (see next paragraph).

PWM modules (PWM)

The six 16-bit PWM modules have independently programmable periods and duty-cycles, with 5+3 bit prescaler factor.

Timebase timers (TB)

The three 16-bit timebase timers with 8-bit prescaler for general purpose time triggering operations.

Real-time clock (RTC)

The RTC provides a set of continuously running counters driven by separate clock signal derived from the main oscillator. The RTC can be used as a general timebase or

clock/calendar/alarm function. When the STR73xF is in LPWFI mode the RTC keeps running, powered by the low power voltage regulator.

UARTs

The 4 UARTs allow full duplex, asynchronous, communications with external devices with independently programmable TX and RX baud rates up to 625 Kbaud.

Buffered serial peripheral interfaces (BSPi)

Each of the three BSPi allow full duplex, synchronous communications with external devices, master or slave communication at up to 6 Mb/s in master mode and up to 4.5 Mb/s in slave mode (@36 MHz system clock).

I²C interfaces

The two I²C Interfaces provide multi-master and slave functions, support normal and fast I²C mode (400 kHz) and 7 or 10-bit addressing modes.

A/D converter

The 10-bit analog to digital converter, converts up to 16 channels in single-shot or continuous conversion modes (12 channels in 100-pin devices). The minimum conversion time is 3 μ s.

Watchdog

The 16-bit watchdog timer protects the application against hardware or software failures and ensures recovery by generating a reset.

I/O ports

Up to 112 I/O ports (72 in 100-pin devices) are programmable as general purpose input/output or alternate function.

External interrupts and wake-up lines

16 external interrupts lines are available for application use. In addition, up to 32 external Wake-up lines (18 in 100-pin devices) can be used as general purpose interrupts or to wake-up the application from STOP mode.

3 Block diagram

Figure 1. STR730F/STR735F block diagram

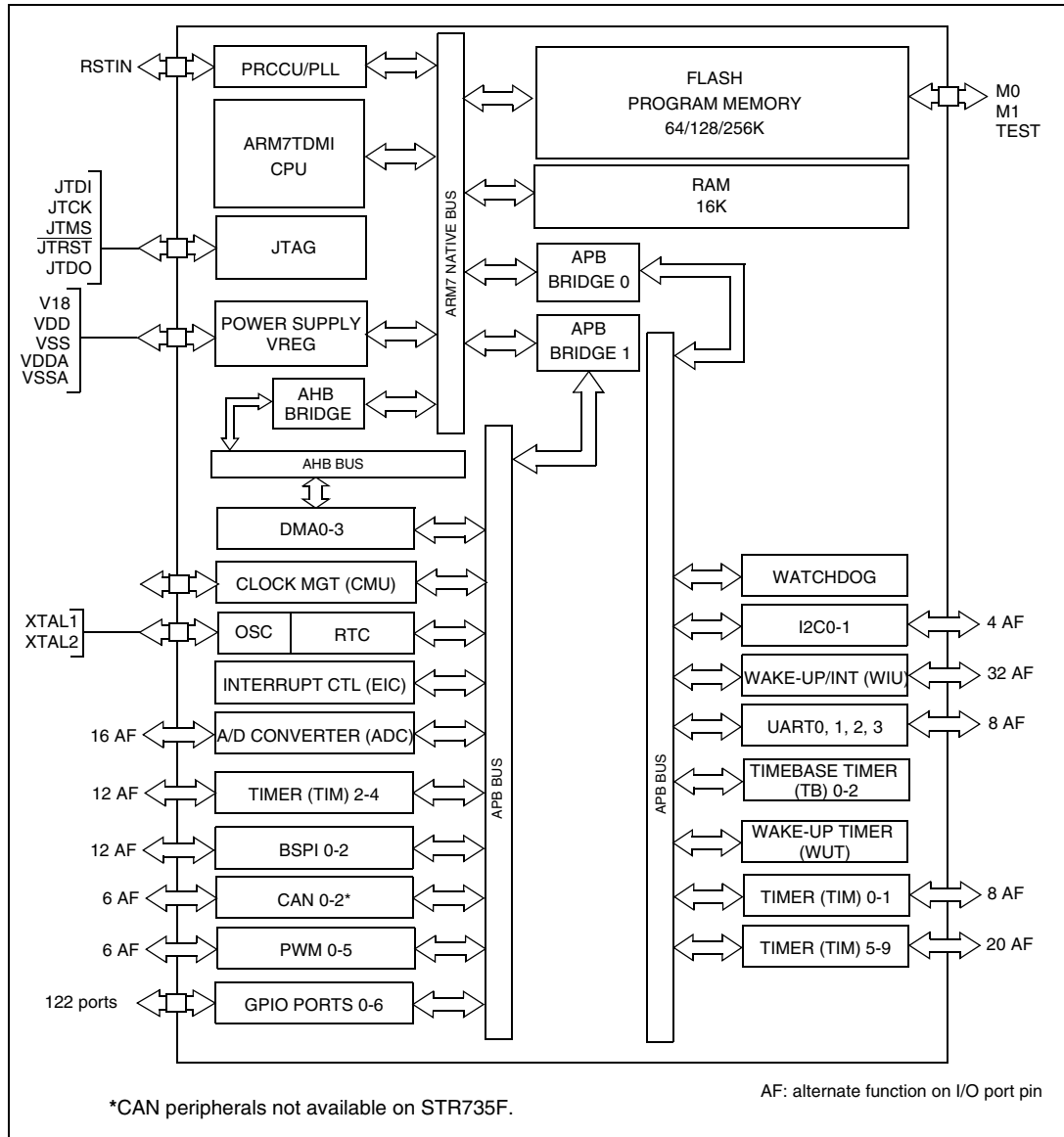
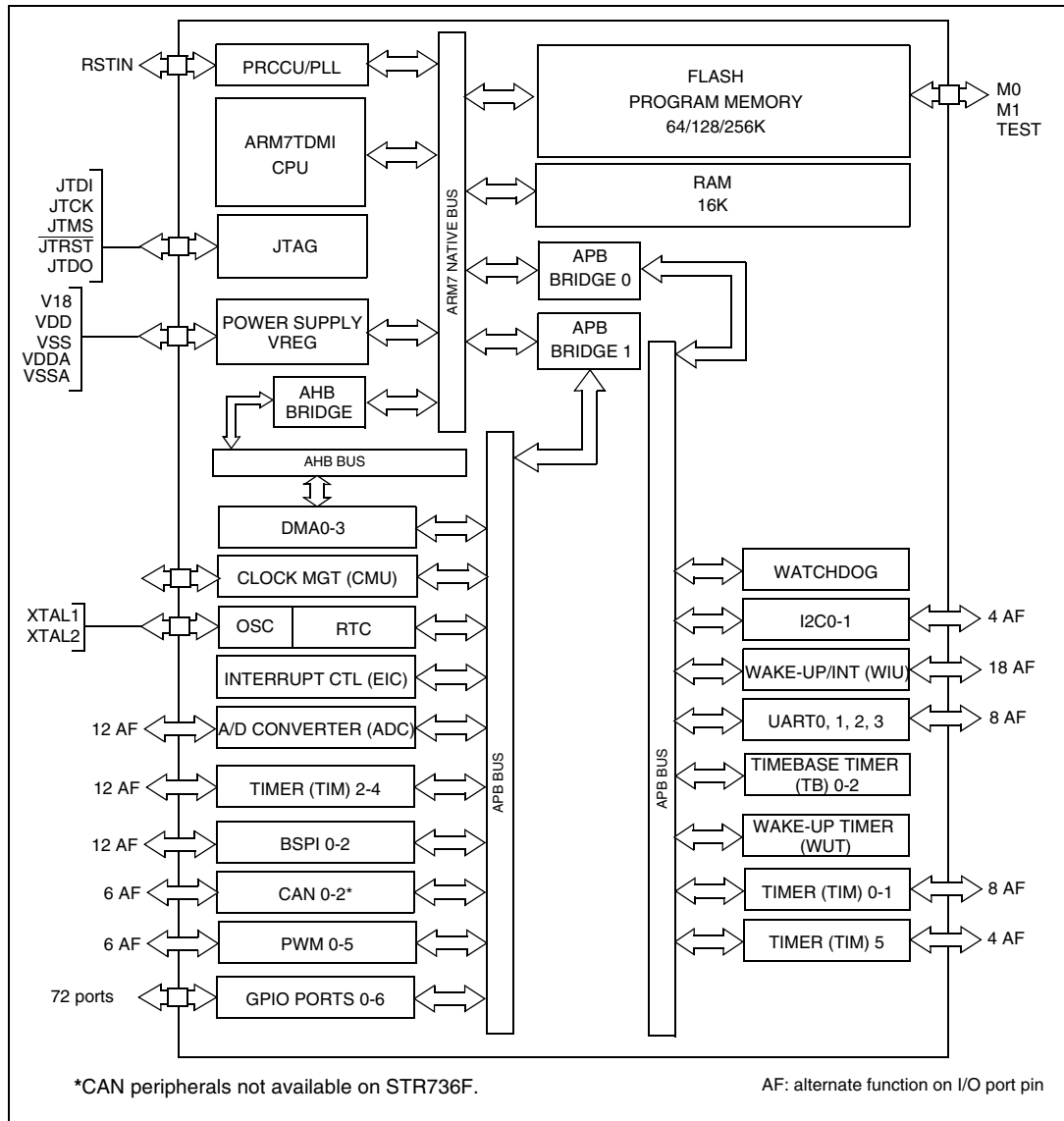


Figure 2. STR731F/STR736 block diagram



3.1 Related documentation

Available from www.arm.com:

ARM7TDMI technical reference manual

Available from <http://www.st.com>:

STR73x reference manual (RM0001)

STR7 Flash programming reference manual

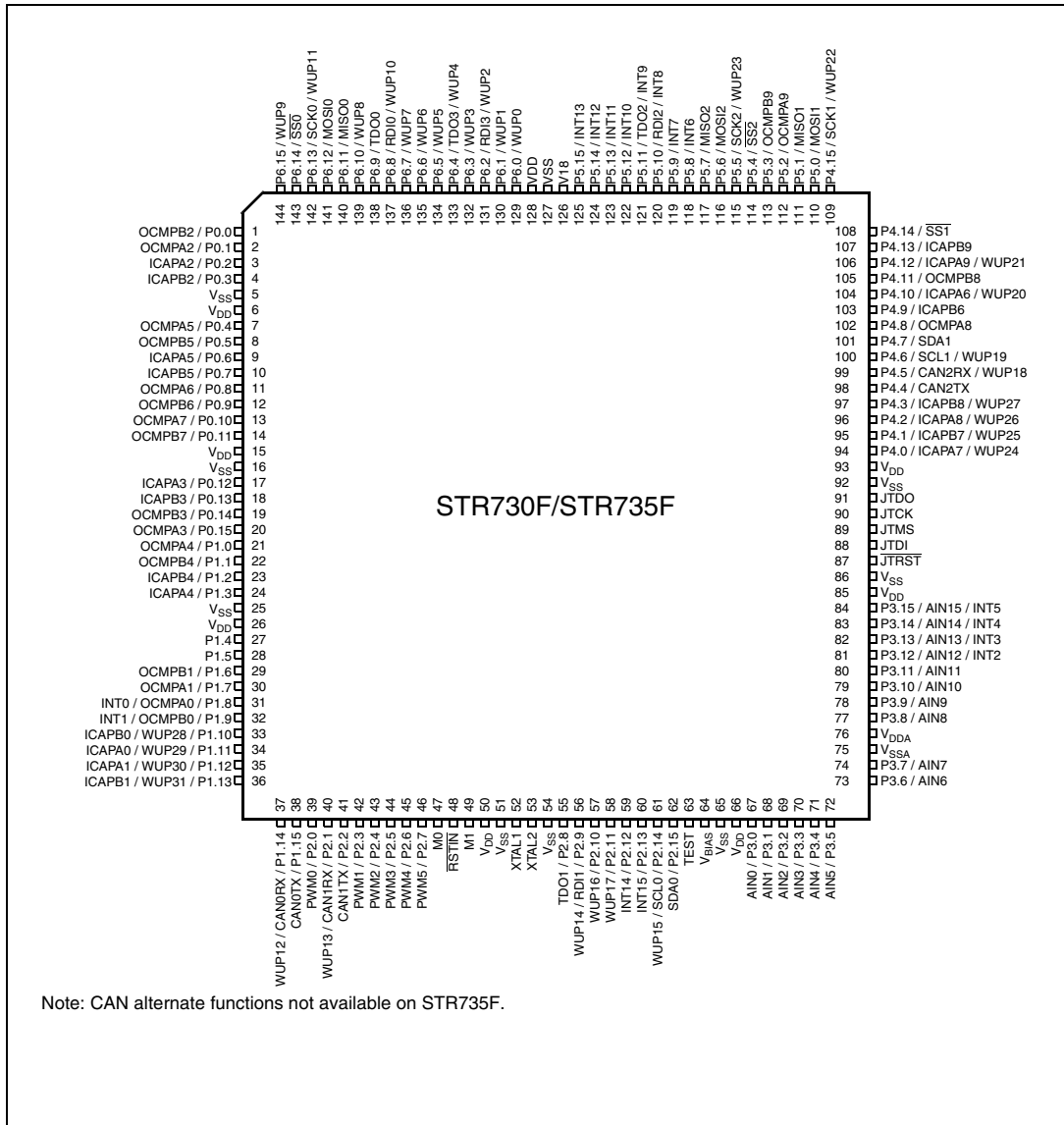
STR73x software library user manual

For a list of related application notes refer to <http://www.st.com>.

3.2 Pin description

3.2.1 STR730F/STR735F (TQFP144)

Figure 3. STR730F/STR735F pin configuration (top view)



3.2.2 STR730F/STR735F (LFBGA144)

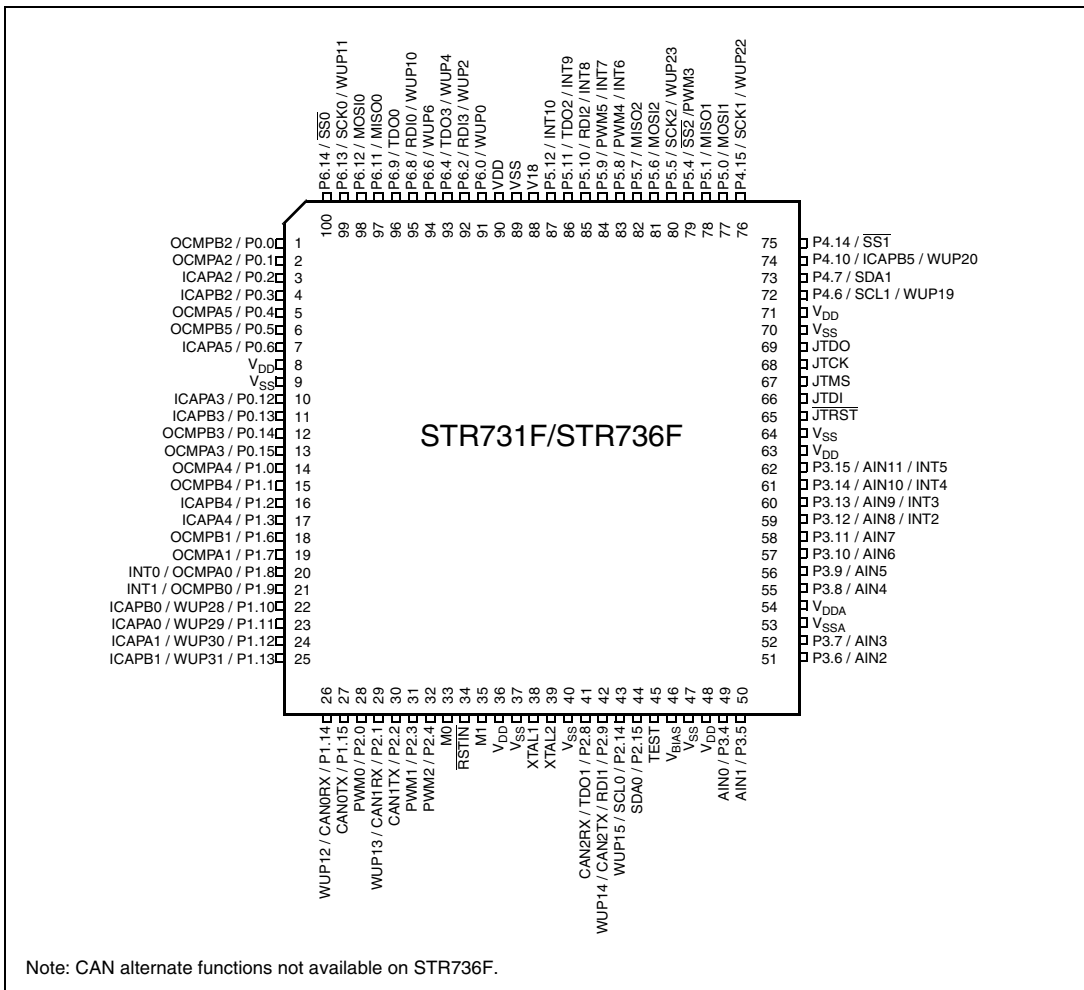
Table 3. STR730F/STR735F LFBGA ball connections

| Ball | Name | Ball | Name | Ball | Name | Ball | Name |
|------|-------------------------------------|------|-------------------------------------|------|------------------------------|------|--------------------------------------|
| A1 | P0.0 / OCMPB2 | B1 | P0.4 / OCMPA5 | C1 | P0.5 / OCMPB5 | D1 | V _{SS} |
| A2 | P6.10 / WUP8 | B2 | P0.1 / OCMPA2 | C2 | P0.2 / ICAPA2 | D2 | V _{DD} |
| A3 | P6.9 / TDO0 | B3 | P6.15 / WUP9 | C3 | P0.3 / ICAPB2 | D3 | P0.6 / ICAPA5 |
| A4 | P6.12 / MOSI0 | B4 | P6.13 / SCK0 / WUP11 | C4 | P6.14 / SSO | D4 | P0.7 / ICAPB5 |
| A5 | P6.6 / WUP6 | B5 | P6.7 / WUP7 | C5 | P6.8 / RDI0 / WUP10 | D5 | P6.11 / MISO0 |
| A6 | V ₁₈ | B6 | P6.2 / WUP2 / RDI3 | C6 | P6.3 / WUP3 | D6 | P6.4 / WUP4 / TDO3 |
| A7 | P5.15 / INT13 | B7 | P5.14 / INT12 | C7 | V _{SS} | D7 | V _{DD} |
| A8 | P5.8 / INT6 | B8 | P5.9 / INT7 | C8 | P5.10 / INT8 / RDI2 | D8 | P5.12 / INT10 |
| A9 | P5.2 / OCMPA9 | B9 | P5.3 / OCMPB9 | C9 | P5.4 / SS2 | D9 | P5.5 / SCK2 / WUP23 |
| A10 | P5.7 / MISO2 | B10 | P5.0 / MOSI1 | C10 | P5.1 / MISO1 | D10 | P4.13 / ICAPB9 |
| A11 | P5.6 / MOSI2 | B11 | P4.15 / SCK1 / WUP22 | C11 | P4.14 / SS1 | D11 | P4.12 / ICAPA9 / WUP21 |
| A12 | P5.11 / TDO2 / INT9 | B12 | P4.8 / OCMPA8 | C12 | P4.7 / SDA1 | D12 | P4.11 / OCMPB8 |
| E1 | P0.8 / OCMPA6 | F1 | V _{DD} | G1 | V _{SS} | H1 | V _{DD} |
| E2 | P0.9 / OCMPB6 | F2 | P0.13 / ICAPB3 | G2 | P1.2 / ICAPB4 | H2 | P1.8 / OCMPA0 / INT0 |
| E3 | P0.10 / OCMPA7 | F3 | P0.14 / OCMPB3 | G3 | P1.3 / ICAPA4 | H3 | P1.9 / OCMPB0 / INT1 |
| E4 | P0.11 / OCMPB7 | F4 | P0.15 / OCMPA3 | G4 | V _{SS} | H4 | P1.10 / ICAPB0 / WUP28 |
| E5 | P0.12 / ICAPA3 | F5 | P1.0 / OCMPA4 | G5 | P1.5 | H5 | XTAL2 |
| E6 | P6.5 / WUP5 | F6 | P1.1 / OCMPB4 | G6 | P2.11 / WUP17 | H6 | P2.10 / WUP16 |
| E7 | P6.0 / WUP0 | F7 | P6.1 / WUP1 | G7 | P4.0 / ICAPA7 / WUP24 | H7 | P2.15 / SDA 0 |
| E8 | P5.13 / INT11 | F8 | P4.4 / CAN2TX ¹⁾ | G8 | V _{DD} | H8 | JTMS |
| E9 | P4.10 / ICAPA6 / WUP20 | F9 | P4.3 / ICAPB8 / WUP27 | G9 | V _{SS} | H9 | V _{SS} |
| E10 | P4.9 / ICAPB6 | F10 | P4.2 / ICAPA8 / WUP26 | G10 | JTDO | H10 | V _{DD} |
| E11 | P4.6 / SCL1 / WUP19 | F11 | P4.1 / ICAPB7 / WUP25 | G11 | JTCK | H11 | P3.15 / AIN15 / INT5 |
| E12 | P4.5 / WUP18 / CAN2RX ¹⁾ | F12 | JTDI | G12 | nJTRST | H12 | P3.14 / AIN14 / INT4 |
| J1 | P1.4 | K1 | P1.6 / OCMPB1 | L1 | P1.7 / OCMPA1 | M1 | P1.14 / CAN0RX ¹⁾ / WUP12 |
| J2 | P1.11 / ICAPA0 / WUP29 | K2 | P1.13 / ICAPB1 / WUP31 | L2 | P1.15 / CAN0TX ¹⁾ | M2 | P2.4 / PWM2 |
| J3 | P1.12 / ICAPA1 / WUP30 | K3 | P2.1 / CAN1RX ¹⁾ / WUP13 | L3 | P2.0 / PWM0 | M3 | P2.5 / PWM3 |
| J4 | P2.7 / PWM5 | K4 | P2.6 / PWM4 | L4 | P2.3 / PWM1 | M4 | P2.2 / CAN1TX ¹⁾ |
| J5 | V _{DD} | K5 | M1 | L5 | RSTIN | M5 | M0 |
| J6 | P2.9 / RDI1 / WUP14 | K6 | P2.8 / TDO1 | L6 | V _{SS} | M6 | V _{SS} |
| J7 | P2.14 / SCL 0 / WUP15 | K7 | P2.13 / INT15 | L7 | P2.12 / INT14 | M7 | XTAL1 |
| J8 | P3.1 / AIN1 | K8 | P3.0 / AIN0 | L8 | VBIAS | M8 | TST |
| J9 | P3.13 / AIN13 / INT3 | K9 | P3.4 / AIN4 | L9 | P3.3 / AIN3 | M9 | P3.2 / AIN2 |
| J10 | P3.12 / AIN12 / INT2 | K10 | V _{DDA} | L10 | P3.5 / AIN5 | M10 | V _{SS} |
| J11 | P3.9 / AIN9 | K11 | V _{SSA} | L11 | P3.7 / AIN7 | M11 | V _{DD} |
| J12 | P3.8 / AIN8 | K12 | P3.11 / AIN11 | L12 | P3.10 / AIN10 | M12 | P3.6 / AIN6 |

Note: CAN alternate functions not available on STR735F.

3.2.3 STR731F/STR736F (TQFP100)

Figure 4. STR731F/STR736F pin configuration (top view)



Legend / Abbreviations for Table 4:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: T_T = TTL 0.8 V / 2 V with input trigger
 C_T = CMOS 0.3V_{DD}/0.7V_{DD} with input trigger

Port and control configuration:

Input: pu/pd = with internal 100 kΩ weak pull-up or pull down

Output: OD = open drain (logic level)
 PP = push-pull

Interrupts:

INTx = external interrupt line

WUPx = wake-up interrupt line

The reset state (during and just after the reset) of the I/O ports is input floating (Input tristate TTL mode). To avoid excess power consumption, unused I/O ports must be tied to ground.

Table 4. STR73xF pin description

| Pin n° | | | Pin name | Type | Input | | | Output | | | Main function (after reset) | Alternate function |
|---------|----------|---------|-----------------|------|-------------|-------|-----------|------------|----|----|-----------------------------|-------------------------------|
| TQFP144 | LFBGA144 | TQFP100 | | | Input Level | pu/pd | interrupt | Capability | OD | PP | | |
| 1 | A1 | 1 | P0.0/OCMPB2 | I/O | T_T | | | 2mA | X | X | Port 0.0 | TIM2: output compare B output |
| 2 | B2 | 2 | P0.1/OCMPA2 | I/O | T_T | | | 2mA | X | X | Port 0.1 | TIM2: output compare A output |
| 3 | C2 | 3 | P0.2/ICAPA2 | I/O | T_T | | | 2mA | X | X | Port 0.2 | TIM2: input capture A input |
| 4 | C3 | 4 | P0.3/ICAPB2 | I/O | T_T | | | 2mA | X | X | Port 0.3 | TIM2: input capture B input |
| 5 | D1 | | V _{SS} | S | | | | | | | Ground | |
| 6 | D2 | | V _{DD} | S | | | | | | | Supply voltage (5 V) | |
| 7 | B1 | 5 | P0.4/OCMPA5 | I/O | T_T | | | 2mA | X | X | Port 0.4 | TIM5: output compare A output |
| 8 | C1 | 6 | P0.5/OCMPB5 | I/O | T_T | | | 2mA | X | X | Port 0.5 | TIM5: output compare B output |
| 9 | D3 | 7 | P0.6/ICAPA5 | I/O | T_T | | | 2mA | X | X | Port 0.6 | TIM5: input capture A input |
| 10 | D4 | | P0.7/ICAPB5 | I/O | T_T | | | 2mA | X | X | Port 0.7 | TIM5: input capture B input |
| 11 | E1 | | P0.8/OCMPA6 | I/O | T_T | | | 2mA | X | X | Port 0.8 | TIM6: output compare A output |
| 12 | E2 | | P0.9/OCMPB6 | I/O | T_T | | | 2mA | X | X | Port 0.9 | TIM6: output compare B output |
| 13 | E3 | | P0.10/OCMPA7 | I/O | T_T | | | 2mA | X | X | Port 0.10 | TIM7: output compare A output |
| 14 | E4 | | P0.11/OCMPB7 | I/O | T_T | | | 2mA | X | X | Port 0.11 | TIM7: output compare B output |
| 15 | F1 | 8 | V _{DD} | S | | | | | | | Supply voltage (5 V) | |
| 16 | G1 | 9 | V _{SS} | S | | | | | | | Ground | |
| 17 | E5 | 10 | P0.12/ICAPA3 | I/O | T_T | | | 2mA | X | X | Port 0.12 | TIM3: input capture A input |
| 18 | F2 | 11 | P0.13/ICAPB3 | I/O | T_T | | | 2mA | X | X | Port 0.13 | TIM3: input capture B input |

Table 4. STR73xF pin description

| Pin n° | | | Pin name | Type | Input | | | Output | | | Main function (after reset) | Alternate function |
|---------|----------|---------|-----------------|------|----------------|-------|-----------|------------|----|----|------------------------------|-------------------------------|
| TQFP144 | LFBGA144 | TQFP100 | | | Input Level | pu/pd | interrupt | Capability | OD | PP | | |
| 19 | F3 | 12 | P0.14/OCMPB3 | I/O | T _T | | | 2mA | X | X | Port 0.14 | TIM3: output compare B output |
| 20 | F4 | 13 | P0.15/OCMPA3 | I/O | T _T | | | 2mA | X | X | Port 0.15 | TIM3: output compare A output |
| 21 | F5 | 14 | P1.0/OCMPA4 | I/O | T _T | | | 2mA | X | X | Port 1.0 | TIM4: output compare A output |
| 22 | F6 | 15 | P1.1/OCMPB4 | I/O | T _T | | | 2mA | X | X | Port 1.1 | TIM4: output compare B output |
| 23 | G2 | 16 | P1.2/ICAPB4 | I/O | T _T | | | 2mA | X | X | Port 1.2 | TIM4: input capture B input |
| 24 | G3 | 17 | P1.3/ICAPA4 | I/O | T _T | | | 2mA | X | X | Port 1.3 | TIM4: input capture A input |
| 25 | G4 | | V _{SS} | S | | | | | | | Ground | |
| 26 | H1 | | V _{DD} | S | | | | | | | Supply voltage (5 V) | |
| 27 | J1 | | P1.4 | I/O | T _T | | | 2mA | X | X | Port 1.4 | |
| 28 | G5 | | P1.5 | I/O | T _T | | | 2mA | X | X | Port 1.5 | |
| 29 | K1 | 18 | P1.6/OCMPB1 | I/O | T _T | | | 2mA | X | X | Port 1.6 | TIM1: output compare B output |
| 30 | L1 | 19 | P1.7/OCMPA1 | I/O | T _T | | | 2mA | X | X | Port 1.7 | TIM1: output compare A output |
| 31 | H2 | 20 | P1.8/OCMPA0 | I/O | T _T | | INT0 | 2mA | X | X | Port 1.8 | TIM0: output compare A output |
| 32 | H3 | 21 | P1.9/OCMPB0 | I/O | T _T | | INT1 | 2mA | X | X | Port 1.9 | TIM0: output compare B output |
| 33 | H4 | 22 | P1.10/ICAPB0 | I/O | T _T | | WUP28 | 2mA | X | X | Port 1.10 | TIM0: input capture B input |
| 34 | J2 | 23 | P1.11/ICAPA0 | I/O | T _T | | WUP29 | 2mA | X | X | Port 1.11 | TIM0: input capture A input |
| 35 | J3 | 24 | P1.12/ICAPA1 | I/O | T _T | | WUP30 | 2mA | X | X | Port 1.12 | TIM1: input capture A input |
| 36 | K2 | 25 | P1.13/ICAPB1 | I/O | T _T | | WUP31 | 2mA | X | X | Port 1.13 | TIM1: input capture B input |
| 37 | M1 | 26 | P1.14/CAN0RX | I/O | T _T | | WUP12 | 2mA | X | X | Port 1.14 | CAN0: receive data input |
| 38 | L2 | 27 | P1.15/CAN0TX | I/O | T _T | | | 2mA | X | X | Port 1.15 | CAN0: transmit data output |
| 39 | L3 | 28 | P2.0/PWM0 | I/O | T _T | | | 2mA | X | X | Port 2.0 | PWM0: PWM output |
| 40 | K3 | 29 | P2.1/CAN1RX | I/O | T _T | | WUP13 | 2mA | X | X | Port 2.1 | CAN1: receive data input |
| 41 | M4 | 30 | P2.2/CAN1TX | I/O | T _T | | | 2mA | X | X | Port 2.2 | CAN1: transmit data output |
| 42 | L4 | 31 | P2.3/PWM1 | I/O | T _T | | | 2mA | X | X | Port 2.3 | PWM1: PWM output |
| 43 | M2 | 32 | P2.4/PWM2 | I/O | T _T | | | 2mA | X | X | Port 2.4 | PWM2: PWM output |
| 44 | M3 | | P2.5/PWM3 | I/O | T _T | | | 2mA | X | X | Port 2.5 | PWM3: PWM output |
| 45 | K4 | | P2.6/PWM4 | I/O | T _T | | | 2mA | X | X | Port 2.6 | PWM4: PWM output |
| 46 | J4 | | P2.7/PWM5 | I/O | T _T | | | 2mA | X | X | Port 2.7 | PWM5: PWM output |
| 47 | M5 | 33 | M0 | I | T _T | pd | | | | | BOOT: mode selection 0 input | |
| 48 | L5 | 34 | RSTIN | I | C _T | pu | | | | | Reset input | |
| 49 | K5 | 35 | M1 | I | T _T | pd | | | | | BOOT: mode selection 1 input | |

Table 4. STR73xF pin description

| Pin n° | | | Pin name | Type | Input | | | Output | | | Main function (after reset) | Alternate function |
|---------|----------|---------|-------------------|------|----------------|-------|-----------|------------|----|----|--|--|
| TQFP144 | LFPGA144 | TQFP100 | | | Input Level | pu/pd | interrupt | Capability | OD | PP | | |
| 50 | J5 | 36 | V _{DD} | S | | | | | | | Supply voltage (5 V) | |
| 51 | M6 | 37 | V _{SS} | S | | | | | | | Ground | |
| 52 | M7 | 38 | XTAL1 | I | | | | | | | Oscillator amplifier circuit input and internal clock generator input. | |
| 53 | H5 | 39 | XTAL2 | O | | | | | | | Oscillator amplifier circuit output. | |
| 54 | L6 | 40 | V _{SS} | S | | | | | | | Ground | |
| 55 | K6 | 41 | P2.8/TDO1/CAN2RX | I/O | T _T | | | 2mA | X | X | Port 2.8 | UART1: transmit data output CAN2: receive data input (TQFP100 only) |
| 56 | J6 | 42 | P2.9/RDI1/CAN2TX | I/O | T _T | | WUP14 | 2mA | X | X | Port 2.9 | UART1: receive data input CAN2: transmit data output (TQFP100 only) |
| 57 | H6 | | P2.10 | I/O | T _T | | WUP16 | 2mA | X | X | Port 2.10 | |
| 58 | G6 | | P2.11 | I/O | T _T | | WUP17 | 2mA | X | X | Port 2.11 | |
| 59 | L7 | | P2.12 | I/O | T _T | | INT14 | 2mA | X | X | Port 2.12 | |
| 60 | K7 | | P2.13 | I/O | T _T | | INT15 | 2mA | X | X | Port 2.13 | |
| 61 | J7 | 43 | P2.14/SCL0 | I/O | T _T | | WUP15 | 2mA | X | X | Port 2.14 | I2C0: serial clock |
| 62 | H7 | 44 | P2.15/SDA0 | I/O | T _T | | | 2mA | X | X | Port 2.15 | I2C0: serial data |
| 63 | M8 | 45 | Test | I | | pd | | | | | Reserved pin. Must be tied to ground | |
| 64 | L8 | 46 | V _{BIAS} | S | | | | | | | Internal RC oscillator bias. A 1.3 MΩ external resistor has to be connected to this pin when a 32 kHz RC oscillator frequency is used. | |
| 65 | M10 | 47 | V _{SS} | S | | | | | | | Ground | |
| 66 | M11 | 48 | V _{DD} | S | | | | | | | Supply voltage (5 V) | |
| 67 | K8 | | P3.0/AIN0 | I/O | T _T | | | 2mA | X | X | Port 3.0 | ADC: analog input 0 |
| 68 | J8 | | P3.1/AIN1 | I/O | T _T | | | 2mA | X | X | Port 3.1 | ADC: analog input 1 |
| 69 | M9 | | P3.2/AIN2 | I/O | T _T | | | 2mA | X | X | Port 3.2 | ADC: analog input 2 |
| 70 | L9 | | P3.3/AIN3 | I/O | T _T | | | 2mA | X | X | Port 3.3 | ADC: analog input 3 |
| 71 | K9 | 49 | P3.4/AIN4 | I/O | T _T | | | 2mA | X | X | Port 3.4 | ADC: analog input 4 (AIN0 in TQFP100) |
| 72 | L10 | 50 | P3.5/AIN5 | I/O | T _T | | | 2mA | X | X | Port 3.5 | ADC: Analog input 5 (AIN1 in TQFP100) |

Table 4. STR73xF pin description

| Pin n° | | | Pin name | Type | Input | | | Output | | | Main function (after reset) | Alternate function |
|---------|----------|---------|------------------|------|----------------|-------|-----------|------------|----|----|-------------------------------------|---|
| TQFP144 | LFPGA144 | TQFP100 | | | Input Level | pu/pd | interrupt | Capability | OD | PP | | |
| 73 | M12 | 51 | P3.6/AIN6 | I/O | T _T | | | 2mA | X | X | Port 3.6 | ADC: analog input 6 (AIN2 in TQFP100) |
| 74 | L11 | 52 | P3.7/AIN7 | I/O | T _T | | | 2mA | X | X | Port 3.7 | ADC: analog input 7 (AIN3 in TQFP100) |
| 75 | K11 | 53 | V _{SSA} | S | | | | | | | Reference ground for A/D converter | |
| 76 | K10 | 54 | V _{DDA} | S | | | | | | | Reference voltage for A/D converter | |
| 77 | J12 | 55 | P3.8/AIN8 | I/O | T _T | | | 2mA | X | X | Port 3.8 | ADC: analog input 8 (AIN4 in TQFP100) |
| 78 | J11 | 56 | P3.9/AIN9 | I/O | T _T | | | 2mA | X | X | Port 3.9 | ADC: analog input 9 (AIN5 in TQFP100) |
| 79 | L12 | 57 | P3.10/AIN10 | I/O | T _T | | | 2mA | X | X | Port 3.10 | ADC: analog input 10 (AIN6 in TQFP100) |
| 80 | K12 | 58 | P3.11/AIN11 | I/O | T _T | | | 2mA | X | X | Port 3.11 | ADC: analog input 11 (AIN7 in TQFP100) |
| 81 | J10 | 59 | P3.12/AIN12 | I/O | T _T | | INT2 | 2mA | X | X | Port 3.12 | ADC: analog input 12 (AIN8 in TQFP100) |
| 82 | J9 | 60 | P3.13/AIN13 | I/O | T _T | | INT3 | 2mA | X | X | Port 3.13 | ADC: analog input 13 (AIN9 in TQFP100) |
| 83 | H12 | 61 | P3.14/AIN14 | I/O | T _T | | INT4 | 2mA | X | X | Port 3.14 | ADC: analog input 14 (AIN10 in TQFP100) |
| 84 | H11 | 62 | P3.15/AIN15 | I/O | T _T | | INT5 | 2mA | X | X | Port 3.15 | ADC: analog input 15 (AIN11 in TQFP100) |
| 85 | H10 | 63 | V _{DD} | S | | | | | | | Supply voltage (5 V) | |
| 86 | H9 | 64 | V _{SS} | S | | | | | | | Ground | |
| 87 | G12 | 65 | JTRST | I | T _T | pu | | | | | | JTAG reset Input |
| 88 | F12 | 66 | JTDI | I | T _T | pu | | | | | | JTAG data input |
| 89 | H8 | 67 | JTMS | I | T _T | pu | | | | | | JTAG mode selection Input |
| 90 | G11 | 68 | JTCK | I | T _T | pd | | | | | | JTAG clock Input |
| 91 | G10 | 69 | JTDO | O | | | | 4mA | | | | JTAG data output. Note: Reset state = HiZ |
| 92 | G9 | 70 | V _{SS} | S | | | | | | | Ground | |
| 93 | G8 | 71 | V _{DD} | S | | | | | | | Supply voltage (5 V) | |
| 94 | G7 | | P4.0/ICAPA7 | I/O | T _T | | WUP24 | 2mA | X | X | Port 4.0 | TIM7: input capture A input |
| 95 | F11 | | P4.1/ICAPB7 | I/O | T _T | | WUP25 | 2mA | X | X | Port 4.1 | TIM7: input capture B input |
| 96 | F10 | | P4.2/ICAPA8 | I/O | T _T | | WUP26 | 2mA | X | X | Port 4.2 | TIM8: input capture A input |

Table 4. STR73xF pin description

| Pin n° | | | Pin name | Type | Input | | | Output | | | Main function (after reset) | Alternate function |
|---------|----------|---------|------------------------------|------|----------------|-------|-----------|------------|----|----|-----------------------------|--|
| TQFP144 | LFPGA144 | TQFP100 | | | Input Level | pu/pd | interrupt | Capability | OD | PP | | |
| 97 | F9 | | P4.3/ICAPB8 | I/O | T _T | | WUP27 | 2mA | X | X | Port 4.3 | TIM8: input capture B input |
| 98 | F8 | | P4.4/CAN2TX | I/O | T _T | | | 2mA | X | X | Port 4.4 | CAN2: transmit data output |
| 99 | E12 | | P4.5/CAN2RX | I/O | T _T | | WUP18 | 2mA | X | X | Port 4.5 | CAN2: receive data input |
| 100 | E11 | 72 | P4.6/SCL1 | I/O | T _T | | WUP19 | 2mA | X | X | Port 4.6 | I2C1: serial clock |
| 101 | C12 | 73 | P4.7/SDA1 | I/O | T _T | | | 2mA | X | X | Port 4.7 | I2C1: serial data |
| 102 | B12 | | P4.8/OCMPA8 | I/O | T _T | | | 2mA | X | X | Port 4.8 | TIM8: output compare A output |
| 103 | E10 | | P4.9/ICAPB6 | I/O | T _T | | | 2mA | X | X | Port 4.9 | TIM6: input capture B input |
| 104 | E9 | 74 | P4.10/ICAPA6/ CAPB5 | I/O | T _T | | WUP20 | 2mA | X | X | Port 4.10 | TIM6: input capture A input (144-pin pkg only) TIM5: input capture B input (TQFP100 only) |
| 105 | D12 | | P4.11/OCMPB8 | I/O | T _T | | | 2mA | X | X | Port 4.11 | TIM8: output compare B output |
| 106 | D11 | | P4.12/ICAPA9 | I/O | T _T | | WUP21 | 2mA | X | X | Port 4.12 | TIM9: input capture A input |
| 107 | D10 | | P4.13/ICAPB9 | I/O | T _T | | | 2mA | X | X | Port 4.13 | TIM9: input capture B input |
| 108 | C11 | 75 | P4.14/ \overline{SS} 1 | I/O | T _T | | | 2mA | X | X | Port 4.14 | BSPI1: slave select |
| 109 | B11 | 76 | P4.15/SCK1 | I/O | T _T | | WUP22 | 2mA | X | X | Port 4.15 | BSPI1: serial clock |
| 110 | B10 | 77 | P5.0/MOSI1 | I/O | T _T | | | 2mA | X | X | Port 5.0 | BSPI1: master output/slave input |
| 111 | C10 | 78 | P5.1/MISO1 | I/O | T _T | | | 2mA | X | X | Port 5.1 | BSPI1: master input/Slave output |
| 112 | A9 | | P5.2/OCMPA9 | I/O | T _T | | | 2mA | X | X | Port 5.2 | TIM9: output compare A output |
| 113 | B9 | | P5.3/OCMPB9 | I/O | T _T | | | 2mA | X | X | Port 5.3 | TIM9: output compare B output |
| 114 | C9 | 79 | P5.4/ \overline{SS} 2/PWM3 | I/O | T _T | | | 2mA | X | X | Port 5.4 | BSPI2: slave select PWM3: PWM output (TQFP100 only) |
| 115 | D9 | 80 | P5.5/SCK2 | I/O | T _T | | WUP23 | 2mA | X | X | Port 5.5 | BSPI2: serial clock |
| 116 | A11 | 81 | P5.6/MOSI2 | I/O | T _T | | | 2mA | X | X | Port 5.6 | BSPI2: master output/slave input |
| 117 | A10 | 82 | P5.7/MISO2 | I/O | T _T | | | 2mA | X | X | Port 5.7 | BSPI2: master input/slave output |
| 118 | A8 | 83 | P5.8/PWM4 | I/O | T _T | | INT6 | 2mA | X | X | Port 5.8 | PWM4: PWM output (TQFP100 only) |

Table 4. STR73xF pin description

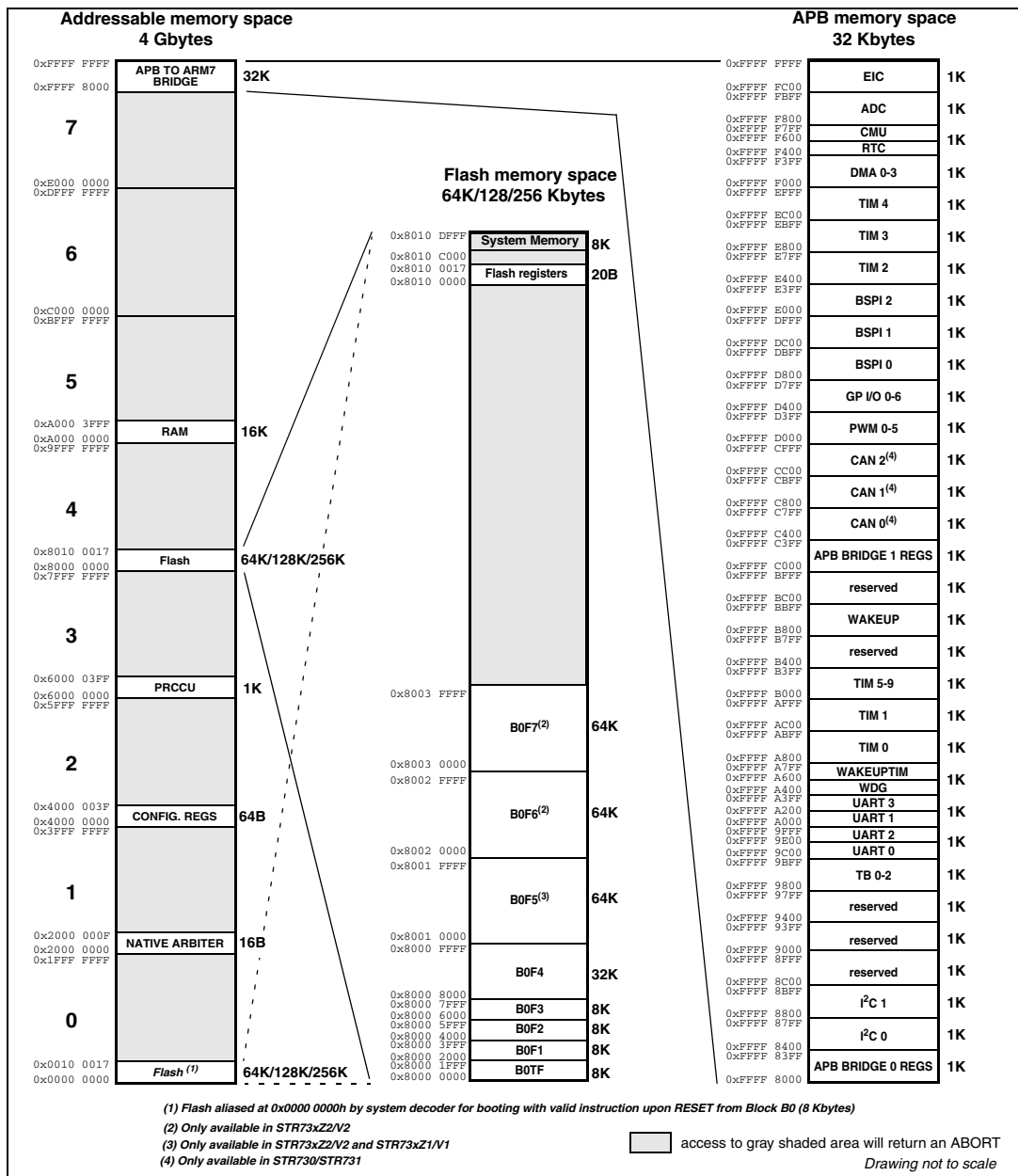
| Pin n° | | | Pin name | Type | Input | | | Output | | | Main function (after reset) | Alternate function |
|---------|----------|---------|--------------------------|------|----------------|-------|-----------|------------|----|----|-----------------------------|--|
| TQFP144 | LFBGA144 | TQFP100 | | | Input Level | pu/pd | interrupt | Capability | OD | PP | | |
| 119 | B8 | 84 | P5.9/PWM5 | I/O | T _T | | INT7 | 2mA | X | X | Port 5.9 | PWM5: PWM output (TQFP100 only) |
| 120 | C8 | 85 | P5.10/RDI2 | I/O | T _T | | INT8 | 2mA | X | X | Port 5.10 | UART2: receive data input |
| 121 | A12 | 86 | P5.11/TDO2 | I/O | T _T | | INT9 | 2mA | X | X | Port 5.11 | UART2: transmit data output |
| 122 | D8 | 87 | P5.12 | I/O | T _T | | INT10 | 2mA | X | X | Port 5.12 | |
| 123 | E8 | | P5.13 | I/O | T _T | | INT11 | 2mA | X | X | Port 5.13 | |
| 124 | B7 | | P5.14 | I/O | T _T | | INT12 | 2mA | X | X | Port 5.14 | |
| 125 | A7 | | P5.15 | I/O | T _T | | INT13 | 2mA | X | X | Port 5.15 | |
| 126 | A6 | 88 | V ₁₈ | S | | | | | | | | 1.8 V decoupling pin: a decoupling capacitor (recommended value: 100 nF) must be connected between this pin and nearest V _{SS} pin. |
| 127 | C7 | 89 | V _{SS} | S | | | | | | | | Ground |
| 128 | D7 | 90 | V _{DD} | S | | | | | | | | Supply voltage (5 V) |
| 129 | E7 | 91 | P6.0 | I/O | T _T | | WUP0 | 8mA | X | X | Port 6.0 | |
| 130 | F7 | | P6.1 | I/O | T _T | | WUP1 | 2mA | X | X | Port 6.1 | |
| 131 | B6 | 92 | P6.2/RDI3 | I/O | T _T | | WUP2 | 2mA | X | X | Port 6.2 | UART3: receive data input |
| 132 | C6 | | P6.3 | I/O | T _T | | WUP3 | 2mA | X | X | Port 6.3 | |
| 133 | D6 | 93 | P6.4/TDO3 | I/O | T _T | | WUP4 | 2mA | X | X | Port 6.4 | UART3: transmit data output |
| 134 | E6 | | P6.5 | I/O | T _T | | WUP5 | 2mA | X | X | Port 6.5 | |
| 135 | A5 | 94 | P6.6 | I/O | T _T | | WUP6 | 2mA | X | X | Port 6.6 | |
| 136 | B5 | | P6.7 | I/O | T _T | | WUP7 | 2mA | X | X | Port 6.7 | |
| 137 | C5 | 95 | P6.8/RDI0 | I/O | T _T | | WUP10 | 2mA | X | X | Port 6.8 | UART0: receive data input |
| 138 | A3 | 96 | P6.9/TDO0 | I/O | T _T | | | 2mA | X | X | Port 6.9 | UART0: transmit data output |
| 139 | A2 | | P6.10 | I/O | T _T | | WUP8 | 2mA | X | X | Port 6.10 | |
| 140 | D5 | 97 | P6.11/MISO0 | I/O | T _T | | | 2mA | X | X | Port 6.11 | BSPI0: master input/slave output |
| 141 | A4 | 98 | P6.12/MOSI0 | I/O | T _T | | | 2mA | X | X | Port 6.12 | BSPI0: master output/slave input |
| 142 | B4 | 99 | P6.13/SCK0 | I/O | T _T | | WUP11 | 2mA | X | X | Port 6.13 | BSPI0: serial clock |
| 143 | C4 | 100 | P6.14/ \overline{SS} 0 | I/O | T _T | | | 2mA | X | X | Port 6.14 | BSPI0: slave select |
| 144 | B3 | | P6.15 | I/O | T _T | | WUP9 | 2mA | X | X | Port 6.15 | |

3.3 Memory mapping

Figure 5 shows the various memory configurations of the STR73xF system. The system memory map (from 0x0000_0000 to 0xFFFF_FFFF) is shown on the left part of the figure, the right part shows maps of the Flash and APB areas. For flexibility the Flash or RAM addresses can be aliased to Block 0 addresses using the remapping feature

Most reserved memory spaces (gray shaded areas in Figure 5) are protected from access by the user code. When an access this memory space is attempted, an ABORT signal is generated. Depending on the type of access, the ARM processor will enter “prefetch abort” state (Exception vector 0x0000_000C) or “data abort” state (Exception vector 0x0000_0010). It is up to the application software to manage these abort exceptions.

Figure 5. Memory map



4 Electrical parameters

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS} .

4.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A=25^\circ\text{C}$ and $T_A=T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean}\pm 3\Sigma$).

4.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A=25^\circ\text{C}$ and $V_{DD}=5\text{V}$. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ($\text{mean}\pm 2\Sigma$).

4.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 6](#).

4.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 7](#).

Figure 6. Pin loading conditions

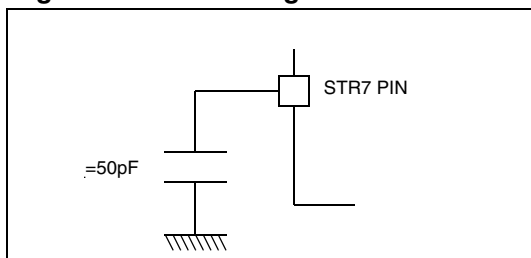
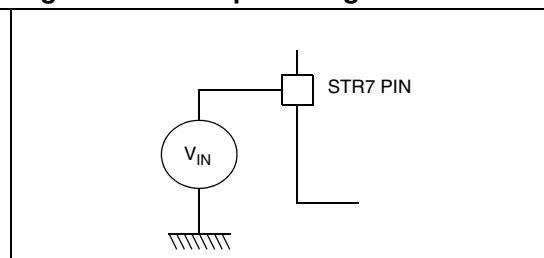


Figure 7. Pin input voltage



4.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

| Symbol | Ratings | Min | Max | Unit |
|----------------------|--|---|--------------|------|
| $V_{DD} - V_{SS}$ | External 5 V Supply voltage | -0.3 | 6.0 | v |
| V_{SSA} | Reference ground for A/D converter | V_{SS} | V_{SS} | v |
| $V_{DDA} - V_{SSA}$ | Reference voltage for A/D converter | -0.3 | $V_{DD}+0.3$ | V |
| V_{IN} | Input voltage on any pin | -0.3 | $V_{DD}+0.3$ | |
| $ ΔV_{DDx} $ | Variations between different 5 V power pins | - | 0.3 | mV |
| $ V_{SSx} - V_{SS} $ | Variations between all the different ground pins | - | 0.3 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (Human Body Model) | see : <i>Absolute maximum ratings (electrical sensitivity) on page 36</i> | | |
| $V_{ESD(MM)}$ | Electrostatic discharge voltage (Machine Model) | | | |

Table 6. Current characteristics

| Symbol | Ratings | Max. | Unit |
|---------------------------|--|-------|------|
| I_{VDD} | Total current into V_{DD} power lines (source) ¹⁾ | 100 | mA |
| I_{VSS} | Total current out of V_{SS} ground lines (sink) ¹⁾ | 100 | |
| I_{IO} | Output current sunk by any I/O and control pin | 10 | |
| | Output current source by any I/O and control pin | 10 | |
| $I_{INJ(PIN)}^{2) \& 3)}$ | Injected current on any other pin ^{4) & 5)} | $±10$ | |
| $ΣI_{INJ(PIN)}^{2)}$ | Total injected current (sum of all I/O and control pins) ⁴⁾ | $±75$ | |

- All 5 V power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external 5 V supply
- $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
- Negative injection disturbs the analog performance of the device. See note in [Section 4.3.6: 10-bit ADC characteristics on page 43](#).
- When several inputs are submitted to a current injection, the maximum $ΣI_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $ΣI_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.
- In 144-pin devices, only +10 mA on P0.3, P1.13, P3.6 and P4.13 pins (negative injection not allowed).

Table 7. Thermal characteristics

| Symbol | Ratings | Value | Unit |
|-----------|---|-------------|------|
| T_{STG} | Storage temperature range | -55 to +150 | °C |
| T_J | Maximum junction temperature (see Section 5.2: Thermal characteristics on page 48) | | |

4.3 Operating conditions

Subject to general operating conditions for V_{DD} , and T_A .

Table 8. General operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------|---|---|------------|--------------|------|
| f_{MCLK} | Internal CPU and system clock frequency | Accessing SRAM or Flash (zero wait state Flash access up to 36 MHz) | 0 | 36 | MHz |
| V_{DD} | Standard Operating Voltage | | 4.5 | 5.5 | V |
| V_{DDA} | Operating analog reference voltage with respect to ground | | 4.5 | $V_{DD}+0.1$ | V |
| T_A | Ambient temperature range | 6 partnumber suffix 7 partnumber suffix | -40 -40 | 85 105 | °C |

Table 9. Operating conditions at power-up / power-down

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|-------------------------|---|-----|-----|-----|------|
| t_{VDD} | V_{DD} rise time rate | Subject to general operating conditions for T_A . | - | 20 | - | ms/V |

4.3.1 Supply current characteristics

The current consumption is measured as described in [Figure 6](#) and [Figure 7](#).

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

Subject to general operating conditions for V_{DD} , and T_A .

Table 10. Total current consumption

| Symbol | Parameter | Conditions | Typ ¹⁾ | Max ²⁾ | Unit |
|--|------------------------------|---|--------------------|-------------------|---------|
| I_{DD} | RUN mode ³⁾ | Formula, f_{MCLK} in MHz, RAM execution | $7 + 1.9 f_{MCLK}$ | | mA |
| | | $f_{MCLK} = 36$ MHz, RAM execution | 76 | | mA |
| | | $f_{MCLK} = 36$ MHz, Flash execution | 86 | | mA |
| | WFI mode | $f_{OSC} = 4$ MHz, $f_{MCLK} = f_{OSC}/16 = 250$ kHz Main voltage regulator ON, LP voltage regulator = 2 mA, RTC and WDG on, other modules off. | 6.7 | 8 | mA |
| | LPWFI mode | $f_{RC} =$ high frequency (CMU_RCCTL= 0x8), $f_{MCLK} = f_{RC}/16$, LP voltage regulator = 2 mA, other modules off. | 220 | 350 | μ A |
| | STOP mode | $f_{OSC} = 4$ MHz, RC oscillator on $f_{RC} =$ high frequency (CMU_RCCTL= 0x0) LP voltage regulator = 6 mA, RTC and WUT ON, other modules off. Internal wake-up possible. | 500 | 700 | μ A |
| | | $f_{RC} =$ high frequency (CMU_RCCTL= 0xF), LP voltage regulator = 2mA. WUT ON, other modules off. Internal wake-up possible. | 150 | 220 | |
| LP voltage regulator = 2 mA, WIU on, Other modules off, external wake-up. | | 50 | 140 | | |
| HALT mode | LP voltage regulator = 2 mA. | 50 | 140 | μ A | |

1. Typical data are based on $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$

2. Data based on characterization results, tested in production at V_{DD} max. and $T_A = 25^\circ\text{C}$.

3. I/O in static configuration (not toggling). RUN mode is almost **independent of temperature**. On the contrary RUN mode current is **highly dependent on the application**. The $I_{DD,RUN}$ value can be significantly reduced by the application in the following ways: switch-off unused peripherals (default), reduce peripheral frequency through internal prescaler, fetch the most frequently-used functions from RAM and use low power mode when possible.

Figure 8. STOP I_{DD} vs. V_{DD}

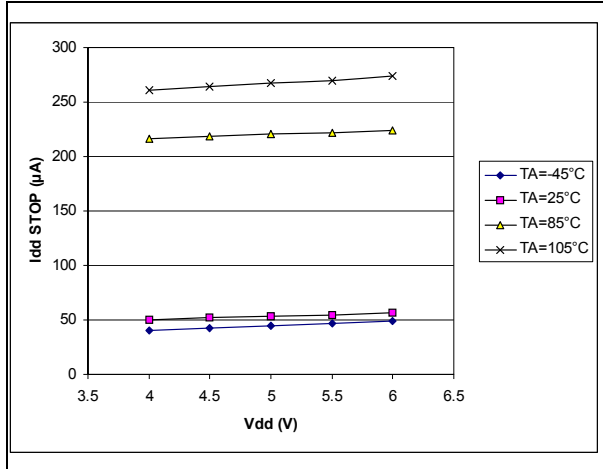


Figure 9. HALT I_{DD} vs. V_{DD}

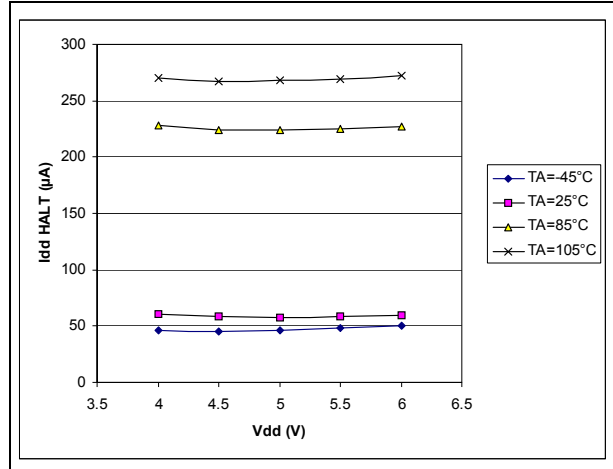


Figure 10. WFI I_{DD} vs. V_{DD}

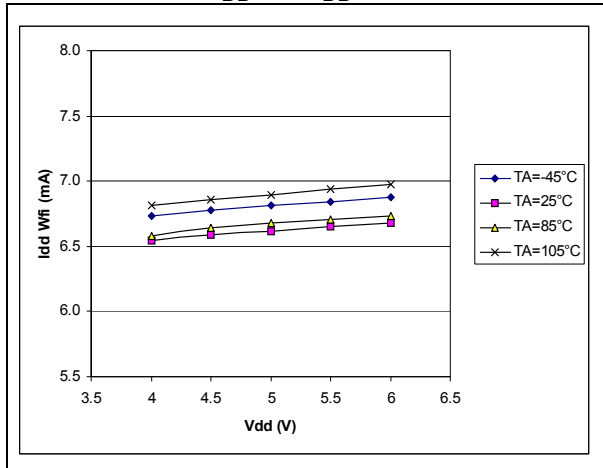
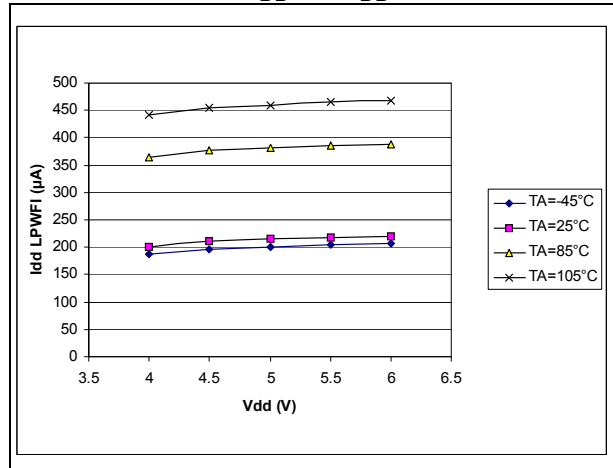


Figure 11. LPWFI I_{DD} vs. V_{DD}



Typical application current consumption

Table 11. Typical consumption in Run mode at 25°C and 85°C

| Conditions | | f _{MCLK} (MHz) | f _{ADC} (MHz) | Typical I _{DD} (mA) |
|---|-------------------------|-------------------------|------------------------|------------------------------|
| V _{DD} = 5.5 V, RC oscillator off, PLL on, RTC enabled, 1 Timer (TIM) running, and ADC running in scan mode. | Code executing in RAM | 10 | 10 | 20 |
| | | 20 | | 29 |
| | | 36 | 9 | 42 |
| | Code executing in Flash | 10 | 10 | 22 |
| | | 20 | | 32 |
| | | 36 | 9 | 48 |

Table 12. Typical consumption in Run and low power modes at 25°C

| Mode | Conditions | f _{MCLK} | Typical I _{DD} |
|-------|---|-------------------|-------------------------|
| RUN | All peripherals on, RAM execution | 36 MHz | 76 mA |
| | | 24 MHz | 56 mA |
| WFI | Main voltage regulator on, Flash on, EIC on, WIU on, GPIOs on. | 36 MHz | 33 mA |
| | | 24 MHz | 31 mA |
| SLOW | PLL off, main voltage regulator on | 4 MHz | 11 mA |
| | CLOCK2/16, main voltage regulator on | 250 kHz | 8 mA |
| | CLOCK2/16, main voltage regulator off | 250 kHz | 3 mA |
| | RC oscillator running in low frequency, main crystal oscillator off, main voltage regulator off | 29 kHz | 2.5 mA |
| LPWFI | CLOCK2/16, main voltage regulator off, LP voltage regulator = 2 mA, Flash in power down mode. | 250 kHz | 528 µA |
| STOP | Main voltage regulator off, RTC on, RC oscillator off, LP voltage regulator = 6 mA | - | 378 µA |
| | Main voltage regulator off, RTC off, RC oscillator off, LP voltage regulator = 6 mA | - | 83 µA |
| | Main voltage regulator off, RTC off, RC oscillator off, LP voltage regulator = 4 mA | - | 64 µA |
| | Main voltage regulator off, RTC off, RC oscillator off, LP voltage regulator = 2 mA | - | 44 µA |
| HALT | RTC off, LP voltage regulator = 2 mA | - | 44 µA |

On-chip peripherals

Table 13. Peripheral current consumption at T_A= 25°C

| Symbol | Parameter | Conditions | Typ | Unit |
|-----------------------|--|---------------------------|------|------|
| I _{DD(RC)} | RC (backup oscillator) supply current | High frequency | 120 | μA |
| | | Low frequency | 60 | μA |
| I _{DD(TIM)} | TIM timer supply current ¹⁾ | f _{MCLK} =36 MHz | 350 | μA |
| I _{DD(BSPI)} | BSPI supply current ¹⁾ | | 1.1 | mA |
| I _{DD(UART)} | UART supply current ¹⁾ | | 850 | μA |
| I _{DD(I2C)} | I2C supply current ¹⁾ | | 430 | μA |
| I _{DD(ADC)} | ADC supply current when converting ²⁾ | | 5 | mA |
| I _{DD(EIC)} | EIC supply current | | 2.88 | mA |
| I _{DD(CAN)} | CAN supply current ¹⁾ | | 2.95 | mA |
| I _{DD(GPIO)} | GPIO supply current | | 150 | μA |
| I _{DD(TB)} | TB supply current | | 250 | μA |
| I _{DD(PWM)} | PWM supply current | | 240 | μA |
| I _{DD(RTC)} | RTC supply current | | 370 | μA |
| I _{DD(DMA)} | DMA supply current | | 2.5 | mA |
| I _{DD(ARB)} | Native arbiter supply current | | 180 | μA |
| I _{DD(AHB)} | AHB arbiter supply current | | 570 | μA |
| I _{DD(WUT)} | WUT supply current | | 300 | μA |
| I _{DD(WIU)} | WIU supply current | | 460 | μA |

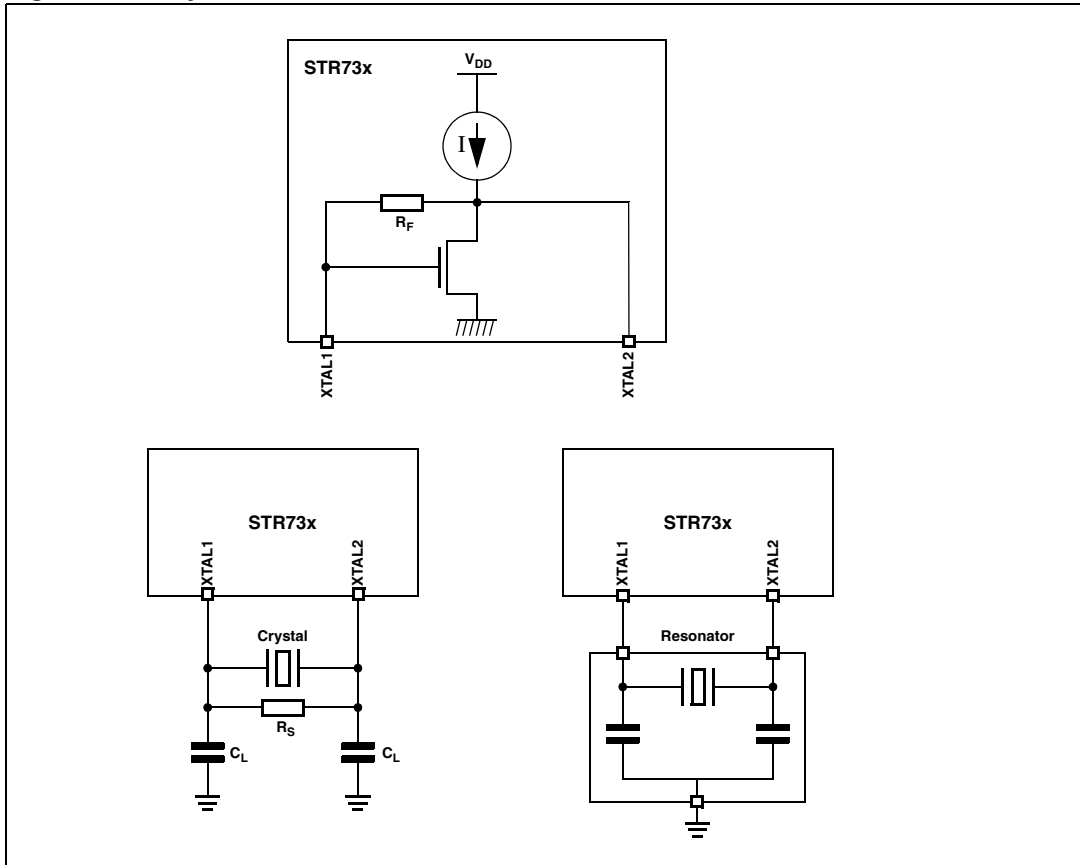
1. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset, not clocked and the on-chip peripheral when clocked and not kept under reset. This measurement does not include the pad toggling consumption.
2. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

4.3.2 Clock and timing characteristics

Crystal / ceramic resonator oscillator

The STR73xF can operate with a crystal oscillator or resonator clock source. [Figure 12](#) describes a simple model of the internal oscillator driver as well as example of connection for an oscillator or a resonator.

Figure 12. Crystal oscillator and resonator



- Note:
- 1 XTAL2 must not be used to directly drive external circuits.
 - 2 For test or boot purpose, XTAL2 can be used as a high impedance input pin to provide an external clock to the device. XTAL1 should be grounded, and XTAL2 connected to a wave signal generator providing a 0 to VDD signal. Directly driving XTAL2 may results in deteriorated jitter and duty cycle.

Main oscillator characteristics

$V_{DD} = 5\text{ V} \pm 10\%$, $T_A = -40^\circ\text{ C}$ to T_{Amax} , unless otherwise specified.

Table 14. Main oscillator characteristics

| Symbol | Parameter | Conditions | Value | | | Unit |
|-----------------|-----------------------------|---|-------|------|-----|------|
| | | | Min | Typ | Max | |
| f_{OSC} | Oscillator frequency | | 4 | | 8 | MHz |
| g_m | Oscillator transconductance | | 1.5 | | 4.2 | mA/V |
| $V_{OSC}^{1)}$ | Oscillation amplitude | $f_{OSC} = 4\text{ MHz}$, $T_A = 25^\circ\text{ C}$ | - | 2.4 | - | V |
| | | $f_{OSC} = 8\text{ MHz}$, $T_A = 25^\circ\text{ C}$ | | 1.- | | |
| $V_{AV}^{1)}$ | Oscillator operating point | Sine wave middle, $T_A = 25^\circ\text{ C}$ | - | 0.77 | - | v |
| $t_{STUP}^{1)}$ | Oscillator start-up time | External crystal, $V_{DD} = 5.5\text{ V}$, $f_{OSC} = 4\text{ MHz}$, $T_A = -40^\circ\text{ C}$ | - | - | 12 | ms |
| | | External crystal, $V_{DD} = 5.0\text{ V}$, $f_{OSC} = 4\text{ MHz}$, $T_A = 25^\circ\text{ C}$ | - | 5.5 | - | ms |
| | | External crystal, $V_{DD} = 5.5\text{ V}$, $f_{OSC} = 6\text{ MHz}$, $T_A = -40^\circ\text{ C}$ | - | - | 8 | ms |
| | | External crystal, $V_{DD} = 5.0\text{ V}$, $f_{OSC} = 6\text{ MHz}$, $T_A = 25^\circ\text{ C}$ | - | 3.3 | - | ms |
| | | External crystal, $V_{DD} = 5.5\text{ V}$, $f_{OSC} = 8\text{ MHz}$, $T_A = -40^\circ\text{ C}$ | - | - | 7 | ms |
| | | External crystal, $V_{DD} = 5.0\text{ V}$, $f_{OSC} = 8\text{ MHz}$, $T_A = 25^\circ\text{ C}$ | - | 2.7 | - | ms |

Table 14. Main oscillator characteristics (continued)

| Symbol | Parameter | Conditions | Value | | | Unit | |
|------------------------------|-------------------|--|---|-----|------|------|---|
| | | | Min | Typ | Max | | |
| R _F ¹⁾ | Feedback resistor | f _{OSC} = 4 MHz C _p ²⁾ = 10 pF | C ₁ ³⁾ = C ₂ ⁴⁾ = 10 pF | 150 | 555 | - | Ω |
| | | | C ₁ = C ₂ = 20 pF | 490 | 1035 | - | |
| | | | C ₁ = C ₂ = 30 pF | 490 | 1030 | - | |
| | | | C ₁ = C ₂ = 40 pF | 380 | 850 | - | |
| | | f _{OSC} = 5 MHz C _p = 10 pF | C ₁ = C ₂ = 10 pF | 160 | 470 | - | |
| | | | C ₁ = C ₂ = 20 pF | 415 | 800 | - | |
| | | | C ₁ = C ₂ = 30 pF | 340 | 735 | - | |
| | | | C ₁ = C ₂ = 40 pF | 260 | 580 | - | |
| | | f _{OSC} = 6 MHz C _p = 10 pF | C ₁ = C ₂ = 10 pF | 160 | 415 | - | |
| | | | C ₁ = C ₂ = 20 pF | 325 | 640 | - | |
| | | | C ₁ = C ₂ = 30 pF | 250 | 550 | - | |
| | | | C ₁ = C ₂ = 40 pF | 180 | 420 | - | |
| | | f _{OSC} = 7 MHz C _p = 10 pF | C ₁ = C ₂ = 10 pF | 160 | 375 | - | |
| | | | C ₁ = C ₂ = 20 pF | 260 | 525 | - | |
| | | | C ₁ = C ₂ = 30 pF | 185 | 420 | - | |
| | | | C ₁ = C ₂ = 40 pF | 135 | 315 | - | |
| | | f _{OSC} = 8 MHz C _p = 10 pF | C ₁ = C ₂ = 10 pF | 155 | 340 | - | |
| | | | C ₁ = C ₂ = 20 pF | 210 | 435 | - | |
| | | | C ₁ = C ₂ = 30 pF | 145 | 335 | - | |
| | | | C ₁ = C ₂ = 40 pF | 100 | 245 | - | |

1. Min and max values are guaranteed by characterization, not tested in production.
2. C_p represents the total capacitance between XTAL1 and XTAL2, including the shunt capacitance of the external quartz crystal as well as the total board parasitic cross-capacitance between XTAL1 track and XTAL2 track.
3. C₁ represents the total capacitance between XTAL1 and ground, including the external capacitance tied to XTAL1 pin (C_L) as well as the total parasitic capacitance between XTAL1 track and ground (this includes application board track capacitance to ground and device pin capacitance).
4. C₂ represents the total capacitance between XTAL2 and ground, including the external capacitance tied to XTAL2 pin (C_L) as well as the total parasitic capacitance between XTAL2 track and ground (this includes application board track capacitance to ground and device pin capacitance).

RC/backup oscillator characteristics

$V_{DD} = 5V \pm 10\%$, $T_A = -40^\circ\text{C}$ to T_{Amax} , unless otherwise specified.

Table 15. RC oscillator characteristics

| Symbol | Parameter | Conditions | Value | | | Unit |
|------------------|-----------------------------|--|-------|------|-----|---------------|
| | | | Min | Typ | Max | |
| f_{RC} | RC frequency | High frequency mode ¹⁾ | | 2.35 | | MHz |
| | | Low frequency mode ¹⁾ | | 29 | | kHz |
| f_{RCHF} | RC high frequency | CMU_RCCTL = 0x0 | 3 | | | MHz |
| | | CMU_RCCTL = 0xF | | | 2.3 | MHz |
| f_{RCLF} | RC low frequency | CMU_RCCTL = 0x0 | 35 | | | kHz |
| | | CMU_RCCTL = 0xF | | | 30 | kHz |
| $f_{RCHFS}^{2)}$ | RC high frequency stability | Fixed CMU_RCCTL | | | 10 | % |
| $f_{RCLFS}^{2)}$ | RC low frequency stability | Fixed CMU_RCCTL | | | 23 | % |
| t_{RCSTUP} | RC start-up time | Stable V_{DD} , $f_{RC} = 2.35$ MHz, $T_A = 25^\circ\text{C}$ | | 2.35 | | μs |

1) CMU_RCCTL = 0x8

2) RC frequency shift versus average value (%)

PLL electrical characteristics

$V_{DD} = 5\text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to T_{Amax} , unless otherwise specified

Table 16. PLL characteristics

| Symbol | Parameter | Conditions | Value | | | Unit |
|--------------------|----------------------------|--|--|--------------------------|------------|---------------|
| | | | Min | Typ | Max | |
| $f_{PLLIN}^{(1)}$ | PLL reference clock | FREF_RANGE = '0' FREF_RANGE = '1' | 1.5 3.0 | | 3.0 5.0 | MHz |
| f_{PULO} | PLL output clock | MX = "00" MX = "01" MX = "10" MX = "11" | 20 x f_{PLLIN} 12 x f_{PLLIN} 28 x f_{PLLIN} 16 x f_{PLLIN} | | | MHz |
| f_{MCLK} | System clock | DX = 1..7 | f_{PULO}/DX | | 36 | MHz |
| $f_{FREE}^{(2)}$ | PLL free running frequency | FREF_RANGE = '0', MX0 = '1' FREF_RANGE = '0', MX0 = '0' FREF_RANGE = '1', MX0 = '1' FREF_RANGE = '1', MX0 = '0' | | 120 240 240 480 | | kHz |
| $t_{LOCK}^{(3)}$ | PLL lock time | Stable oscillator ($f_{PLLIN} = 4\text{ MHz}$), stable V_{DD} | | 100 | 300 | μs |
| Δt_{PKJIT} | PLL jitter (pk to pk) | $f_{PLLIN} = 4\text{ MHz}$ (pulse generator) | | | 1.5 | ns |

1. f_{PLLIN} is obtained from f_{OSC} directly or through an optional divider by 2.

2. Typical data are based on $T_A=25^\circ\text{C}$, $V_{DD}=5\text{V}$

3. Max value is guaranteed by characterization, not tested in production.

Table 17. Low-power mode wake-up timing

| Symbol | Parameter | Conditions | Typ | Unit |
|--------------------|-------------------------|--|-----|---------------|
| t_{WUHALT} | Wake-up from HALT mode | | 200 | μs |
| t_{WUSTOP} | Wake-up from STOP mode | RC high frequency in STOP mode | 180 | μs |
| | | RC low frequency in STOP mode | 234 | μs |
| $t_{WULPWF1}^{1)}$ | Wake-up from LPWFI mode | Main voltage regulator on RC oscillator off $f_{OSC} = 4\text{ MHz}$, $f_{MCLK} = f_{OSC}/16$ RAM or FLASH execution | 27 | μs |
| | | Main voltage regulator on RC oscillator = high frequency Flash execution | 46 | μs |
| | | Main voltage regulator on RC oscillator = low frequency Flash execution | 3.6 | ms |

1. Flash memory programmed to enter Power Down mode during LPWFI.

4.3.3 Memory characteristics

Flash memory

Table 18. Flash memory characteristics

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|--------------------------------|-----------------------------|---|-------|-----|-------------------|---------|
| | | | Min | Typ | Max ¹⁾ | |
| t _{WP} | Word program (32-bit) | | | 35 | 80 | μs |
| t _{DWP} | Double word program(64-bit) | | | 64 | 150 | μs |
| t _{BP64} | Bank program (64 K) | Double word program | | 0.5 | 1.25 | s |
| t _{BP128} | Bank program (128 K) | Double word program | | 1 | 2.5 | s |
| t _{BP256} | Bank program (256 K) | Double word program | | 2 | 4.9 | s |
| t _{SE8} | Sector erase (8 K) | Not preprogrammed Preprogrammed ²⁾ | | 0.6 | 0.9 | s |
| | | | | 0.5 | 0.8 | |
| t _{SE32} | Sector erase (32 K) | Not preprogrammed Preprogrammed ²⁾ | | 1.1 | 2 | s |
| | | | | 0.8 | 1.8 | |
| t _{SE64} | Sector erase (64 K) | Not preprogrammed preprogrammed ²⁾ | | 1.7 | 3.7 | s |
| | | | | 1.3 | 3.3 | |
| t _{RPD} ³⁾ | Recovery from power-down | | | | 20 | μs |
| t _{PSL} ³⁾ | Program suspend latency | | | | 10 | μs |
| t _{ESL} ³⁾ | Erase suspend latency | | | | 30 | μs |
| t _{ESR} ³⁾ | Erase suspend rate | Min. time from erase resume to next erase suspend | | 20 | 20 | ms |
| t _{SP} ³⁾ | Set protection | | | 40 | 170 | μs |
| t _{FPW} ³⁾ | First word program | | | 1 | | ms |
| N _{END} | Endurance | | 10 | | | kcycles |
| t _{RET} | Data retention | T _A = 85° C | 20 | | | Years |

1. T_A = -45° C after 0 cycles, Guaranteed by characterization, not tested in production.
2. All bits programmed to 0.
3. Guaranteed by design, not tested in production.

4.3.4 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD:** Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB:** A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 19. EMS data

| Symbol | Parameter | Conditions | Level/Class |
|------------|---|---|-------------|
| V_{FESD} | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}=5$ V, $T_A=+25^\circ$ C, $f_{MCLK}=36$ MHz conforms to IEC 1000-4-2 | 4A |
| V_{EFTB} | Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance | $V_{DD}=5$ V, $T_A=+25^\circ$ C, $f_{MCLK}=36$ MHz conforms to IEC 1000-4-4 | 4A |

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 20. EMI data

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [f _{OSC4M} /f _{MCLK}] | | Unit |
|------------------|------------|--|--------------------------|--|---------|------|
| | | | | 6/36 MHz | 8/8 MHz | |
| S _{EMI} | Peak level | V _{DD} =5.0V, T _A =+25°C, All packages | 0.1 MHz to 30 MHz | 23 | 30 | dBμV |
| | | | 30 MHz to 130 MHz | 37 | 34 | |
| | | | 130 MHz to 1 GHz | 20 | 7 | |
| | | | SAE EMI Level | 4 | 3.5 | - |

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: human body model and machine model. This test conforms to the JESD22-A114A/A115A standard.

Table 21. ESD Absolute Maximum ratings

| Symbol | Ratings | Conditions | Maximum value ¹⁾ | Unit |
|-----------------------|---|------------------------|-----------------------------------|------|
| V _{ESD(HBM)} | Electrostatic discharge voltage (human body model) | T _A =+25° C | 2000 | V |
| V _{ESD(MM)} | Electrostatic discharge voltage (machine model) | | 200 | |
| V _{ESD(CDM)} | Electrostatic discharge voltage (charge device model) | | 750 on corner pins, 500 on others | |

Notes:

- 1. Data based on characterization results, not tested in production.

Static and dynamic latch-up

- **LU:** 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each

sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

- **DLU:** Electrostatic discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Table 22. Electrical sensitivities

| Symbol | Parameter | Conditions | Class ¹⁾ |
|--------|------------------------|--|---------------------|
| LU | Static latch-up class | $T_A=+25^{\circ}\text{C}$ | A |
| | | $T_A=+85^{\circ}\text{C}$ | A |
| | | $T_A=+105^{\circ}\text{C}$ | A |
| DLU | Dynamic latch-up class | $V_{DD}= 5.5 \text{ V}$, $f_{OSC4M} = 4 \text{ MHz}$, $f_{MCLK} = 32 \text{ MHz}$, $T_A = +25^{\circ} \text{ C}$ | A |

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

4.3.5 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 23. I/O static characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|----------------------------------|-----|-----|----------|------------|
| V_{IL} | Input low level voltage ¹⁾ | TTL ports | | | 0.8 | V |
| V_{IH} | Input high level voltage ¹⁾ | | 2.0 | | | |
| $I_{INJ(PIN)}$ | Injected current on any I/O pin | | | | ± 10 | mA |
| $\Sigma I_{INJ(PIN)}$ ²⁾ | Total injected current (sum of all I/O and control pins) | | | | ± 75 | mA |
| I_{lkg} | Input leakage current ³⁾ | $V_{SS} \leq V_{IN} \leq V_{DD}$ | | | ± 1 | μA |
| I_S | Static current consumption ⁴⁾ | Floating input mode | | 200 | | μA |
| R_{PU} | Weak pull-up equivalent resistor ⁵⁾ | $V_{IN} = V_{SS}$ | 55 | 120 | 220 | k Ω |
| R_{PD} | Weak pull-down equivalent resistor ⁵⁾ | $V_{IN} = V_{DD}$ | 55 | 120 | 220 | k Ω |
| C_{IO} | I/O pin capacitance | | | 5 | | pF |

1. Data based on characterization results, not tested in production.
2. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN} > V_{33}$ while a negative injection is induced by $V_{IN} < V_{SS}$. Refer to [Section 4.2 on page 22](#) for more details.
3. Leakage could be higher than max. if negative current is injected on adjacent pins.
4. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor. Data based on design simulation and/or technology characteristics, not tested in production.
6. The R_{PU} pull-up and R_{PD} pull-down equivalent resistor are based on a resistive transistor (corresponding I_{PU} and I_{PD} current characteristics described in [Figure 19](#)).

Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 24. Output driving current

| I/O Type | Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|---------------|---|-----------------------|--------------|-----|------|
| Standard | $V_{OL}^{1)}$ | Output low level voltage for an I/O pin when 8 pins are sunk at same time | $I_{IO}=+2\text{ mA}$ | | 0.4 | V |
| | $V_{OH}^{2)}$ | Output high level voltage for an I/O pin when 4 pins are sourced at same time | $I_{IO}=-2\text{ mA}$ | $V_{DD}-0.8$ | | |
| Med. Current (JTDO) | $V_{OL}^{1)}$ | Output low level voltage for an I/O pin | $I_{IO}=+6\text{ mA}$ | | 0.4 | |
| | $V_{OH}^{2)}$ | Output high level voltage for an I/O pin | $I_{IO}=-6\text{ mA}$ | $V_{DD}-0.8$ | | |
| High Current P6.0 | $V_{OL}^{1)}$ | Output low level voltage for an I/O pin | $I_{IO}=+8\text{ mA}$ | | 0.4 | |
| | $V_{OH}^{2)}$ | Output high level voltage for an I/O pin | $I_{IO}=-8\text{ mA}$ | $V_{DD}-0.8$ | | |

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in [Table 6](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in [Table 6](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .

Figure 13. V_{OH} standard ports vs I_{OH} @ V_{DD} 5V **Figure 14. V_{OL} standard ports vs I_{OL} @ V_{DD} 5 V**
 $T_A -45^\circ\text{C}$

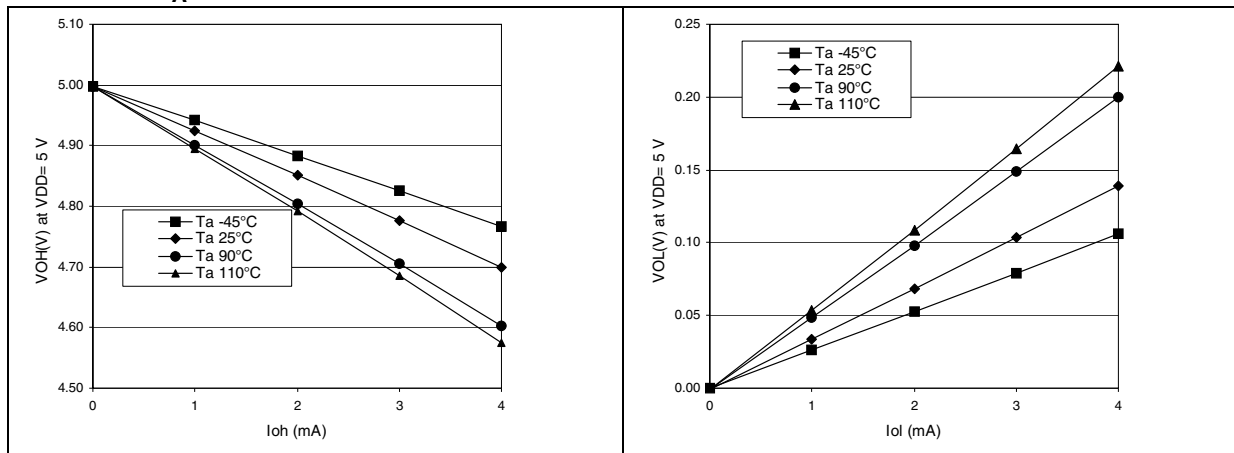


Figure 15. V_{OH} JTDO pin vs I_{OL} @ V_{DD} 5 V

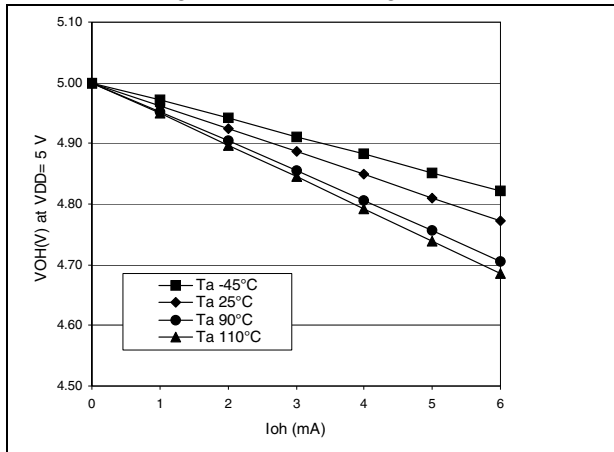


Figure 16. V_{OL} JTDO pin vs I_{OL} @ V_{DD} 5 V

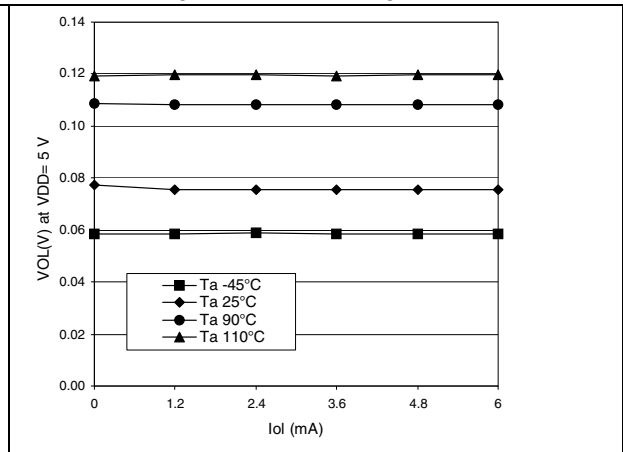


Figure 17. V_{OH} P6.0 pin vs I_{OL} @ V_{DD} 5 V

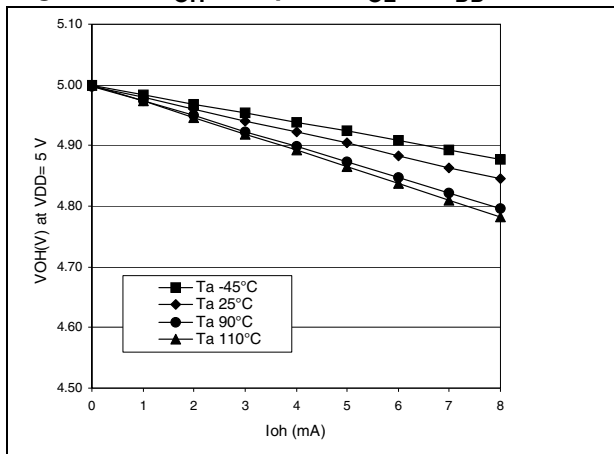
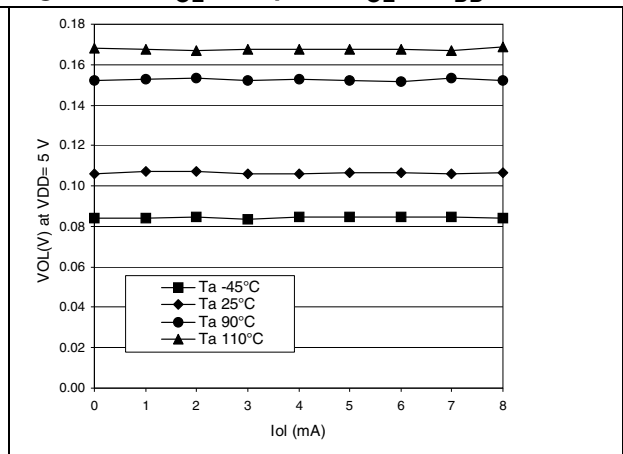


Figure 18. V_{OL} P6.0 pin vs I_{OL} @ V_{DD} 5 V



NRSTIN pin

The NRSTIN pin input driver is CMOS. A permanent pull-up is present which is the same as R_{PU} (see : [General characteristics on page 38](#))

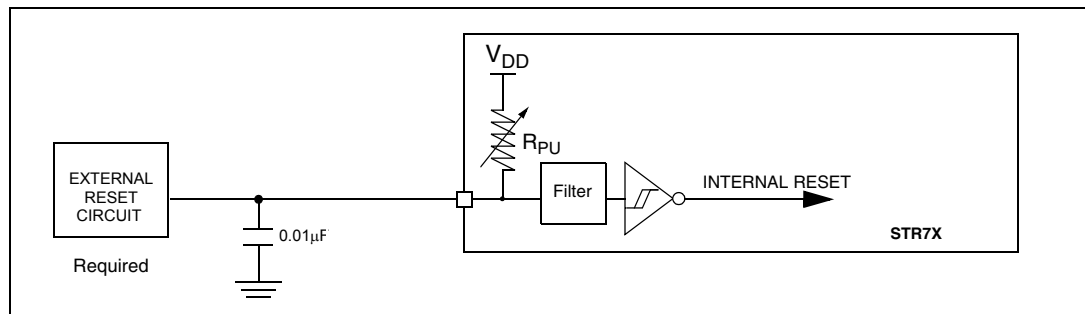
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 25. Reset pin characteristics

| Symbol | Parameter | Conditions | Min | Typ ¹⁾ | Max | Unit |
|-------------------|---|------------|--------------|-------------------|--------------|---------|
| $V_{IL(NRSTIN)}$ | NRSTIN Input low level voltage ¹⁾ | | | | $0.3 V_{DD}$ | V |
| $V_{IH(NRSTIN)}$ | NRSTIN Input high level voltage ¹⁾ | | $0.7 V_{DD}$ | | | |
| $V_{hys(NRSTIN)}$ | NRSTIN Schmitt trigger voltage hysteresis ²⁾ | | | 800 | | mV |
| $V_{F(RSTINn)}$ | NRSTIN Input filtered pulse ³⁾ | | | | 500 | ns |
| $V_{NF(RSTINn)}$ | NRSTIN Input not filtered pulse ³⁾ | | 2 | | | μ s |
| $V_{RP(RSTINn)}$ | NRSTIN removal after Power-up ³⁾ | | 100 | | | μ s |

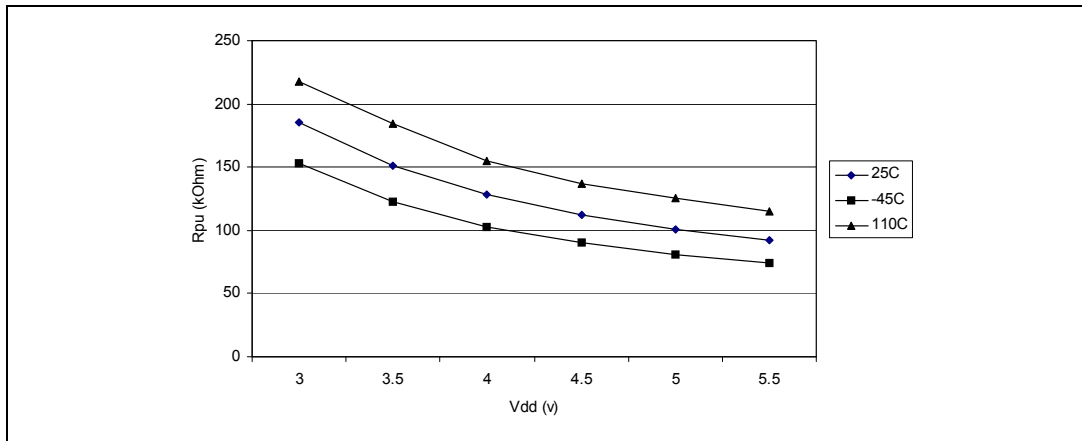
1. Data based on characterization results, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels.
3. Data guaranteed by design, not tested in production.

Figure 19. Recommended NRSTIN pin protection¹⁾



1. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.
2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the NRSTIN pin can go below the $V_{IL(NRSTIN)}$ max. level specified in [Table 25](#). Otherwise the reset will not be taken into account internally.

Figure 20. NRSTIN R_{PJ} vs. V_{DD}



4.3.6 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA} , f_{MCLK} , and T_A unless otherwise specified.

Table 26. ADC characteristics

| Symbol | Parameter | Conditions | Min | Typ ¹⁾ | Max | Unit |
|----------------|---|---|---|-------------------|-----------|-------------|
| f_{ADC} | | | 0.4 | | 10 | MHz |
| V_{AIN} | Conversion voltage range ²⁾ | | V_{SSA} | | V_{DDA} | V |
| I_{Ikg} | Negative input leakage current on analog pins | $V_{IN} < V_{SS}$, $ I_{IN} < 400 \mu A$ on adjacent analog pin | | 5 | 6 | μA |
| C_{ADC} | Internal sample and hold capacitor | | | | 3.5 | pF |
| $t_{CAL}^{2)}$ | Calibration time | $f_{ADC} = 10 \text{ MHz}$ | 580.2 | | | μs |
| | | | 5802 | | | $1/f_{ADC}$ |
| $t_S^{3)}$ | Sampling time | $f_{ADC} = 10 \text{ MHz}$ | 1 | | 14 | μs |
| t_{CONV} | Total conversion time (including sampling time) | $f_{ADC} = 10 \text{ MHz}$ | 3 | | | μs |
| | | | 30 (10 for sampling +20 for successive approximation) | | | |
| I_{ADC} | Running mode | Normal mode | | | 5 | mA |
| | Power-down mode | | | | 1 | μA |

1. Unless otherwise specified, typical data are based on $T_A=25^\circ C$ and $V_{DDA}-V_{SS}=5.0V$. They are given only as design guidelines and are not tested.
2. Calibration is recommended once after each power-up.
3. During the sample time the input capacitance C_{AIN} (6.8 max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S . After the end of the sample time t_S , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

Table 27. ADC accuracy with $f_{MCLK} = 20 \text{ MHz}$, $f_{ADC} = 10 \text{ MHz}$, $R_{AIN} < 10 \text{ k}\Omega$ RAIN, $V_{DDA} = 5 \text{ V}$. This assumes that the ADC is calibrated²⁾

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|---------|--|------------|------|-----|------|
| $ E_T $ | Total unadjusted error ¹⁾ | | 1.0 | 2.0 | LSB |
| $ E_O $ | Offset error ¹⁾ | | 0.15 | 1.0 | |
| $ E_G $ | Gain error ¹⁾ | | 0.97 | 1.1 | |
| $ E_D $ | Differential linearity error ¹⁾ | | 0.7 | 1.0 | |
| $ E_L $ | Integral linearity error ¹⁾ | | 0.76 | 1.5 | |

1. ADC accuracy vs. negative injection current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. The effect of negative injection current on robust pins is specified in [Section 4.3.5](#). Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 4.3.5](#) does not affect the ADC accuracy.
2. Calibration is needed once after each power-up.

Figure 21. ADC accuracy characteristics

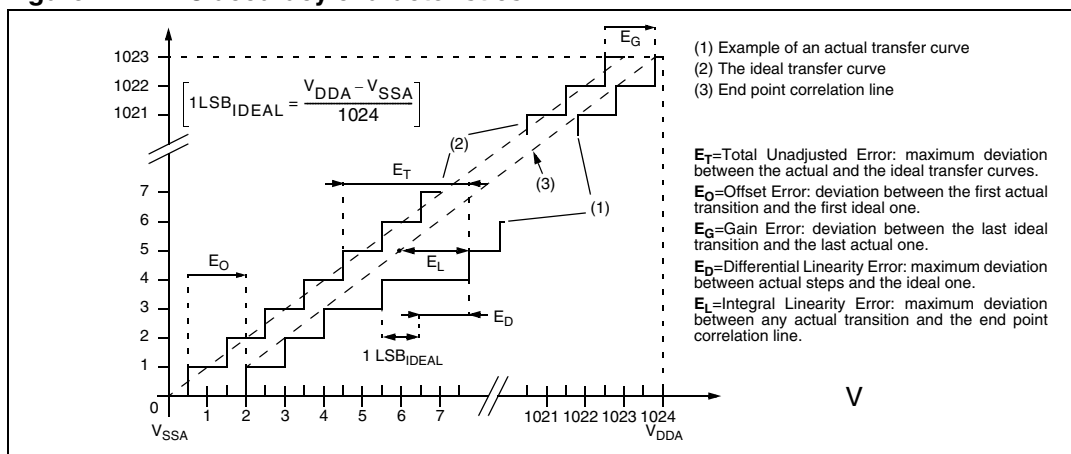
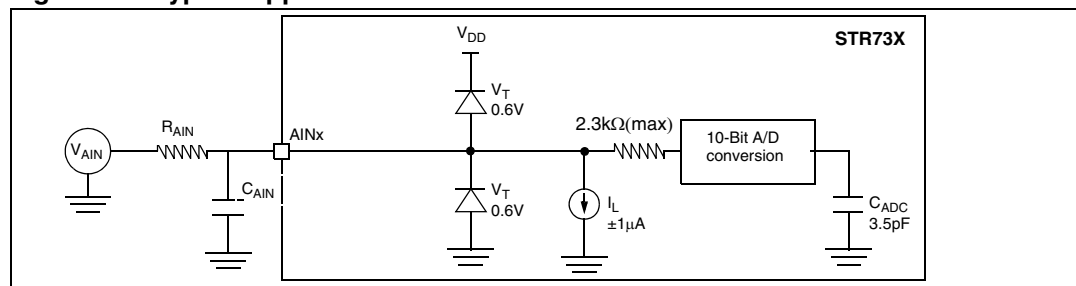


Figure 22. Typical application with ADC



Analog power supply and reference pins

The V_{DDA} and V_{SSA} pins are the analog power supply of the A/D converter cell. They act as the high and low reference voltages for the conversion.

Separation of the digital and analog power pins allow board designers to improve A/D performance. Conversion accuracy can be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines (see: [General PCB design guidelines](#)).

General PCB design guidelines

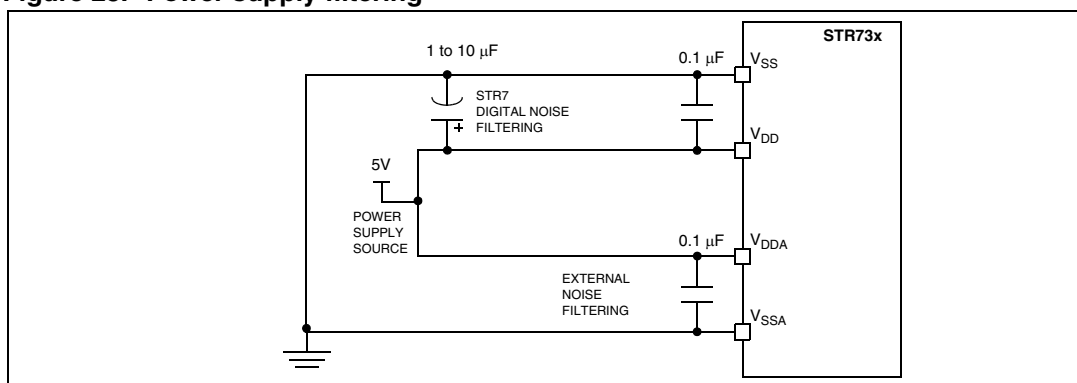
To obtain best results, some general design and layout rules should be followed when designing the application PCB to shield the noise-sensitive, analog physical interface from noise-generating CMOS logic signals.

- Use separate digital and analog planes. The analog ground plane should be connected to the digital ground plane via a single point on the PCB.
- Filter power to the analog power planes. It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing 0.1 μF and optionally, if needed 10 pF capacitors as close as possible to the STR7 power supply pins and a 1 to 10 μF capacitor close to the power source (see [Figure 23](#)).
- The analog and digital power supplies should be connected in a star network. Do not use a resistor, as V_{DDA} is used as a reference voltage by the A/D converter and any resistance would cause a voltage drop and a loss of accuracy.
- Properly place components and route the signal traces on the PCB to shield the analog inputs. Analog signals paths should run over the analog ground plane and be as short as possible. Isolate analog signals from digital signals that may switch while the analog inputs are being sampled by the A/D converter. Do not toggle digital outputs near the A/D input being converted.

Software filtering of spurious conversion results

For EMC performance reasons, it is recommended to filter A/D conversion outliers using software filtering techniques.

Figure 23. Power supply filtering



5 Package characteristics

5.1 Package mechanical data

Figure 24. 100-pin thin quad flat package

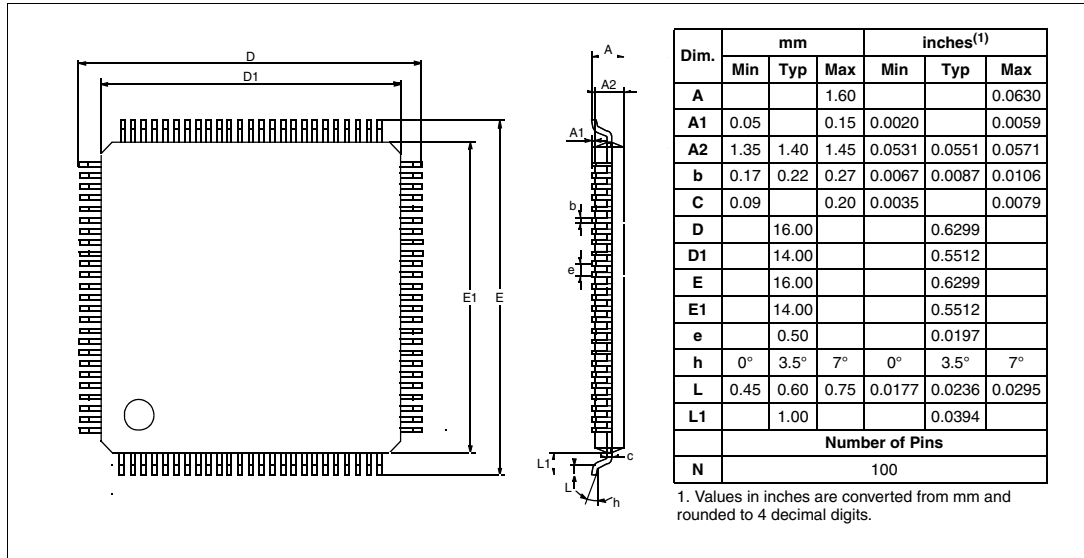


Figure 25. 144-pin thin quad flat package

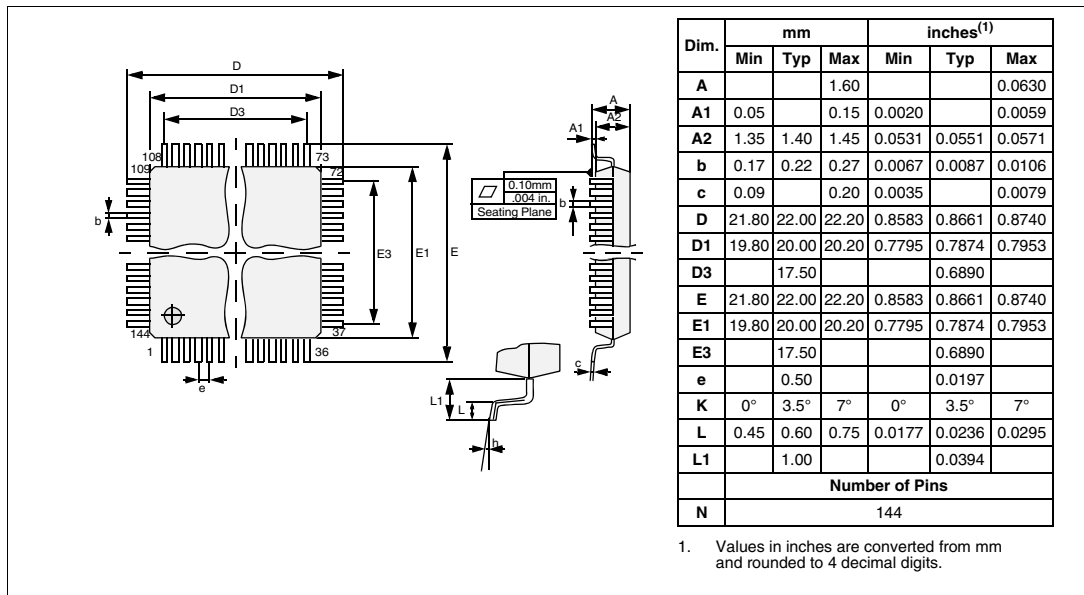


Figure 26. 144-ball low profile fine pitch ball grid array package

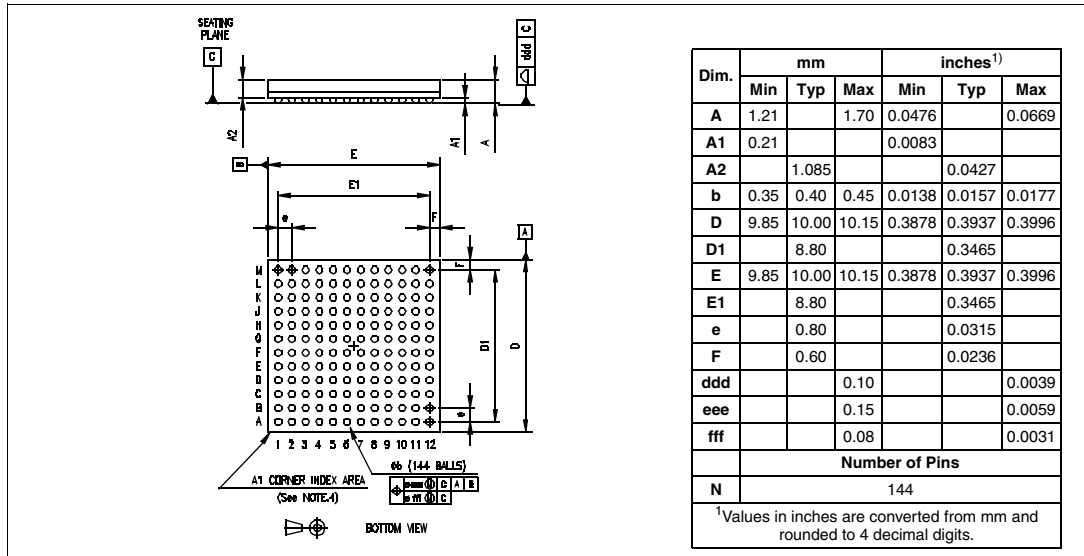
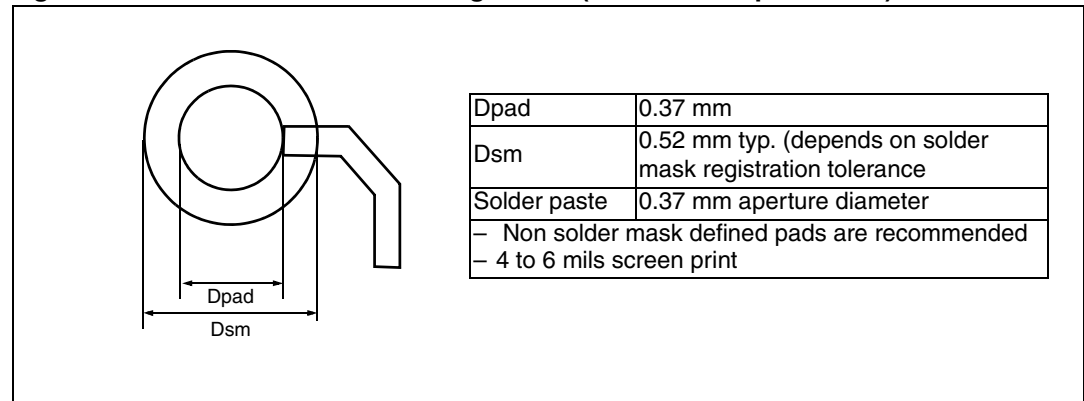


Figure 27. Recommended PCB design rules (0.80/0.75mm pitch BGA)



5.2 Thermal characteristics

The average chip-junction temperature, T_J , in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \tag{1}$$

Where:

- T_A is the ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD} , expressed in Watts. This is the chip internal power,
- $P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273^\circ\text{C}) \tag{2}$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273^\circ\text{C}) + \Theta_{JA} \times P_D^2 \tag{3}$$

Where:

- K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A . Using this value of K , the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A

Table 28. Thermal characteristics

| Symbol | Description | Package | Value (typical) | Unit |
|---------------|-------------------------------------|----------|-----------------|------|
| Θ_{JA} | Thermal resistance junction-ambient | LFBGA144 | 50 | °C/W |
| | | TQFP144 | 40 | |
| | | TQFP100 | 40 | |

6 Order codes

Table 29. Order codes

| Partnumber | Flash Kbytes | Package | RAM Kbytes | TIM timers | 6x PWM module | CAN periph | A/D chan. | Wake-up lines | I/O ports | Temp. range | | | | | |
|-------------|--------------|-------------------|------------|------------|---------------|------------|-----------|---------------|-----------|------------------|---|---|----|----|----|
| STR730FZ1T6 | 128 | TQFP144 20x20 | 16 | 10 | 1 | 3 | 16 | 32 | 112 | -40 to +85°C | | | | | |
| STR730FZ2T6 | 256 | | | | | | | | | | | | | | |
| STR730FZ1H6 | 128 | LFBGA144 10x10 | | | | | | | | | | | | | |
| STR730FZ2H6 | 256 | | | | | | | | | | | | | | |
| STR735FZ1T6 | 128 | TQFP144 20x20 | | | | | | | | | | | | | |
| STR735FZ2T6 | 256 | | | | | | | | | | | | | | |
| STR735FZ1H6 | 128 | LFBGA144 10x10 | | 6 | 1 | 0 | 12 | 18 | 72 | | | | | | |
| STR735FZ2H6 | 256 | | | | | | | | | | | | | | |
| STR731FV0T6 | 64 | TQFP100 14x14 | | | | | | | | | | | | | |
| STR731FV1T6 | 128 | | | | | | | | | | | | | | |
| STR731FV2T6 | 256 | TQFP100 14x14 | | | | | | | | | | | | | |
| STR736FV0T6 | 64 | | | | | | | | | | | | | | |
| STR736FV1T6 | 128 | | | | | | | | | | | | | | |
| STR736FV2T6 | 256 | | | | | | | | | | | | | | |
| STR730FZ1T7 | 128 | TQFP144 20x20 | 16 | 10 | 1 | 3 | 16 | 32 | 112 | -40 to +105°C | | | | | |
| STR730FZ2T7 | 256 | | | | | | | | | | | | | | |
| STR730FZ1H7 | 128 | LFBGA144 10x10 | | | | | | | | | | | | | |
| STR730FZ2H7 | 256 | | | | | | | | | | | | | | |
| STR735FZ1T7 | 128 | TQFP144 20x20 | | | | 6 | | | | | 1 | 0 | 12 | 18 | 72 |
| STR735FZ2T7 | 256 | | | | | | | | | | | | | | |
| STR735FZ1H7 | 128 | LFBGA144 10x10 | | | | | | | | | | | | | |
| STR735FZ2H7 | 256 | | | | | | | | | | | | | | |
| STR731FV0T7 | 64 | TQFP100 14x14 | | | | | | | | | | | | | |
| STR731FV1T7 | 128 | | | | | | | | | | | | | | |
| STR731FV2T7 | 256 | TQFP100 14x14 | | | | | | | | | | | | | |
| STR736FV0T7 | 64 | | | | | | | | | | | | | | |
| STR736FV1T7 | 128 | | | | | | | | | | | | | | |
| STR736FV2T7 | 256 | | | | | | | | | | | | | | |

7 Known limitations

7.1 Low power wait for interrupt mode

When the STR73x device is put in Low Power Wait For Interrupt mode (LPWFI), the Flash goes into low power mode or power down mode, depending on the setting of the PWD bit in the Flash Control Register 0 (default is '0', Low Power mode). This default mode can create excessive voltage conditions on the transistor gates and may affect the long term behavior of the Low Power mode circuitry.

Workaround

There is no workaround. If Low Power Wait For Interrupt mode is used, it is strongly suggested to configure the Flash to enter power down mode (bit PWD = '1').

7.2 PLL free running mode at high temperature

When the STR73x device is operated and an ambient temperature (T_A) of more than 55° C and the main system clock (f_{MCLK}) is sourced by the PLL in free running mode, the device may not work properly.

Workaround

At high temperature (more than 55° C), it is recommended to use the internal RC oscillator as a backup clock source rather than the PLL free running mode.

8 Revision history

Table 30. Document revision history

| Date | Revision | Description of changes |
|-------------|----------|--|
| 19-Sep-2005 | 1 | First release |
| 02-Nov-2005 | 2 | Removed Table 8 power consumption in LP modes Updated PLL frequency in Section 1.1 and Table 12 |
| 08-Mar-2006 | 3 | Section 3.4: Preliminary power consumption data updated Section 3.5: DC electrical characteristics updated Section 7: Known limitations added |
| 04-Jun-2006 | 4 | Section 4: Electrical parameters updated Section 7: Known limitations updated Added temperature range -40°C to 85°C in Section 6: Order codes |
| 19-Jun-2006 | 5 | Changed Flash data retention to 20 years at 85°C in Table 18 on page 34 . |
| 08-Sep-2006 | 6 | Changed Table 24: Output driving current on page 39 Added Figure 14: VOL standard ports vs IOL @ VDD 5 V thru Figure 18: VOL P6.0 pin vs IOL @ VDD 5 V on page 40 . Added Figure 20: NRSTIN RPU vs. VDD |
| 08-Jun-2008 | 7 | Inch values rounded to 4 decimal digits in Section 5.1: Package mechanical data Modified BSPI speed in Section 2.1: On-chip peripherals |

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