Document Number: MMRF1306H
Rev. 1, 8/2014

RoHS

RF Power LDMOS Transistors

High Ruggedness N-Channel Enhancement-Mode Lateral MOSFETs

These high ruggedness devices are designed for use in high VSWR CW or pulse applications, such as HF, VHF, and low-band UHF radar and high power radio communications. They are unmatched input and output designs allowing wide frequency utilization from 1.8 to 600 MHz.

- Typical Performance: V_{DD} = 50 Vdc, I_{DQ} = 100 mA

Signal Type	P_{out} (W)	f (MHz)	G_{ps} (dB)	η_D (%)
Pulse (100 μsec, 20% Duty Cycle)	1250 Peak	230	24.0	74.0
CW	1250 CW	230	22.9	74.6

Application Circuits (1) — Typical Performance

Frequency (MHz)	Signal Type	P_{out} (W)	G_{ps} (dB)	η_D (%)
27	CW	1300	27	81
40	CW	1300	26	85
81.36	CW	1250	27	84
87.5-108	CW	1100	24	80
144-148	CW	1250	26	78
170-230	DVB-T	225	25	30
352	Pulse (200 μsec, 20% Duty Cycle)	1250	21.5	66
352	CW	1150	20.5	68
500	CW	1000	18	58

1. Contact your local Freescale sales office for additional information on specific circuit designs.

Load Mismatch/Ruggedness

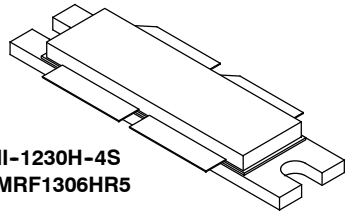
Frequency (MHz)	Signal Type	VSWR	P_{out} (W)	Test Voltage	Result
230	Pulse (100 μsec, 20% Duty Cycle)	>65:1 at all Phase Angles	1500 Peak (3 dB Overdrive)	50	No Device Degradation

Features

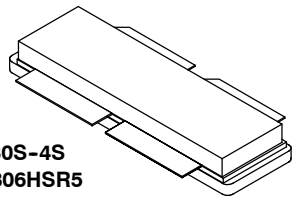
- Unmatched Input and Output Allowing Wide Frequency Range Utilization
- Device can be used Single-Ended or in a Push-Pull Configuration
- Qualified Up to a Maximum of 50 V_{DD} Operation
- Characterized from 30 V to 50 V for Extended Power Range
- Suitable for Linear Application with Appropriate Biasing
- Integrated ESD Protection with Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R5 Suffix = 50 Units, 56 mm Tape Width, 13-inch Reel.

MMRF1306HR5
MMRF1306HSR5

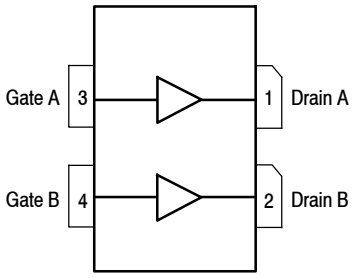
1.8–600 MHz, 1250 W CW, 50 V WIDEBAND RF POWER LDMOS TRANSISTORS



NI-1230H-4S
MMRF1306HR5



NI-1230S-4S
MMRF1306HSR5



(Top View)

Note: The backside of the package is the source terminal for the transistors.

Figure 1. Pin Connections

freescale

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +133	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1333 6.67	W W/°C
Operating Junction Temperature (1)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2)	Unit
Thermal Resistance, Junction to Case CW: Case Temperature 63°C, 1250 W CW, I_{DQ} = 100 mA, 230 MHz	$R_{\theta JC}$	0.15	°C/W
Thermal Impedance, Junction to Case Pulse: Case Temperature 66°C, 1250 W Pulse, 100 μsec Pulse Width, 20% Duty Cycle, I_{DQ} = 100 mA, 230 MHz	$Z_{\theta JC}$	0.027	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2, passes 3500 V
Machine Model (per EIA/JESD22-A115)	B, passes 250 V
Charge Device Model (per JESD22-C101)	IV, passes 4000 V

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (3)					
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Drain-Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 mA)	$V_{(BR)DSS}$	133	—	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	20	μAdc
On Characteristics					
Gate Threshold Voltage (3) (V_{DS} = 10 Vdc, I_D = 1776 μAdc)	$V_{GS(th)}$	1.7	2.2	2.7	Vdc
Gate Quiescent Voltage (V_{DD} = 50 Vdc, I_D = 100 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.9	2.2	2.9	Vdc
Drain-Source On-Voltage (3) (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.15	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 30 Adc)	g_{fs}	—	28.0	—	S
Dynamic Characteristics (3)					
Reverse Transfer Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2.8	—	pF
Output Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	185	—	pF
Input Capacitance (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	562	—	pF

1. Continuous use at maximum temperature will affect MTTF.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
3. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 100 mA, P_{out} = 1250 W Peak (250 W Avg.), f = 230 MHz, 100 μsec Pulse Width, 20% Duty Cycle					
Power Gain	G_{ps}	23.0	24.0	26.0	dB
Drain Efficiency	η_D	72.5	74.0	—	%
Input Return Loss	IRL	—	-14	-10	dB

Table 5. Load Mismatch/Ruggedness (In Freescale Test Fixture, 50 ohm system) I_{DQ} = 100 mA

Frequency (MHz)	Signal Type	VSWR	P_{out} (W)	Test Voltage, V_{DD}	Result
230	Pulse (100 μsec, 20% Duty Cycle)	>65:1 at all Phase Angles	1500 Peak (3 dB Overdrive)	50	No Device Degradation

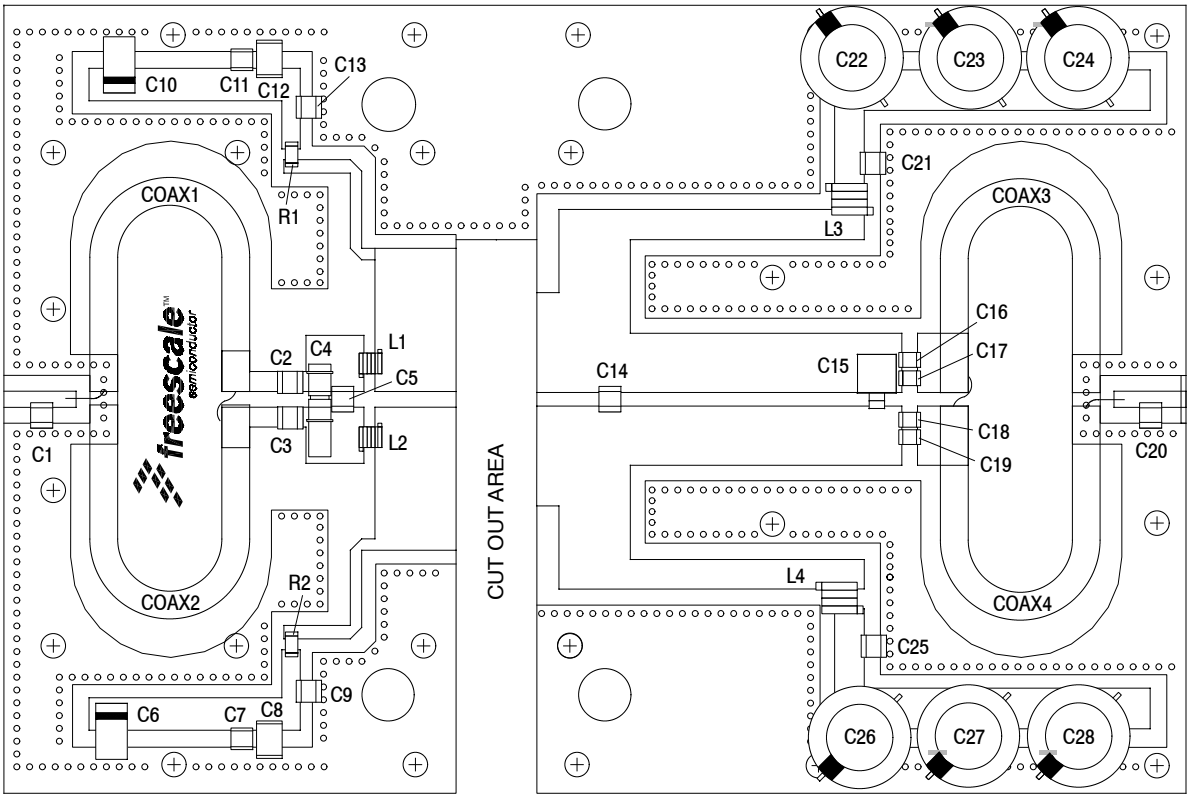


Figure 2. MMRF1306HR5(HSR5) 230 MHz Production Test Circuit Component Layout — Pulse

Table 6. MMRF1306HR5(HSR5) 230 MHz Production Test Circuit Component Designations and Values — Pulse

Part	Description	Part Number	Manufacturer
C1	20 pF Chip Capacitor	ATC100B200JT500XT	ATC
C2, C3, C5	27 pF Chip Capacitors	ATC100B270JT500XT	ATC
C4	0.8–8.0 pF Variable Capacitor, Gigatrim	27291SL	Johanson
C6, C10	22 μF, 35 V Tantalum Capacitors	T491X226K035AT	Kemet
C7, C11	0.1 μF Chip Capacitors	CDR33BX104AKYS	AVX
C8, C12	220 nF Chip Capacitors	C1812C224K5RACTU	Kemet
C9, C13, C21, C25	1000 pF Chip Capacitors	ATC100B102JT50XT	ATC
C14	43 pF Chip Capacitor	ATC100B430JT500XT	ATC
C15	75 pF Metal Mica	MIN02-002EC750J-F	CDE
C16, C17, C18, C19	240 pF Chip Capacitors	ATC100B241JT200XT	ATC
C20	6.2 pF Chip Capacitor	ATC100B6R2BT500XT	ATC
C22, C23, C24, C26, C27, C28	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
Coax1, 2, 3, 4	25 Ω Semi Rigid Coax, 2.2″ Shield Length	UT-141C-25	Micro-Coax
L1, L2	5 nH Inductors	A02TKLC	Coilcraft
L3, L4	6.6 nH Inductors	GA3093-ALC	Coilcraft
R1, R2	10 Ω Chip Resistors	CRCW120610R0JNEA	Vishay
PCB	0.030″, ε_r = 2.55	AD255A	Arlon

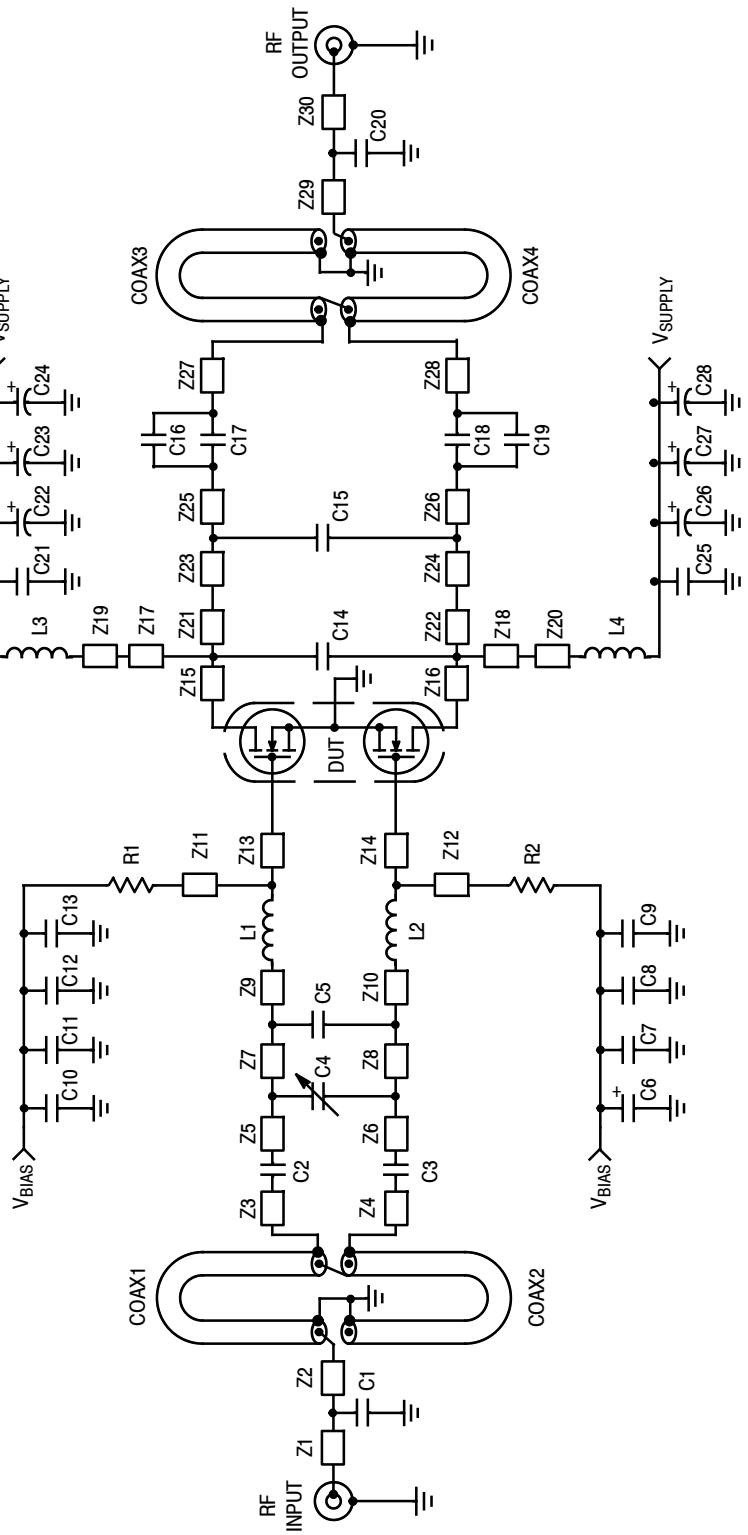


Figure 3. MMRF1306HR5(HSR5) 230 MHz Production Test Circuit Schematic — Pulse

Table 7. MMRF1306HR5(HSR5) 230 MHz Production Test Circuit Microstrips — Pulse

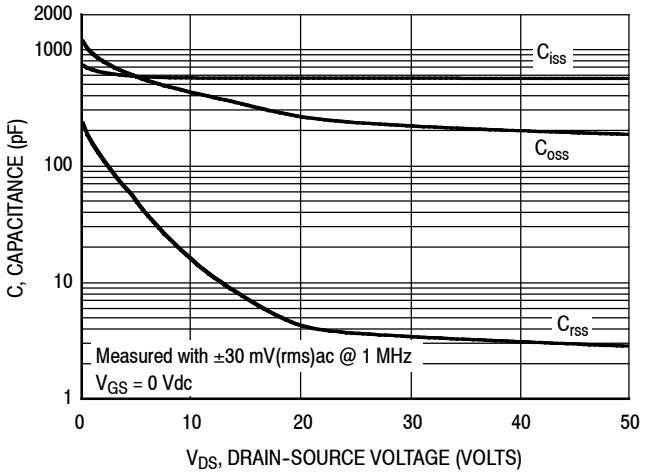
Microstrip	Description
Z1	0.192″ × 0.082″ Microstrip
Z2	0.175″ × 0.082″ Microstrip
Z3, Z4	0.170″ × 0.100″ Microstrip
Z5, Z6	0.116″ × 0.285″ Microstrip
Z7, Z8	0.116″ × 0.285″ Microstrip
Z9, Z10	0.108″ × 0.285″ Microstrip

Microstrip	Description
Z11*, Z12*	0.872″ × 0.058″ Microstrip
Z13, Z14	0.412″ × 0.726″ Microstrip
Z15, Z16	0.371″ × 0.507″ Microstrip
Z17*, Z18*	0.466″ × 0.363″ Microstrip
Z19*, Z20*	0.187″ × 0.154″ Microstrip
Z21, Z22	0.104″ × 0.507″ Microstrip

Microstrip	Description
Z23, Z24	1.251″ × 0.300″ Microstrip
Z25, Z26	0.127″ × 0.300″ Microstrip
Z27, Z28	0.116″ × 0.300″ Microstrip
Z29	0.186″ × 0.082″ Microstrip
Z30	0.179″ × 0.082″ Microstrip

* Line length includes microstrip bends

TYPICAL CHARACTERISTICS



Note: Each side of device measured separately.

Figure 4. Capacitance versus Drain-Source Voltage

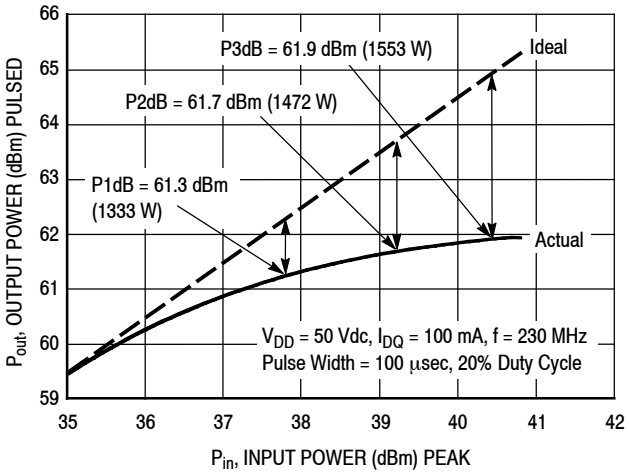


Figure 5. Output Power versus Input Power

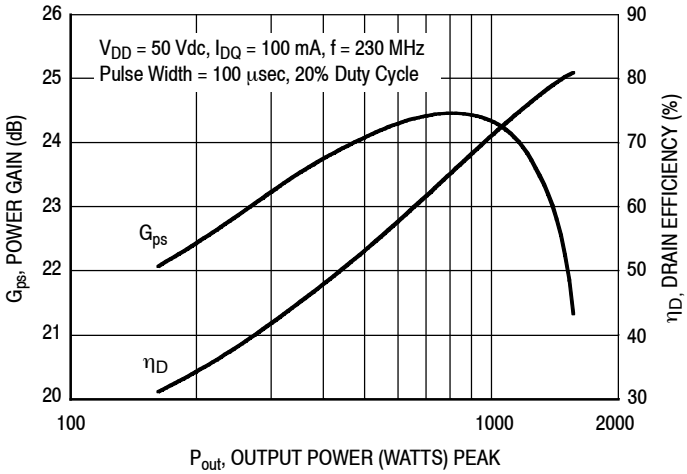


Figure 6. Power Gain and Drain Efficiency versus Output Power

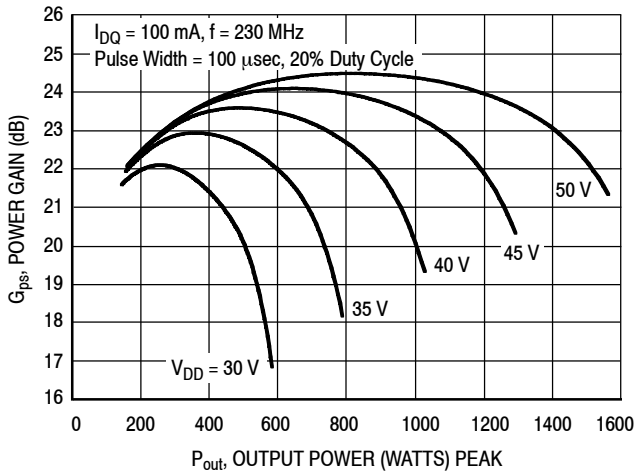


Figure 7. Power Gain versus Output Power

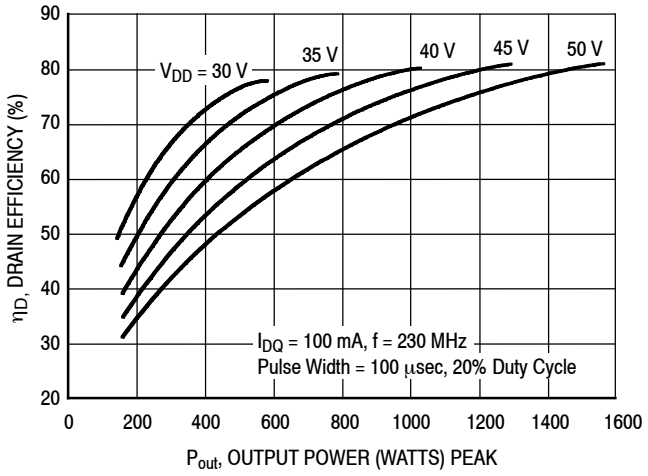


Figure 8. Drain Efficiency versus Output Power

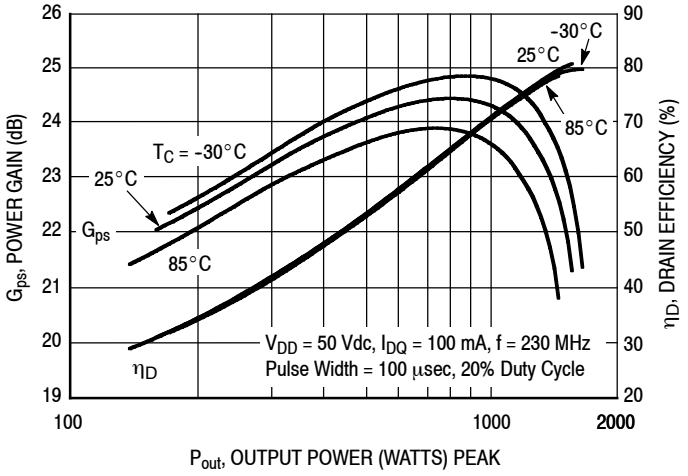
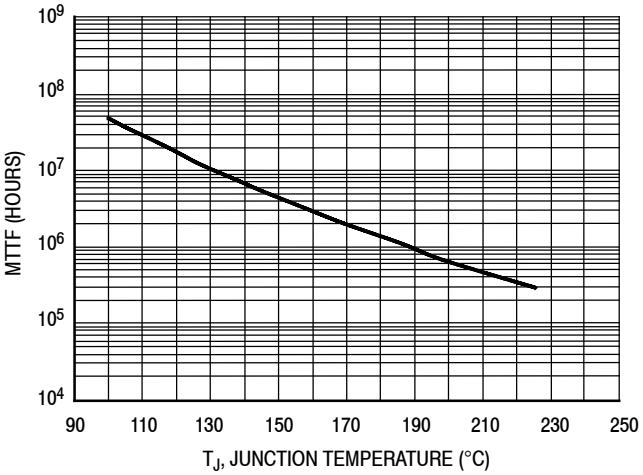


Figure 9. Power Gain and Drain Efficiency versus Output Power

TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 50 Vdc, P_{out} = 1250 W CW, and η_D = 74.6%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 10. MTTF versus Junction Temperature — CW

V_{DD} = 50 Vdc, I_{DQ} = 100 mA, P_{out} = 1250 W Peak

f MHz	Z_{source} Ω	Z_{load} Ω
230	1.29 + j3.54	2.12 + j2.68

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

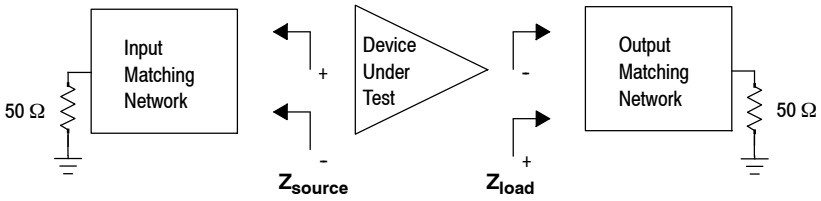


Figure 11. Series Equivalent Test Circuit Source and Load Impedance — 230 MHz Pulse

V_{DD} = 50 Vdc, I_{DQ} = 100 mA

f (MHz)	Z_{source} (Ω)	Z_{load} (Ω)
1.8 (1)	34.4 + j192.0 (1)	5.00 - j4.00 (1)
27	12.5 + j7.00	7.00 + j0.70
40	5.75 + j5.06	5.39 + j2.62
81.36	4.04 + j5.93	4.89 + j2.95
88	2.20 + j6.70	4.90 + j2.90
98	2.30 + j6.90	4.10 + j2.50
108	2.30 + j7.00	4.40 + j3.60
144	1.60 + j5.00	3.90 + j1.50
175	1.33 + j3.90	3.50 + j2.50
230	1.29 + j3.54	2.12 + j2.68
352	0.98 + j1.45	1.82 + j2.05
500	0.29 + j1.47	1.79 + j1.80

1. Simulated data.

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

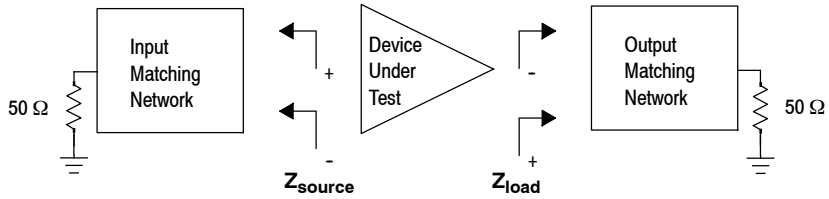
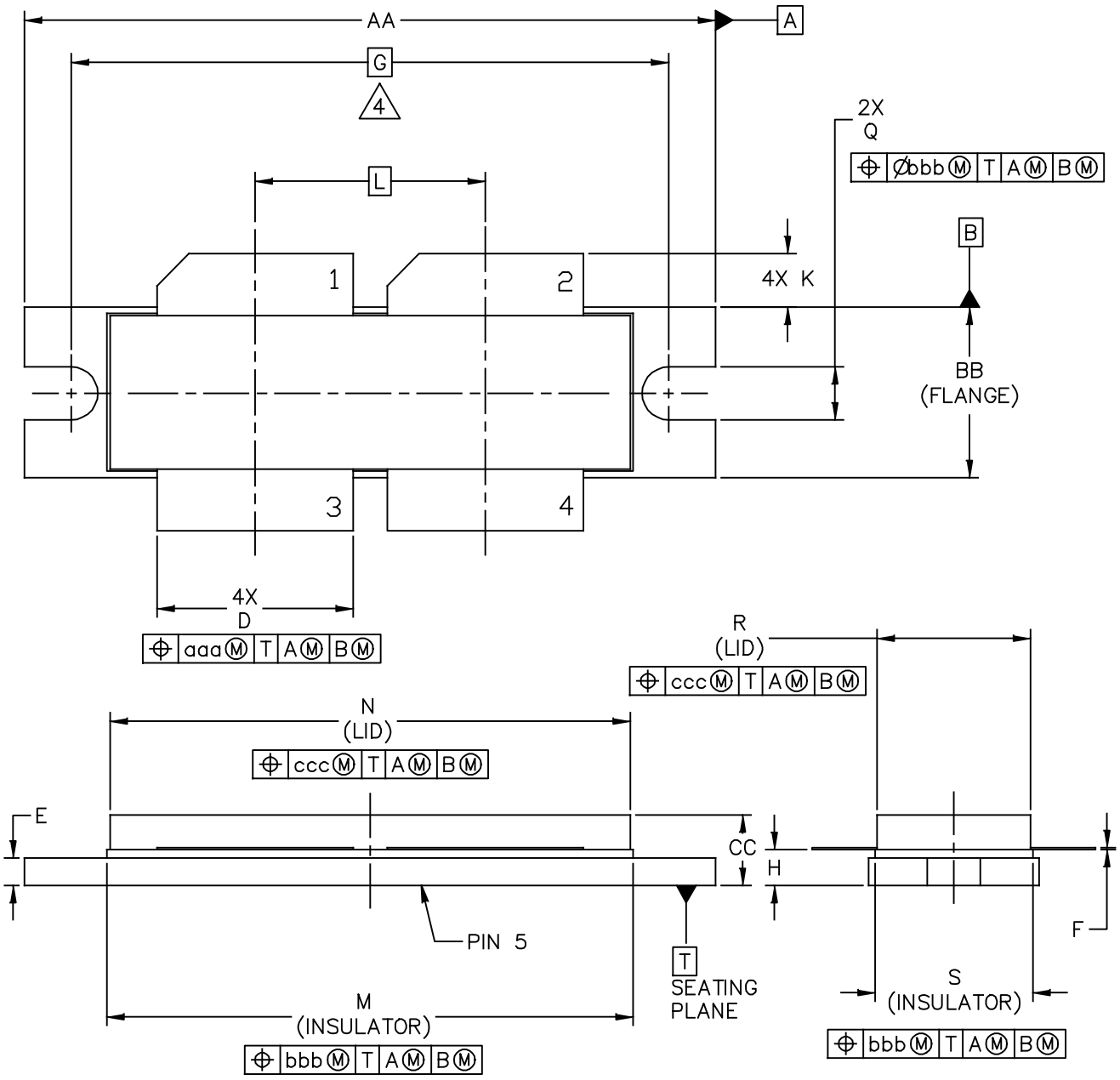


Figure 12. Source and Load Impedances Optimized for IRL, Power and Efficiency — Push-Pull

PACKAGE DIMENSIONS



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NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH
3. DIMENSION H IS MEASURED .030 INCH (0.762 MM) AWAY FROM PACKAGE BODY.
4. RECOMMENDED BOLT CENTER DIMENSION OF 1.52 INCH (38.61 MM) BASED ON M3 SCREW.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	1.615	1.625	41.02	41.28	N	1.218	1.242	30.94	31.55
BB	.395	.405	10.03	10.29	Q	.120	.130	3.05	3.30
CC	.170	.190	4.32	4.83	R	.355	.365	9.02	9.27
D	.455	.465	11.56	11.81	S	.365	.375	9.27	9.53
E	.062	.066	1.57	1.68					
F	.004	.007	0.10	0.18					
G	1.400 BSC		35.56 BSC		aaa	.013		0.33	
H	.082	.090	2.08	2.29	bbb	.010		0.25	
K	.117	.137	2.97	3.48	ccc	.020		0.51	
L	.540 BSC		13.72 BSC						
M	1.219	1.241	30.96	31.52					

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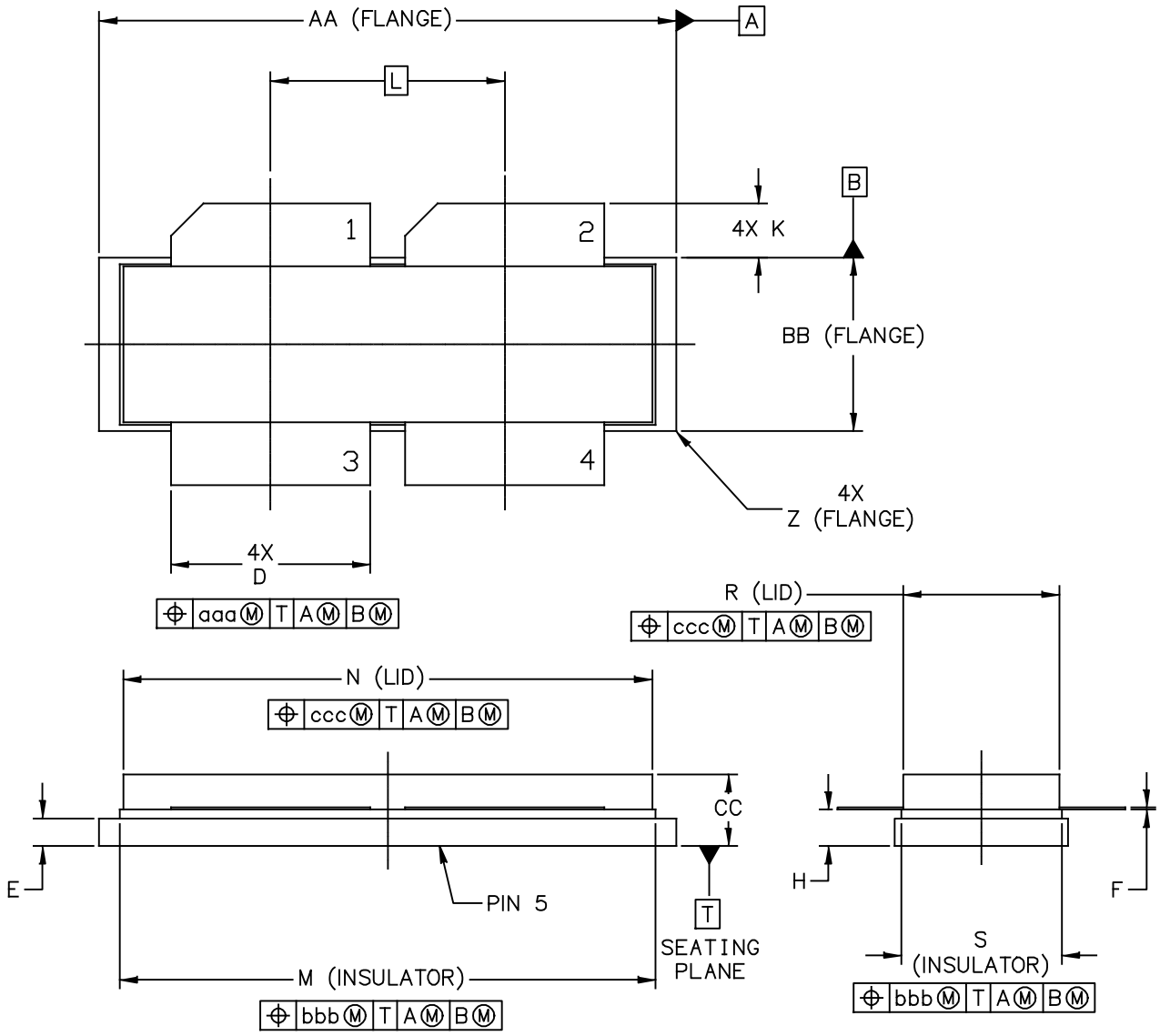

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1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH
3. DIMENSION H IS MEASURED .030 INCH (0.762 MM) AWAY FROM PACKAGE BODY

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
AA	1.265	1.275	32.13	32.39	R	.355	.365	9.02	9.27
BB	.395	.405	10.03	10.29	S	.365	.375	9.27	9.53
CC	.170	.190	4.32	4.83	Z	R.000	R.040	R0.00	R1.02
D	.455	.465	11.56	11.81					
E	.062	.066	1.57	1.68	aaa	.013		0.33	
F	.004	.007	0.10	0.18	bbb	.010		0.25	
H	.082	.090	2.08	2.29	ccc	.020		0.51	
K	.117	.137	2.97	3.48					
L	.540 BSC		13.72 BSC						
M	1.219	1.241	30.96	31.52					
N	1.218	1.242	30.94	31.55					

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PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Dec. 2013	• Initial Release of Data Sheet
1	Aug. 2014	• Application circuit table added and band of operation updated to 1.8–600 MHz to reflect performance of device, p. 1

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