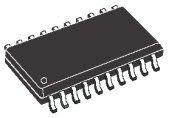
L6376

0.5 A high-side driver quad intelligent power switch

Features

- Multipower BCD technology
- 0.5 A four independent outputs
- 9.5 to 35 V supply voltage range
- Internal current limit
- Non-dissipative over-current protection
- Thermal shutdown
- Under voltage lockout with hysteresys
- Diagnostic output for under voltage, over temperature and over current
- External asynchronous reset input
- Presettable delay for overcurrent
- Diagnostic
- Open ground protection
- Immunity against burst transient (IEC 61000-4-4)
- ESD protection (human body model ± 2 kV)



PowerSO-20

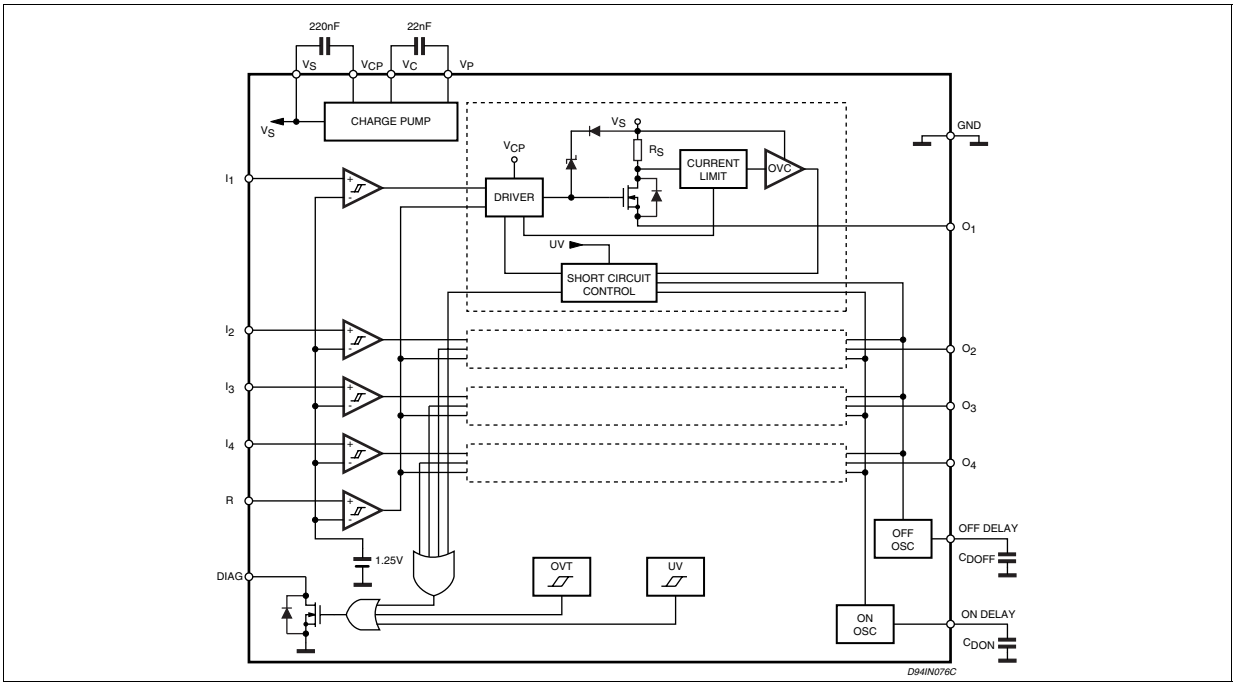
Description

This device is a monolithic quad intelligent power switch in multipower BCD technology, for driving inductive, capacitive or resistive loads. Diagnostic for CPU feedback and extensive use of electrical protections make this device inherently indistructible and suitable for general purpose industrial applications.

Table 1. Device summary

Order codes	Package	Packaging
L6376D	PowerSO-20	Tube
L6376D013TR	PowerSO-20	Tape and reel

Figure 1. Block diagram



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1 Maximum rating

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_s	6	Supply voltage ($t_w \leq 10$ ms)	50	V
		Supply voltage (DC)	40	V
V_s - V_{out}		Difference between supply voltage and output voltage	internally limited	
V_{id}	16, 17	Externally forced voltage	-0.3 to 7	V
I_{id}		Externally forced current	±1	mA
I_i	12, 13, 14, 15, 18	Channel input current (forced)	±2	mA
V_i		Channel input voltage	-0.3 to 40	V
I_{out}	2, 3, 8, 9	Output current (see also I_{sc})	internally limited	
V_{out}		Output voltage	internally limited	
E_{il}		Energy inductive load (T_J =125 °C); each channel	200	mJ
P_{tot}		Power dissipation	internally limited	
V_{diag}	19	External voltage	-0.3 to Vs+0.7	V
I_{diag}		Externally forced current	-10 to 10	mA
T_{op}		Ambient temperature, operating range	-25 to 85	°C
T_J		Junction temperature, operating range (see overtemperature protection)	-25 to 125	°C
T_{stg}		Storage temperature	-55 to 150	°C

2 Pin connections

Figure 2. Pin connections (top view)

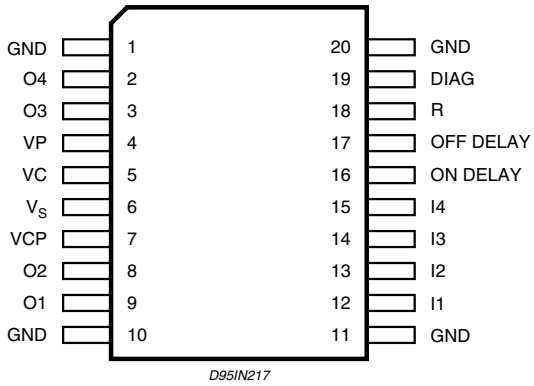


Table 3. Pin description

N#	Pin name	Function
6	V_S	Positive supply voltage. An internal circuit, monitoring the supply voltage, maintains the IC in OFF-state until V_S reaches 9 V or when V_S falls under 8.5 V. The diagnostic is availlable since V_S = 5 V.
7	V_{CP}	Switch driver supply. To minimize the output drop voltage, a supply of about 10 V higher than V_S is required. In order to use the built-in charge pump, connect a filter capacitor from pin1 to pin. The suggested value assures a fast transition and a low supply ripple even in worse condition. Using the four channels contemporarily, values less than 68 nF have to be avoided.
2, 3, 8, 9	O_1, O_2, O_3, O_4	High side outputs. Four independently controlled outputs with built-in current limitation.
1, 10, 11, 20	GND	Ground and power dissipating pins. These pins are connected to the bulk ground of the IC, so are useful for heat dissipation.
12,13, 14, 15	I_1, I_2, I_3, I_4	Control inputs. Four independent control signals. The output is held OFF until the voltage at the corresponding input pin reaches 1.35 V and is turned OFF when the voltage at the pin goes below 1.15 V.
16	ON DELAY	Programmable ON duration in short circuit. If an output is short circuited to ground or carryng a current exceeding the limit, the output is turned OFF and the diagnostic activation are delayed. This procedure allows the driving of hard surge current loads. The delay is programmed connecting a capacitor (50 pF to 15 nF) versus ground with the internal time constant of 1.28 µs/pF. The function can be disabled short circuiting this pin to ground.
17	OFF DELAY	Programmable OFF duration in short circuit. After the short circuit or overcurrent detection, the switch is held OFF before the next attempt to switch on again. The delay is programmed connecting a capacitor (50 pF to 15 nF) versus ground with the internal time constant of 1.28 µs/pF. Short circuiting this pin to ground the OFF delay is 64 times the ON delay.
18	R	Asyncronous reset input. This active low input (with hysteresis), switch off all the outputs independently from the input signal. By default it is biased low.

Table 3. Pin description (continued)

N#	Pin name	Function
19	DIAG	Diagnostic output. This open drain output reports the IC working condition. The bad condition (as undervoltage, overcurrent, overtemperature) turns the output low.
5	V_C	Pump oscillator voltage. At this pin is available the built-in circuitry to supply the switch driver at about 10 V higher than V_S. To use this feature, connect a capacitor across pin 4 and pin 5. The suggested value assures a fast transition and a minimum output drop voltage even in worse condition. Using the four channels contemporarily, values less than 6.8 nF have to be avoided.
4	V_P	Bootstrapped voltage. At this pin is available the 11 V oscillation for the charge pump, at a typical frequency of 200 kHz.

3 Thermal characteristics

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance, junction to ambient (see thermal characteristics)	50	°C/W
R_{thJC}	Thermal resistance junction-case	1.5	°C/W

Note: Additional data on the PowerSO-20 can be found in Application note AN668

4 Electrical characteristics

Table 5. Electrical characteristcs
(V_S = 24 V; T_J = -25 to 125 °C; unless otherwise specified.)

Symbol	Pin#	Parameter	Test condition	Min	Typ	Max	Unit
DC operation							
V_s	6	Supply voltage		9.5	24	35	V
V_{sth}		UV upperthreshold		8.5	9	9.5	V
V_{shys}		UV hysteresis		200	500	800	mV
I_{qsc}		Quiescent current	Outputs ON, no load		3	5	mA
V_{il}	12,13, 14,15, 18	Input low level		0		0.8	V
V_{ih}		Input high level		2		40	V
I_{bias}		Input bias current	V_i = 0 V	-5	-1	0	µA
			V_i = 40 V	0	5	20	µA
V_{ihys}		Input comparators hysteresis		100	200	400	mV
Θ_{lim}		OVT upper threshold			150		°C
Θ_H		Threshold hysteresis			20	30	°C
I_{sc}	2, 3, 8, 9	Short circuit current	V_s = 9.5 to 35 V; R_l = 2 Ω	0.65	0.9	1.2	A
		Output voltage drop	I_{out} = 500 mA; T_J = 25 °C		320	500	mV
			I_{out} = 500 mA; T_J = 125 °C		460	640	mV
I_{olk}		Output leakage current	V_o = 0 V; V_i < 0.8 V			100	µA
V_{cl}		Internal voltage clamp (V_s-V_o each output)	I_o = 100 mA single pulsed T_p = 300 µs	47	52	57	V
V_{ol}		Low state output voltage	V_i = V_{il}; R_L = ∞		0.8	1.5	V
I_{dlkg}	19	Diagnostic output leakage	Diagnostic off			25	µA
V_{diag}		Diagnostic output voltage drop	I_{diag} = 5 mA			1.5	V
I_{dch}	16, 17	Delay capacitors charge current			40		µA

Table 5. Electrical characteristcs (continued)
(V_S = 24 V; T_J = -25 to 125 °C; unless otherwise specified.)

Symbol	Pin#	Parameter	Test condition	Min	Typ	Max	Unit
AC operation							
t_r -t_f	2, 3, 8, 9	Rise or fall time	V_s = 24 V; R_l = 47 Ω R_l to ground		3.8		µs
t_d	12 vs 9 13 vs 8 14 vs 3 15 vs 2	Delay time			1		µs
dV/dt	2, 3, 8, 9	Slew rate (Rise and fall edge)	V_s = 24 V; R_l = 47 Ω R_l to ground Rise Fall	 3 4	 5 7.6	 7 10	 V/µs V/µs
t_{ON}	16	On time during short circuit condition	50 pF < C_{DON} < 15 nF		1.28		µs/pF
t_{OFF}	17	Off time during short circuit condition	pin 13 grounded		64		t_{ON}
			50 pF < C_{DOFF}< 15 nF		1.28		µs/pF
f_{max}		Maximum operating frequency			25		kHz
Source drain ndmos diode							
V_{fsd}		Forward on voltage	I_{fsd} = 500 mA		1	1.5	V
I_{fp}		Forward peak current	tp = 10 ms; duty cycle = 20 %			1.5	A
t_{rr}		Reverse recovery time	I_{fsd} = 500 mA; dI_{fsd}/dt = 25 A/ms		200		ns
t_{fr}		Forward recovery time			50		ns

Figure 3. Undervoltage comparator hysteresis

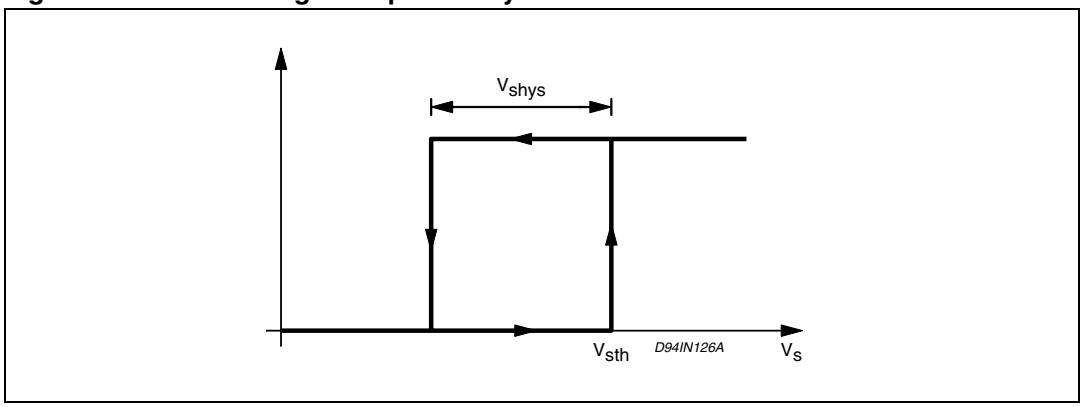
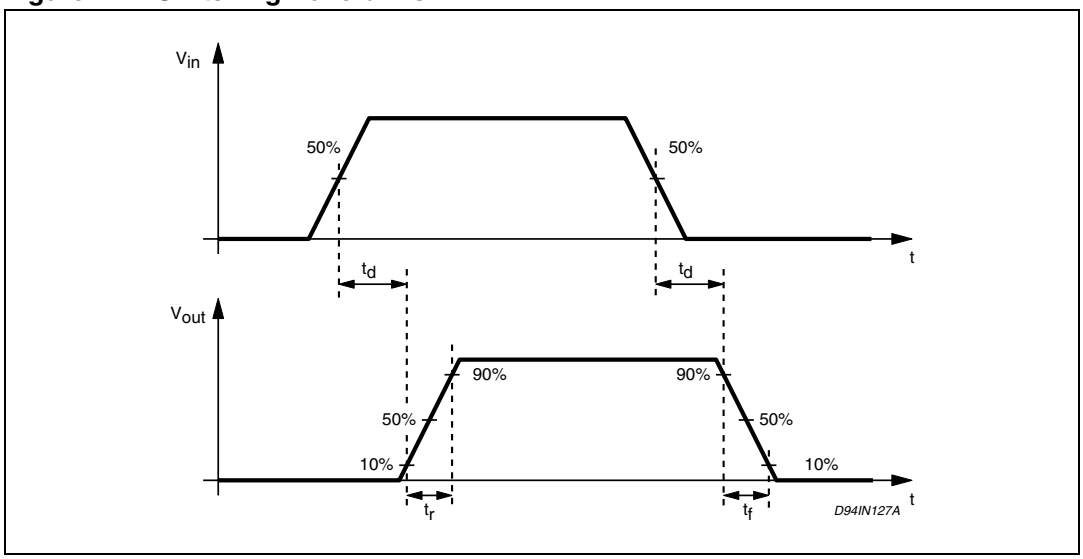


Figure 4. Switching waveforms



5 Overtemperature protection (OVT)

If the chip temperature exceeds Θlim (measured in a central position in the chip) the chip deactivates itself.

The following actions are taken:

- all the output stages are switched off;
- the signal DIAG is activated (active low).

Normal operation is resumed as soon as (typically after some seconds) the chip temperature monitored goes back below Θ_{lim}-Θ_H.

The different thresholds with hysteretic behavior assure that no intermittent conditions can be generated.

6 Undervoltage protection (UV)

The supply voltage is expected to range from 9.5 V to 35 V, even if its reference value is considered to be 24 V. In this range the device operates correctly. Below 9.5 V the overall system has to be considered not reliable. Consequently the supply voltage is monitored continuously and a signal, called UV, is internally generated and used.

The signal is “on” as long as the supply voltage does not reach the upper internal threshold of the Vs comparator V_{sth}. The UV signal disappears above V_{sth}.

Once the UV signal has been removed, the supply voltage must decrease below the lower threshold (i.e. V_{sth}-V_{shys}) before it is turned on again.

The hysteresis V_{shys} is provided to prevent intermittent operation of the device at low supply voltages that may have a superimposed ripple around the average value.

The UV signal switches off the outputs, but has no effect on the creation of the reference voltages for the internal comparators, nor on the continuous operation of the charge-pump circuits.

7 Diagnostic logic

The situations that are monitored and signalled with the DIAG output pin are:

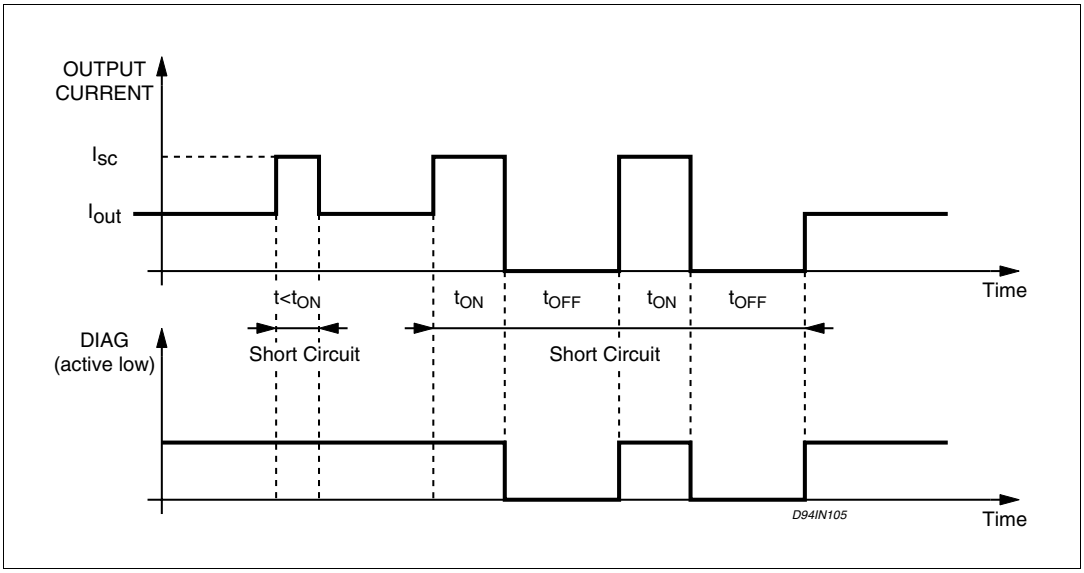
- current limit (OVC) in action; there are 4 individual current limiting circuits, one per each output; they limit the current that can be sunk from each output, to a typical value of 800 mA, equal for all of them;
- under voltage (UV);
- over temperature protection (OVT).

The diagnostic signal is transmitted via an open drain output (for ease of wired-or connection of several such signals) and a low level represents the presence of at least one of the monitored conditions, mentioned above.

8 Short circuit operation

In order to allow normal operation of the other inputs when one channel is in short cirtuit, an innovative non dissipative over current protection (patent pending) is implemented in the device.

Figure 5. Short circuit operation waveforms



In this way, the temperature of the device is kept enough low to prevent the intervention of the thermal protection (in most of the cases) and so to avoid the shut down of the whole device.

If a short circuit condition is present on one output, the current limiting circuit puts that channel in linear mode — sourcing the ISC current (typically 800 mA) — for a time period (t_{ON}) defined by an external capacitor (C_{DON} connected to the ON DELAY pin).

After that period, if the short circuit condition is still present the output is turned off for another time period (t_{OFF}) defined by a second external capacitor (C_{DOFF} connected to the OFF DELAY pin).

When also this period is expired:

- if the short circuit condition is still present the output stays on for the tON period and the sequence starts again;
- if the short circuit condition is not present anymore the normal operation of the output is resumed.

The t_{ON} and t_{OFF} periods are completely independent and can be set from 64 µs to 15 µs, using external capacitors ranging from 50 pF to 15 nF (1.28 µs/pF).

If the OFF DELAY pin is tied to ground (i.e. the C_{DOFF} capacitor is not used) the t_{OFF} time period is 64 times the t_{ON} period.

The diagnostic output (DIAG) is active when the output is switched off, while it is not active when the output is on (i.e. during the t_{ON} period) even if in that period a short circuit condition is present.

Typical waveforms for short circuit operation are shown in *Figure 5*.

If both the ON DELAY and the OFF DELAY pins are grounded the non dissipative over current protection is inhibited and the outputs in short circuit remain on until the thermal shutdown switch OFF the whole device. In this case the short circuit condition is not signalled by the DIAG pin (that continues to signal the under voltage and over temperature conditions).

9 Programmable diagnostic delay

The current limiting circuits can be requested to perform even in absence of a real fault condition, for a short period, if the load is of capacitive nature or if it is a filament lamp (that exhibits a very low resistance during the initial heating phase).

To avoid the forwarding of misleading — i.e. short diagnostic pulses in coincidence with the intervention of the current limiting circuits when operating on capacitive loads — the activation of the diagnostic can be delayed with respect to the intervention of one of the current limiting circuits.

This delay can be defined by an external capacitor (C_{DON}) connected between the ON DELAY pin and ground.

10 Reset input

An external reset input R (pin 18) is provided to simultaneously switch OFF all the outputs: this signal (active low) is in effect an asynchronous reset that keeps the outputs low independently from the input signals. For example, this reset input can be used by the CPU to keep the outputs low after a fault condition (signaled by the DIAG pin).

11 Demagnetization of inductive loads

The device has four internal clamping diodes able to demagnetize inductive loads.

The limitation is the peak power dissipation of the packages, so — if the loads are big or if there is the possibility to demagnetize more loads contemporarly — it is necessary to use external demagnetization circuits.

In *Figure 7* and *Figure 8* are shown two topologies for the demagnetization versus ground and versus V_S.

The breakdown voltage of the external device (V_Z) must be chosen considering the minimum internal clamping voltage (V_{cl}) and the maximum supply voltage (V_S).

Figure 6. Input comparator hysteresis

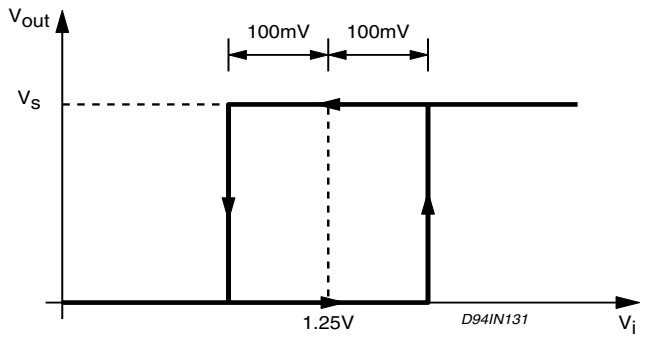


Figure 7. External demagnetization circuit (versus ground)

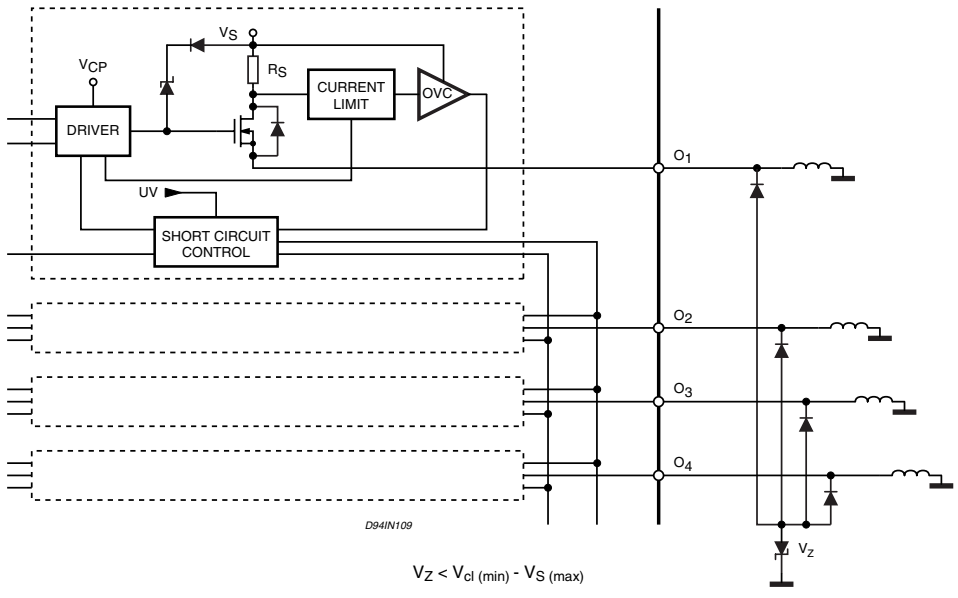
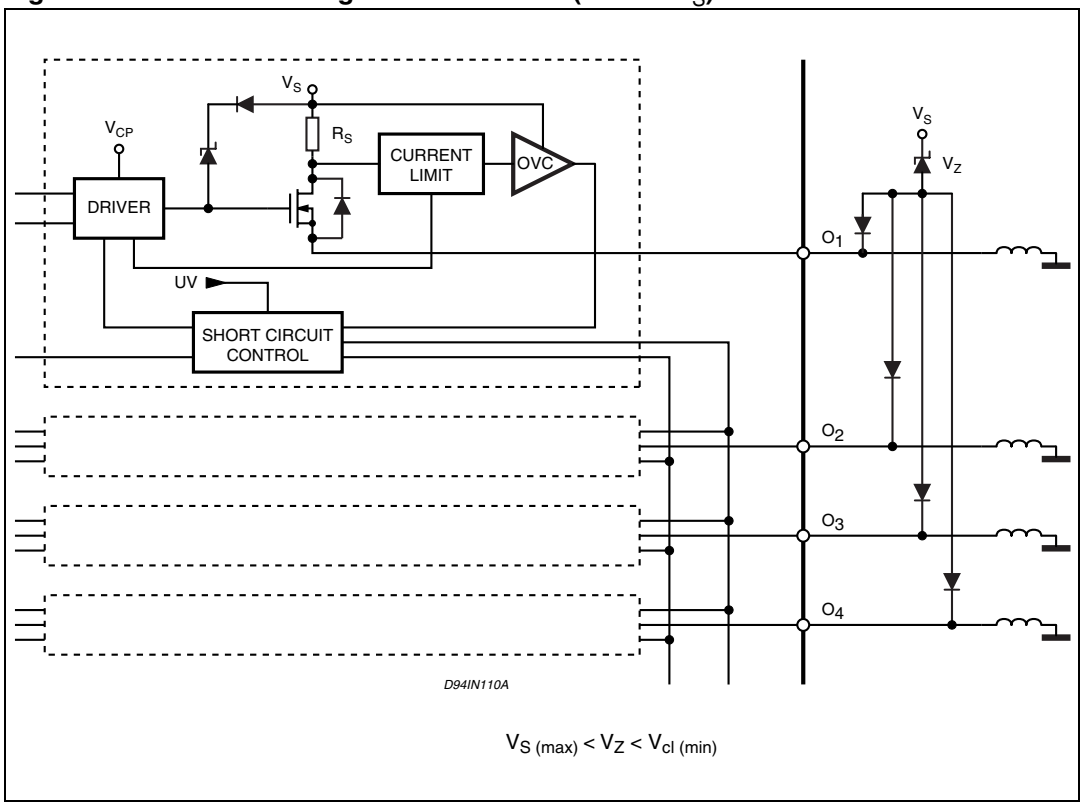


Figure 8. External demagnetization circuit (versus V_S)



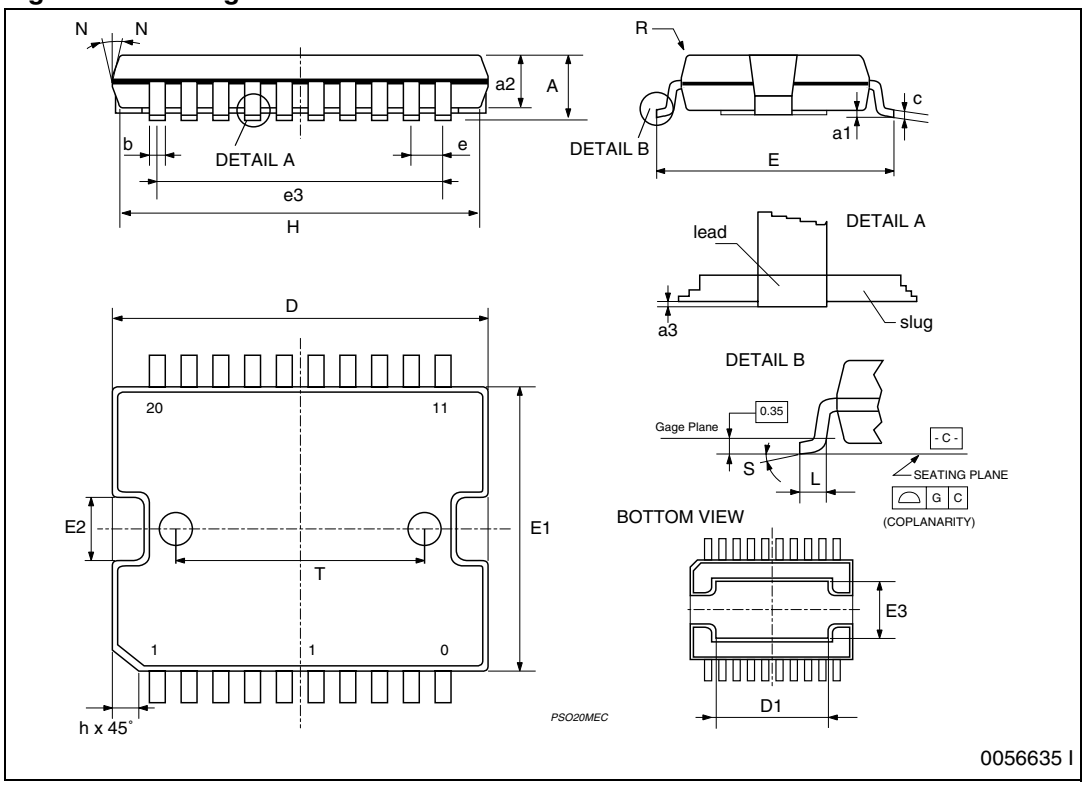
12 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 6. PowerSO-20 mechanical data

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1 (2)	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	8°(typ.)					
S	8°(max.)					
T		10			0.394	

Figure 9. Package dimensions



13 Revision history

Table 7. Document revision history

Date	Revision	Changes
September 2003	5	First issue in EDOCS dms.
03-Mar-2008	6	Modified: Removed obsolete package DIP-20

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