

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

#### description

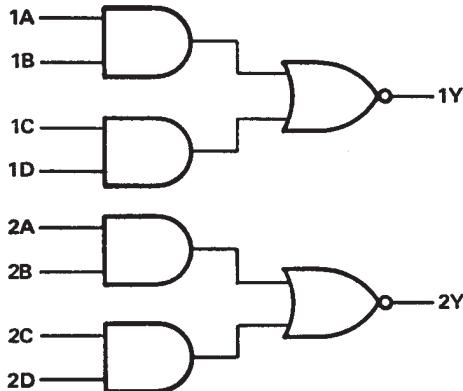
The '51 and 'S51 contain two independent 2-wide 2-input AND-OR-INVERT gates. They perform the Boolean function  $Y = AB + CD$ .

The 'LS51 contains one 2-wide 3-input and one 2-wide 2-input AND-OR-INVERT gates. They perform the Boolean functions  $1Y = (\overline{1A} \cdot \overline{1B} \cdot \overline{1C}) + (\overline{1D} \cdot \overline{1E} \cdot \overline{1F})$  and  $2Y = (\overline{2A} \cdot \overline{2B}) + (\overline{2C} \cdot \overline{2D})$ .

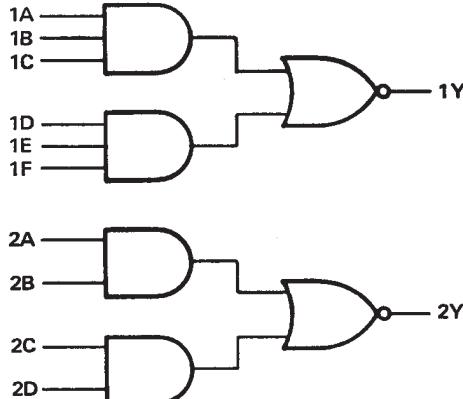
The SN5451, SN54LS51, and SN54S51 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7451, SN74LS51 and SN74S51 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

#### logic diagrams

'51, 'S51

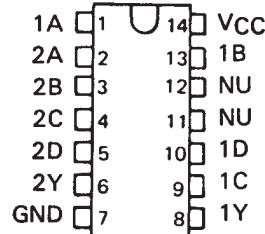


'LS51



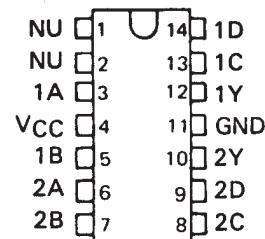
SN5451 . . . J PACKAGE  
 SN54S51 . . . J OR W PACKAGE  
 SN7451 . . . N PACKAGE  
 SN74S51 . . . D OR N PACKAGE

(TOP VIEW)



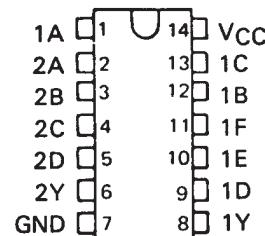
SN5451 . . . W PACKAGE

(TOP VIEW)



SN54LS51 . . . J OR W PACKAGE  
 SN74LS51 . . . D OR N PACKAGE

(TOP VIEW)



NC - No internal connection

NU - Make no external connection

SN5451, SN54LS51, SN54S51

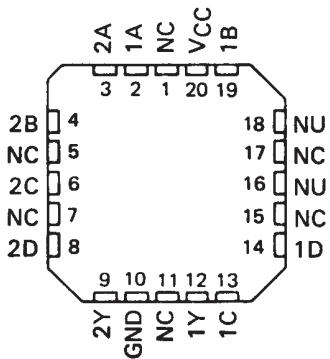
SN7451, SN74LS51, SN74S51

## AND-OR-INVERT GATES

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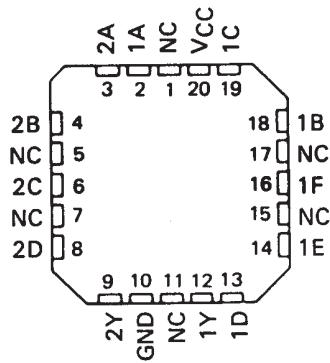
### SN54S51 . . . FK PACKAGE

(TOP VIEW)



### SN54LS51 . . . FK PACKAGE

(TOP VIEW)

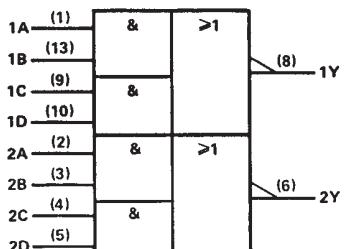


NC - No internal connection

NU - Make no external connection

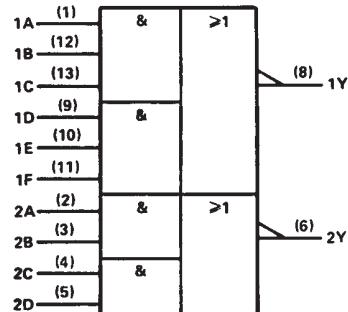
### logic symbols<sup>†</sup>

'51, 'S51



positive logic:  $Y = \overline{AB + CD}$

'LS51



positive logic:

$$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$$

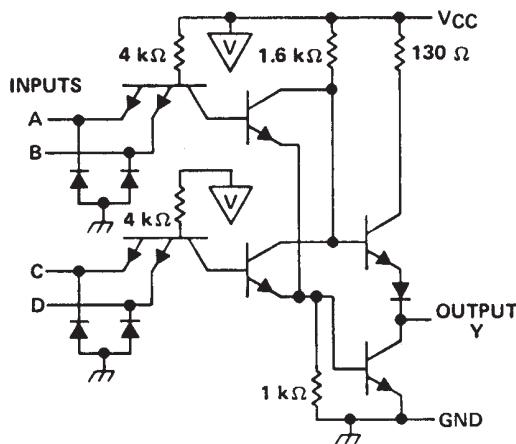
$$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$$

<sup>†</sup>These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

### schematics

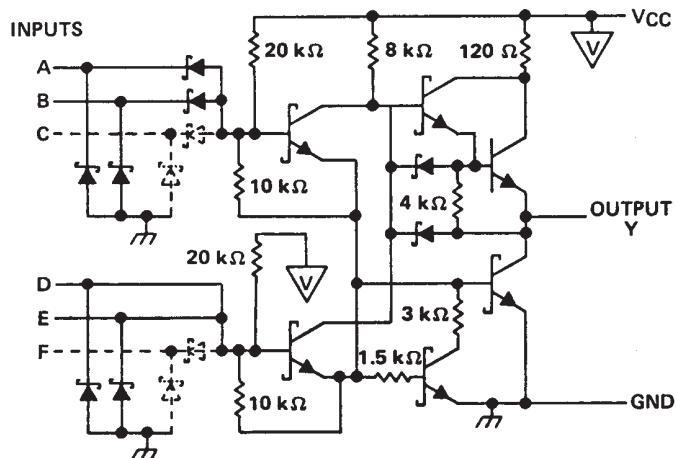
'51



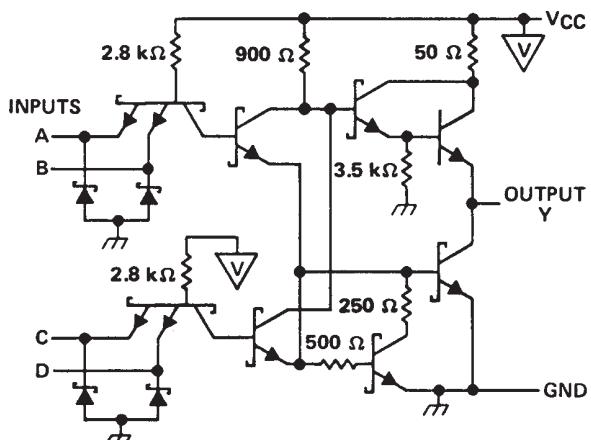
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'LS51



'S51



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, V <sub>CC</sub> (See Note 1): '51, 'LS51, 'S51	7 V
Input voltage: '51, 'S51	5.5 V
'LS51	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

SN5451, SN54LS51, SN54S51

SN7451, SN74LS51, SN74S51

## AND-OR-INVERT GATES

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### recommended operating conditions

		SN5451			SN7451			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{OH}$	High-level output current			-0.4			-0.4	mA
$I_{OL}$	Low-level output current			16			16	mA
$T_A$	Operating free-air temperature	-55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN5451			SN7451			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$			-1.5			-1.5	V
$V_{OH}$	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
$V_{OL}$	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
$I_I$	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$	$V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$			40			40	μA
$I_{IL}$	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS\$}$	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
$I_{CCH}$	$V_{CC} = \text{MAX}$ , $V_I = 0 \text{ V}$		4	8		4	8	mA
$I_{CCL}$	$V_{CC} = \text{MAX}$ , See Note 2		7.4	14		7.4	14	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>§</sup> Not more than one output should be shorted at a time.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Any	Y	$R_L = 400 \Omega$ , $C_L = 15 \text{ pF}$	13	22		ns
$t_{PHL}$				8	15		

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54LS51			SN74LS51			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			-0.4			-0.4	mA
$I_{OL}$	Low-level output current			4			8	mA
$T_A$	Operating free-air temperature	-55		125	0		70	$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54LS51			SN74LS51			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}$ , $I_I = -18 \text{ mA}$			-1.5			-1.5	V
$V_{OH}$	$V_{CC} = \text{MIN}$ , $V_{IL} = \text{MAX}$ , $I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
$V_{OL}$	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $I_{OL} = 4 \text{ mA}$		0.25	0.4	0.25	0.4		V
	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $I_{OL} = 8 \text{ mA}$				0.35	0.5		
$I_I$	$V_{CC} = \text{MAX}$ , $V_I = 7 \text{ V}$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = \text{MAX}$ , $V_I = 2.7 \text{ V}$			20			20	$\mu\text{A}$
$I_{IL}$	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS\$}$	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
$I_{CCH}$	$V_{CC} = \text{MAX}$ , $V_I = 0 \text{ V}$		0.8	1.6	0.8	1.6		mA
$I_{CCL}$	$V_{CC} = \text{MAX}$ , See Note 2		1.4	2.8	1.4	2.8		mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$  (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Any	Y	$R_L = 2 \text{ k}\Omega$ , $C_L = 15 \text{ pF}$	12	20		ns
				12.5	20		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN5451, SN54LS51, SN54S51

SN7451, SN74LS51, SN74S51

## AND-OR-INVERT GATES

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### recommended operating conditions

		SN54S51			SN74S51			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{OH}$	High-level output current			-1			-1	mA
$I_{OL}$	Low-level output current			20			20	mA
$T_A$	Operating free-air temperature	-55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54S51			SN74S51			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}$ , $I_I = -18 \text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
$V_{OL}$	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $I_{OL} = 20 \text{ mA}$			0.5			0.5	V
$I_I$	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$	$V_{CC} = \text{MAX}$ , $V_I = 2.7 \text{ V}$			50			50	μA
$I_{IL}$	$V_{CC} = \text{MAX}$ , $V_I = 0.5 \text{ V}$			-2			-2	mA
$I_{OS\$}$	$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
$I_{CCH}$	$V_{CC} = \text{MAX}$ , $V_I = 0 \text{ V}$		8.2	17.8		8.2	17.8	mA
$I_{CCL}$	$V_{CC} = \text{MAX}$ , See Note 2		13.6	22		13.6	22	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Any	Y	$R_L = 280 \Omega$ , $C_L = 15 \text{ pF}$	3.5	5.5		ns
$t_{PHL}$				3.5	5.5		ns
$t_{PLH}$		Y	$R_L = 280 \Omega$ , $C_L = 50 \text{ pF}$	5			ns
$t_{PHL}$				5.5			ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/00502BCA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 00502BCA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
JM38510/07401BCA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 07401BCA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
JM38510/07401BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 07401BDA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
JM38510/30401BCA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30401BCA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
JM38510/30401BCA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30401BCA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
M38510/00502BCA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 00502BCA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
M38510/00502BCA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 00502BCA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
M38510/07401BCA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 07401BCA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
M38510/07401BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 07401BDA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
M38510/30401BCA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30401BCA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
M38510/30401BCA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30401BCA	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN5451J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SN5451J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN5451J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SN5451J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN54LS51J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SN54LS51J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN54LS51J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SN54LS51J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN54S51J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SN54S51J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS51D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS51	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS51D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS51	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS51DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS51	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS51DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS51	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS51N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS51N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS51N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS51N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS51NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS51	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LS51NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS51	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74S51D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	S51	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74S51D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	S51	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74S51N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74S51N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74S51N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74S51N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ5451J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SNJ5451J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ5451J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SNJ5451J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ5451W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ5451W	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ5451W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ5451W	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54LS51J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS51J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54LS51J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS51J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54LS51W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ54LS51W	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54LS51W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ54LS51W	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54S51FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S51FK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54S51J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S51J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS51, SN54S51, SN74LS51, SN74S51 :**

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- Catalog: [SN74LS51](#), [SN74S51](#)

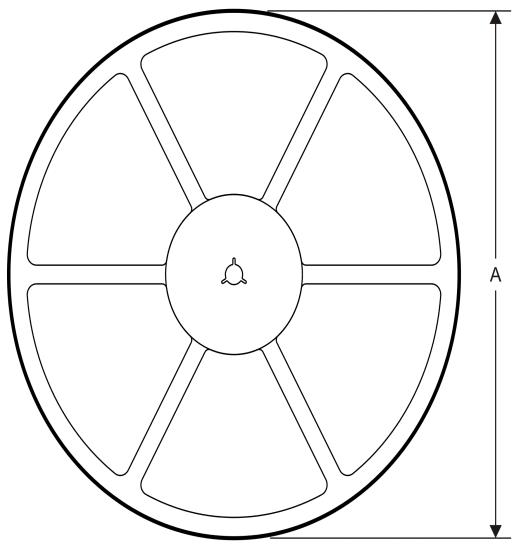
- Military: [SN54LS51](#), [SN54S51](#)

NOTE: Qualified Version Definitions:

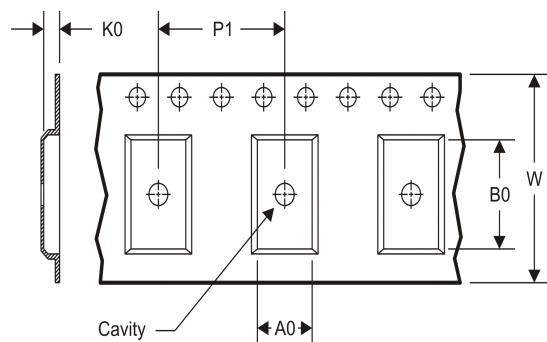
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

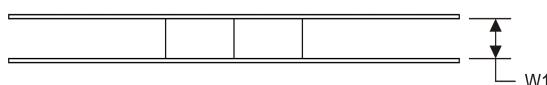
### REEL DIMENSIONS



### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



### TAPE AND REEL INFORMATION

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS51DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS51NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

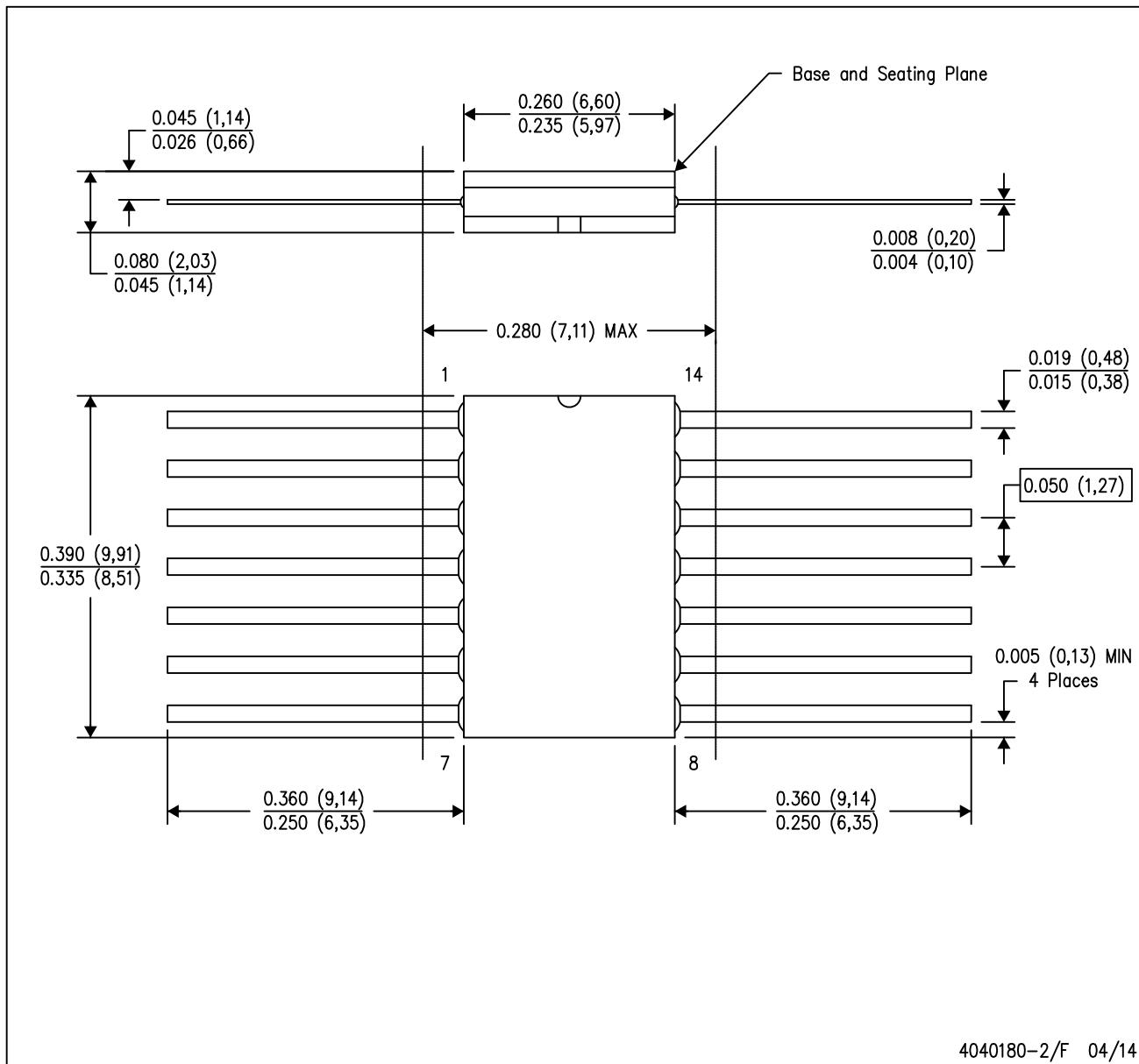
**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS51DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LS51NSR	SO	NS	14	2000	367.0	367.0	38.0

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

NOTES:

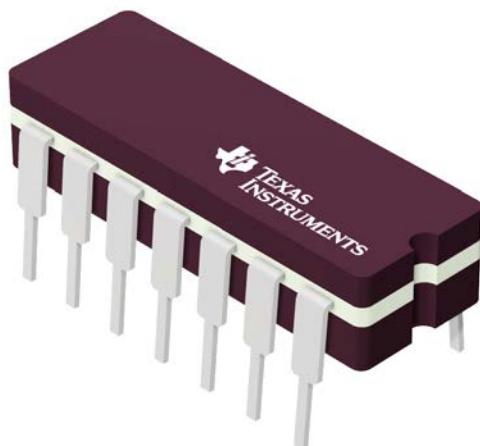
- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL-STD 1835 GDFP1-F14

# GENERIC PACKAGE VIEW

**J 14**

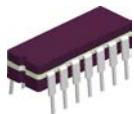
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

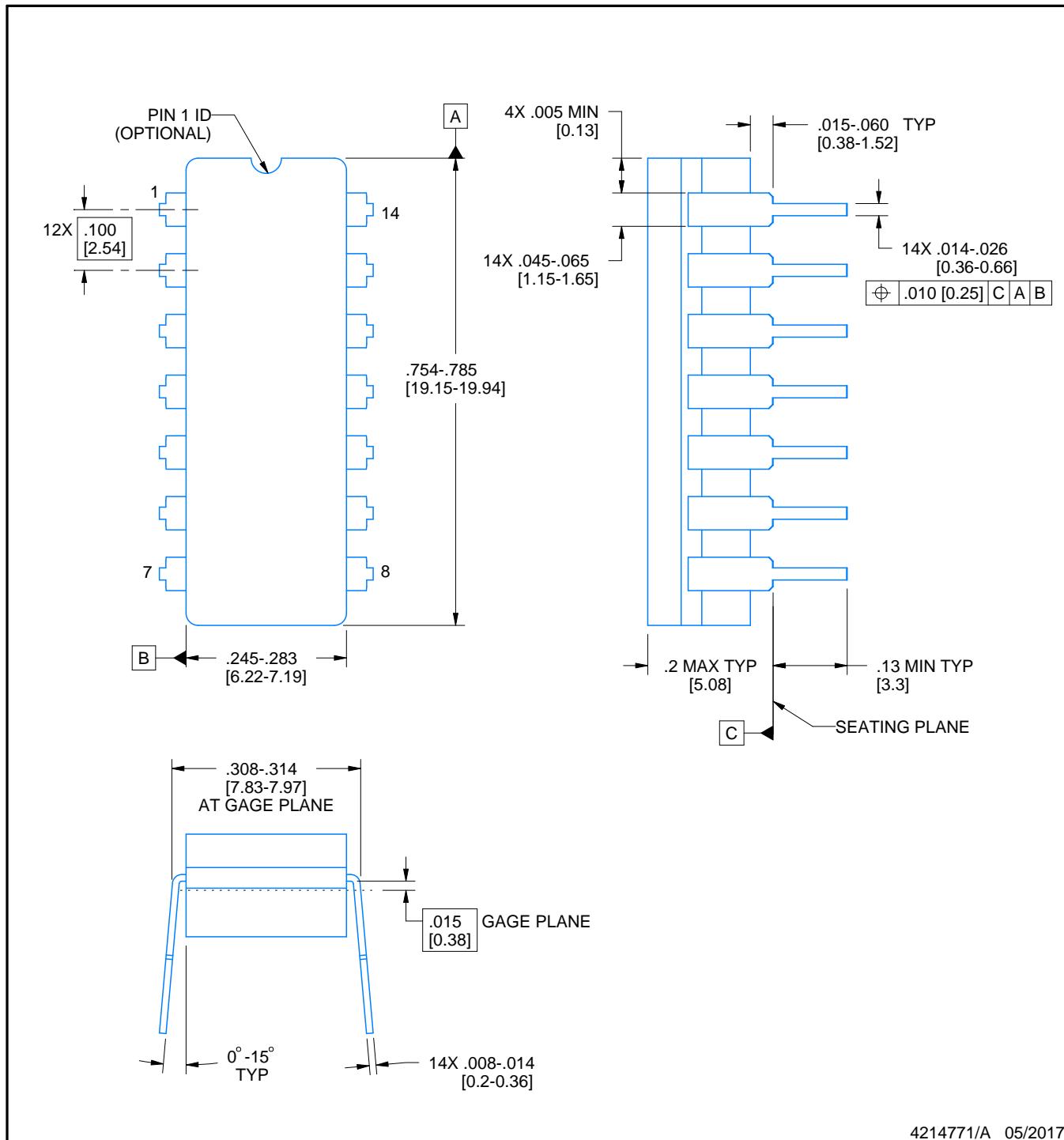


# PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

## NOTES:

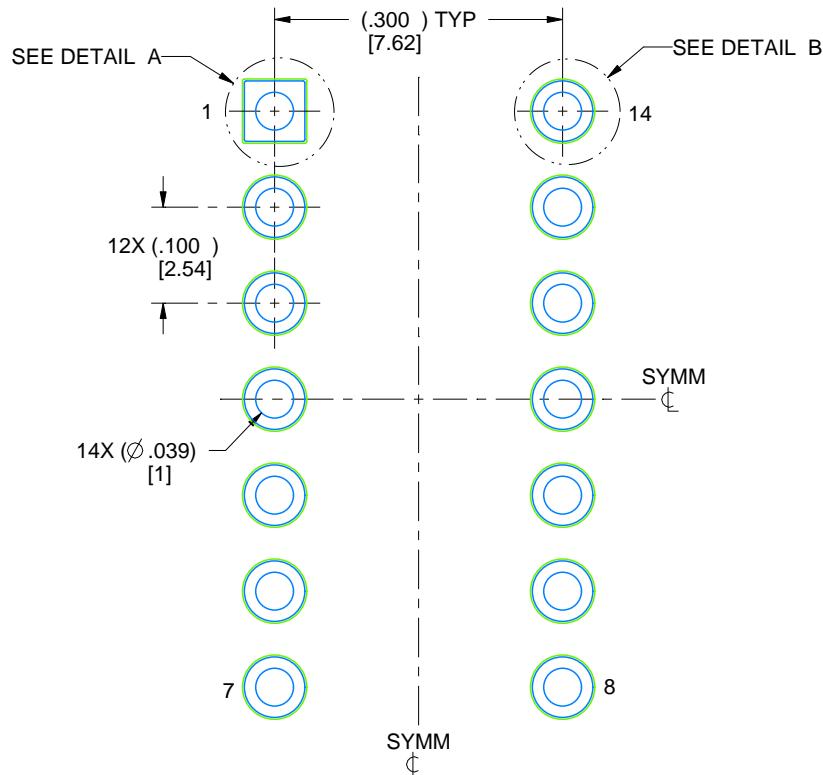
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

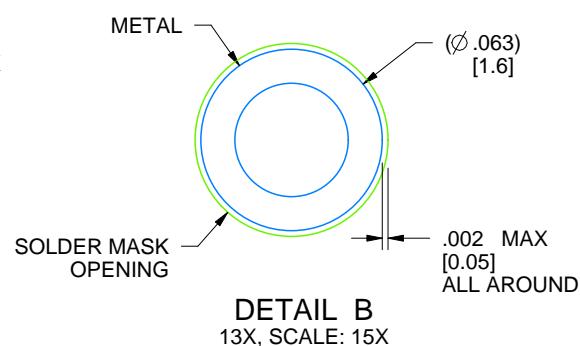
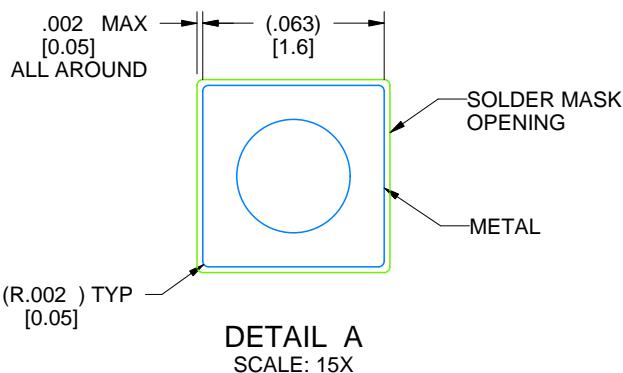
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



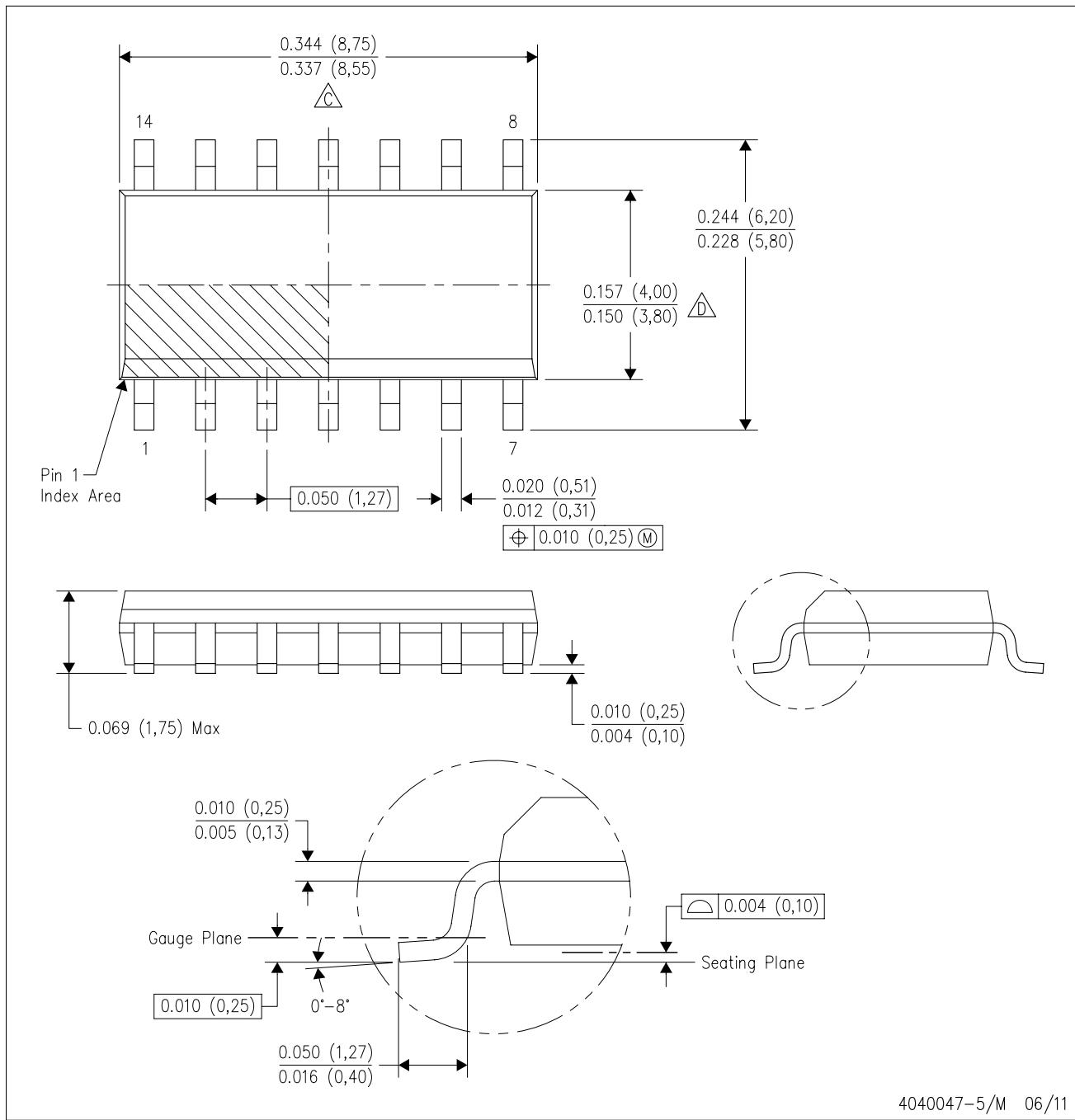
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

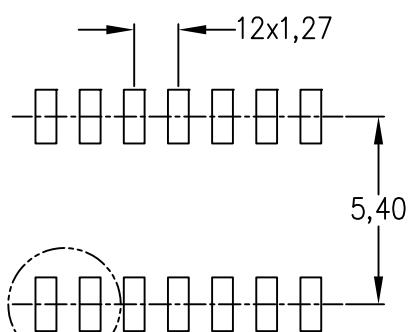
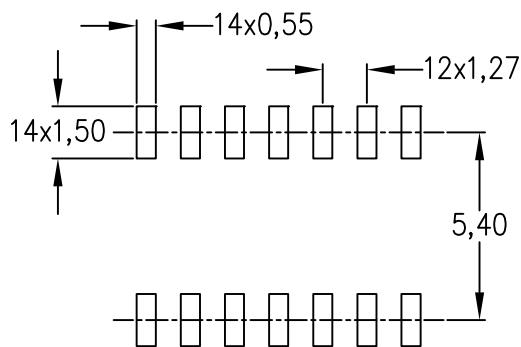
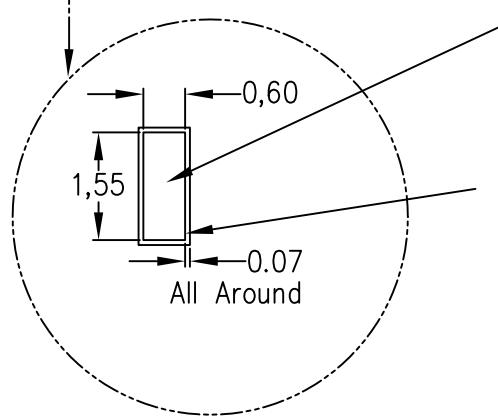
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

4211283-3/E 08/12

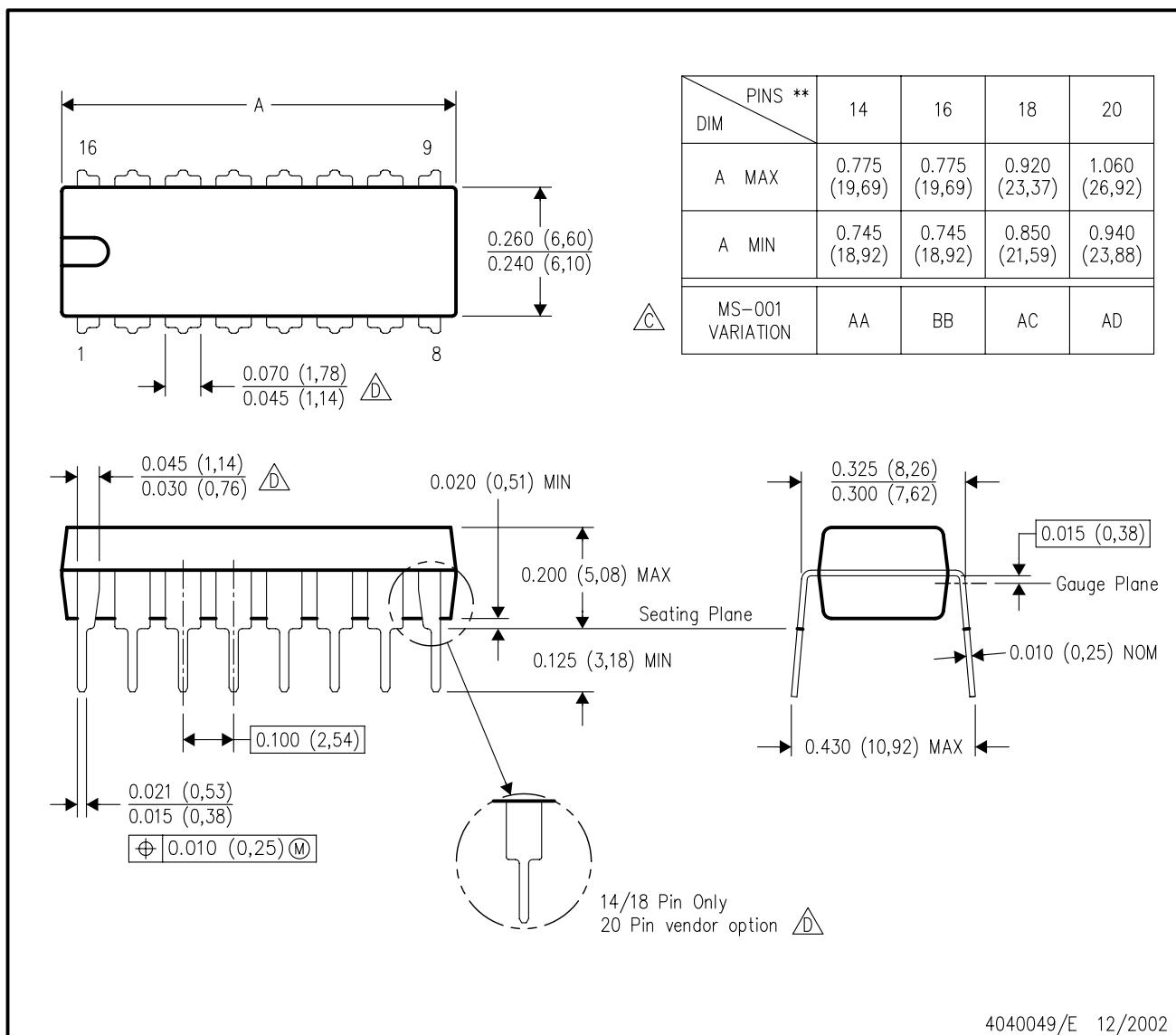
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

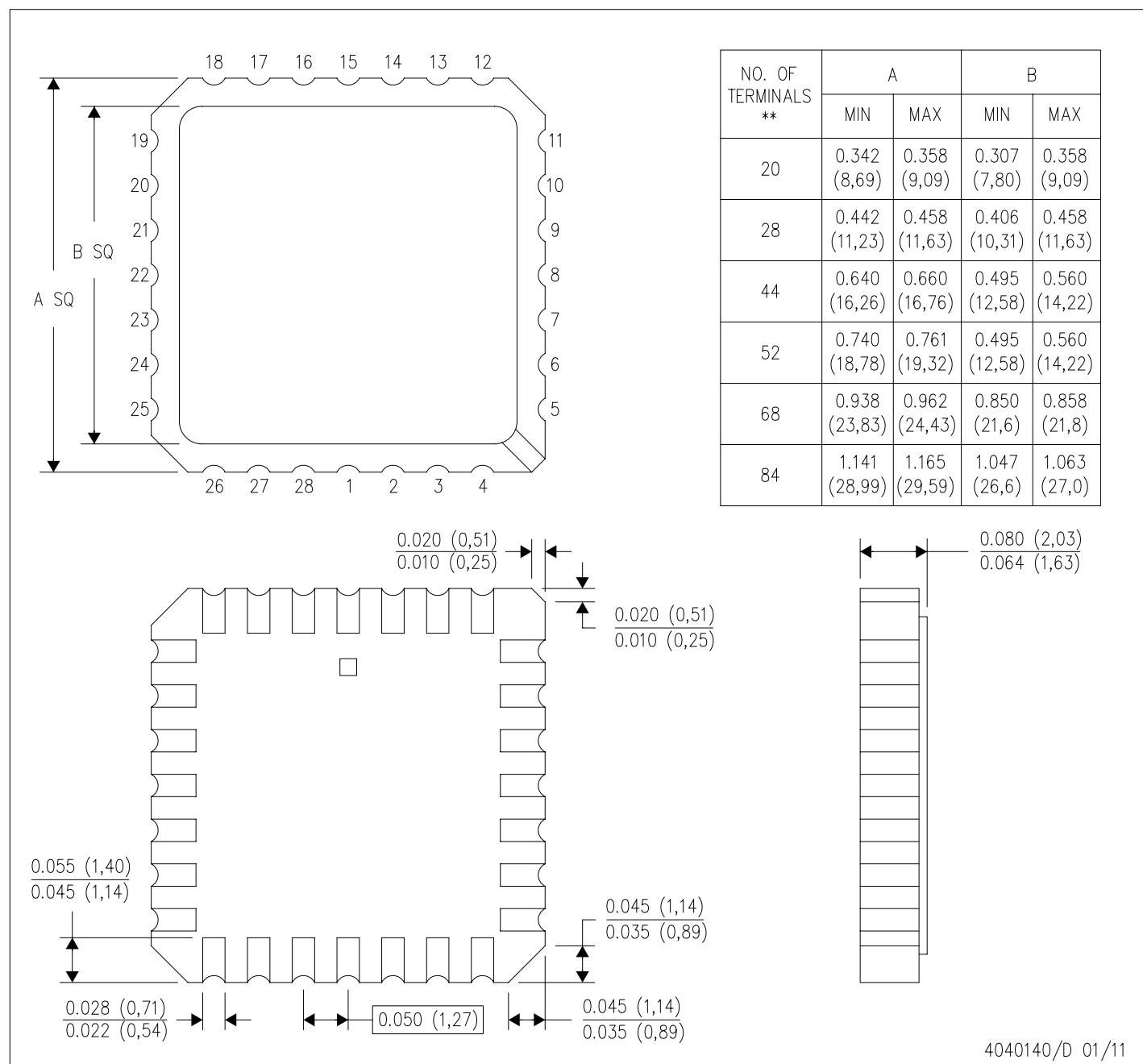
△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a metal lid.  
 D. Falls within JEDEC MS-004

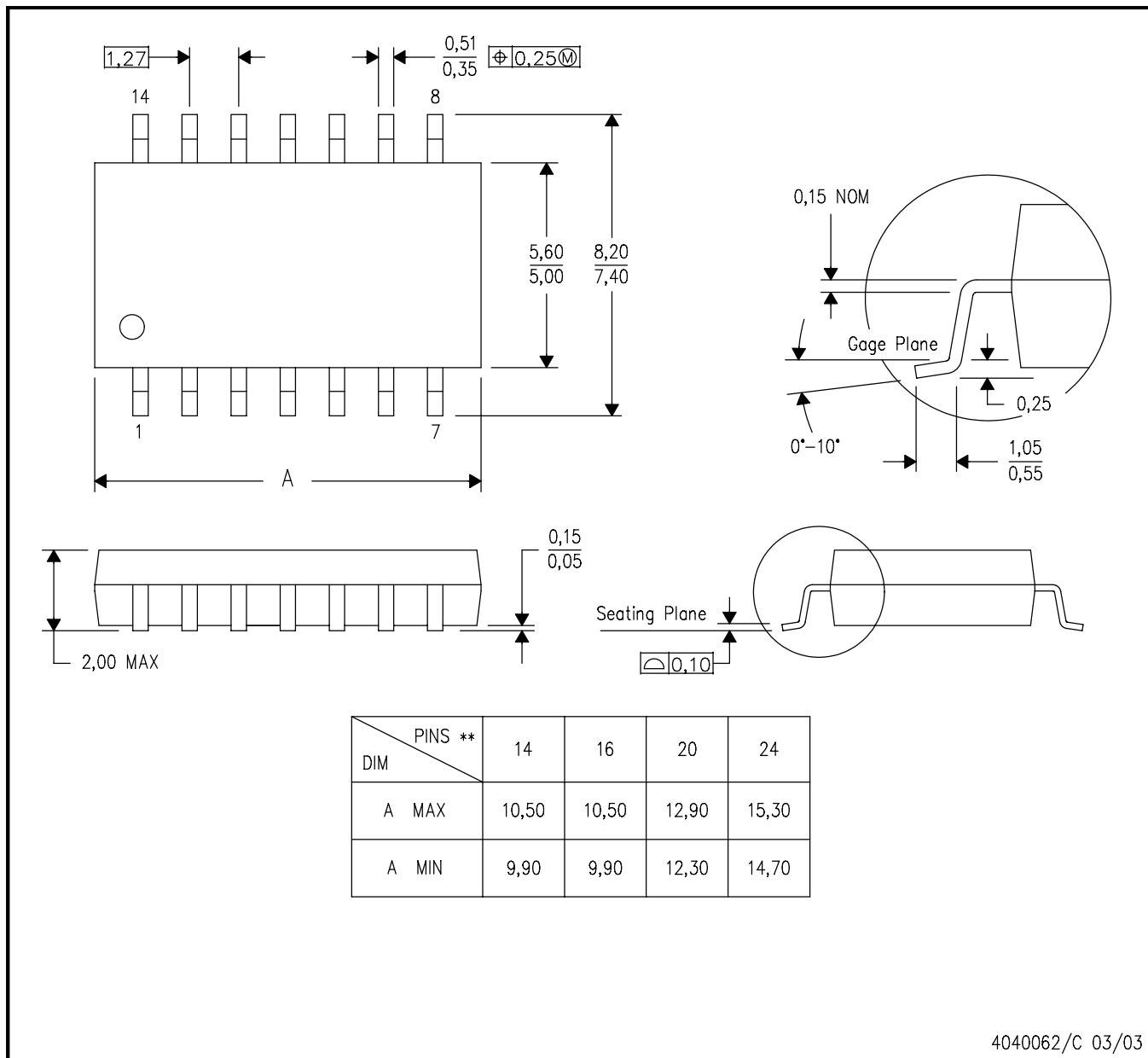
4040140/D 01/11

## MECHANICAL DATA

## NS (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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