19-3971; Rev 2; 10/07

EVALUATION KIT AVAILABLE

6A, 2MHz Step-Down Regulator with Integrated Switches

MAX8646

General Description

The MAX8646 high-efficiency switching regulator delivers up to 6A load current at output voltages from 0.6V to 0.9 x V_{IN}. The IC operates from 2.35V to 3.6V, making it ideal for on-board point-of-load and postregulation applications. Total output error is less than ±1% over load, line, and temperature ranges.

The MAX8646 features fixed-frequency PWM mode operation with a switching frequency range of 500kHz to 2MHz set by an external resistor. High-frequency operation allows for an all-ceramic capacitor design. The high operating frequency also allows for small-size external components.

The low-resistance on-chip nMOS switches ensure high efficiency at heavy loads while minimizing critical inductances, making the layout a much simpler task with respect to discrete solutions. Following a simple layout and footprint ensures first-pass success in new designs.

The MAX8646 comes with a high bandwidth (> 14MHz) voltage-error amplifier. The voltage-mode control architecture and the voltage-error amplifier permit a type III compensation scheme to be utilized to achieve maximum loop bandwidth, up to 20% of the switching frequency. High loop bandwidth provides fast transient response, resulting in less required output capacitance and allowing for all-ceramic-capacitor designs.

The MAX8646 provides two tri-state logic inputs to select one of nine preset output voltages. The preset output voltages allow customers to achieve ±1% output-voltage accuracy without using expensive 0.1% resistors. In addition, the output voltage can be set to any customer value by either using two external resistors at the feedback with 0.6V internal reference or applying an external reference voltage to the REFIN input. The MAX8646 offers programmable soft-start time using one capacitor to reduce input inrush current. The MAX8646 is available in a lead-free, 24-pin, 4mm x 4mm, thin QFN package.

Applications

POLs
ASIC/CPU/DSP Core and I/O Voltages
DDR Power Supplies
Base-Station Power Supplies
Telecom and Networking Power Supplies
RAID Control Power Supplies

Pin Configuration appears at end of data sheet.

Features

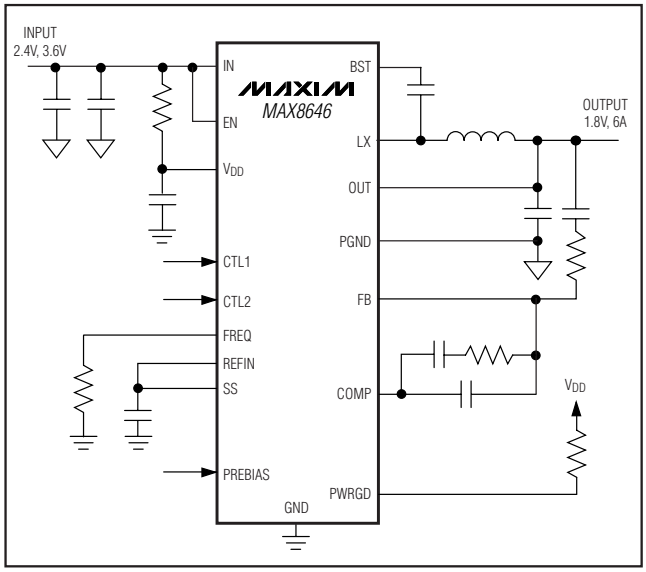
- **Internal 23mΩ $R_{DS(ON)}$ MOSFETs**
- **Continuous 6A Output Current**
- **±1% Output Accuracy over Load, Line, and Temperature**
- **Operates from 2.35V to 3.6V Supply**
- **Adjustable Output from 0.6V to (0.9 x V_{IN})**
- **Soft-Start Reduces Inrush Supply Current**
- **500kHz to 2MHz Adjustable Switching Frequency**
- **Compatible with Ceramic, Polymer, and Electrolytic Output Capacitors**
- **VID-Selectable Output Voltages**
  0.6V, 0.7V, 0.8V, 1.0V, 1.2V, 1.5V, 1.8V, 2.0V, and 2.5V
- **Fully Protected Against Overcurrent and Overtemperature**
- **Safe-Start into Prebiased Output**
- **Sink/Source Current in DDR Applications**
- **Lead-Free, 24-Pin, 4mm x 4mm Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX8646ETG+	-40°C to +85°C	24 Thin QFN-EP* 4mm x 4mm	T2444-4

+Denotes a lead-free package.
**EP = Exposed pad.*

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

6A, 2MHz Step-Down Regulator with Integrated Switches

ABSOLUTE MAXIMUM RATINGS

IN, V_{DD}, PWRGD to GND .....-0.3V to +4.5V
COMP, FB, REFIN, OUT,
CTL_, EN, SS, FREQ to GND.....-0.3V to (V_{DD} + 0.3V)
LX Current (Note 1).....-8A to +8A
BST to LX.....-0.3V to +4V
PGND to GND .....-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
(derate 27.8mW/°C above +70°C).....2222.2mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: LX has internal clamp diodes to GND and IN. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{DD} = 3.3V, V_{FB} = 0.5V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, circuit of Figure 1, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN/V_{DD}						
IN and V_{DD} Voltage Range			2.35		3.60	V
IN Supply Current	f_S = 1MHz, no load, (includes gate-drive current)	V_{IN} = 2.5V		4	4.6	mA
		V_{IN} = 3.3V		5.5		
V_{DD} Supply Current	f_S = 1MHz	V_{IN} = 2.5V		1.4	2.3	mA
		V_{IN} = 3.3V		2		
Total Shutdown Current from IN and V_{DD}	V_{IN} = V_{DD} = V_{BST} - V_{LX} = 3.6V, V_{EN} = 0V				13	µA
V_{DD} Undervoltage Lockout Threshold	LX starts/stops switching	V_{DD} rising		2	2.1	V
		V_{DD} falling	1.8	1.9		
		Deglitching		2		µs
BST						
BST Supply Current	V_{BST} = V_{DD} = V_{IN} = 3.6V, V_{LX} = 3.6V or 0V, V_{EN} = 0V	T_A = +25°C			5	µA
		T_A = +85°C		10		
PWM COMPARATOR						
PWM Comparator Propagation Delay	10mV overdrive			20		ns
COMP						
COMP Clamp Voltage, High	V_{IN} = 2.35V to 3.6V			2		V
COMP Slew Rate				1.4		V/µs
PWM Ramp Amplitude				1		V
COMP Shutdown Resistance	From COMP to GND, V_{EN} = V_{SS} = 0V			8		Ω
ERROR AMPLIFIER						
Preset Output-Voltage Accuracy	REFIN = SS		-1	Select from Table 1	+1	%
FB Regulation Accuracy Using External Resistors	CTL1 = CTL2 = GND		0.594	0.600	0.606	V
FB to OUT Resistor	All VID settings except CTL1 = CTL2 = GND		5	8	11	kΩ
Open-Loop Voltage Gain	1kΩ from COMP to GND			115		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{DD} = 3.3V, V_{FB} = 0.5V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, circuit of Figure 1, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Error-Amplifier Unity-Gain Bandwidth	Parallel 10kΩ, 40pF from COMP to GND (Note 3)			14	26		MHz
Error-Amplifier Common-Mode Input Range	V_{DD} = 2.35V to 2.6V			0		V_{DD} - 1.65	V
	V_{DD} = 2.6V to 3.6V			0		V_{DD} - 1.7	
Error-Amplifier Minimum Output Current	V_{COMP} = 1V	Sourcing		1000			µA
		Sinking		-500			
FB Input Bias Current	V_{FB} = 0.7, CTL1 = CTL2 = GND, T_A = +25°C			-200	-40		nA
CTL_							
CTL_ Input Bias Current	$V_{CTL_}$ = 0V				-7		µA
	$V_{CTL_}$ = V_{DD}				+7		
High-Z Threshold	Rising					0.75	V
	Falling			V_{DD} - 1.2			
Hysteresis	All VID transitions				50		mV
REFIN							
REFIN Input Bias Current	V_{REFIN} = 0.6V, T_A = +25°C			-500	-100		nA
REFIN Common-Mode Range	V_{DD} = 2.3V to 2.6V			0		V_{DD} - 1.65	V
	V_{DD} = 2.6V to 3.6V			0		V_{DD} - 1.7	
REFIN Offset Voltage	CTL1 = CTL2 = GND, T_A = +25°C			-3		+3	mV
LX (All pins combined)							
LX On-Resistance, High Side	I_{LX} = -2A	V_{IN} = V_{BST} - V_{LX} = 2.5V			27		mΩ
		V_{IN} = V_{BST} - V_{LX} = 3.3V			26	45	
LX On-Resistance, Low Side	I_{LX} = 2A	V_{IN} = 2.5V			24		mΩ
		V_{IN} = 3.3V			23	38	
LX Current-Limit Threshold	V_{IN} = 2.5V, high-side sourcing			8	11		A
LX Leakage Current	V_{IN} = 3.6V, V_{EN} = V_{SS} = 0V	T_A = +25°C	V_{LX} = 0V	-2			µA
			V_{LX} = 3.6V			+2	
		T_A = +85°C	V_{LX} = 0V		1		
			V_{LX} = 3.6V		1		
LX Switching Frequency	V_{IN} = 2.5V to 3.3V	R_{FREQ} = 50kΩ		0.9	1	1.1	MHz
		R_{FREQ} = 23.2kΩ		1.8	2	2.2	

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{DD} = 3.3V, V_{FB} = 0.5V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, circuit of Figure 1, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency Range			500		2000	kHz
LX Minimum Off-Time	V_{IN} = 2.5V to 3.3V			40	75	ns
LX Maximum Duty Cycle	R_{FREQ} = 50kΩ, V_{IN} = 2.5V to 3.3V		93	96		%
LX Minimum On-Time	R_{FREQ} = 50kΩ, V_{IN} = 2.5V to 3.3V			80		ns
RMS LX Output Current			6			A
ENABLE						
EN Input Logic Low, Falling				1.2	0.7	V
EN Input Logic High, Rising			1.7	1.4		V
EN Hysteresis				200		mV
EN, Input Current	V_{EN} = 0V or 3.6V, V_{DD} = 3.6V	T_A = +25°C			1	µA
		T_A = +85°C		0.01		
SS						
SS Charging Current	V_{SS} = 0.45V		7	8	9	µA
SS Discharge Resistance				500		Ω
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold				+165		°C
Thermal-Shutdown Hysteresis				20		°C
POWER-GOOD (PWRGD)						
Power-Good Threshold Voltage	V_{FB} falling, 3mV hysteresis		87	90	93	%
Power-Good Falling Edge Deglitch				48		Clock cycles
PWRGD Output Voltage Low	I_{PWRGD} = 4mA			0.03	0.15	V
PWRGD Leakage Current	V_{DD} = V_{PWRGD} = 3.6V, V_{FB} = 0.9V			0.01		µA
OVERCURRENT LIMIT						
Current-Limit Startup Blanking				128		Clock cycles
Restart Time				1024		Clock cycles

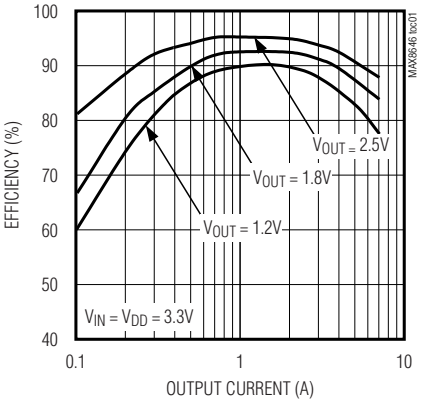
Note 2: Specifications are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.

Note 3: Guaranteed by design.

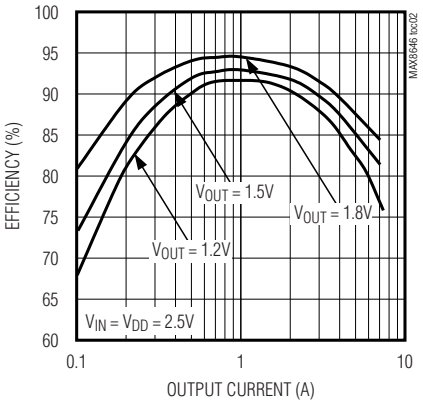
Typical Operating Characteristics

(Typical values are: V_{IN} = V_{DD} = 3.3V; V_{OUT} = 1.8V, R_{FREQ} = 50kΩ, I_{OUT} = 6A, and T_A = +25°C, unless otherwise noted.)

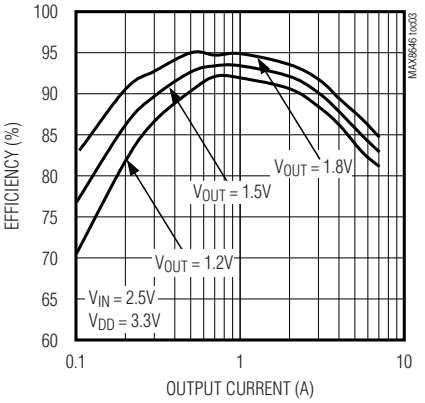
EFFICIENCY vs. OUTPUT CURRENT



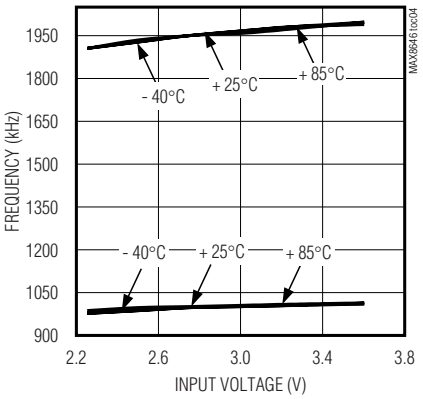
EFFICIENCY vs. OUTPUT CURRENT



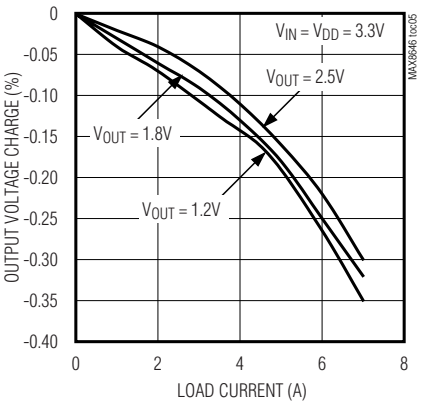
EFFICIENCY vs. OUTPUT CURRENT



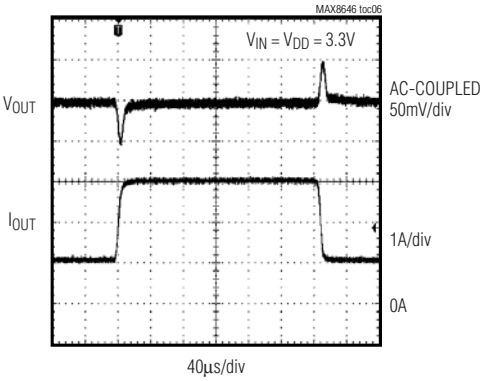
FREQUENCY vs. INPUT VOLTAGE



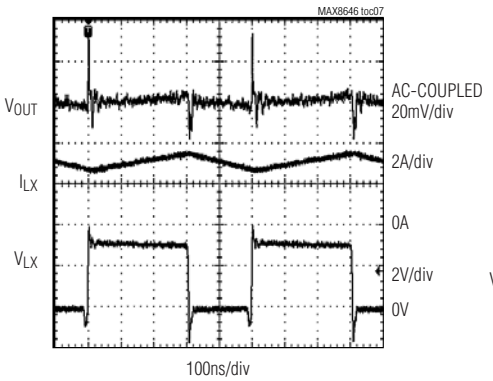
LOAD REGULATION



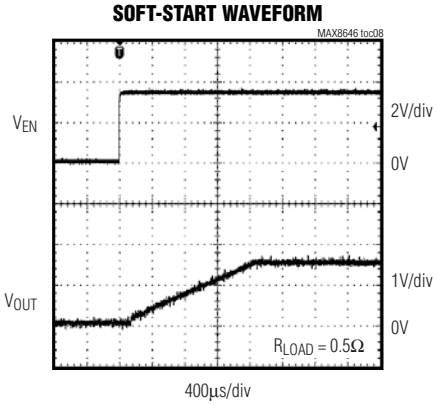
LOAD TRANSIENT



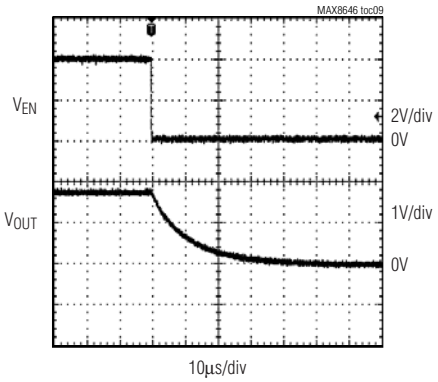
SWITCHING WAVEFORMS



SOFT-START WAVEFORM



SHUTDOWN WAVEFORMS

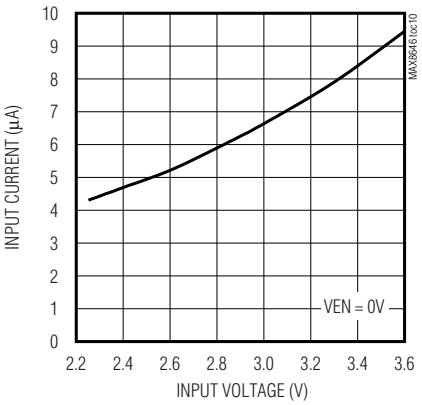


6A, 2MHz Step-Down Regulator with Integrated Switches

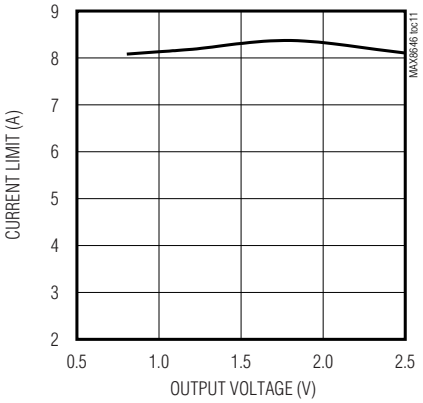
Typical Operating Characteristics (continued)

(Typical values are: V_{IN} = V_{DD} = 3.3V; V_{OUT} = 1.8V, R_{FREQ} = 50kΩ, I_{OUT} = 6A, and T_A = +25°C, unless otherwise noted.)

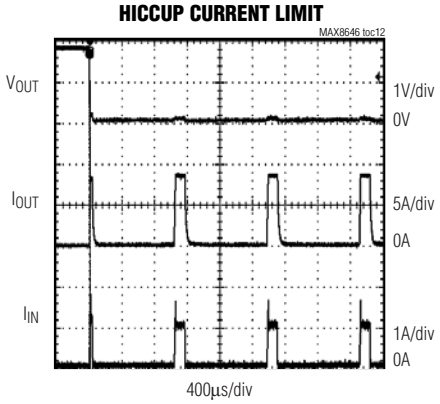
INPUT CURRENT vs. INPUT VOLTAGE



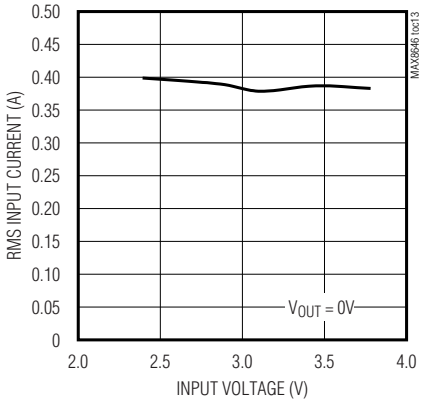
CURRENT LIMIT vs. OUTPUT VOLTAGE



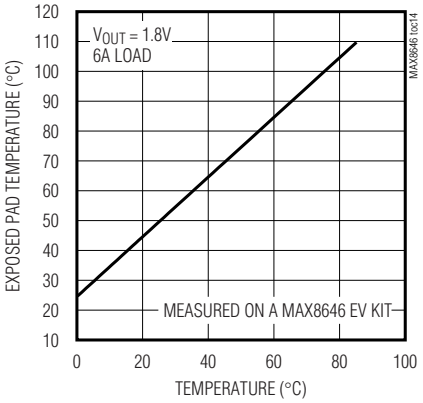
HICCUP CURRENT LIMIT



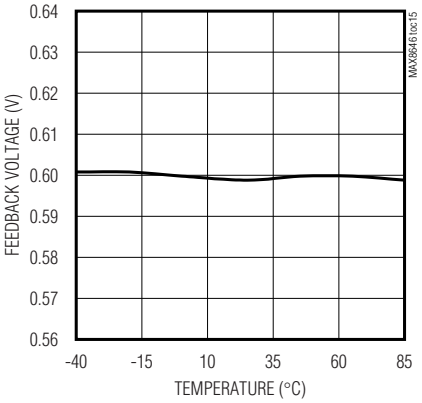
RMS INPUT CURRENT DURING SHORT-CIRCUIT vs. INPUT VOLTAGE (C_4 = 0.022µF)



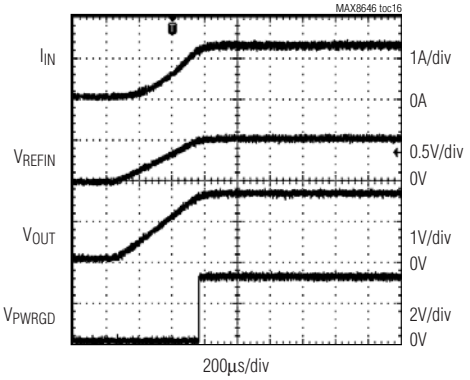
EXPOSED PAD TEMPERATURE vs. AMBIENT TEMPERATURE



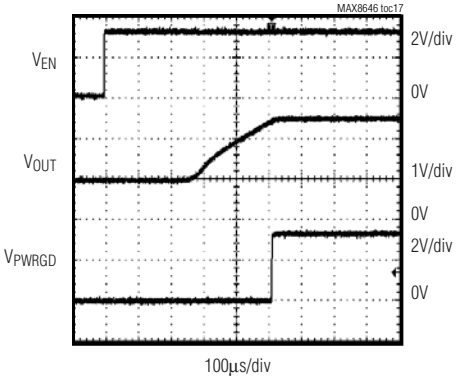
FEEDBACK VOLTAGE vs. TEMPERATURE



SOFT-START WITH REFIN



STARTING INTO PREBIASED OUTPUT



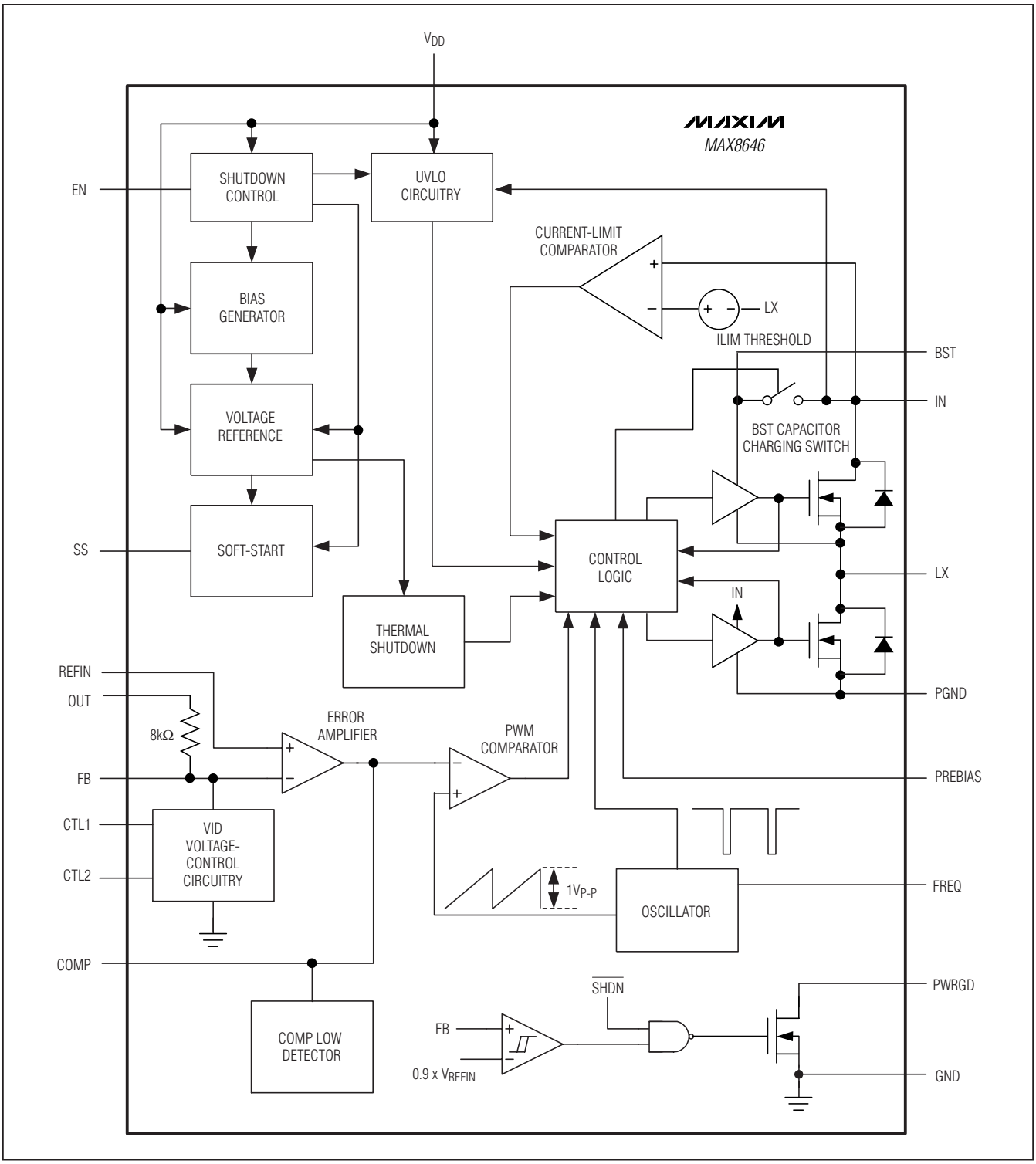
C_{SS} = 6800pF, C_O = 122µF, L = 0.56µH, V_{OUT} = 2.5V

Pin Description

PIN	NAME	FUNCTION
1	PREBIAS	Leave Pin Unconnected to Prevent Discharging of Output Capacitor During Soft-Start. Connect to GND otherwise. See the *Soft-Starting into a Prebiased Output* section.
2	V_{DD}	Supply Voltage and Bypass Input. Connect V_{DD} to IN with a 10Ω resistor. Connect a 1µF ceramic capacitor from V_{DD} to GND.
3, 4	CTL1, CTL2	Preset Output Voltage Selection Input. CTL1 and CTL2 set the output voltage to one of nine preset voltages. See Table 1 for preset voltages.
5	REFIN	External Reference Input. Connect REFIN to SS to use the internal 0.6V reference. Connecting REFIN to an external reference voltage forces FB to regulate the voltage applied to REFIN. REFIN is internally pulled to GND when the IC is in shutdown mode.
6	SS	Soft-Start Input. Connect a capacitor from SS to GND to set the startup time. See the *Soft-Start and REFIN* section for details on setting the soft-start time.
7	GND	Analog Circuit Ground
8	COMP	Output of the Voltage-Error Amplifier. Connect the necessary compensation network from COMP to FB. COMP is internally pulled to GND when the IC is in shutdown mode.
9	FB	Feedback Input. Connect FB to the center tap of an external resistor-divider from the output to GND to set the output voltage from 0.6V to 90% of V_{IN}. Connect FB through an RC network to the output when using CTL1 and CTL2 to select any of nine preset voltages.
10	OUT	Output Voltage Sense. Connect to the output. Leave OUT unconnected when an external resistor-divider is used.
11	FREQ	Oscillator Frequency Selection. Connect a resistor from FREQ to GND to select the switching frequency.
12	PWRGD	Power-Good Output. Open-drain output that is high impedance when $V_{FB} \geq 90\%$ of V_{REFIN} or 0.6V. PWRGD is internally pulled low when V_{FB} falls below 90% of its regulation point. PWRGD is internally pulled low when the IC is in shutdown mode, V_{DD} or V_{IN} is below the UVLO threshold, or the IC is in thermal shutdown.
13	BST	High-Side MOSFET Driver Supply. Bypass BST to LX with a 0.1µF capacitor.
14, 15, 16	LX	Inductor Connection. All LX pins are internally connected together. Connect all LX pins to the output inductor. LX is high impedance when the IC is in shutdown mode.
17–20	PGND	Power Ground. Connect all PGND pins externally to the power ground plane.
21, 22, 23	IN	Power-Supply Input. Input supply range is from 2.35V to 3.6V. Bypass with 22µF ceramic capacitance to PGND externally. See the *Typical Application Circuit*.
24	EN	Enable Input. Logic input to enable/disable the MAX8646.
—	EP	Exposed Pad. Connect to a large ground plane to optimize thermal performance.

6A, 2MHz Step-Down Regulator with Integrated Switches

Block Diagram



Typical Application Circuit

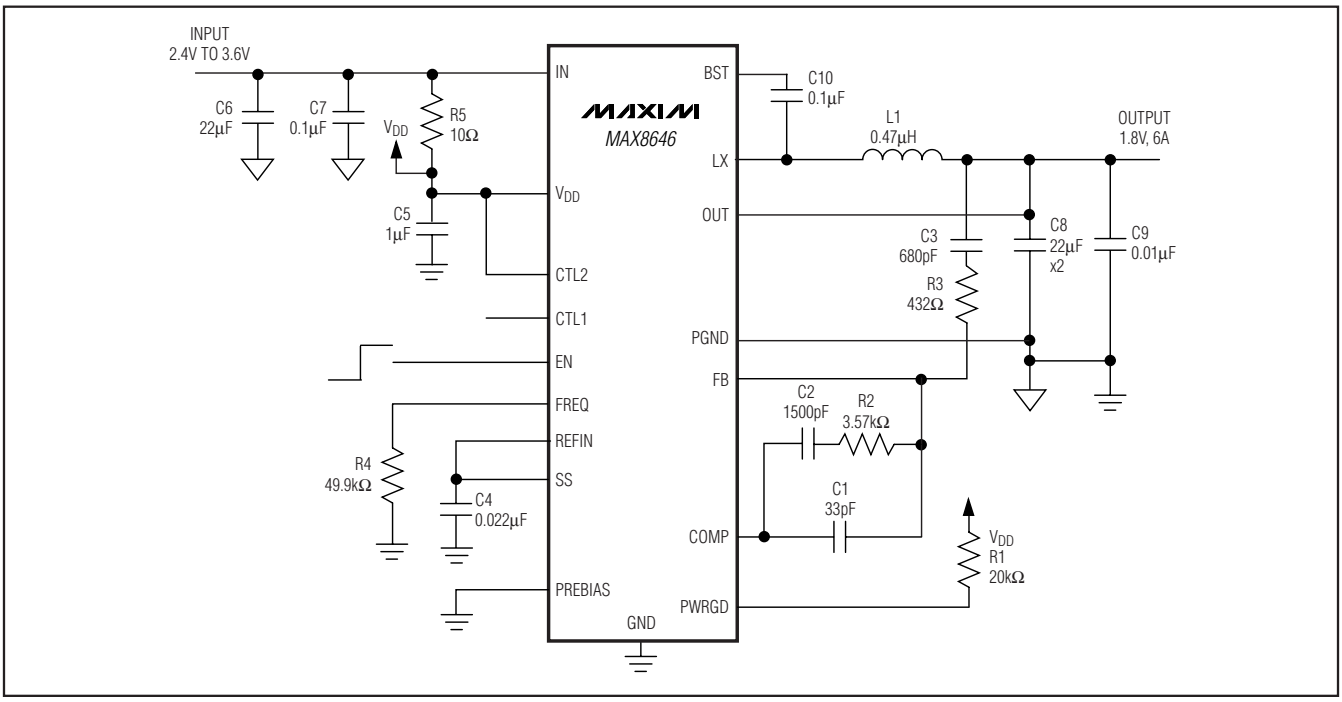


Figure 1. MAX8646 1MHz, All-Ceramic-Capacitor Design with V_{OUT} = 1.8V

Detailed Description

The MAX8646 high-efficiency, voltage-mode switching regulator is capable of delivering up to 6A of output current. The MAX8646 provides output voltages from 0.6V to 0.9 x V_{IN} from 2.35V to 3.6V input supplies, making it ideal for on-board point-of-load applications. The output voltage accuracy is better than ±1% over load, line, and temperature.

The MAX8646 features a wide switching frequency range, allowing the user to achieve all-ceramic-capacitor designs and fast transient responses (see Figure 1). The high operating frequency minimizes the size of external components. The MAX8646 is available in a small (4mm x 4mm), lead-free, 24-pin thin QFN package. The REFIN function makes the MAX8646 an ideal candidate for DDR and tracking power supplies. Using internal low-$R_{DS(ON)}$ (23mΩ) n-channel MOSFETs for both high- and low-side switches maintains high efficiency at both heavy-load and high-switching frequencies.

The MAX8646 employs voltage-mode control architecture with a high bandwidth (> 14MHz) error amplifier. The voltage-mode control architecture allows up to 2MHz switching frequency, reducing board area. The op-amp voltage-error amplifier works with type III compensation to fully utilize the bandwidth of the high-frequency switching to obtain fast transient response. Adjustable soft-start time provides flexibilities to minimize input startup inrush current. An open-drain, power-good (PWRGD) output goes high when V_{FB} reaches 90% of V_{REFIN} or 0.54V.

Controller Function

The controller logic block is the central processor that determines the duty cycle of the high-side MOSFET under different line, load, and temperature conditions. Under normal operation, where the current-limit and temperature protection are not triggered, the controller logic block takes the output from the PWM comparator and generates the driver signals for both high-side and low-side MOSFETs. The break-before-make logic and the timing for charging the bootstrap capacitors are calculated by the controller logic block. The error signal from the voltage-error amplifier is compared with the ramp signal generated by the oscillator at the PWM comparator and, thus, the required PWM signal is produced. The high-side switch is turned on at the beginning of the oscillator cycle and turns off when the ramp

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voltage exceeds the V_{COMP} signal or the current-limit threshold is exceeded. The low-side switch is then turned on for the remainder of the oscillator cycle.

Current Limit

The internal, high-side MOSFET has a typical 11A peak current-limit threshold. When current flowing out of LX exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. The synchronous rectifier remains on until the inductor current falls below the low-side current limit. This lowers the duty cycle and causes the output voltage to droop until the current limit is no longer exceeded. The MAX8646 uses a hiccup mode to prevent overheating during short-circuit output conditions.

During current limit if V_{FB} drops below 420mV and stays below this level for 12µs or more, the part enters hiccup mode. The high-side MOSFET and the synchronous rectifier are turned off and both COMP and REFIN are internally pulled low. If REFIN and SS are connected together, then both are pulled low. The part remains in this state for 1024 clock cycles and then attempts to restart for 128 clock cycles. If the fault causing current limit has cleared, the part resumes normal operation. Otherwise, the part reenters hiccup mode again.

Soft-Start and REFIN

The MAX8646 utilizes an adjustable soft-start function to limit inrush current during startup. An 8µA (typ) current source charges an external capacitor connected to SS. The soft-start time is adjusted by the value of the external capacitor from SS to GND. The required capacitance value is determined as:

$$C = \frac{8\mu A \times t_{SS}}{0.6V}$$

where t_{SS} is the required soft-start time in seconds. The MAX8646 also features an external reference input (REFIN). The IC regulates FB to the voltage applied to REFIN. The internal soft-start is not available when using an external reference. A method of soft-start when using an external reference is shown in Figure 2. Connect REFIN to SS to use the internal 0.6V reference.

Undervoltage Lockout (UVLO)

The UVLO circuitry inhibits switching when V_{DD} is below 2V (typ). Once V_{DD} rises above 2V (typ), UVLO clears and the soft-start function activates. A 100mV hysteresis is built in for glitch immunity. Figure 3 is the type III compensation network.

BST

The gate-drive voltage for the high-side, n-channel switch is generated by a flying-capacitor boost circuit. The capacitor between BST and LX is charged from the V_{IN} supply while the low-side MOSFET is on. When the low-side MOSFET is switched off, the voltage of the capacitor is stacked above LX to provide the necessary turn-on voltage for the high-side internal MOSFET.

Frequency Select (FREQ)

The switching frequency is resistor programmable from 500kHz to 2MHz. Set the switching frequency of the IC with a resistor (R_{FREQ}) connected from FREQ to GND. R_{FREQ} is calculated as:

$$R_{FREQ} = \frac{49.9k\Omega}{0.95\mu s} \times \left(\frac{1}{f_S} - 0.05\mu s\right)$$

where f_S is the desired switching frequency in Hz.

Power-Good Output (PWRGD)

PWRGD is an open-drain output that goes high impedance when V_{FB} is above 0.9 x V_{REFIN}. PWRGD pulls low when V_{FB} is below 90% of its regulation for at least 48 clock cycles. PWRGD is low during shutdown.

Programming the Output Voltage (CTL1, CTL2)

As shown in Table 1, the output voltage is pin programmable by the logic states of CTL1 and CTL2. CTL1 and CTL2 are tri-level inputs: V_{DD}, unconnected, and GND. The logic states of CTL1 and CTL2 should be programmed only before power-up. Once the part is enabled, CTL1 and CTL2 should not be changed. If the output voltage needs to be reprogrammed, cycle power or EN and reprogram before enabling.

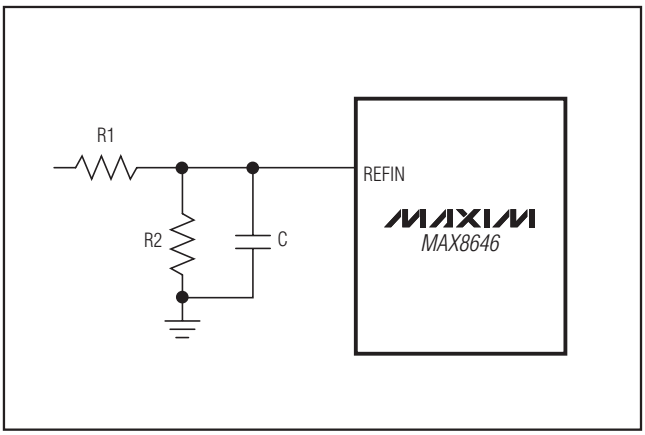

Figure 2. Typical Soft-Start Implementation with External Reference

Shutdown Mode

Drive EN to GND to shut down the IC and reduce quiescent current to less than 12µA. During shutdown, the LX is high impedance. Drive EN high to enable the MAX8646.

Thermal Protection

Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds T_J = +165°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C, causing a pulsed output during continuous overload conditions. The soft-start sequence begins after recovery from a thermal-shutdown condition.

Applications Information

IN and V_{DD} Decoupling

To decrease the noise effects due to the high switching frequency and maximize the output accuracy of the MAX8646, decouple V_{IN} with a 22µF capacitor from V_{IN} to PGND. Also decouple V_{DD} with a 1µF from V_{DD} to GND. Place these capacitors as close to the IC as possible.

Inductor Selection

Choose an inductor with the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_S \times V_{IN} \times LIR \times I_{OUT(MAX)}}$$

where LIR is the ratio of the inductor ripple current to full load current at the minimum duty cycle. Choose LIR between 20% to 40% for best performance and stability.

Use an inductor with the lowest possible DC resistance that fits in the allotted dimensions. Powdered iron ferrite core types are often the best choice for performance. With any core material, the core must be large enough not to saturate at the current limit of the MAX8646.

Output-Capacitor Selection

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and voltage-rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Calculate the output voltage ripple due to the output capacitance, ESR, and ESL:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

Table 1. CTL1 and CTL2 Output Voltage Selection

CTL1	CTL2	V_{OUT} (V)
GND	GND	0.6
V_{DD}	V_{DD}	0.7
GND	Unconnected	0.8
GND	V_{DD}	1.0
Unconnected	GND	1.2
Unconnected	Unconnected	1.5
Unconnected	V_{DD}	1.8
V_{DD}	GND	2.0
V_{DD}	Unconnected	2.5

where the output ripple due to output capacitance, ESR, and ESL is:

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_S}$$

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{ON}} \times ESL$$

or:

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{OFF}} \times ESL$$

or whichever is larger.

The peak inductor current (I_{P-P}) is:

$$I_{P-P} = \frac{V_{IN} - V_{OUT}}{f_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Use these equations for initial capacitor selection. Determine final values by testing a prototype or an evaluation circuit. A smaller ripple current results in less output-voltage ripple. Since the inductor ripple current is a factor of the inductor value, the output voltage ripple decreases with larger inductance. Use ceramic capacitors for low ESR and low ESL at the switching frequency of the converter. The ripple voltage due to ESL is negligible when using ceramic capacitors.

Load-transient response depends on the selected output capacitance. During a load transient, the output instantly changes by ESR x ΔI_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time, the controller responds by regu-

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lating the output voltage back to its predetermined value. The controller response time depends on the closed-loop bandwidth. A higher bandwidth yields a faster response time, preventing the output from deviating further from its regulating value. See the *Compensation Design* section for more details.

Input-Capacitor Selection

The input capacitor reduces the current peaks drawn from the input power supply and reduces switching noise in the IC. The total input capacitance must be equal or greater than the value given by the following equation to keep the input-ripple voltage within specs and minimize the high-frequency ripple current being fed back to the input source:

$$C_{IN_MIN} = \frac{D \times T_S \times I_{OUT}}{V_{IN-RIPPLE}}$$

where $V_{IN-RIPPLE}$ is the maximum allowed input ripple voltage across the input capacitors and is recommended to be less than 2% of the minimum input voltage. D is the duty cycle (V_{OUT}/V_{IN}) and T_S is the switching period ($1/f_S$).

The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source but are instead shunted through the input capacitor. High source impedance requires high input capacitance. The input capacitor must meet the ripple current requirement imposed by the switching currents. The RMS input ripple current is given by:

$$I_{RIPPLE} = I_{LOAD} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}}}$$

where I_{RIPPLE} is the input RMS ripple current.

Compensation Design

The power transfer function consists of one double pole and one zero. The double pole is introduced by the output filtering inductor L and the output filtering capacitor C_O. The ESR of the output filtering capacitor determines the zero. The double pole and zero frequencies are given as follows:

$$f_{P1_LC} = f_{P2_LC} = \frac{1}{2\pi \times \sqrt{L \times C_O \times \left(\frac{R_O + ESR}{R_O + R_L}\right)}}$$

$$f_{Z_ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

where R_L is equal to the sum of the output inductor's DCR and the internal switch resistance, $R_{DS(ON)}$. A typical value for $R_{DS(ON)}$ is 23mΩ. R_O is the output load resistance, which is equal to the rated output voltage divided by the rated output current. ESR is the total equivalent series resistance of the output filtering capacitor. If there is more than one output capacitor of the same type in parallel, the value of the ESR in the above equation is equal to that of the ESR of a single output capacitor divided by the total number of output capacitors.

The high switching frequency range of the MAX8646 allows the use of ceramic output capacitors. Since the ESR of ceramic capacitors is typically very low, the frequency of the associated transfer function zero is higher than the unity-gain crossover frequency, f_C, and the zero cannot be used to compensate for the double pole created by the output filtering inductor and capacitor. The double pole produces a gain drop of 40dB/decade and a phase shift of 180°/decade. The error amplifier must compensate for this gain drop and phase shift to achieve a stable high-bandwidth closed-loop system. Therefore, use type III compensation as shown in Figures 3 and 4. Type III compensation possesses three poles and two zeros with the first pole, f_{P1_EA}, located at zero frequency (DC). Locations of other poles and zeros of the type III compensation are given by:

$$f_{Z1_EA} = \frac{1}{2\pi \times R1 \times C1}$$

$$f_{Z2_EA} = \frac{1}{2\pi \times R3 \times C3}$$

$$f_{P3_EA} = \frac{1}{2\pi \times R1 \times C2}$$

$$f_{P2_EA} = \frac{1}{2\pi \times R2 \times C3}$$

The above equations are based on the assumptions that C1>>C2, and R3>>R2, which are true in most applications. Placements of these poles and zeros are determined by the frequencies of the double pole and ESR zero of the power transfer function. It is also a function of the desired close-loop bandwidth. The following section outlines the step-by-step design procedure to calculate the required compensation components for the MAX8646. When the output voltage of the MAX8646 is programmed to a preset voltage, R3 is internal to the IC and R4 does not exist (Figure 3b).

When externally programming the MAX8646 (Figure 3a), the output voltage is determined by:

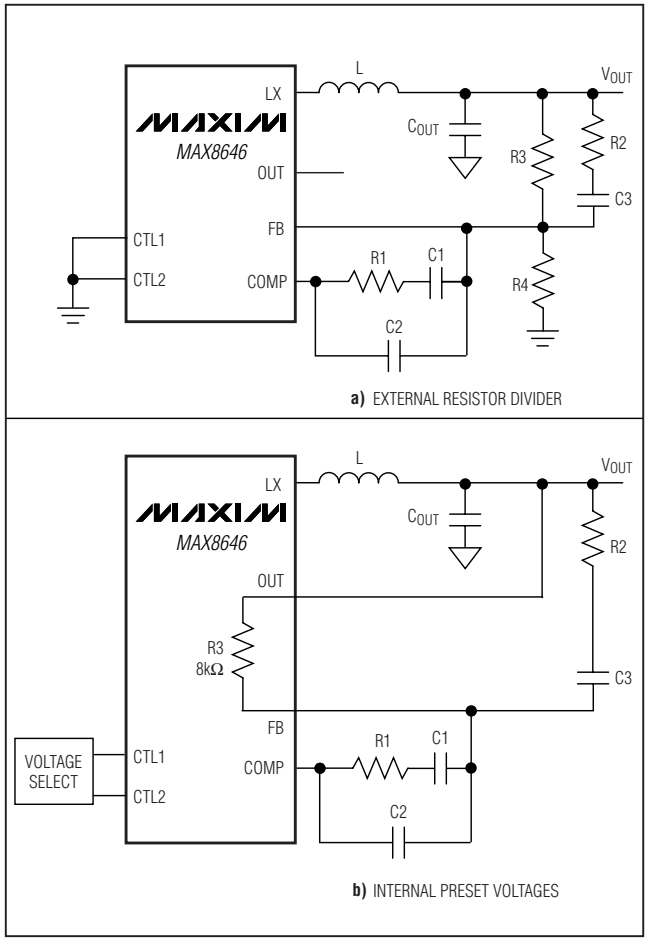

Figure 3. Type III Compensation Network

$$R4 = \frac{0.6 \times R3}{(V_{OUT} - 0.6)}$$

The zero-cross frequency of the close-loop, f_C should be between 10% and 20% of the switching frequency, f_S. A higher zero-cross frequency results in faster transient response. Once f_C is chosen, C1 is calculated from the following equation:

$$C1 = \frac{1.5625 \times V_{IN}}{2 \times \pi \times R3 \times (1 + \frac{R_L}{R_O}) \times f_C}$$

Due to the underdamped nature of the output LC double pole, set the two zero frequencies of the type III compensation less than the LC double-pole frequency to provide adequate phase boost. Set the two zero frequencies to 80% of the LC double-pole frequency. Hence:

$$R1 = \frac{1}{0.8 \times C1} \times \sqrt{\frac{L \times C_O \times (R_O + ESR)}{R_L + R_O}}$$

$$C3 = \frac{1}{0.8 \times R3} \times \sqrt{\frac{L \times C_O \times (R_O + ESR)}{R_L + R_O}}$$

Setting the second compensation pole, f_{P2_EA}, at f_{Z_ESR} yields:

$$R2 = \frac{C_O \times ESR}{C_3}$$

Set the third compensation pole at 1/2 of the switching frequency. Calculate C2 as follows:

$$C2 = \frac{1}{\pi \times R1 \times f_S \times 2}$$

The above equations provide application compensation when the zero-cross frequency is significantly higher than the double-pole frequency. When the zero-cross frequency is near the double-pole frequency, the actual zero-cross frequency is higher than the calculated frequency. In this case, lowering the value of R1 reduces the zero-cross frequency. Also, set the third pole of the type III compensation close to the switching frequency if the zero-cross frequency is above 200kHz to boost the phase margin. The recommended range for R3 is 2kΩ to 10kΩ. Note that the loop compensation remains unchanged if only R4's resistance is altered to set different outputs.

Soft-Starting into a Prebiased Output

When the PREBIAS pin is left unconnected, the MAX8646 is capable of soft-starting up into a prebiased output without discharging the output capacitor. This type of operation is also termed monotonic start-up. However, in order to avoid output voltage glitches during soft-start it should be ensured that the inductor current is in continuous conduction mode during the end of the soft-start period. this is done by satisfying the following equation:

$$C_O \times \frac{V_O}{t_{SS}} \geq \frac{I_{P-P}}{2}$$

where C_O is the output capacitor, V_O is the output voltage, t_{SS} is the soft-start time set by the soft-start capacitor C_{SS}, and I_{P-P} is the peak inductor ripple current (as defined in the *Output-Capacitor Selection* section). Depending on the application, one of these parameters may drive the selection of the others. See *Starting into*

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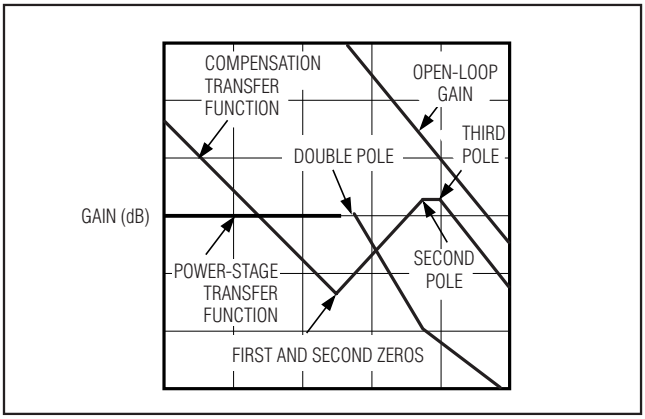


Figure 4. Type III Compensation Illustration

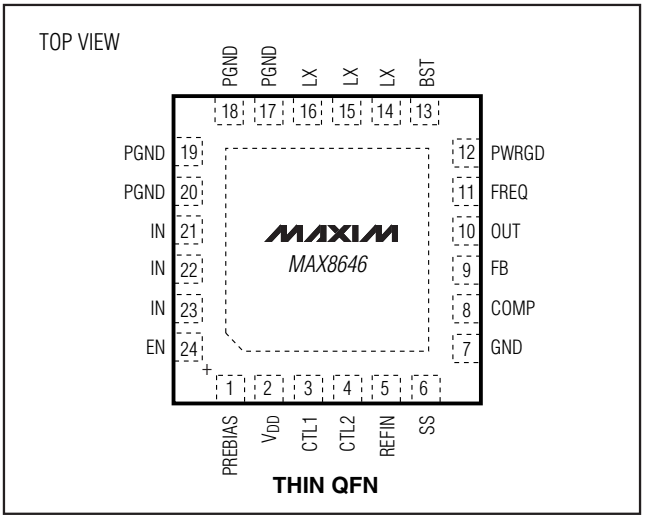
Prebiased Output waveforms in the *Typical Operating Characteristics* section for an example selection of the above parameters. Connecting the PREBIAS pin to the GND disables the prebias soft-start feature and causes the MAX8646 to discharge any voltage present on the output capacitors and then commence its soft-start.

PCB Layout Considerations and Thermal Performance

Careful PCB layout is critical to achieve clean and stable operation. It is highly recommended to duplicate the MAX8646 EV kit layout for optimum performance. If deviation is necessary, follow these guidelines for good PCB layout:

1) Connect input and output capacitors to the power ground plane; connect all other capacitors to the signal ground plane.
2) Place capacitors on V_{DD}, V_{IN}, and SS as close as possible to the IC and its corresponding pin using direct traces. Keep power ground plane (connected to PGND) and signal ground plane (connected to GND) separate.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current short and minimize the loop area formed by LX, the output capacitors, and the input capacitors.
4) Connect IN, LX, and PGND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.
5) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the IC as possible.
6) Route high-speed switching nodes, such as LX, away from sensitive analog areas (FB, COMP).

Pin Configuration

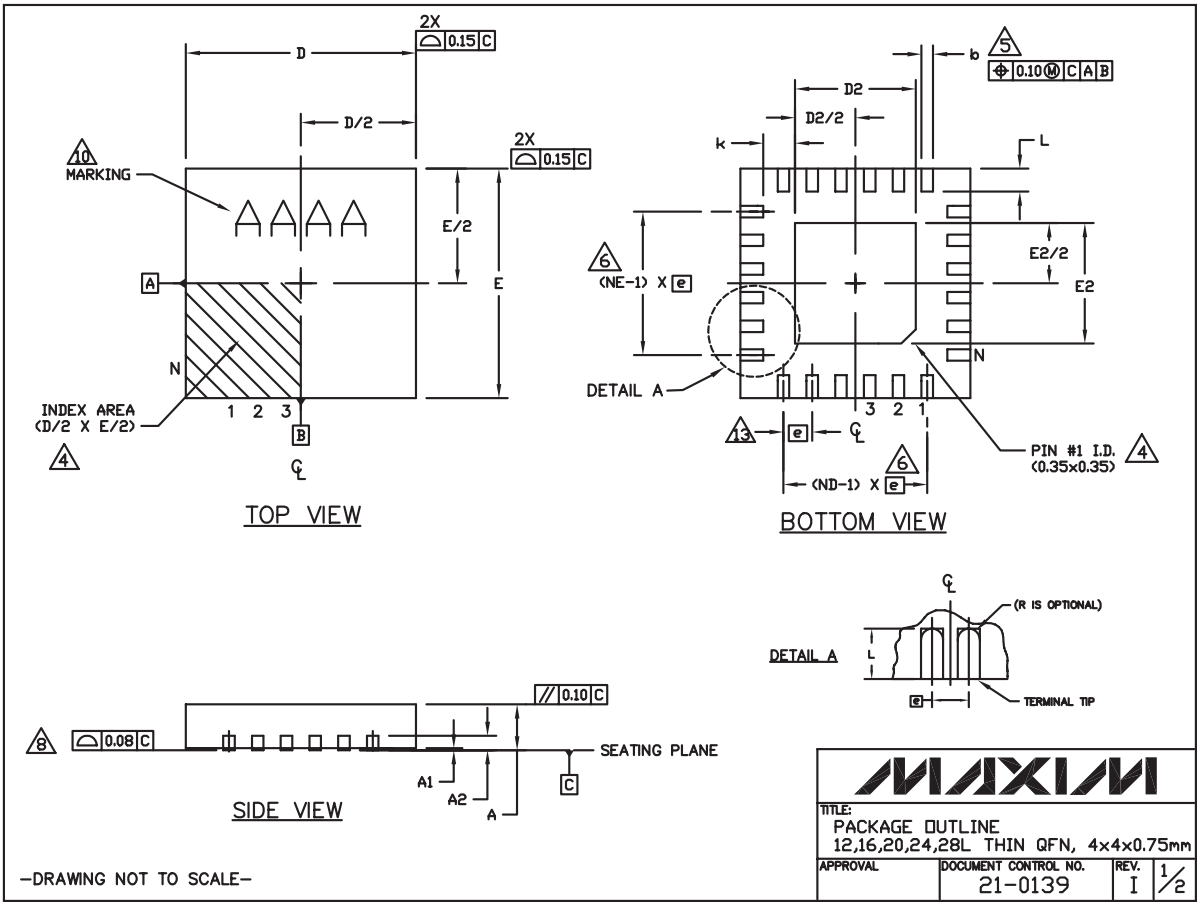


Chip Information

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



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Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444N-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444M-1	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

—DRAWING NOT TO SCALE—

MAXIM

TITLE: PACKAGE OUTLINE 12,16,20,24,28L THIN QFN, 4x4x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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Pages changed at Rev 2: 1, 2, 4, 8, 9, 13, 15, 16

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