

# LED DRIVER

Check for Samples: [TLC5922](#)

## FEATURES

- 16 Channels
- Drive Capability
  - 0 to 80 mA (Constant-Current Sink)
- Constant Current Accuracy
  - ±1% (typical)
- Serial Data Interface, SPI Compatible
- Fast Switching Output:  $T_r / T_f = 10\text{ns}$  (typical)
- CMOS Level Input/Output
- 30 MHz Data Transfer Rate
- $V_{CC} = 3.0\text{ V to } 5.5\text{ V}$
- Operating Temperature =  $-20^\circ\text{C to } 85^\circ\text{C}$
- LED Supply Voltage up to 17 V
- 32-pin HTSSOP ( PowerPAD™) Package
- Dot Correction
  - 7 bit (128 Steps)
  - Individually Adjustable For Each Channel

- Controlled In-Rush Current

## APPLICATIONS

- Monocolor, Multicolor, Fullcolor LED Display
- Monocolor, Multicolor LED Signboard
- Display Backlighting
- Multicolor LED Lighting Applications

## DESCRIPTION

The TLC5922 is a 16-channel constant-current sink driver. Each channel has an On/Off state and a 128-step adjustable constant-current sink (dot correction). The dot correction adjusts the brightness variations between LED, LED channels, and other LED drivers. Both dot correction and On/Off state are accessible via a serial data interface. A single external resistor sets the maximum current of all 16 channels.

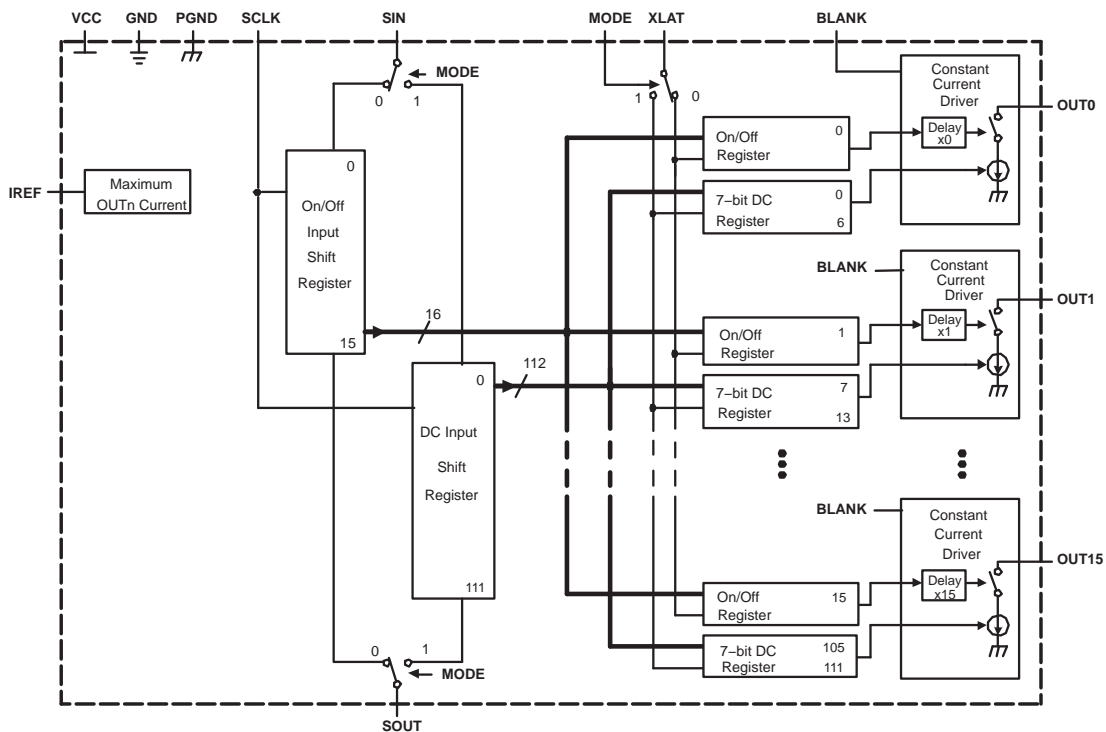


Figure 1. Functional Block Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**ORDERING INFORMATION<sup>(1)</sup>**

T <sub>A</sub>	Package	Part Number <sup>(2)</sup>
-20 °C to 85 °C	4 mm x 4 mm, 32-pin HTSSOP	TLC5922DAP

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) The DAP package is available in tape and reel. Add R suffix (TLC5922DAPR) to order quantities of 2000 parts per reel.

**ABSOLUTE MAXIMUM RATINGS <sup>(1) (2)</sup>**

		TLC5922	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>	-0.3 to 6	V
I <sub>O</sub>	Output current (dc)	I <sub>L(LC)</sub>	90 mA
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	V <sub>(BLANK)</sub> , V <sub>(XLAT)</sub> , V <sub>(SCLK)</sub> , V <sub>(SIN)</sub> , V <sub>(MODE)</sub>	-0.3 to V <sub>CC</sub> + 0.3 V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	V <sub>(SOUT)</sub>	-0.3 to V <sub>CC</sub> + 0.3 V
		V <sub>(OUT0)</sub> - V <sub>(OUT15)</sub>	-0.3 to 18 V
ESD rating	HBM (JEDEC JESD22-A114, Human Body Model)	2	kV
	CDM (JEDEC JESD22-C101, Charged Device Model)	500	V
T <sub>stg</sub>	Storage temperature range	-40 to 150	°C
	Continuous total power dissipation at (or below) T <sub>A</sub> = 25°C	3.9	W
	Power dissipation rating at (or above) T <sub>A</sub> = 25°C	31.4	mW/°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

**RECOMMENDED OPERATING CONDITIONS**  
**DC Characteristics**

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3		5.5	V
V <sub>O</sub>	Voltage applied to output, (Out0 - Out15)			17	V
V <sub>IH</sub>	High-level input voltage	0.8 V <sub>CC</sub>		V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage	GND		0.2 V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		V <sub>CC</sub> = 5 V at SOUT	-1	mA
I <sub>OL</sub>	Low-level output current		V <sub>CC</sub> = 5 V at SOUT	1	mA
I <sub>OLC</sub>	Constant output current		OUT0 to OUT15	80	mA
T <sub>A</sub>	Operating free-air temperature range <sup>(1)</sup>	-20		85	°C

- (1) Contact TI sales for slightly extended temperature range.

## AC Characteristics

 $V_{CC} = 3\text{ V to }5.5\text{ V}$ ,  $T_A = -20^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

			MIN	TYP	MAX	UNIT
$f_{SCLK}$	Clock frequency	SCLK			30	MHz
$t_{wh0}/t_{w10}$	CLK pulse duration	SCLK = H/L	16			ns
$t_{wh1}$	XLAT pulse duration	XLAT = H	20			ns
$t_{su0}$	Setup time	SIN – SCLK↑	10			ns
$t_{su1}$		SCLK↑ – XLAT↓	10			ns
$t_{su2}$		MODE↑↓ – SCLK↑	10			ns
$t_{su3}$		MODE↑↓ – XLAT↓	10			ns
$t_{h0}$	Hold time	SCLK↑ – SIN	10			ns
$t_{h1}$		XLAT↓ – SCLK↑	10			ns
$t_{h2}$		SCLK↑ – MODE↑↓	10			ns
$t_{h3}$		XLAT↓ – MODE↑↓	10			ns

## ELECTRICAL CHARACTERISTICS

 $V_{CC} = 3\text{ V to }5.5\text{ V}$ ,  $T_A = -20^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage $I_{OH} = -1\text{ mA}$ , SOUT	$V_{CC} - 0.5$			V
$V_{OL}$	Low-level output voltage $I_{OL} = 1\text{ mA}$ , SOUT			0.5	V
$I_I$	Input current $V_I = V_{CC}$ or GND, BLANK, XLAT, SCLK, SIN, MODE	-1		1	$\mu\text{A}$
$I_{CC}$	Supply current	No data transfer, All output OFF, $V_O = 1\text{ V}$ , $R_{(IREF)} = 10\text{ k}\Omega$		6	mA
	No data transfer, All output OFF, $V_O = 1\text{ V}$ , $R_{(IREF)} = 1.3\text{ k}\Omega$		12		
	Data transfer 30 MHz, All output ON, $V_O = 1\text{ V}$ , $R_{(IREF)} = 1.3\text{ k}\Omega$		25		
	Data transfer 30 MHz, All output ON, $V_O = 1\text{ V}$ , $R_{(IREF)} = 600\text{ k}\Omega$	36	65 <sup>(1)</sup>		
$I_{OLC}$	Constant output current All output ON, $V_O = 1\text{ V}$ , $R_{(IREF)} = 600\ \Omega$	70	80	90	mA
$I_{LO0}$	Leakage output current All output OFF, $V_O = 15\text{ V}$ , $R_{(IREF)} = 600\ \Omega$ , OUT0 to OUT15			0.1	$\mu\text{A}$
$\Delta I_{OLC0}$	Constant current error All output ON, $V_O = 1\text{ V}$ , $R_{(IREF)} = 600\ \Omega$ , OUT0 to OUT15		$\pm 1\%$	$\pm 4\%$	
$\Delta I_{OLC1}$	Constant current error device to device, averaged current from OUT0 to OUT15, $R_{(IREF)} = 600\ \Omega$		$\pm 4\%$	$\pm 8.5\%$	
$\Delta I_{OLC2}$	Power supply rejection ratio All output ON, $V_O = 1\text{ V}$ , $R_{(IREF)} = 600\ \Omega$ , OUT0 to OUT15		$\pm 1$	$\pm 4$	$\%/V$
$\Delta I_{OLC3}$	Load regulation All output ON, $V_O = 1\text{ V to }3\text{ V}$ , $R_{(IREF)} = 600\ \Omega$ , OUT0 to OUT15		$\pm 2$	$\pm 6$	$\%/V$
$V_{(IREF)}$	Reference voltage output $R_{(IREF)} = 600\ \Omega$	1.20	1.24	1.28	V

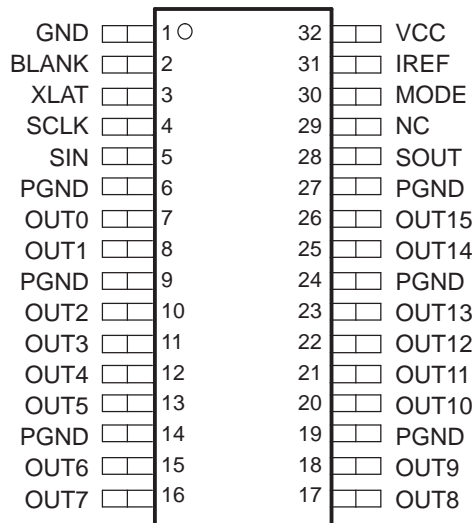
(1) Measured at device start-up temperature. Once the IC is operating (self heating), lower  $I_{CC}$  values are seen. See [Figure 12](#).

**SWITCHING CHARACTERISTICS**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r0}$	Rise time	SOUT(see <sup>(1)</sup> )			16	ns
$t_{r1}$		OUTx, V <sub>CC</sub> = 5 V, T <sub>A</sub> = 60°C, DCx = 7F (see <sup>(2)</sup> )		10	30	
$t_{f0}$	Fall time	SOUT (see <sup>(1)</sup> )			16	ns
$t_{f1}$		OUTx, V <sub>CC</sub> = 5 V, T <sub>A</sub> = 60°C, DCx = 7F (see <sup>(2)</sup> )		10	30	
$t_{pd0}$	Propagation delay time	SCLK↑ – SOUT↑↓ (see <sup>(3)</sup> )			30	ns
$t_{pd1}$		MODE↑↓ – SOUT↑↓ (see <sup>(3)</sup> )			30	
$t_{pd2}$		BLANK↓ – OUT0↑↓ (see <sup>(4)</sup> )			60	
$t_{pd3}$		XLAT↑ – OUT0↑↓ (see <sup>(4)</sup> )			60	
$t_{pd4}$		XLAT↑ – I <sub>OUT</sub> (dot-correction) (see <sup>(5)</sup> )			1000	
$t_d$	Output delay time	OUTn↑↓ – OUT(n+1)↑↓ (see <sup>(4)</sup> )	14	22	30	ns

- (1) See Figure 4 . Defined as from 10% to 90%
- (2) See Figure 5 . Defined as from 10% to 90%
- (3) See Figure 4 . Figure 10
- (4) See Figure 5 and Figure 10
- (5) See Figure 5 and Figure 10

**DAP PACKAGE  
(TOP VIEW)**



**Terminal Functions**

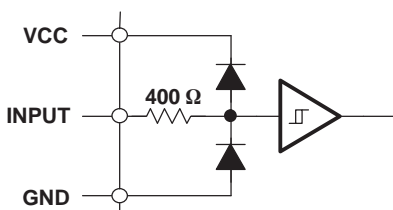
TERMINAL NAME	NO.	I/O	DESCRIPTION
BLANK	2	I	Blank (Light OFF). When BLANK = H, All OUTx outputs are forced OFF. When BLANK = L, ON/OFF of OUTx outputs are controlled by input data.
GND	1		Ground
IREF	31	I/O	Reference current terminal
MODE	30	I	Mode select. When MODE = L, SIN, SOUT, SCLK, XLAT are connected to ON/OFF control logic. When MODE = H, SIN, SOUT, SCLK, XLAT are connected to dot-correction logic.
OUT0	7	O	Constant current output
OUT1	8	O	Constant current output
OUT2	10	O	Constant current output
OUT3	11	O	Constant current output
OUT4	12	O	Constant current output
OUT5	13	O	Constant current output

**Terminal Functions (continued)**

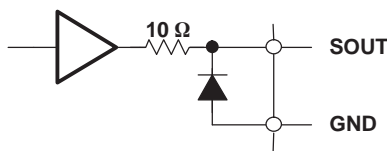
TERMINAL NAME	NO.	I/O	DESCRIPTION
OUT6	15	O	Constant current output
OUT7	16	O	Constant current output
OUT8	17	O	Constant current output
OUT9	18	O	Constant current output
OUT10	20	O	Constant current output
OUT11	21	O	Constant current output
OUT12	22	O	Constant current output
OUT13	23	O	Constant current output
OUT14	25	O	Constant current output
OUT15	26	O	Constant current output
PGND	6, 14, 19, 24, 27		Power ground
SCLK	4	I	Data shift clock. Note that the internal connections are switched by MODE (pin #30). At SCLK↑, the shift-registers selected by MODE shift the data.
SIN	5	I	Data input of serial I/F
SOUT	28	O	Data output of serial I/F
VCC	32		Power supply voltage
NC	29	–	Not Connected
XLAT	3	I	Data latch. Note that the internal connections are switched by MODE (pin #30). At XLAT↑, the latches selected by MODE get new data.

**PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS**

(Note: Resistor values are equivalent resistance and not tested).



**Figure 2. Input Equivalent Circuit (BLANK, XLAT, SCLK, SIN, MODE)**



**Figure 3. Output Equivalent Circuit**

PARAMETER MEASUREMENT INFORMATION

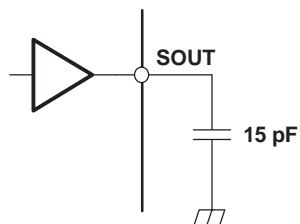


Figure 4. Test Circuit for  $t_{r0}$ ,  $t_{f0}$ ,  $t_{d0}$ ,  $t_{d1}$

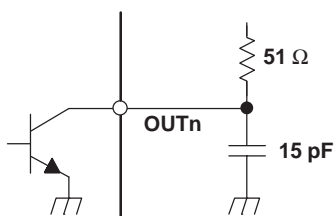


Figure 5. Test Circuit for  $t_{r1}$ ,  $t_{f1}$ ,  $t_{pd2}$ ,  $t_{pd3}$ ,  $t_{pd4}$

## PRINCIPLES OF OPERATION

### Setting Maximum Channel Current

The maximum output current per channel is set by a single external resistor,  $R_{(IREF)}$ , which is placed between IREF and GND. The voltage on IREF is set by an internal band gap  $V_{(IREF)}$  with a typical value of 1.24V. The maximum channel current is equivalent to the current flowing through  $R_{(IREF)}$  multiplied by a factor of 40. The maximum output current can be calculated by Equation 1:

$$I_{MAX} = \frac{V_{IREF}}{R_{IREF}} \times 40 \tag{1}$$

where:

$V_{IREF} = 1.24V$  typ.

$R_{IREF} =$  User selected external resistor ( $R_{IREF}$  should not be smaller than 600  $\Omega$ )

Figure 6 shows the maximum output current,  $I_{O(LC)}$ , versus  $R_{(IREF)}$ . In Figure 6,  $R_{(IREF)}$  is the value of the resistor between IREF terminal to ground, and  $I_{O(LC)}$  is the constant output current of OUT0,.....OUT15.

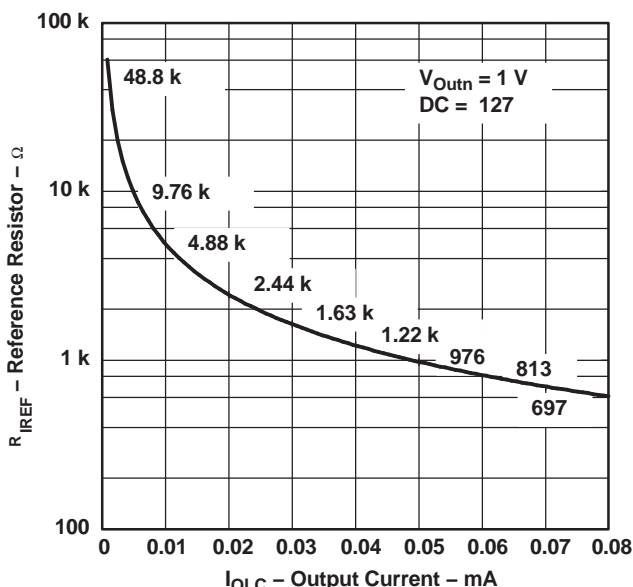


Figure 6. Reference Resistor vs Output Current

### Setting Dot-Correction

The TLC5922 has the capability to fine adjust the current of each channel, OUT0 to OUT15 independently. This is also called dot correction. This feature is used to adjust the brightness deviations of LED connected to the output channels OUT0 to OUT15. Each of the 16 channels can be programmed with a 7-bit word. The channel output can be adjusted in 128 steps from 0% to 100% of the maximum output current  $I_{MAX}$ . Equation 2 determines the output current for each OUTn:

$$I_{Outn} = \frac{I_{MAX} \times DC_n}{127} \tag{2}$$

where:

$I_{Max}$  = the maximum programmable current of each output

$DC_n$  = the programmed dot-correction value for output n ( $DC_n = 0, 1, 2 \dots 127$ )

$n = 0, 1, 2 \dots 15$

Dot-correction data are entered for all channels at the same time. The complete dot-correction data format consists of 16 x 7-bit words, which forms a 112-bit wide serial data packet. The channel data is put one after another. All data is clocked in with MSB first. Figure 7 shows the DC data format.

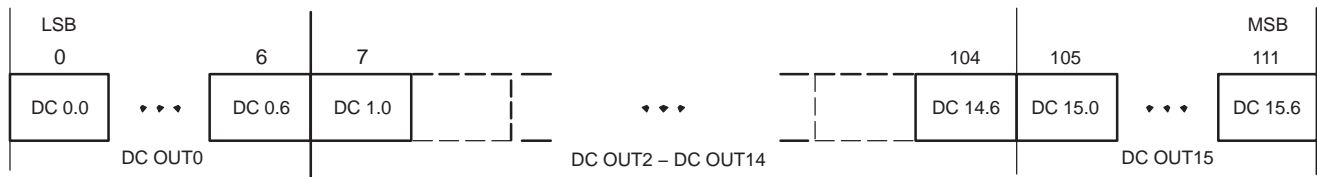


Figure 7. DC Data Format

MODE must be set to high to input data into the dot-correction register. The internal input shift register is then set to 112-bit width. After all serial data is clocked in, a rising edge of XLAT latches the data to the dot-correction register (Figure 10).

**Output Enable**

All OUTn channels of TLC5922 can be switched off with one signal. When BLANK signal is set to high, all OUTn are disabled, regardless of On/Off status of each OUTn. When BLANK is set to low, all OUTn work under normal conditions.

Table 1. BLANK Signal Truth Table

BLANK	OUT0 - OUT15
LOW	Normal condition
HIGH	Disabled

**Setting Channel On/Off Status**

All OUTn channels of TLC5922 can be switched on or off independently. Each of the channels can be programmed with a 1-bit word. On/Off data are entered for all channels at the same time. The complete On/Off data format consists of 16 x 1-bit words, which form a 16-bit wide data packet. The channel data is put one after another. All data is clocked in with MSB first. Figure 8 shows the On/Off data format.

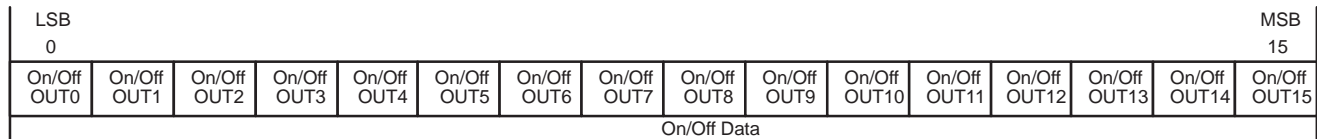


Figure 8. On/Off Data

MODE must be set to low to input On/Off data into the On/Off register. The internal input shift register is then set to 16-bit width. After all serial data is clocked in, a rising edge of XLAT, during BLANK = high, is used to latch data into the On/Off register. Figure 10 shows the On/Off data input timing chart.

**Delay Between Outputs**

The TLC5922 has graduated delay circuits between outputs. These delay circuits can be found in the constant current block of the device (see Figure 1). The fixed delay time is 20 ns (typical), OUT0 has no delay, OUT1 has 20-ns delay, OUT2 has 40-ns delay, etc. This delay prevents large inrush currents, which reduce power supply bypass capacitor requirements when the outputs turn on.



### Serial Interface Data Transfer Rate

The TLC5922 includes a flexible serial interface, which can be connected to a microcontroller or digital signal processor. Only 3 pins are required to input data into the device. The rising edge of SCLK signal shifts the data from SIN pin to internal shift register. After all data is clocked in, a rising edge of XLAT latches the serial data to the internal registers. All data is clocked in with MSB first. Multiple TLC5922 devices can be cascaded by connecting SOUT pin of one device to the SIN pin of following device.

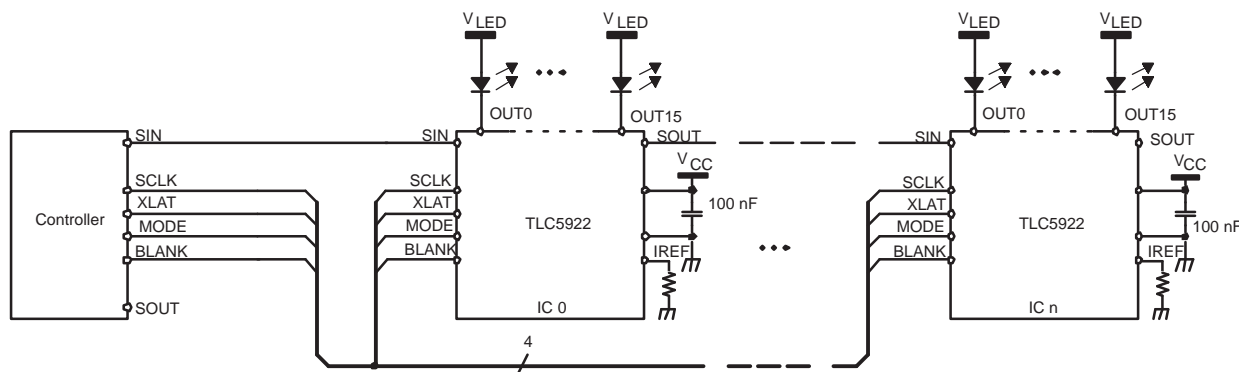


Figure 9. Cascading Devices

Figure 9 shows an example application with  $n$  cascaded TLC5922 devices connected to a controller. The maximum number of cascaded TLC5922 devices depends on the application system, and data transfer rate. Equation 3 calculates the minimum data input frequency needed.

$$f_{(SCLK)} = 112 \times f_{(update)} \times n \tag{3}$$

where:

$f_{(SCLK)}$ : The minimum data input frequency for SCLK and SIN.

$f_{(update)}$ : The update rate of the whole cascaded system.

$n$ : The number of cascaded TLC5922 devices.

### Operating Modes

The TLC5922 has different operating modes, depending on the MODE signal. Table 2 shows the available operating modes.

Table 2. TLC5922 Operating Modes Truth Table

MODE SIGNAL	INPUT SHIFT REGISTER	MODE
LOW	16 bit	On/Off Mode
HIGH	112 bit	Dot-Correction Data Input Mode

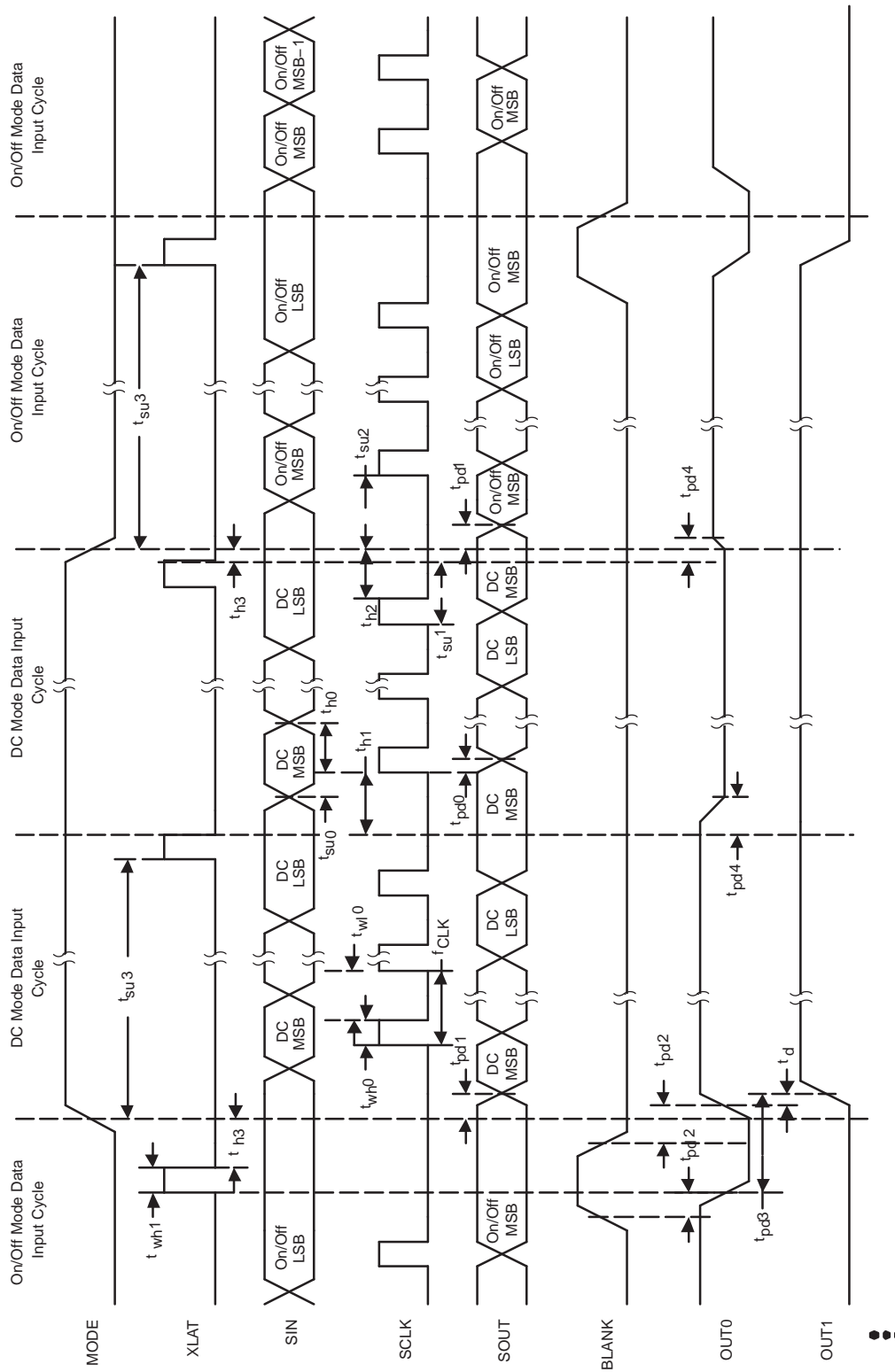
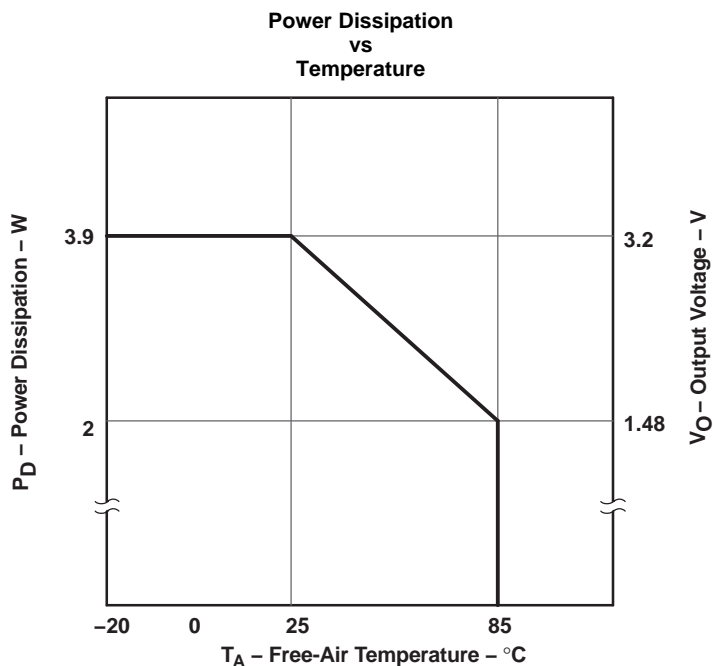


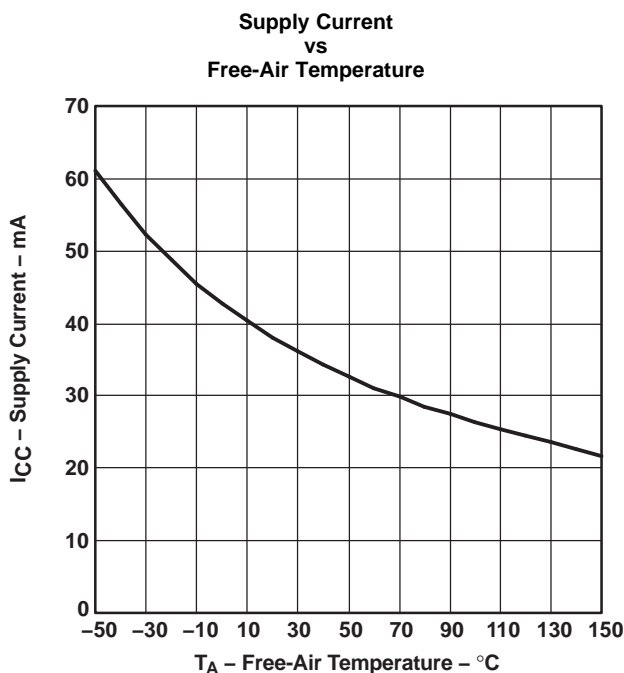
Figure 10. Timing Chart Example for ON/OFF Setting to Dot-Correction

**Power Rating - Free-Air Temperature**

Figure 11 shows total power dissipation. Figure 12 shows supply current versus free-air temperature.



**Figure 11.**



Data Transfer = 30 MHz / All Outputs, ON/VO = 1 V / RIREF = 600 Ω / AVDD = 5 V

**Figure 12.**

### REVISION HISTORY

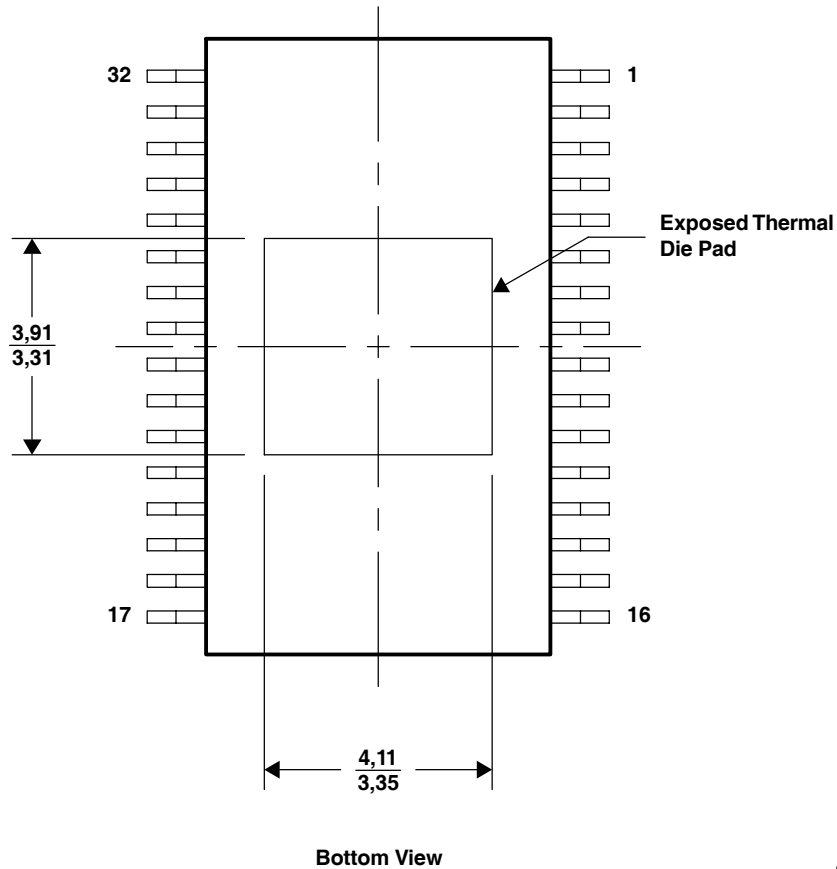
NOTE: Page numbers of current version may differ from previous versions.

Changes from Revision A (March 2005) to Revision B	Page
• Changed Propagation delay time $t_{PD0}$ and $t_{PD1}$ from 300 ns MAX (typographical error) to 30 ns MAX .....	4

**THERMAL INFORMATION**

The DAP PowerPAD™ package incorporates an exposed thermal die pad that is designed to be attached directly to an external heat sink. When the thermal die pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal die pad can be attached directly to a ground plane or special heat sink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPAD Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002 and Application Brief, *PowerPAD Made Easy*, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com. See Figure 1 for DAP package exposed thermal die pad dimensions.



PPTD001

NOTE: All linear dimensions are in millimeters.

**Figure 1. DAP Package Exposed Thermal Die Pad Dimensions**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLC5922DAP	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-20 to 85	TLC5922	<a href="#">Samples</a>
TLC5922DAPG4	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-20 to 85	TLC5922	<a href="#">Samples</a>
TLC5922DAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-20 to 85	TLC5922	<a href="#">Samples</a>
TLC5922DAPRG4	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-20 to 85	TLC5922	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

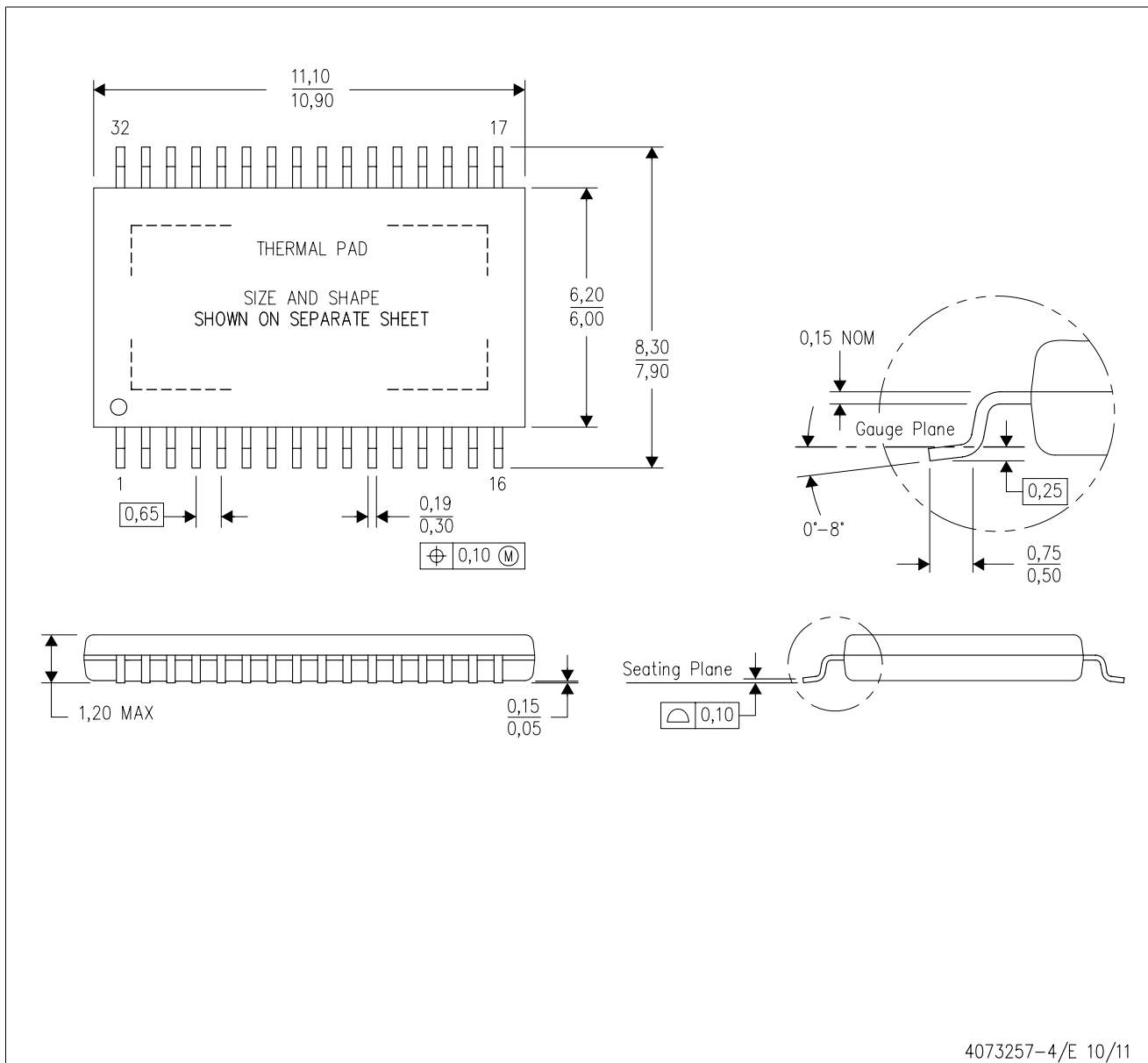
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# MECHANICAL DATA

DAP (R-PDSO-G32) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
- △ Falls within JEDEC MO-153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.



# THERMAL PAD MECHANICAL DATA

DAP (R-PDSO-G32)

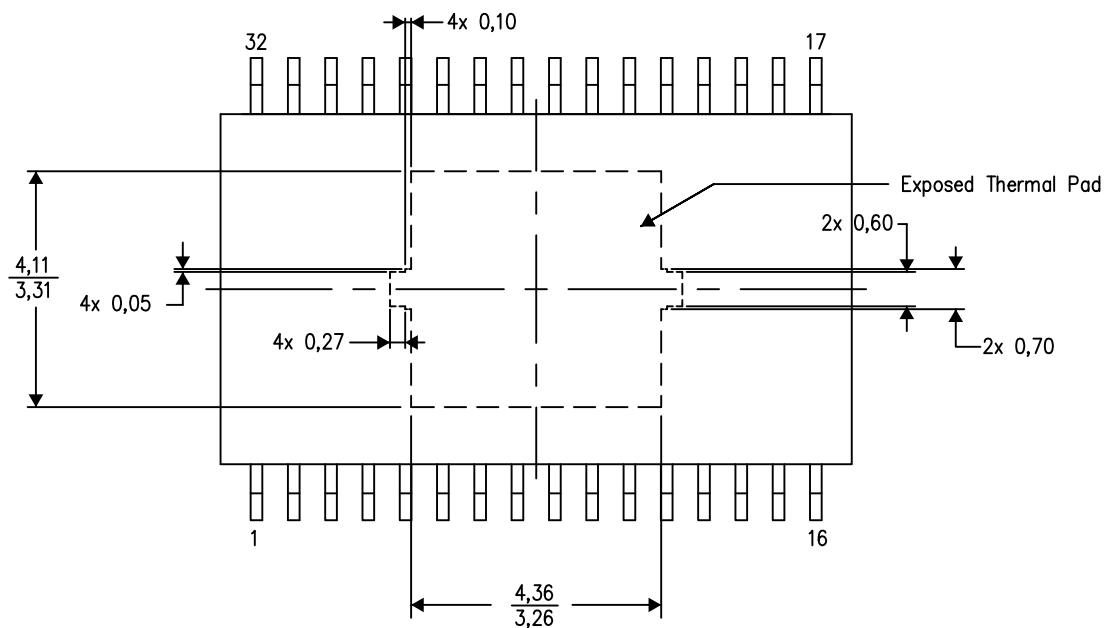
PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View  
Exposed Thermal Pad Dimensions

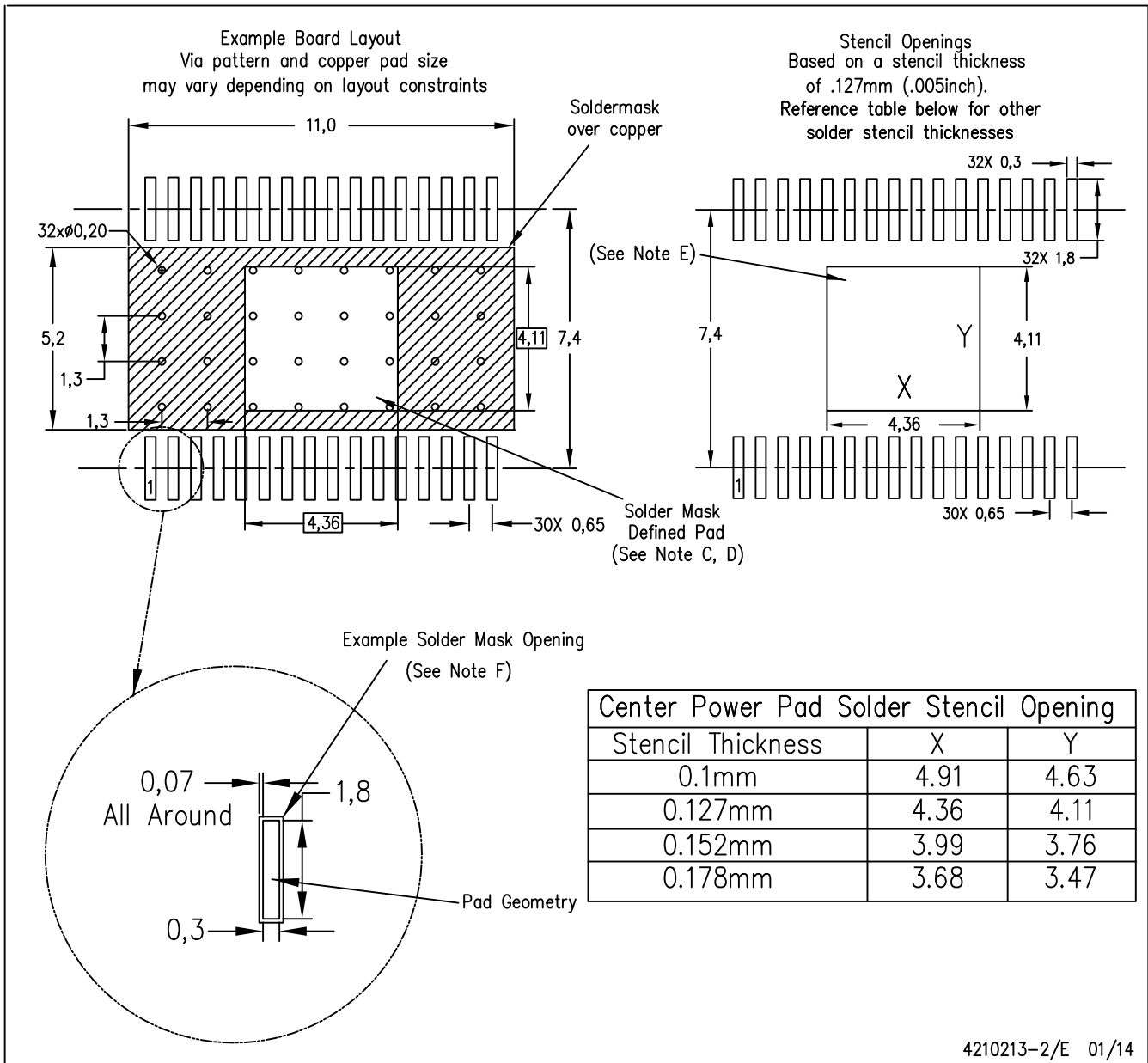
4206319-3/M 09/13

NOTE: All linear dimensions are in millimeters

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# LAND PATTERN DATA

## DAP (R-PDSO-G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Contact the board fabrication site for recommended soldermask tolerances.

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