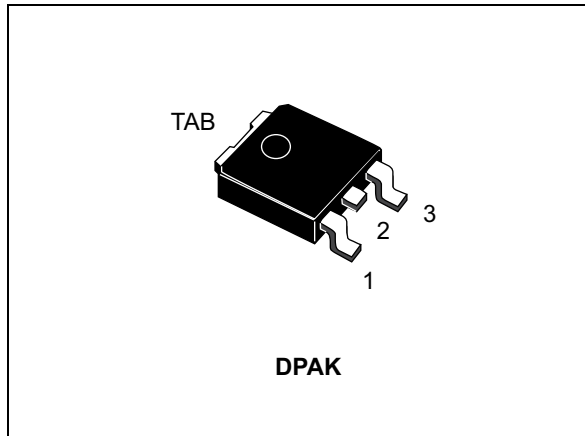


Automotive-grade N-channel 30 V, 0.0045 Ω typ, 80 A STripFET H5 Power MOSFET in a DPAK package

Datasheet - production data



Features

Order code	V_{DSS}	$R_{DS(on) max}$	I_D
STD86N3LH5	30 V	< 0.005 Ω	80 A

- Designed for automotive applications and AEC-Q101 qualified
- Low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power losses

Application

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™ H5 technology. The device has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Figure 1. Internal schematic diagram

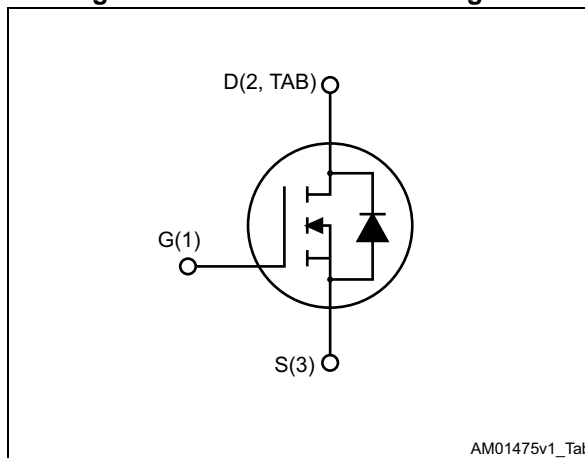


Table 1. Device summary

Order code	Marking	Package	Packaging
STD86N3LH5	86N3LH5	DPAK	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuit	8
4	Package information	10
5	Packing information	14
6	Revision history	16

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0\text{ V}$)	30	V
V_{DS}	Drain-source voltage ($V_{GS} = 0\text{ V}$) @ T_{JMAX}	35	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	55	A
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	W
	Derating factor	0.47	W/ $^\circ\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy	165	mJ
T_{stg}	Storage temperature	-55 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature	175	$^\circ\text{C}$

1. Limited by wire bonding
2. Pulse width limited by safe operating area
3. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 40\text{ A}$, $V_{DD} = 25\text{ V}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.14	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	50	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4 Oz Cu board

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	30	-	-	V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0\ \text{V}$)	$V_{DS} = 20\ \text{V}$ $V_{DS} = 20\ \text{V}$, $T_c = 125\text{ °C}$	-	-	1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0\ \text{V}$)	$V_{GS} = \pm 20\ \text{V}$	-	-	± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1	1.8	2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ \text{V}$, $I_D = 40\ \text{A}$	-	0.0045	0.005	Ω
		$V_{GS} = 5\ \text{V}$, $I_D = 40\ \text{A}$	-	0.0055	0.0065	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0\ \text{V}$	-	1850	-	pF
C_{oss}	Output capacitance		-	380	-	pF
C_{rss}	Reverse transfer capacitance		-	58	-	pF
Q_g	Total gate charge	$V_{DD} = 15\ \text{V}$, $I_D = 80\ \text{A}$ $V_{GS} = 5\ \text{V}$ <i>Figure 16</i>	-	14	-	nC
Q_{gs}	Gate-source charge		-	6.8	-	nC
Q_{gd}	Gate-drain charge		-	4.7	-	nC
Q_{gs1}	Pre V_{th} gate-to-source charge	$V_{DD} = 15\ \text{V}$, $I_D = 80\ \text{A}$ $V_{GS} = 5\ \text{V}$ <i>Figure 16</i>	-	2.3	-	nC
Q_{gs2}	Post V_{th} gate-to-source charge		-	4.5	-	nC
R_G	Gate input resistance	$f = 1\ \text{MHz}$ gate bias Bias = 0 test signal level = 20 mV, open drain	-	1.2	-	Ω

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$, $I_D = 40\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 5\text{ V}$ <i>Figure 15</i>	-	6	-	ns
t_r	Rise time		-	14	-	ns
$t_{d(off)}$	Turn-off delay time		-	23.6	-	ns
t_f	Fall time		-	10.8	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		80	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				320	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 40\text{ A}$, $V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 80\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 20\text{ V}$ <i>Figure 17</i>	-	31.8		ns
Q_{rr}	Reverse recovery charge		-	26.1		nC
I_{RRM}	Reverse recovery current		-	1.6		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

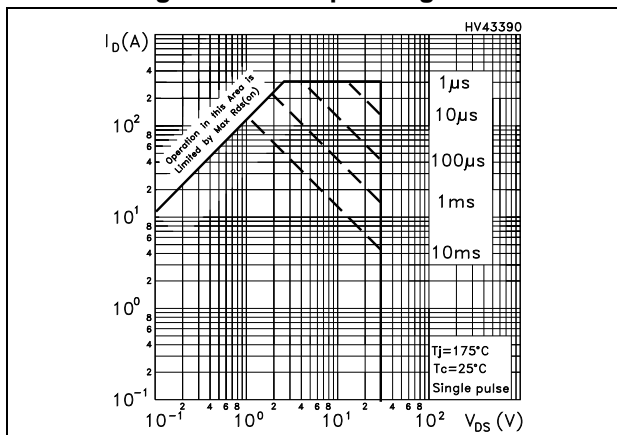


Figure 3. Thermal impedance

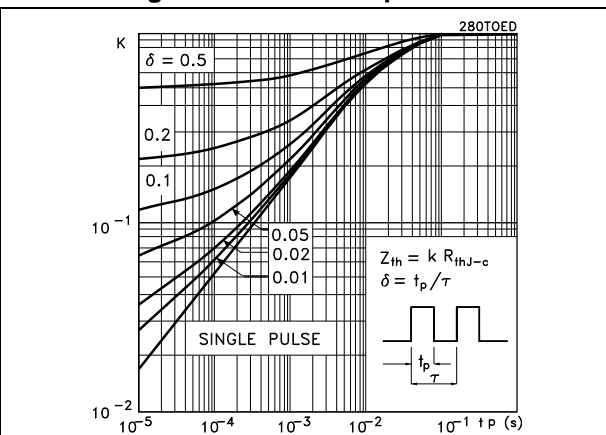


Figure 4. Output characteristics

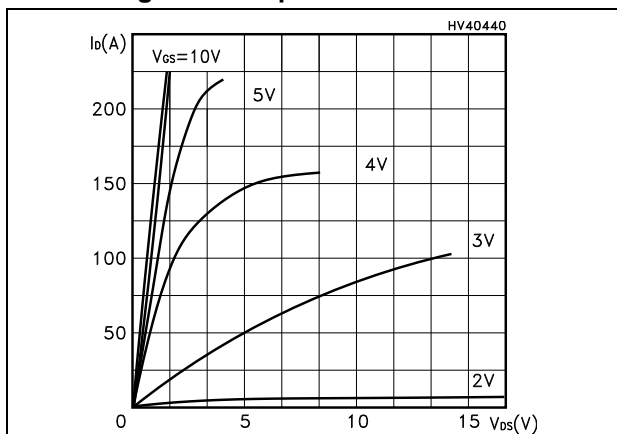


Figure 5. Transfer characteristics

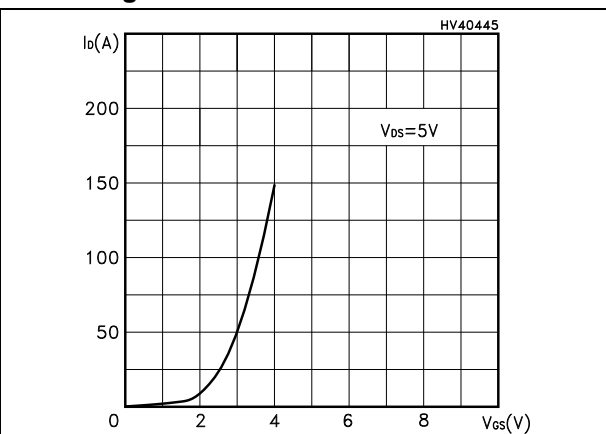


Figure 6. Normalized B_{VDSS} vs temperature

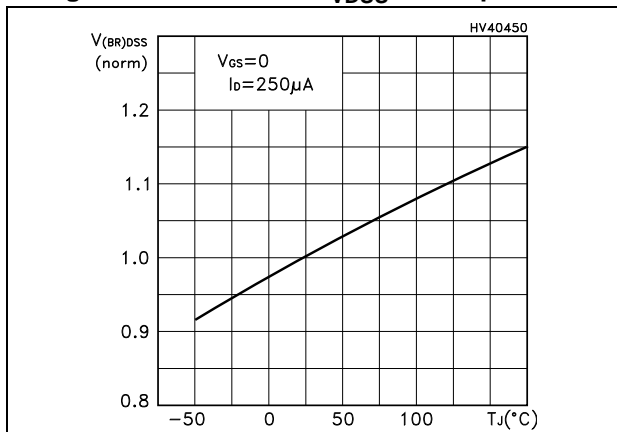


Figure 7. Static drain-source on resistance

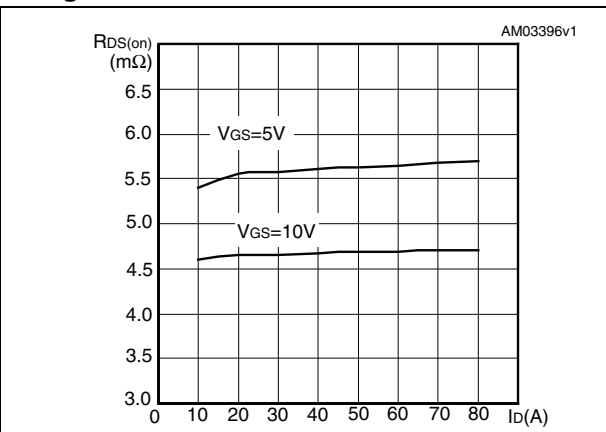


Figure 8. Gate charge vs gate-source voltage

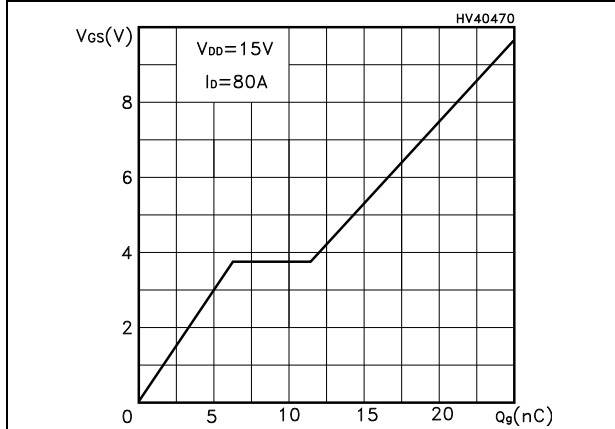


Figure 9. Capacitance variations

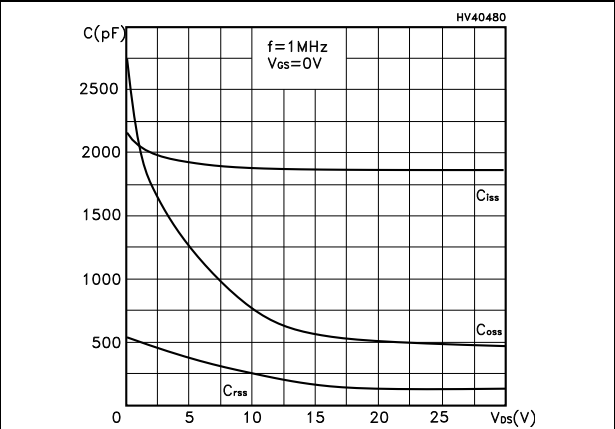


Figure 10. Normalized gate threshold voltage vs temperature

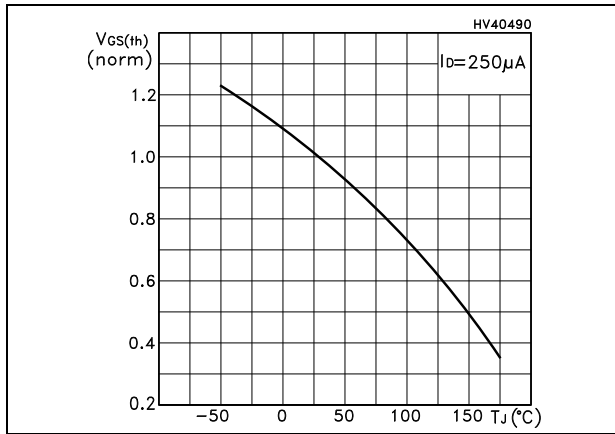


Figure 11. Normalized on resistance vs temperature

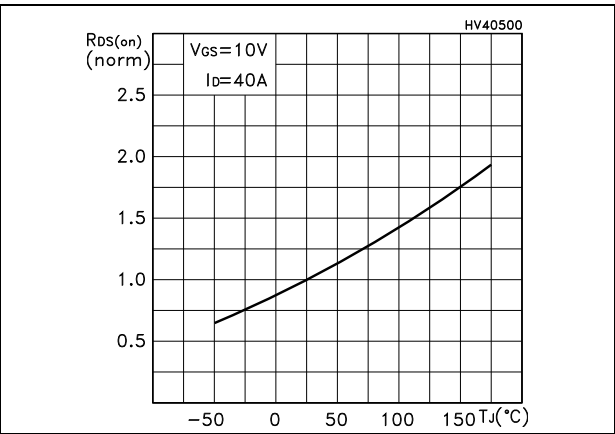
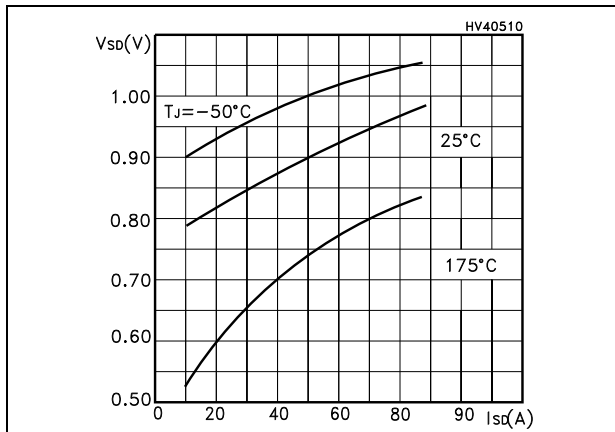


Figure 12. Source-drain diode forward characteristics



3 Test circuit

Figure 13. Switching times test circuit for resistive load



Figure 14. Gate charge test circuit

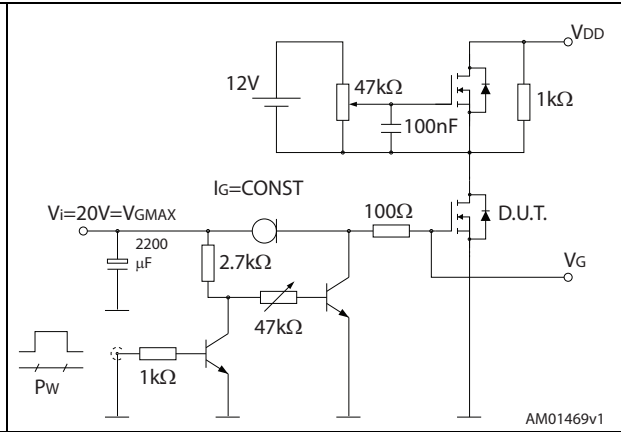


Figure 15. Test circuit for inductive load switching and diode recovery times



Figure 16. Unclamped inductive load test circuit



Figure 17. Unclamped inductive waveform

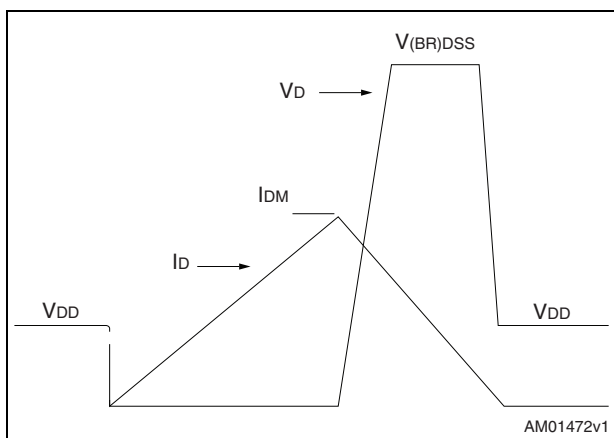


Figure 18. Switching time waveform

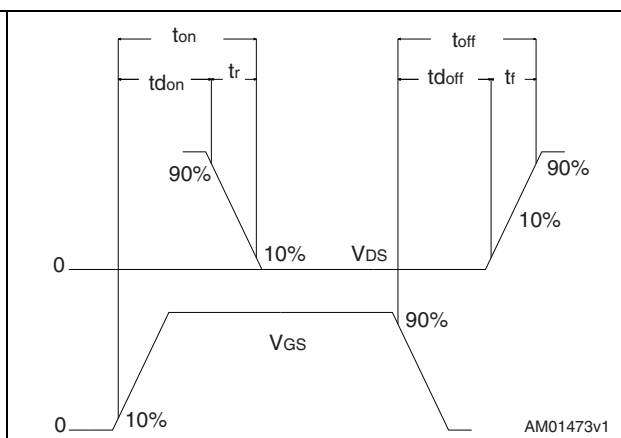
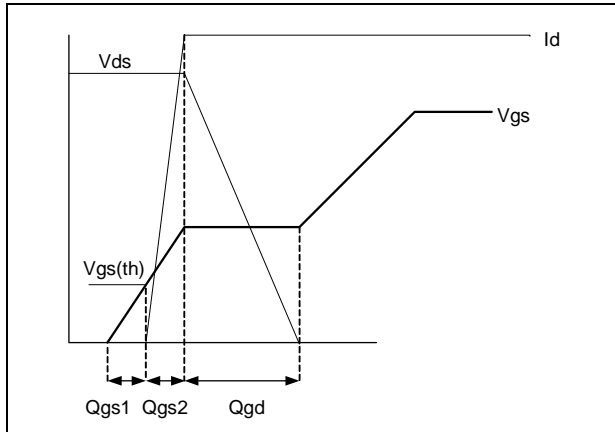


Figure 19. Gate charge waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 20. DPAK (TO-252) type A2 outline

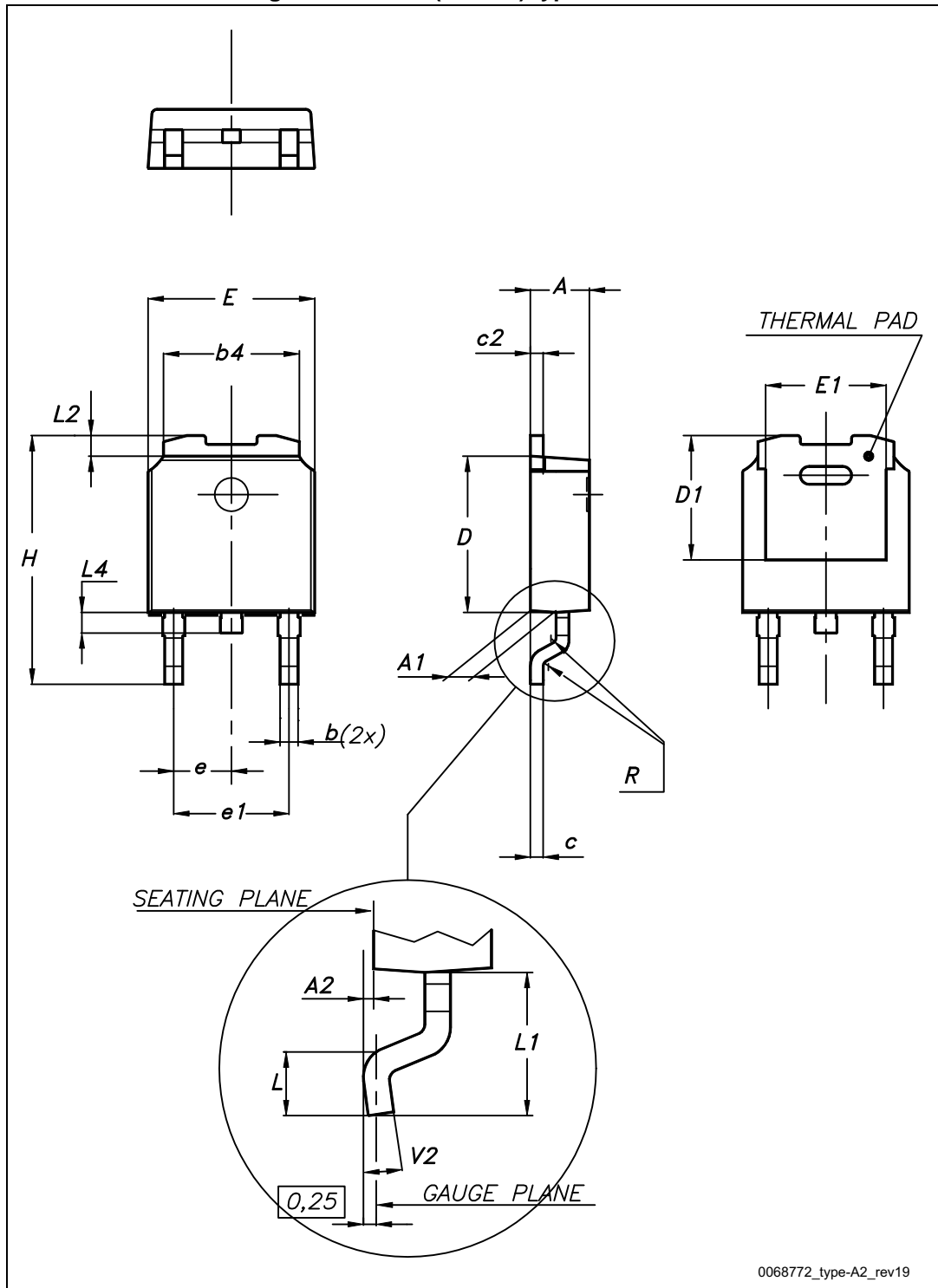
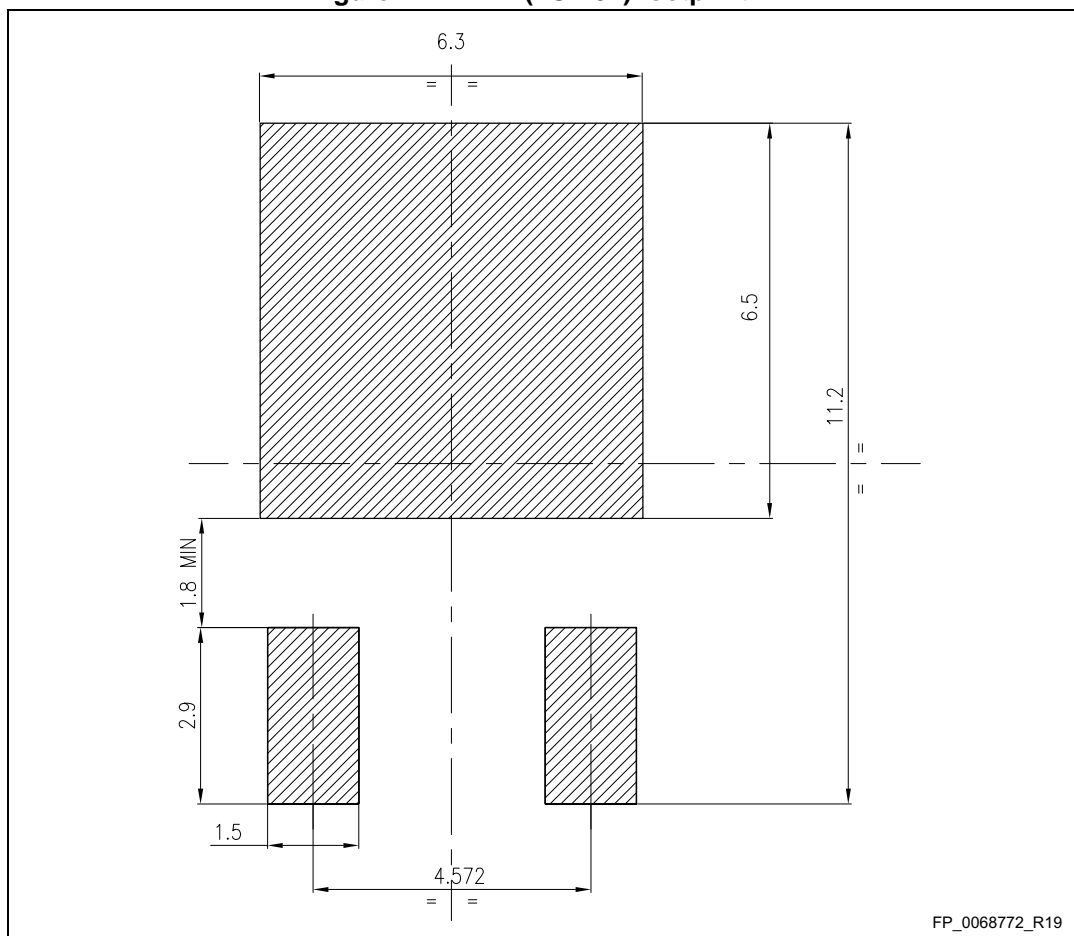


Table 8. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 21. DPAK (TO-252) footprint (a)



a. All dimensions are in millimeters

5 Packing information

Figure 22. Tape for DPAK (TO-252)

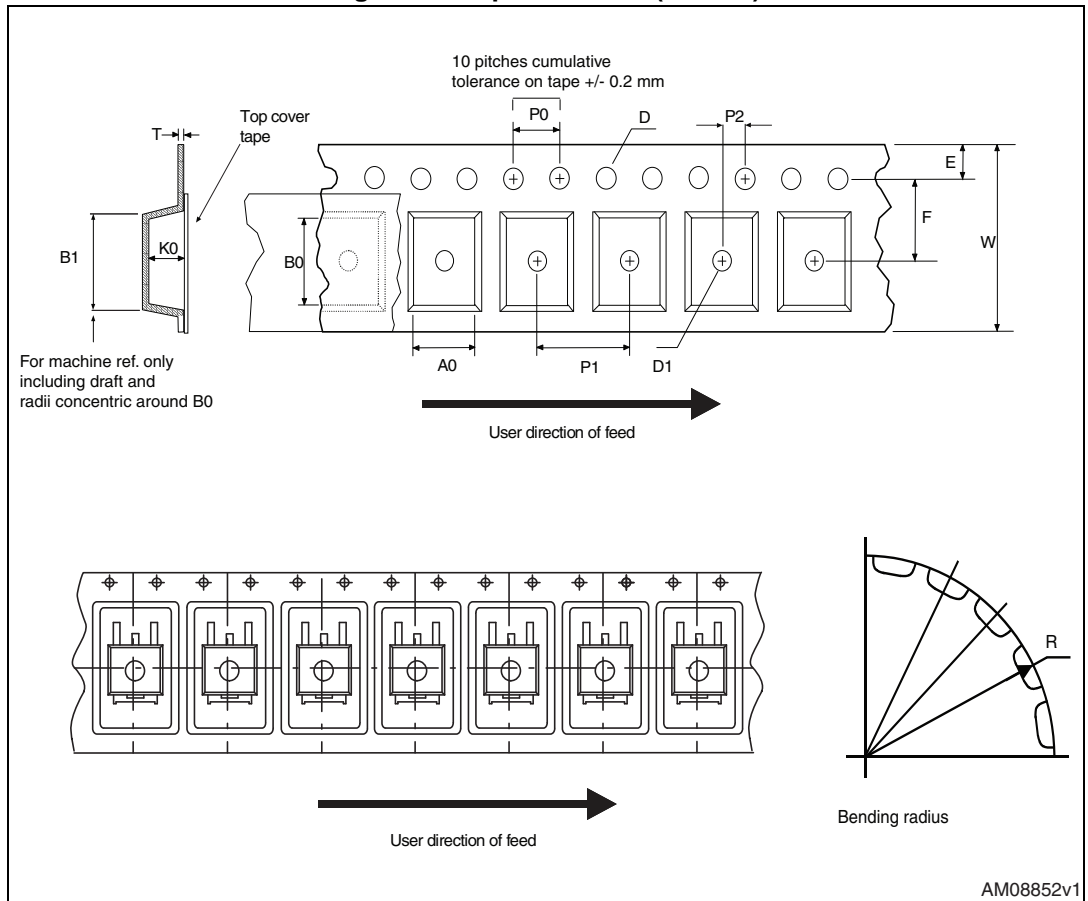


Figure 23. Reel for DPAK (TO-252)

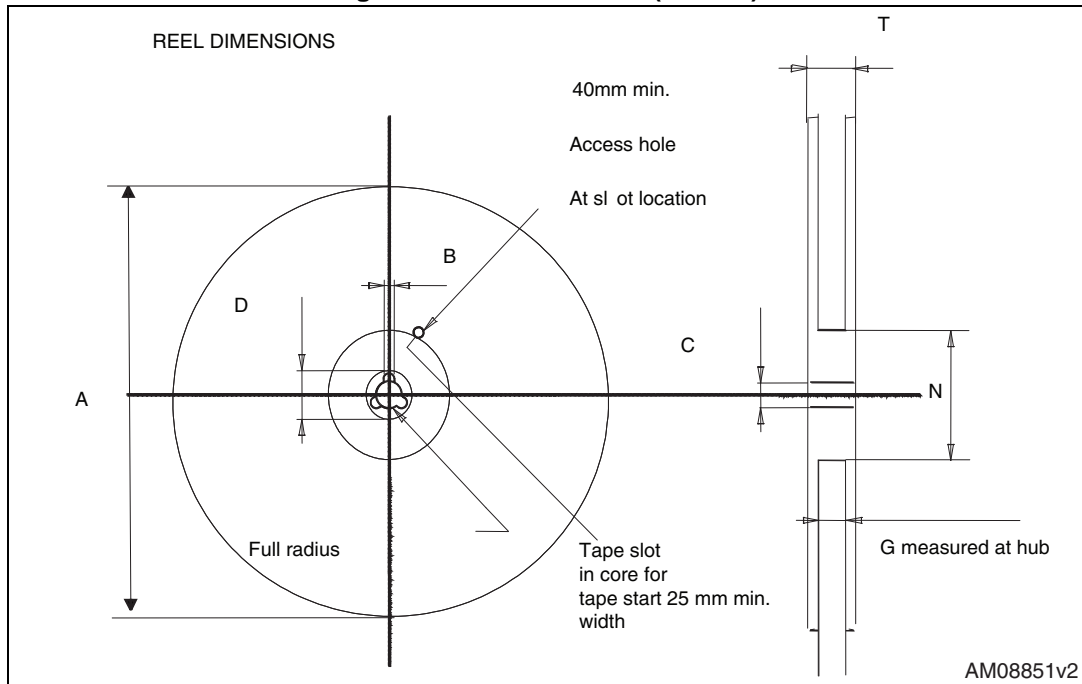


Table 9. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
10-Apr-2009	1	First release.
22-Mar-2011	2	V_{GS} value has been corrected in Table 2 and Table 4 .
13-May-2015	3	Updated title, features and description in cover page. Updated Section 4: Package information .

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