SM72295 Photovoltaic Full Bridge Driver

Check for Samples: SM72295

FEATURES

- **Renewable Energy Grade**
- **Dual Half Bridge MOSFET Drivers**
- **Integrated 100V Bootstrap Diodes**
- **Independent High and Low Driver Logic Inputs**
- **Bootstrap Supply Voltage Range up to 115V DC**
- **Two Current Sense Amplifiers with Externally Programmable Gain and Buffered Outputs**
- **Programmable Over Voltage Protection**
- **Supply Rail Under-Voltage Lockouts with Power Good Indicator**

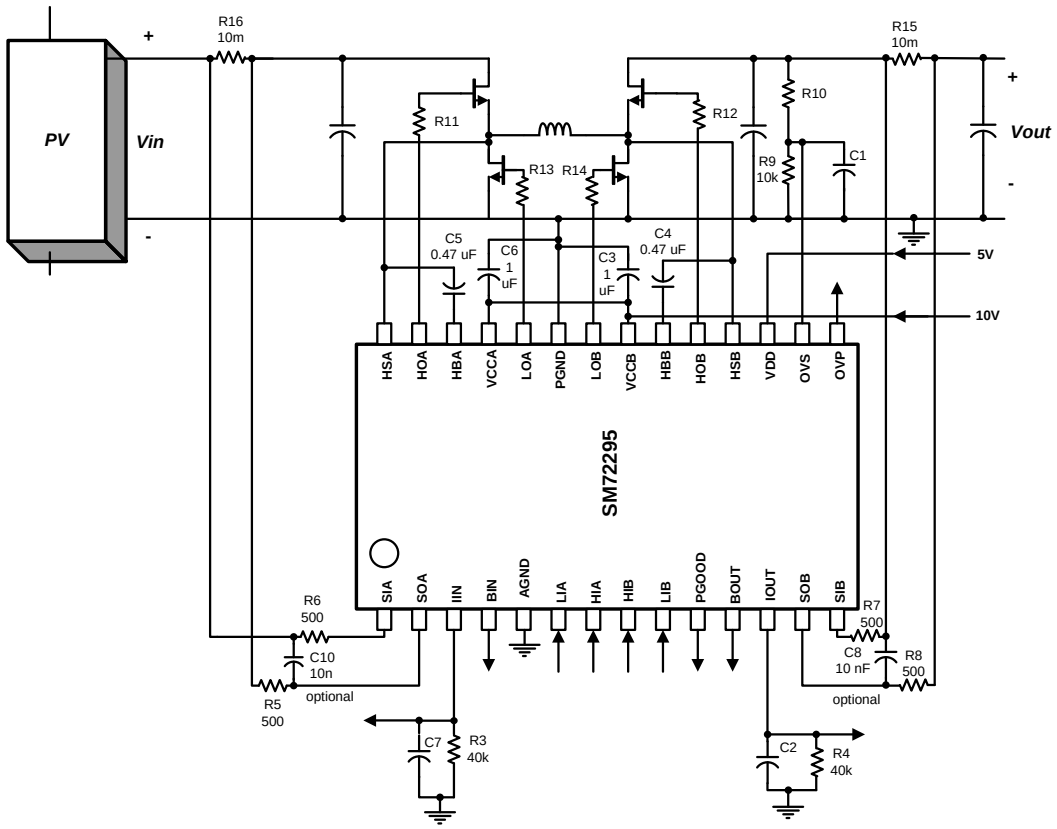
PACKAGE

- **SOIC-28**

DESCRIPTION

The SM72295 is designed to drive 4 discrete N type MOSFET's in a full bridge configuration. The drivers provide 3A of peak current for fast efficient switching and integrated high speed bootstrap diodes. Current sensing is provided by 2 transconductance amplifiers with externally programmable gain and filtering to remove ripple current to provide average current information to the control circuit. The current sense amplifiers have buffered outputs available to provide a low impedance interface to an A/D converter if needed. An externally programmable input over voltage comparator is also included to shutdown all outputs. Under voltage lockout with a PGOOD indicator prevents the drivers from operating if VCC is too low.

Typical Application Circuit



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Connection Diagram

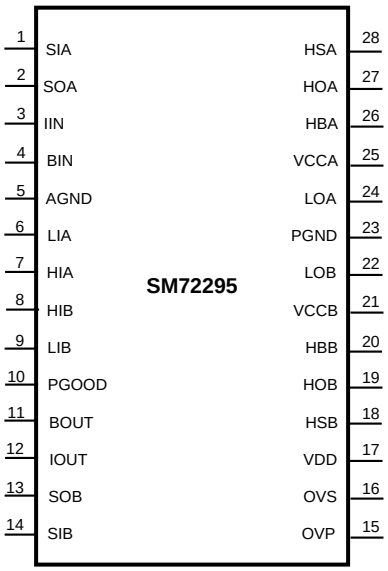


Figure 1. Top View
SOIC-28

PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	SIA	Sense high input for input current sense transconductance amplifier	Tie to positive side of the current sense resistor through an external gain programming resistor (RI). Amplifier transconductance is 1/RI.
2	S0A	Sense low input for input current sense transconductance amplifier	Tie to negative side of the current sense resistor through an external gain programming resistor. Amplifier transconductance is 1/RI.
3	IIN	Output for current sense transconductance amplifier	Output of the input current sense amplifier. Requires an external resistor to ground (RL). Gain is RL/RI, where RI is the external resistor in series with the SIA pin.
4	BIN	Buffered IIN	Buffered IIN.
5	AGND	Analog ground	Ground return for the analog circuitry. Tie to the ground plane under the IC
6, 9	LIA, LIB	Low side driver control input	The inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
7, 8	HIA, HIB	High side driver control input	The inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
10	PGOOD	Power good indicator output	Open drain output with an internal pull-up resistor to VDD indicating VCC is in regulation. PGOOD low implies VCC is out of regulation.
11	BOUT	Buffered IOUT	Buffered IOUT.
12	IOUT	Output for current sense comparator.	Output of the output current sense amplifier. Requires an external resistor to ground (RL). Gain is RL/RI, where RI is the external resistor in series with the SIB pin.
13	S0B	Sense low input for output current sense amplifier	Tie to negative side of the current sense resistor through an external gain programming resistor. Amplifier transconductance is 1/RI.
14	SIB	Sense high input for output current sense amplifier	Tie to positive side of the current sense resistor through an external gain programming resistor (RI). Amplifier transconductance is 1/RI.
15	OVP	Over voltage indicator output	Open drain output with an internal pull-up resistor to VDD indicating OVS >VDD. OVP is low when OVS>VDD.
16	OVS	Sense input for over voltage	Requires an external resistor divider. VDD is the reference voltage.
17	VDD	3.3V or 5V regulator output	Bypass with 0.1uF. Reference for over voltage shutdown and IOUT/IIN clamp
18, 28	HSA, HSB	High side MOSFET source connection	Connect to bootstrap capacitor negative terminal and the source of the high side MOSFET.

PIN DESCRIPTIONS (continued)

Pin	Name	Description	Application Information
19, 27	HOA, HOB	High side gate driver output	Connect to gate of high side MOSFET with a short low inductance path.
20,26	HBA, HBB	High side gate driver bootstrap rail.	Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The bootstrap capacitor should be placed as close to IC as possible.
21,25	VCCA, VCCB	Positive gate drive supply	Locally decouple to PGND using low ESR/ESL capacitor located as close to IC as possible.
22, 24	LOA, LOB	Low side gate driver output	Connect to the gate of the low side MOSFET with a short low inductance path.
23	PGND	Power ground return	Ground return for the LO drivers. Tie to the ground plane under the IC

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

VCCA, VCCB		-0.3 to 14V
VDD		-0.3 to 7V
HBA to HSA, HBB to HSB		-0.3 to 15V
LIA,LIB,HIA,HIB,OVS		-0.3 to 7V
LOA,LOB		-0.3 to VCC+ 0.3V
HOA,HOB		HS–0.3 to HB + 0.3V
SIA,SOA,SIB,SOB		-0.3 to 100V
SIA to SOA, SIB to SOB		-0.8 to 0.8V
HSA,HSB(3)		-5 to 100V
HBA, HBB		115V
PGOOD, OVP		-0.3 to VDD
IIN, IOUT		-0.3 to VDD
BIN, BOUT		-0.3 to VDD
Junction Temperature		150°C
Storage Temperatue Range		-55°C to +150°C
ESD Rating(4)	Human Body Model	2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) In the application the HS nodes are clamped by the body diode of the external lower N-MOSFET, therefore the HS node will generally not exceed –1V. However, in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur, the HS voltage must never be more negative than VCC-15V. For example if VCC = 10V, the negative transients at HS must not exceed –5V.
(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. 2 kV for all pins except HB, HO & HS which are rated at 1000V.

Recommended Operating Conditions

VCCA,VCCB	+8V to +14V
VDD	+3V to 7V
SI, SO common mode	VDD+1V to 100V
HS(1)	-1V to 100V
HBA, HBB	HS+7V to HS+14V
HS Slew Rate	<50V/ns
Junction Temperature	-40°C to +125°C

(1) In the application the HS nodes are clamped by the body diode of the external lower N-MOSFET, therefore the HS node will generally not exceed –1V. However, in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur, the HS voltage must never be more negative than VCC-15V. For example if VCC = 10V, the negative transients at HS must not exceed –5V.

Electrical Characteristics(1)

Specifications in standard typeface are for T_J = 25°C, and those in boldface type apply over the full operating junction temperature range. No load on LO & HO, VCC = 10V, VDD = 5V, HB-HS = 10V, OVS = 0V unless otherwise indicated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SUPPLY CURRENTS						
I_{DD}	VDD Quiescent Current	SIA = SOB, SIB = SOB.		25	**40**	µA
I_{CC}	VCC Quiescent Current (ICCA+ICCB)	All outputs off		500	**800**	µA
I_{CCO}	VCC Operating Current (ICCA+ICCB)	LOA & LOB switching at 200kHz		2.2	**3**	mA
I_{HB}	HBA, HBB Quiescent Current	All outputs off		55	**200**	µA
I_{HBO}	HBA, HBB Operating Current	HOA & HOB switching at 200kHz		700	**1000**	µA
I_{HBS}	HBA & HBB to V_{SS} Current, Quiescent	HS = 100V, HB = 110V		0.1	**10**	µA
I_{HBSO}	HBA and HBB to V_{SS} Current, Operating	f = 200kHz		130		µA
PGOOD, OVB OUTPUTs						
V_{OL}	Output Low RDS			25	**50**	Ω
R_{PU}	VDD pull up resistor			50	**90**	kΩ
LI ,HI INPUT PINS						
V_{IL}	Input Voltage Threshold		**1.3**	1.8	**2.3**	V
V_{IHYS}	Input Voltage Hysteresis			50		mV
R_I	LI, HI Pull down Resistance		**100**	200	**400**	kΩ
OVER VOLTAGE SHUTDOWN						
V_{OVR}	OVS Rising Threshold		**VDD-50mV**	VDD	**VDD+50mV**	V
V_{OVH}	OVS threshold Hysteresis			5%		VDD
I_{OVS}	OVS input bias current	OVS<VDD		1		nA
UNDER VOLTAGE SHUTDOWN						
V_{CCR}	VCC Rising Threshold		**6**	6.9	**7.4**	V
V_{CCH}	VCC threshold Hysteresis			0.5		V
V_{HBR}	HB-HS Rising Threshold		**5.7**	6.6	**7.1**	V
V_{HBH}	HB-HS Threshold Hysteresis			0.4		V
BOOT STRAP DIODE						
V_{DH}	High-Current Forward Voltage	I_{VCC-HB} = 100mA		0.8	**1**	V
R_D	Dynamic Resistance	I_{VCC-HB} = 100mA		1	**1.65**	Ω

(1) Min and Max limits are 100% production tested at 25ºC. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics[1] (continued)

Specifications in standard typeface are for T_J = 25°C, and those in boldface type apply over the full operating junction temperature range. No load on LO & HO, VCC = 10V, VDD = 5V, HB-HS = 10V, OVS = 0V unless otherwise indicated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LO & HO GATE DRIVER						
V_{OL}	Low-Level Output Voltage	I_{LO} = 100mA V_{OL} = LO-PGND or HO-HS		0.16	**0.4**	V
V_{OH}	High-Level Output Voltage	I_{LO} = -100mA V_{OH} = VCC-LO or VCC-HO		0.28	**0.6**	V
I_{OHL}	Peak Pullup Current	HO, LO = 12V		3		A
I_{OLL}	Peak Pulldown Current	HO, LO = 0V		3		A
t_{LPHL}	LO Turn-Off Propagation Delay	LI Falling to LO Falling		22		ns
t_{LPLH}	LO Turn-On Propagation Delay	LI Rising to LO Rising		26		ns
t_{HPHL}	HO Turn-Off Propagation Delay	HI Falling to HO Falling		22		ns
t_{HPLH}	LO Turn-On Propagation Delay	HI Rising to HO Rising		26		ns
t_{MON}	Delay Matching: LO on & HO off			1		ns
t_{MOFF}	Delay Matching: LO off & HO on			1		ns
t_{RC}, t_{FC}	Either Output Rise/Fall Time	C_L = 1000pF		8		ns
t_{PW}	Minimum Input Pulse Width that Changes the Output			50		ns
t_{BS}	Bootstrap Diode Turn-On or Turn-Off Time	I_F = 100mA/ I_R = 100mA		37		ns
CURRENT SENSE AMPLIFIER						
V_{OS}	Offset voltage	R_{SI} = R_{SO} = 500, 10mV sense resistor voltage	**-2**		**2**	mV
Gain 5mV	Gain is programmed with external resistors IOUT, IIN =(RL/RSI)* (SI-SO)	5mV sense resistor voltage R_{SI} = R_{SO} = 1000, R_L = 75K		390		mV
Gain 50mV	Gain is programmed with external resistors IOUT, IIN =(RL/RSI)* (SI-SO)	50mV sense resistor voltage R_{SI} = R_{SO} = 1000, R_L = 75K		3.85		V
Vclamp	Output Clamp	0.1V sense resistor voltage R_{SI} = R_{SO} = 1000, R_L = 75K		VDD		V
CURRENT SENSE BUFFER						
	Offset voltage (BIN-IIN), (BOUT-IOUT)	IIN = 2.5V	**-60**		**60**	mV
	Output low voltage BOUT,BIN	IIN, IOUT = 0	**0**		**50**	mV
	Output high voltage BOUT,BIN	IIN, IOUT = VDD	**VDD-100mV**	VDD-30mV	**VDD**	mV
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	SOIC-28[2]		60		°C/W

(2) 2 layer board with 2 oz Cu using JEDEC JESD51 thermal board.

Block Diagram

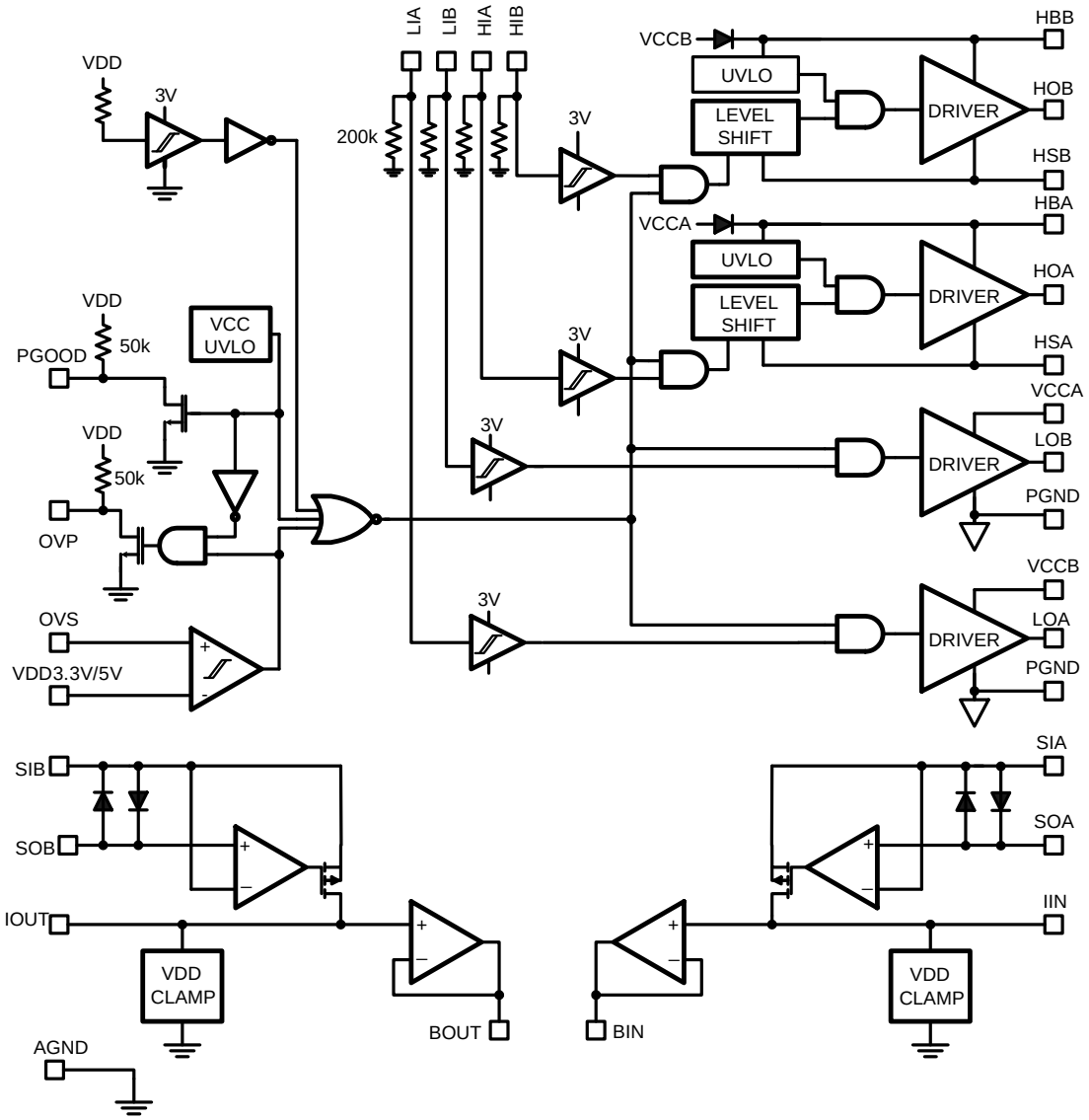


Figure 2. Block Diagram

Typical Performance Characteristics

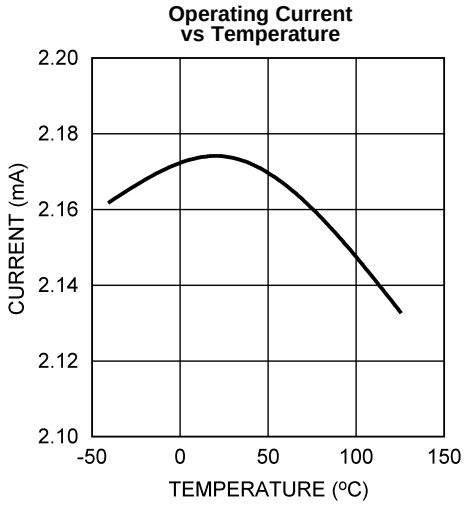


Figure 3.

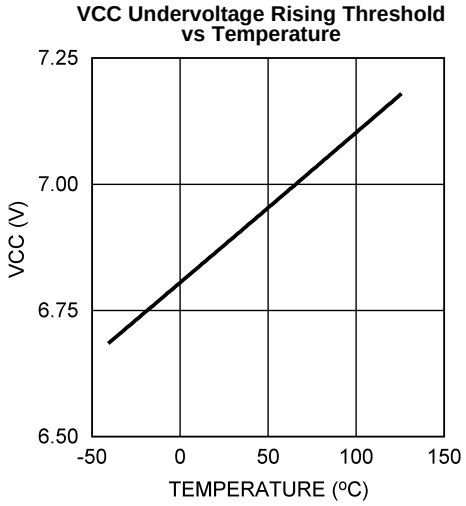


Figure 4.

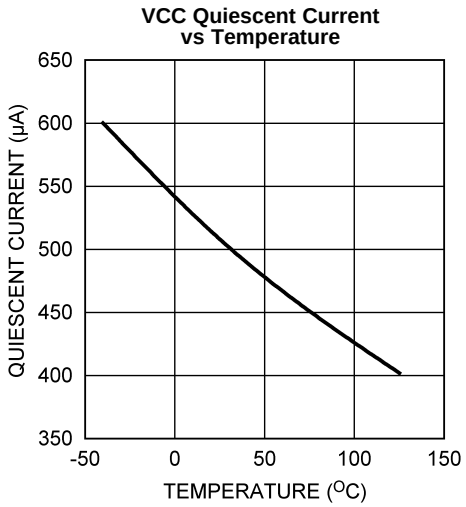
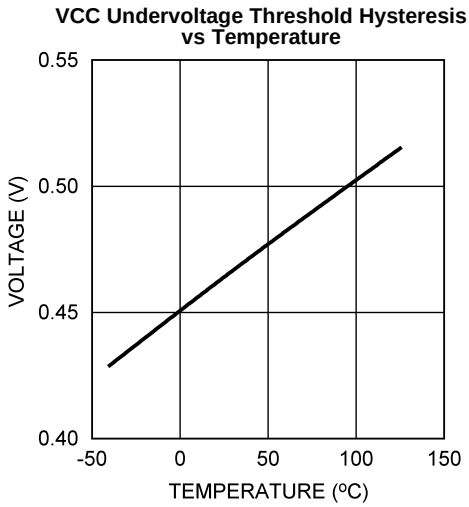


Figure 5.



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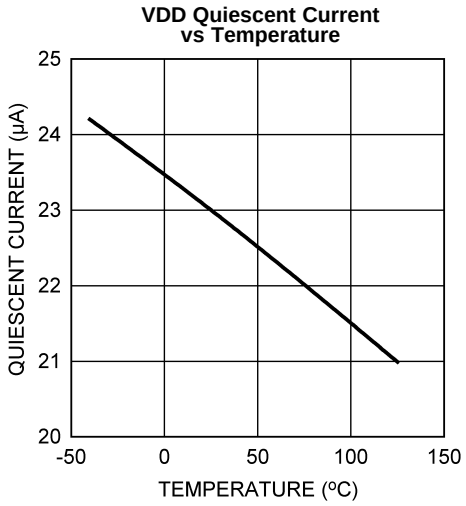

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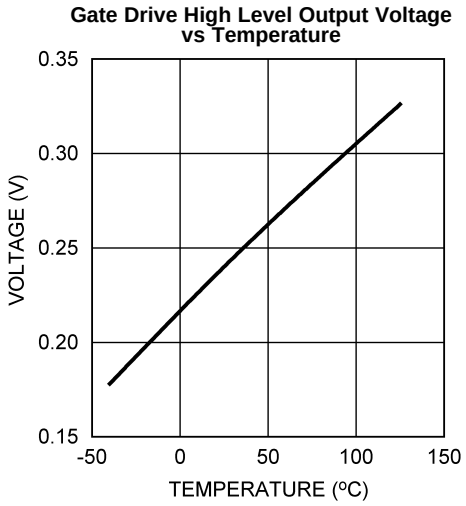


Figure 8.

Typical Performance Characteristics (continued)

Gate Drive Low level Output Voltage vs Temperature

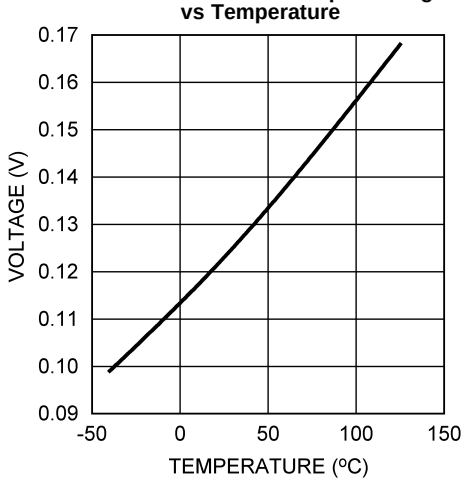


Figure 9.

Bootstrap Diode Forward Voltage vs Temperature

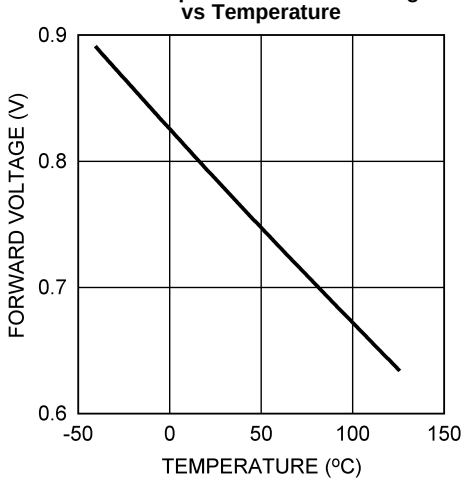


Figure 10.

Current Sense Amplifier Input Offset Voltage vs Temperature

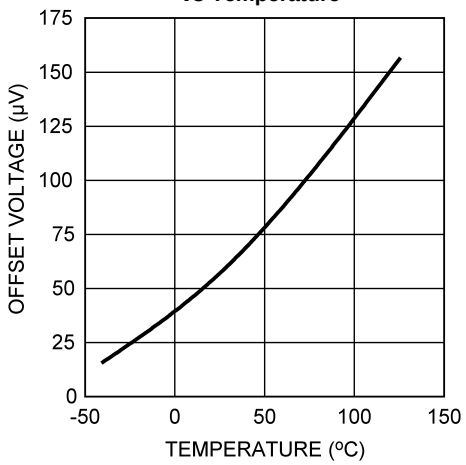


Figure 11.

Current Sense Amplifier Output Buffer Offset Voltage vs Temperature

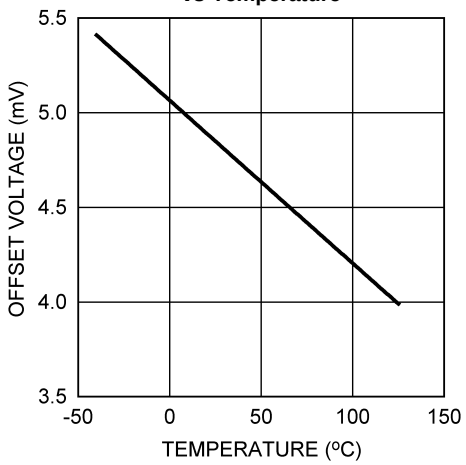
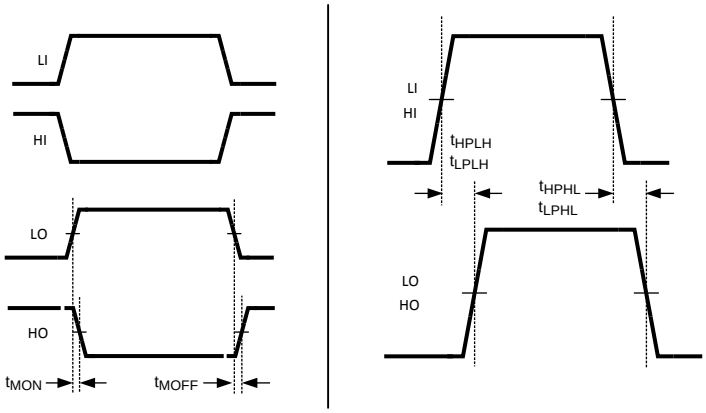


Figure 12.

Timing Diagram



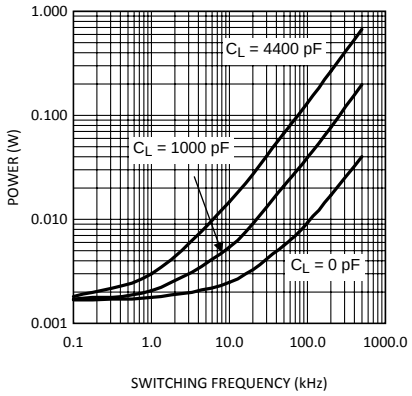
Power Dissipation Considerations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (V_{DD}) and can be roughly calculated as:

$$P_{DGATES} = 2 \bullet f \bullet C_L \bullet V_{DD}^2 \quad (1)$$

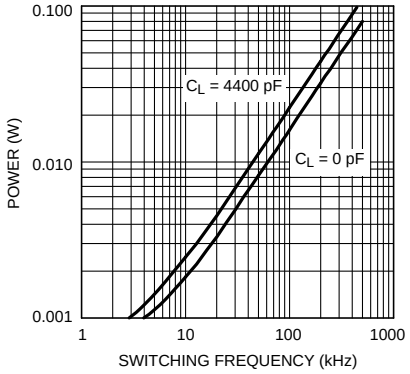
There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equation. This plot can be used to approximate the power losses due to the gate drivers.

Figure 13. Gate Driver Power Dissipation (LO + HO)
V_{CC} = 12V, Neglecting Diode Losses



The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more current to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge result in higher reverse recovery losses. The following plot was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation. The total IC power dissipation can be estimated from the previous plots by summing the gate drive losses with the bootstrap diode losses for the intended application.

Figure 14. Diode Power Dissipation V_{IN} = 50V



Layout Considerations

The optimum performance of high and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. Low ESR / ESL capacitors must be connected close to the IC, between VDD and VSS pins and between the HB and HS pins to support the high peak currents being drawn from VDD during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (VSS).
3. In order to avoid large negative transients on the switch node (HS pin), the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding Considerations:
   (a) The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gate into a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
   (b) The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SM72295MA/NOPB	ACTIVE	SOIC	DW	28	26	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	S72295	Samples
SM72295MAX/NOPB	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	S72295	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

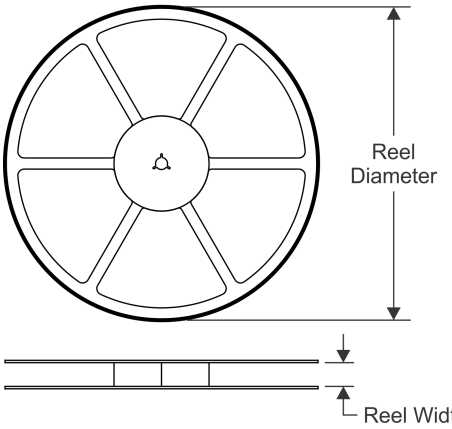
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

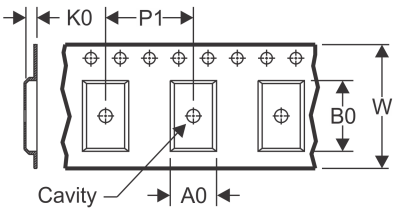
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

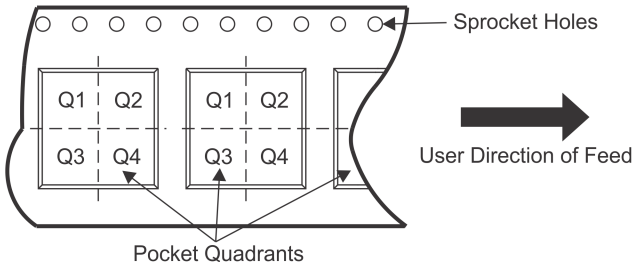


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

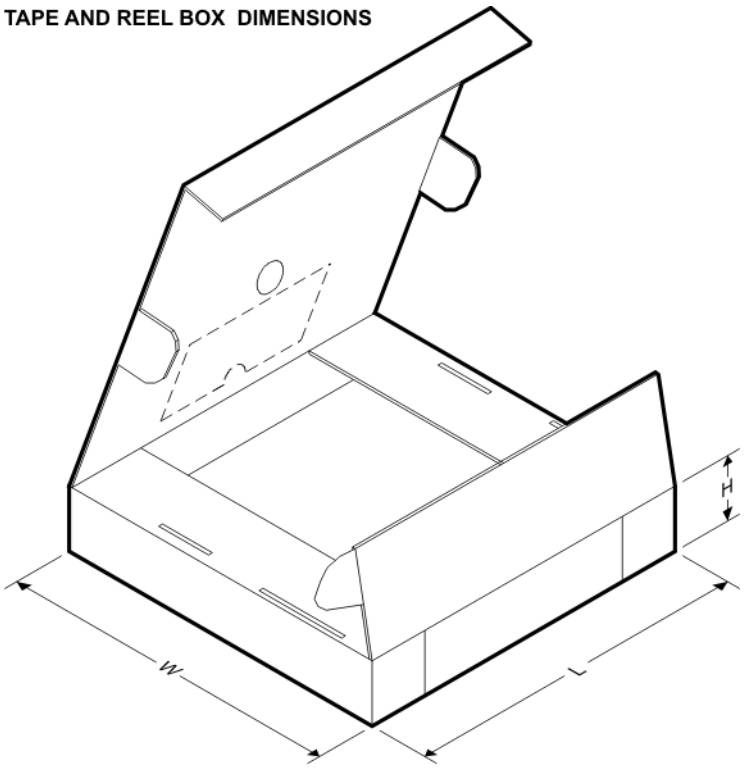
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SM72295MAX/NOPB	SOIC	DW	28	1000	330.0	24.4	10.8	18.4	3.2	12.0	24.0	Q1

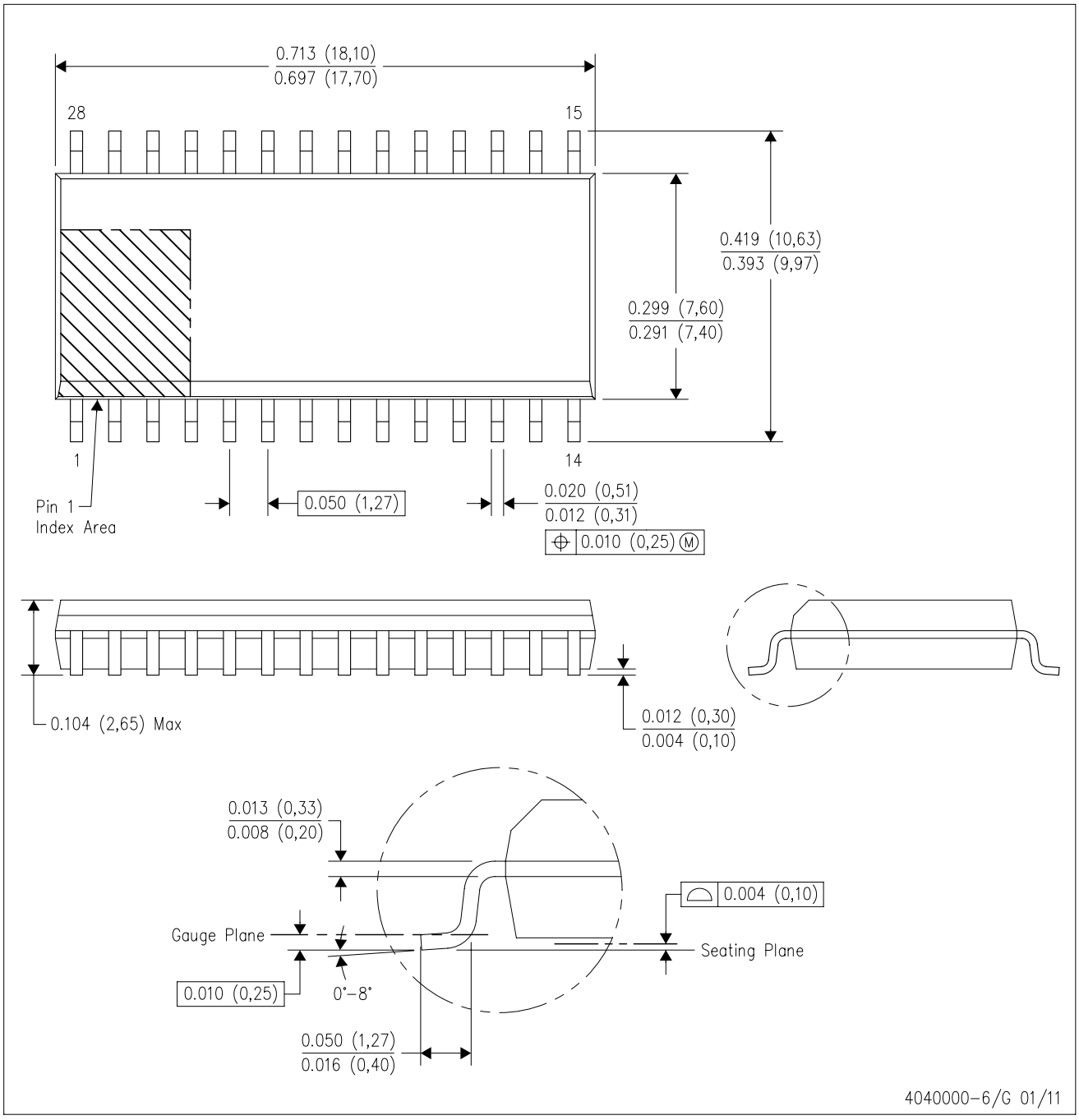
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SM72295MAX/NOPB	SOIC	DW	28	1000	367.0	367.0	45.0

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

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