

**Vishay Siliconix** 

# N-Channel 60 V (D-S), 175 °C MOSFET, Logic Level

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	<b>R<sub>DS(on)</sub> (</b> Ω <b>)</b>	I <sub>D</sub> (A) <sup>a</sup>			
60	0.0093 at V <sub>GS</sub> = 10 V	50			
	0.0122 at V <sub>GS</sub> = 4.5 V	50			

# TO-252

Top View

Ordering Information:

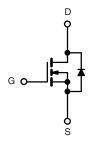
SUD50N06-09L-E3 (Lead (Pb)-free)

Drain Connected to Tab

### FEATURES

- 175 °C Junction Temperature
- TrenchFET<sup>®</sup> Power MOSFET
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912





N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_C =$	= 25 °C, unless othe	rwise noted)			
Parameter	Symbol	Limit	Unit		
Gate-Source Voltage		V <sub>GS</sub>	± 20	V	
	T <sub>C</sub> = 25 °C	1	50		
Continuous Drain Current (T <sub>J</sub> = 175 °C) <sup>b</sup>	T <sub>C</sub> = 100 °C	I <sub>D</sub>	50 <sup>a</sup>		
Pulsed Drain Current	I <sub>DM</sub>	100	А		
Continuous Source Current (Diode Conduction)		۱ <sub>S</sub>	50 <sup>a</sup>		
Avalanche Current	I <sub>AS</sub>	50	1		
Single Avalanche Energy (Duty Cycle $\leq$ 1 %)	L = 0.1 mH	E <sub>AS</sub>	125	mJ	
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	136	w	
Maximum Fower Dissipation	T <sub>A</sub> = 25 °C	' D	3 <sup>b</sup> , 8.3 <sup>b, c</sup>	vv	
Operating Junction and Storage Temperature Range	·	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Marian and han the Amelianta	t ≤ 10 sec	R <sub>thJA</sub>	15	18		
Maximum Junction-to-Ambient <sup>a</sup>	Steady State		40	50	°C/W	
Maximum Junction-to-Case	•	R <sub>thJC</sub>	0.85	1.1		

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c.  $t \leq$  10 s.

# SUD50N06-09L

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Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
Static			1		1 1		
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_D = 250 \mu A$	60			v	
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1	2	3		
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$			50 μΑ		
		$V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$			250	1	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	50			Α	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	0.0074		0.0093		
		$V_{GS}$ = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C			0.0160		
Drain-Source On-State Resistance <sup>b</sup>	R <sub>DS(on)</sub>	$V_{GS}$ = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C			0.0200	Ω	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A			0.0122		
Forward Transconductance <sup>b</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		60		S	
Dynamic	•						
Input Capacitance	C <sub>iss</sub>			2650		pF	
Output Capacitance	C <sub>oss</sub>	$V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1 MHz		470			
Reverse Transfer Capacitance	C <sub>rss</sub>			225			
Total Gate Charge <sup>c</sup>	Qg			47	70	nC	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS}$ = 30 V, $V_{GS}$ = 10 V, $I_D$ = 50 A		10			
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			12			
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			10	20		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = 30 V, $R_L$ = 0.6 $\Omega$		15	25	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$\text{I}_\text{D}\cong$ 50 A, $\text{V}_\text{GEN}$ = 10 V, $\text{R}_\text{g}$ = 2.5 $\Omega$		35	50		
Fall Time <sup>c</sup>	t <sub>f</sub>			20	30		
Source-Drain Diode Ratings and Cha	racteristics (	T <sub>C</sub> = 25 °C)					
Pulsed Current	I <sub>SM</sub>				100	А	
Diode Forward Voltage	V <sub>SD</sub>	$I_{F} = 20 \text{ A}, V_{GS} = 0 \text{ V}$		1	1.5	V	
		I <sub>F</sub> = 20 A, di/dt = 100 A/μs					

Notes:

a. For design aid only; not subject to production testing.

b. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.

c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



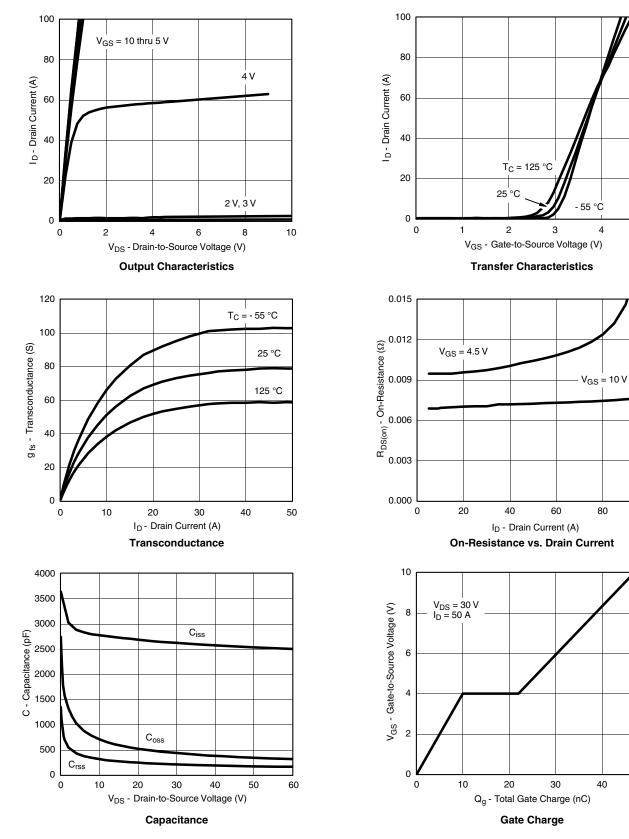
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100

### TYPICAL CHARACTERISTICS (25 °C unless noted)



For technical questions, contact: pmostechsupport@vishay.com

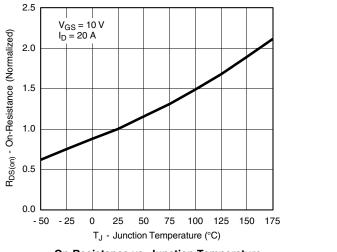
50

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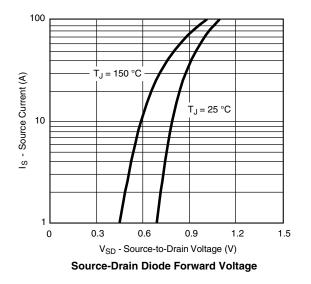
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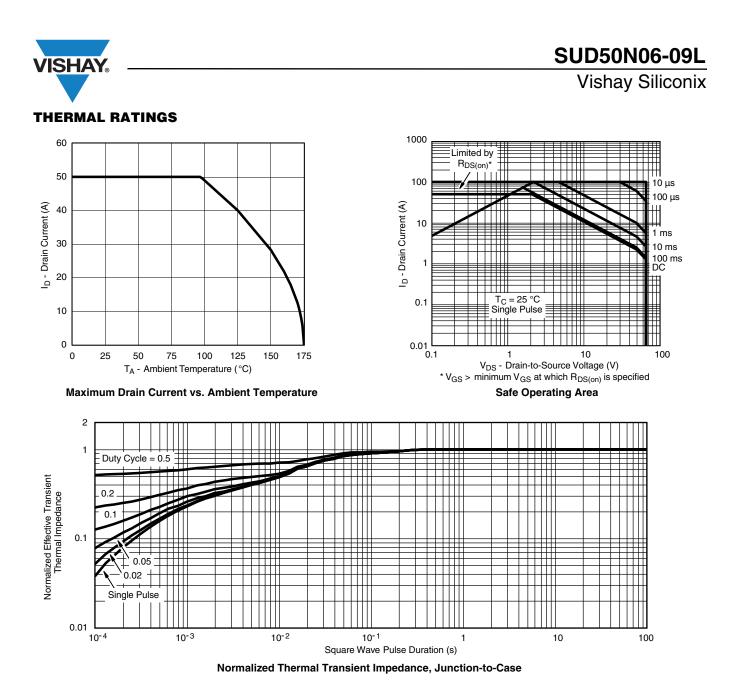
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### TYPICAL CHARACTERISTICS (25 °C unless noted)



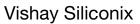
**On-Resistance vs. Junction Temperature** 





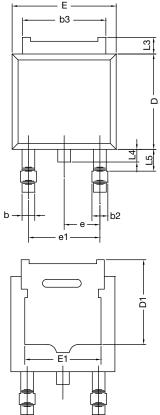
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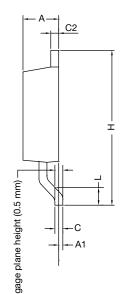
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**TO-252AA Case Outline** 





	MILLIN	IETERS	INC	HES		
DIM.	MIN.	MAX.	MIN.	MAX.		
А	2.18	2.38	0.086	0.094		
A1	-	0.127	-	0.005		
b	0.64	0.88	0.025	0.035		
b2	0.76	1.14	0.030	0.045		
b3	4.95	5.46	0.195	0.215		
С	0.46	0.61	0.018	0.024		
C2	0.46	0.89	0.018	0.035		
D	5.97	6.22	0.235	0.245		
D1	4.10	-	0.161	-		
Е	6.35	6.73	0.250	0.265		
E1	4.32	-	0.170	-		
Н	9.40	10.41	0.370	0.410		
е	2.28	BSC	0.090 BSC			
e1	4.56	BSC	0.180	BSC		
L	1.40	1.78	0.055	0.070		
L3	0.89	1.27	0.035	0.050		
L4	-	1.02	-	0.040		
L5	1.01	1.52	0.040	0.060		
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347						

Notes

• Dimension L3 is for reference only.



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### **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)

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