

Quad Monolithic SPST CMOS Analog Switches

DESCRIPTION

Featuring low on-resistance ($60\ \Omega$) and fast switching (130 ns), the DG308A is supplied in the “normally open” configuration while DG309 is supplied “normally closed”. Input thresholds are high voltage CMOS compatible.

Designed with the Vishay Siliconix PLUS-40 CMOS process to combine low power dissipation with a high breakdown voltage rating of 44 V, each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. An epitaxial layer prevents latch up.

The DG308B, DG309B upgrades are recommended for new designs.

FEATURES

- $\pm 15\text{ V}$ analog input range
- Low on-resistance: $60\ \Omega$
- Fast switching: 130 ns
- Low power dissipation: 30 nW
- CMOS logic compatible



RoHS*
COMPLIANT

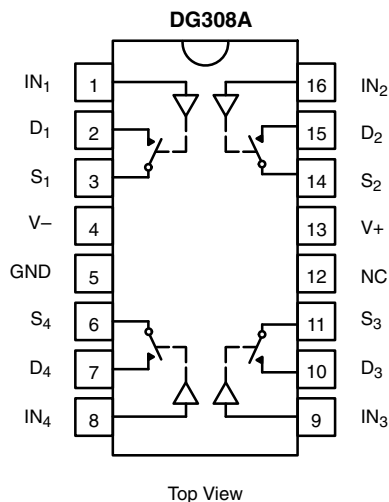
BENEFITS

- Full rail-to-rail analog signal range
- Low signal error
- Wide dynamic range
- Single or dual supply capability
- Static protected logic inputs
- Space savings (TSSOP)

APPLICATIONS

- Portable and battery powered instrumentation
- Communication systems
- Computer peripherals
- High-speed multiplexing

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



For SPST Switches per Package

| TRUTH TABLE | | |
|-------------|--------|-------|
| Logic | DG308A | DG309 |
| 0 | OFF | ON |
| 1 | ON | OFF |

Logic “0” $\leq 3.5\text{ V}$

Logic “1” $\geq 11\text{ V}$

* Pb containing terminations are not RoHS compliant, exemptions may apply



| ORDERING INFORMATION | | |
|----------------------|--------------------|--|
| Temp. Range | Package | Part Number |
| 0 °C to 70 °C | 16-Pin Plastic DIP | DG308ACJ DG308ACJ-E3 |
| | | DG309CJ DG309CJ-E3 |
| - 40 °C to 85 °C | 16-Pin Narrow SOIC | DG308ADY DG308ADY-E3 DG308ADY-T1 DG308ADY-T1-E3 |
| | | DG309DY DG309DY-E3 DG309DY-T1 DG309DY-T1-E3 |
| | 16-Pin TSSOP | DG308ADQ DG308ADQ-E3 DG308ADQ-T1 DG308ADQ-T1-E3 |
| | | DG309DQ DG309DQ-E3 DG309DQ-T1 DG309DQ-T1-E3 |

| ABSOLUTE MAXIMUM RATINGS | | | |
|---|---|--|------|
| Parameter | | Limit | Unit |
| Voltages Referenced V+ to V- | | 44 | V |
| GND | | 25 | |
| Digital Inputs ^a , V _S , V _D | | (V-) - 2 to (V+) + 2 or 20 mA, whichever occurs first | |
| Current, Any Terminal Except S or D | | 30 | mA |
| Continuous Current | S or D | 20 | |
| | (Pulsed at 1 ms, 10 % duty cycle max.) | 70 | |
| Storage Temperature | (AK Suffix) | - 65 to 150 | °C |
| | (CJ, DY and DQ Suffix) | - 65 to 125 | |
| Power Dissipation ^b | 16-Pin Plastic DIP ^c | 470 | mW |
| | 16-Pin Narrow SOIC and TSSOP ^e | 600 | |
| | 16-Pin CerDIP ^d | 900 | |

Notes:

- a. Signals on S_X, D_X, or I_{NX} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 12 mW/°C above 75 °C.
- d. Derate 6.5 mW/°C above 25 °C.
- e. Derate 7.6 mW/°C above 75 °C.

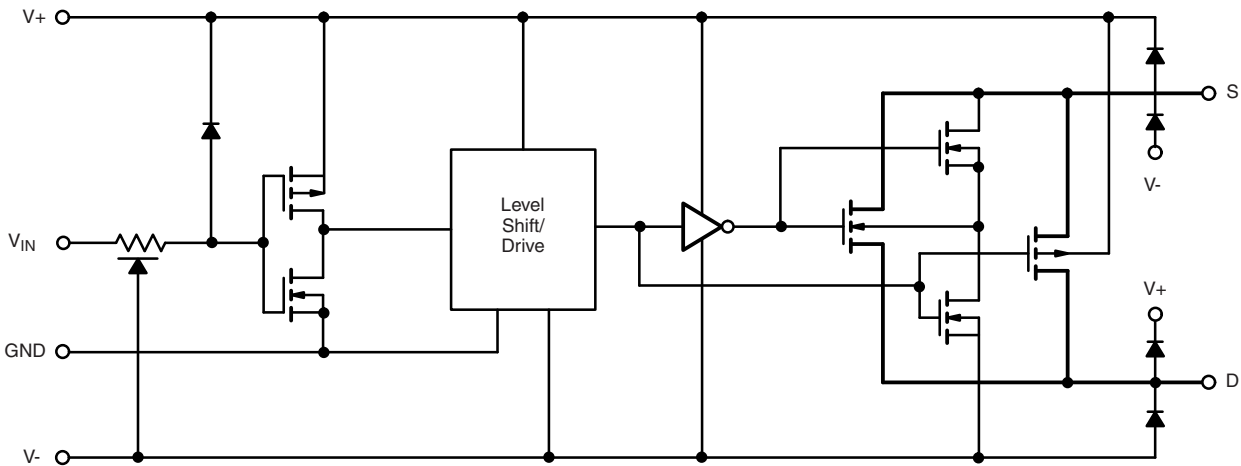
SCHEMATIC DIAGRAM (Typical Channel)


Figure 1.

| SPECIFICATIONS ^a | | | | | | | | | |
|---------------------------------------|--------------|--|--------------------|-------------------|------------------------------|-------------------|-------------------|-------------------|---------------|
| Parameter | Symbol | Test Conditions Unless Specified $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$ $V_{IN} = 3.5\text{ V}$ or 11 V ^f | Temp. ^b | Typ. ^c | A Suffix -55 °C to 125 °C | | C, D Suffix | | Unit |
| | | | | | Min. ^d | Max. ^d | Min. ^d | Max. ^d | |
| Analog Switch | | | | | | | | | |
| Analog Signal Range ^e | V_{ANALOG} | | Full | | -15 | 15 | -15 | 15 | V |
| Drain-Source On-Resistance | $R_{DS(on)}$ | $V_D = \pm 10\text{ V}$, $I_S = 1\text{ mA}$ | Room Full | 60 | | 100 150 | | 100 125 | Ω |
| Source Off Leakage Current | $I_{S(off)}$ | $V_S = \pm 14\text{ V}$, $V_D = \pm 14\text{ V}$ | Room Full | ± 0.1 | -1 100 | 1 100 | -5 -100 | 5 100 | nA |
| Drain Off Leakage Current | $I_{D(off)}$ | $V_D = \pm 14\text{ V}$, $V_S = \pm 14\text{ V}$ | Room Full | ± 0.1 | -1 100 | 1 100 | -5 -100 | 5 100 | |
| Drain On Leakage Current | $I_{D(on)}$ | $V_D = V_S = \pm 14\text{ V}$ | Room Full | ± 0.1 | -1 100 | 1 100 | -5 -200 | 5 200 | |
| Digital Control | | | | | | | | | |
| Input Current with Input Voltage High | I_{INH} | $V_{IN} = 15\text{ V}$ | Full | 0.001 | | 1 | | 1 | μA |
| Input Current with Input Voltage Low | I_{INL} | $V_{IN} = 0\text{ V}$ | Full | -0.001 | -1 | | -1 | | |
| Input Capacitance | C_{IN} | | Room | 8 | | | | | pF |
| Dynamic Characteristics | | | | | | | | | |
| Turn-On Time | t_{ON} | see figure 2 | Room | 130 | | 200 | | 200 | ns |
| Turn-Off Time | t_{OFF} | | Room | 90 | | 150 | | 150 | |
| Charge Injection | Q | $C_L = 0.01\ \mu\text{F}$, $R_{gen} = 0\ \Omega$, $V_{gen} = 0\text{ V}$, | Room | -10 | | | | | pC |
| Source-Off Capacitance | $C_{S(off)}$ | $f = 140\text{ kHz}$, V_S , $V_D = 0\text{ V}$ | Room | 11 | | | | | pF |
| Drain-Off Capacitance | $C_{D(off)}$ | | Room | 8 | | | | | |
| Channel-On Capacitance | $C_{D(on)}$ | | Room | 27 | | | | | |
| Off-Isolation ^f | OIRR | $R_L = 75\ \Omega$, $V_S = 2\text{ V}_{p-p}$, $f = 500\text{ kHz}$ | Room | 78 | | | | | dB |



SPECIFICATIONS^a

| Parameter | Symbol | Test Conditions Unless Specified $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$ $V_{IN} = 3.5\text{ V}$ or 11 V ^f | Temp. ^b | Typ. ^c | A Suffix -55 °C to 125 °C | | C, D Suffix | | Unit |
|-------------------------|--------|--|--------------------|-------------------|------------------------------|-------------------|-------------------|-------------------|---------------|
| | | | | | Min. ^d | Max. ^d | Min. ^d | Max. ^d | |
| Power Supplies | | | | | | | | | |
| Positive Supply Current | I+ | all channels on or off $V_{IN} = 0\text{ V}$ or 15 V | Room Full | 0.001 | | 10 | | 10 | μA |
| Negative Supply Current | I- | | Room Full | -0.001 | -10 -100 | | -100 | | |

Notes:

a. Refer to PROCESS OPTION FLOWCHART.

b. Room = 25 °C, Full = as determined by the operating temperature suffix.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

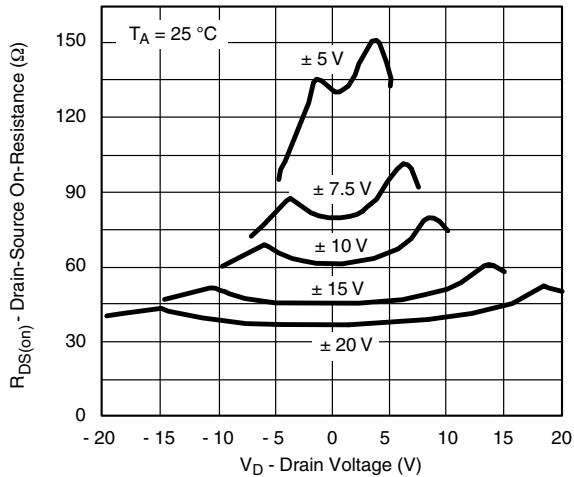
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

e. Guaranteed by design, not subject to production test.

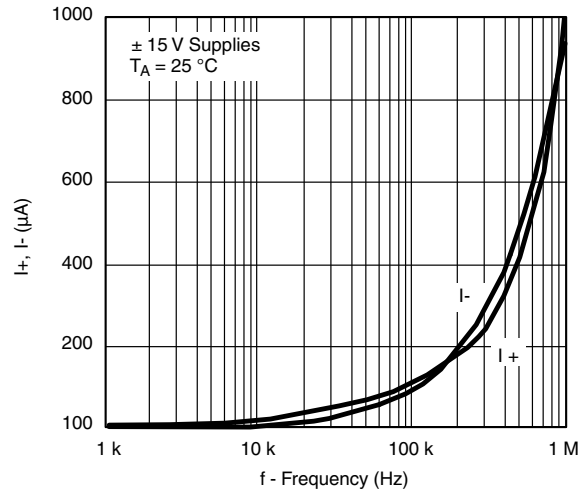
f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

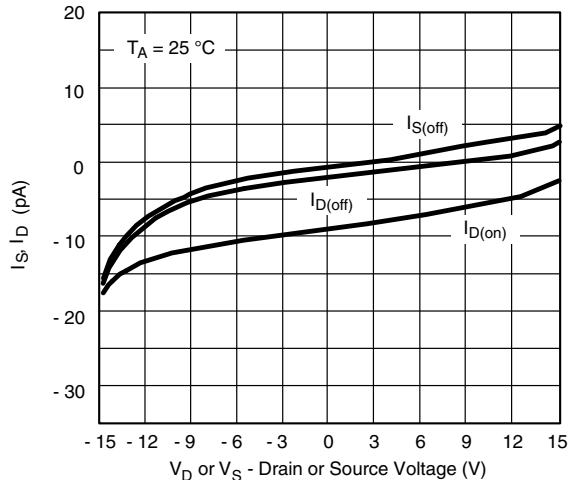
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



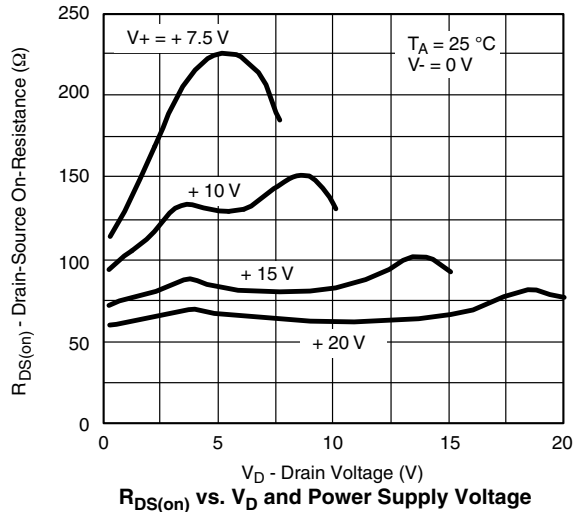
$R_{DS(on)}$ vs. V_D and Power Supply



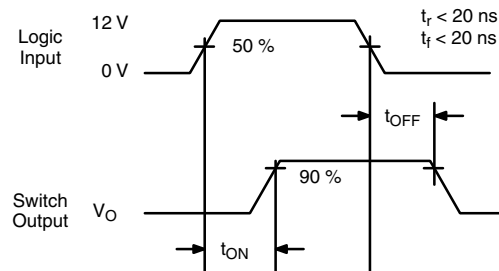
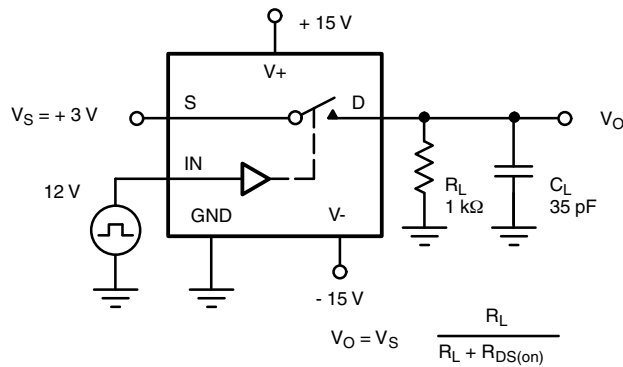
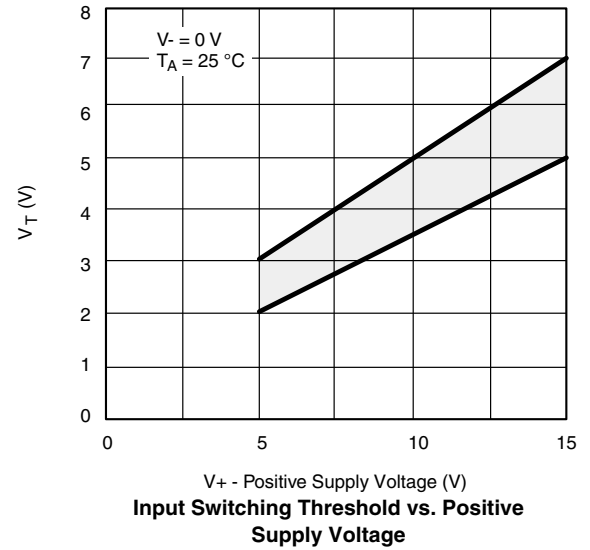
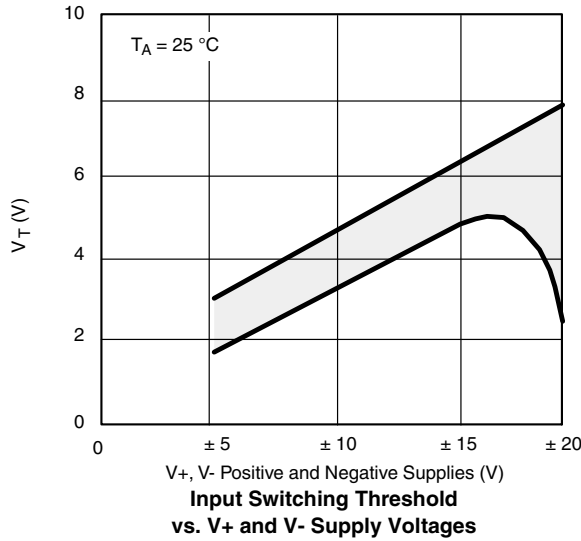
Supply Currents vs. Switching Frequency (All Inputs Active)



Leakage Currents vs. Analog Voltage



$R_{DS(on)}$ vs. V_D and Power Supply Voltage

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Figure 2. Switching Time
APPLICATIONS
Single Supply Operation

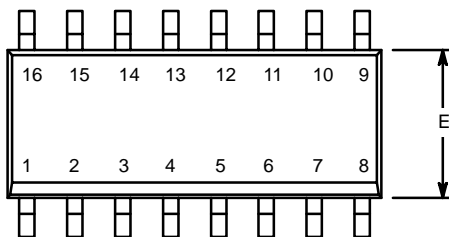
The DG308A and DG309 will switch positive analog signals while using a single positive supply. This will allow use in many applications where only one supply is available. The trade-offs or performance given up while using single supplies are:

1) increased $R_{DS(on)}$ and 2) slower switching speed. As stated in the absolute maximum ratings section of the data sheet, the analog voltage should not go above or below the supply voltages which in single supply operation are $V+$ and 0 V.

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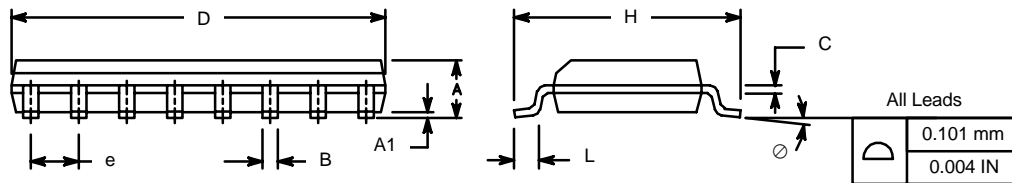


SOIC (NARROW): 16-LEAD
JEDEC Part Number: MS-012

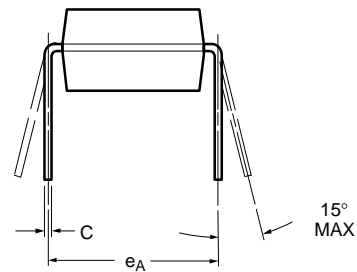
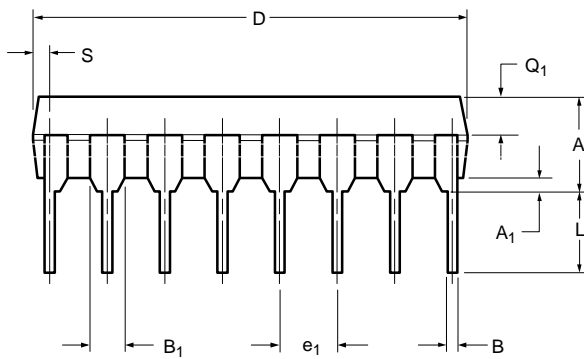
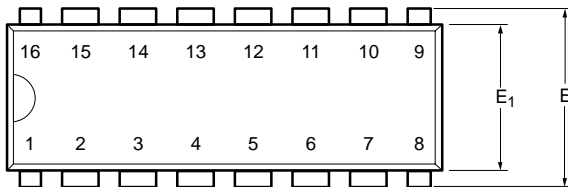


| Dim | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A ₁ | 0.10 | 0.20 | 0.004 | 0.008 |
| B | 0.38 | 0.51 | 0.015 | 0.020 |
| C | 0.18 | 0.23 | 0.007 | 0.009 |
| D | 9.80 | 10.00 | 0.385 | 0.393 |
| E | 3.80 | 4.00 | 0.149 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| L | 0.50 | 0.93 | 0.020 | 0.037 |
| ∅ | 0° | 8° | 0° | 8° |

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



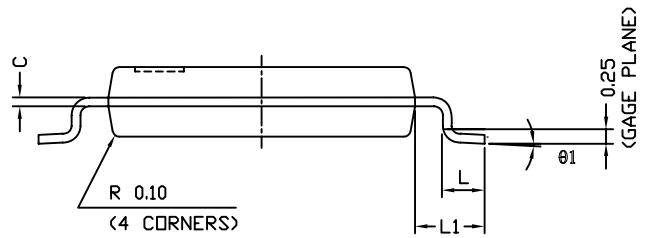
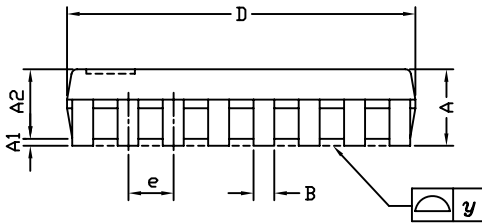
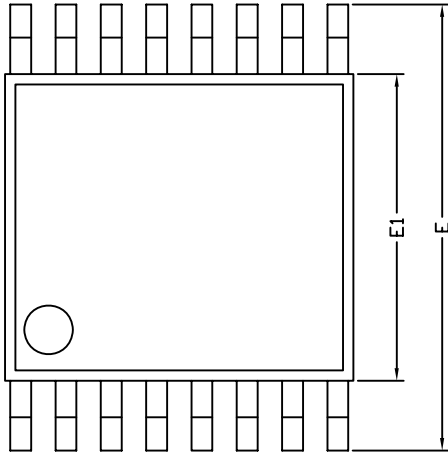
PDIP: 16-LEAD



| Dim | MILLIMETERS | | INCHES | |
|----------------------|-------------|-------|--------|-------|
| | Min | Max | Min | Max |
| A | 3.81 | 5.08 | 0.150 | 0.200 |
| A₁ | 0.38 | 1.27 | 0.015 | 0.050 |
| B | 0.38 | 0.51 | 0.015 | 0.020 |
| B₁ | 0.89 | 1.65 | 0.035 | 0.065 |
| C | 0.20 | 0.30 | 0.008 | 0.012 |
| D | 18.93 | 21.33 | 0.745 | 0.840 |
| E | 7.62 | 8.26 | 0.300 | 0.325 |
| E₁ | 5.59 | 7.11 | 0.220 | 0.280 |
| e₁ | 2.29 | 2.79 | 0.090 | 0.110 |
| e_A | 7.37 | 7.87 | 0.290 | 0.310 |
| L | 2.79 | 3.81 | 0.110 | 0.150 |
| Q₁ | 1.27 | 2.03 | 0.050 | 0.080 |
| S | 0.38 | 1.52 | .015 | 0.060 |

ECN: S-03946—Rev. D, 09-Jul-01
DWG: 5482

TSSOP: 16-LEAD

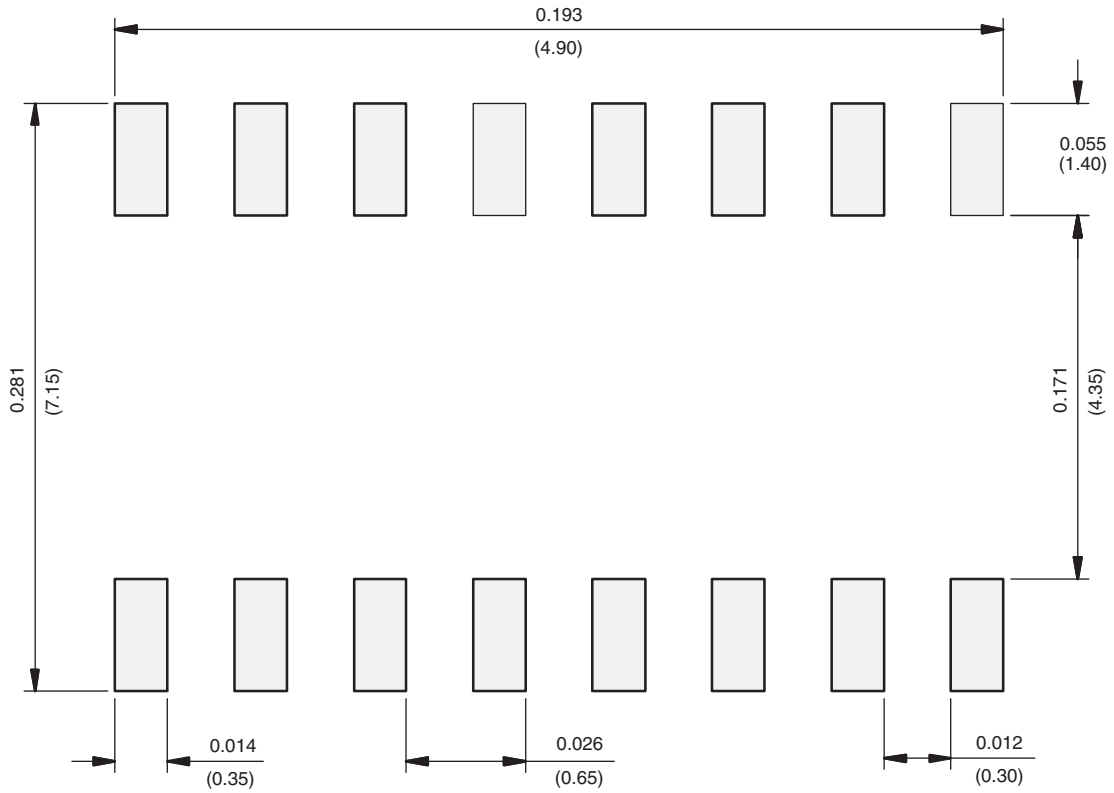


| Symbols | DIMENSIONS IN MILLIMETERS | | |
|---------|---------------------------|-------|------|
| | Min | Nom | Max |
| A | - | 1.10 | 1.20 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | - | 1.00 | 1.05 |
| B | 0.22 | 0.28 | 0.38 |
| C | - | 0.127 | - |
| D | 4.90 | 5.00 | 5.10 |
| E | 6.10 | 6.40 | 6.70 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | - | 0.65 | - |
| L | 0.50 | 0.60 | 0.70 |
| L1 | 0.90 | 1.00 | 1.10 |
| y | - | - | 0.10 |
| theta1 | 0° | 3° | 6° |

ECN: S-61920-Rev. D, 23-Oct-06
DWG: 5624

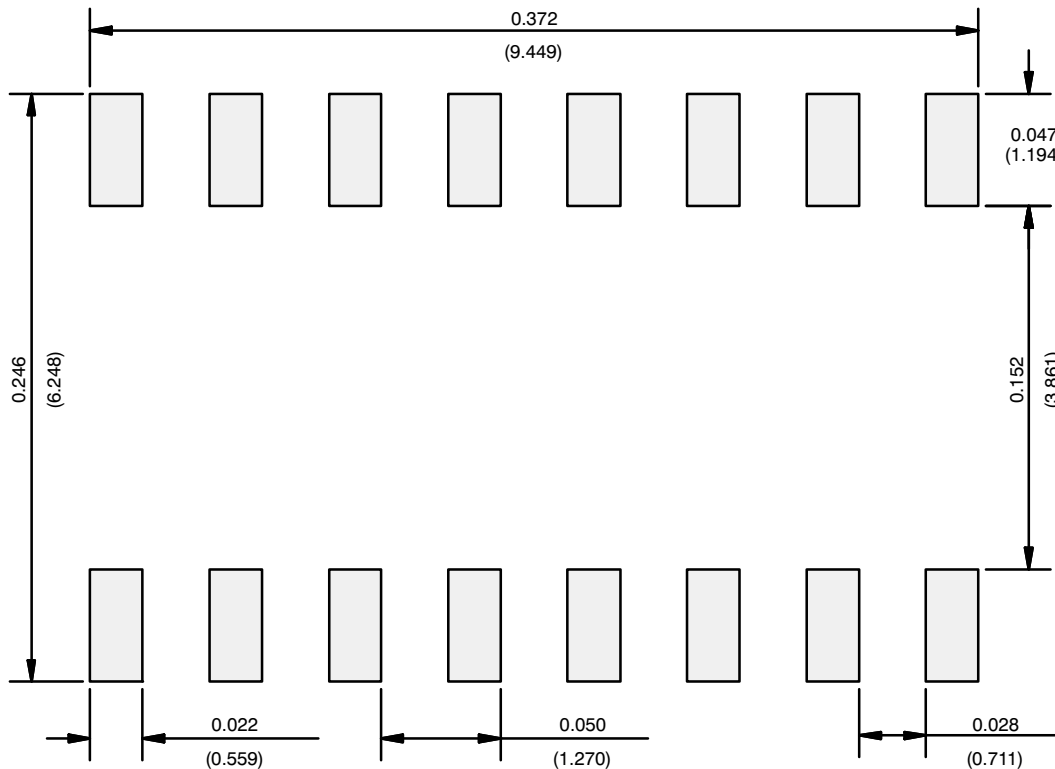


RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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