FEATURES

■ Fast access time : 55/70ns■ Low power consumption:

Operating current : 45/30mA (TYP.) Standby current : 4µA (TYP.) SL-version

■ Single 2.7V ~ 3.6V power supply

■ All inputs and outputs TTL compatible

■ Fully static operation

Tri-state outputData byte control : LB# (DQ0 ~ DQ7)

UB# (DQ8 ~ DQ15)

■ Data retention voltage : 1.2V (MIN.)

Lead free and green package available

■ Package: 48-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The AS6C1616 is a 16,777,216-bit low power CMOS static random access memory organized as 1,048,576 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

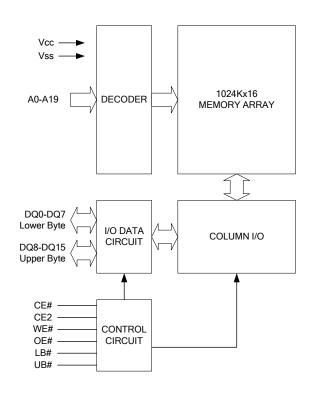
The AS6C1616 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C1616 operates from a single-power supply of $2.7V \sim 3.6V$ and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product	Operating	Vcc Range	Speed	Power D	issipation	
Family	Temperature	vcc range	Speed	Standby(IsB1,TYP.)	Operating (Icc,TYI	
AS6C1616(I)	-40 ~ 85℃	2.7 ~ 3.6V	55/70ns	4µA	45/30mA	

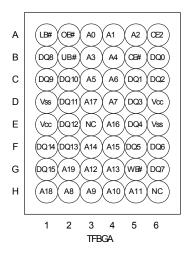
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A19	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
Vœ	Power Supply
Vss	Ground

PIN CONFIGURATION



ABSOLUTE MAXIMUN RATINGS*

PARAMETER SYMBOL		RATING	UNIT
Voltage on Vcc relative to Vss	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	VT2	-0.5 to V∞+0.5 V	
Operating Temperature	TA	-40 to 85(I grade)	$^{\circ}$
Storage Temperature	Tsīg	-65 to 150	$^{\circ}$
Power Dissipation	P _D 1		W
DC Output Current	Іоит 50		mA
Soldering Temperature (under 10 sec)	Tsalder 260		$^{\circ}\mathbb{C}$

^{*}Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	LB# UB#		I/O OPERATION		SUPPLY CURRENT	
	3 2,	<u> </u>	02,				DQ0-DQ7	DQ8-DQ15	33.1 33.1 11	
	Н	Х	Χ	Х	Х	Х	High – Z	High – Z		
standby	Х	L	Χ	Х	Х	X	High – Z	High – Z	ISB,ISB1	
	Χ	Х	Χ	Χ	Н	Н	High – Z	High – Z		
Output Disable	L	Н	Η	Н	L	Х	High – Z	High – Z	lœ,lca	
Output Disable	L	Н	Н	Н	Х	L	High – Z	High – Z	100,100	
	L	Н	L	Н	L	Н	D _{OUT}	High – Z		
Read	L	Н	L	Н	Н	L	High – Z	D_OUT	lœ,lca	
	L	Н	L	Н	L	L	D _{OUT}	D _{OUT}		
	L	Н	Χ	L	L	Н	D _{IN}	High – Z		
Write	L	Н	Χ	L	Н	L	High – Z	D_IN	lœ,lca	
	L	Н	Χ	L	L	L	D_IN	D_IN		

Note: $H = V_{IH}, L = V_{IL}, X = Don't care.$

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. ^{^4}	MAX.	UNIT
Supply Voltage	Vœ			2.7	3.0	3.6	V
Input High Voltage	V _{IH} *1			2.2	-	V∞ +0.3	٧
Input Low Voltage	VIL *2			- 0.2	-	0.6	V
Input Leakage Current	ILI	$V cc \ge V_{IN} \ge V_{SS}$		- 1	-	1	μA
Output Leakage Current	ILO	$Vcc \ge Vour \ge Vss$ Output Disabled		- 1	-	1	μΑ
Output High Voltage	Vон	Iон = -1mA		2.2	2.7	-	V
Output Low Voltage	Vol	I _{OL} = 2mA		-	-	0.4	V
	lα	Cycle time =Min. CE# =V	-55		45	60	mA
AverageOperating		I _{I/O} = 0mA Other pins at V _{IL} or V _H	-70	-	30	45	mA
Power supply Current	Ica	Cyde time = $1\mu s$ CE# $\leq 0.2V$ and CE2 $\geq V\infty$ -0.2V II/O = 0mA Other pins at 0.2V or $V\infty$ -0.2V	/	-	8	16	mA
Chandhu Dawar	I _{SB}	CE# ⇒V _{IH} or CE2 ⇒V _{IL} Other pins at V _{IL} or V _{IH}		-	0.3	2	mA
Standby Power Supply Curent	ISB1	CE# $$\!$	-SLI	-	6	40	μA

- 1. VIH(max) = Vcc + 3.0V for pulse width less than 10ns.
 2. VIL(min) = Vss 3.0V for pulse width less than 10ns.
 3. Over/Undershoot specifications are characterized, not 100% tested.
- 4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at Vcc = Vcc(TYP.) and TA = 25° C



CAPACITANCE (TA = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	Cin		6	pF
Input/Output Capacitance	Ci/o	æ	8	pF

Note: These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to Vcc - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	CL = 30pF + 1TTL, lон/loL = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS6C1	616-55	AS6C1616-70		UNIT	
		MIN.	MAX.	MIN.	MAX.		
Read Cycle Time	trc	55		70		ns	
Address Access Time	taa	10 (10)	55	155 155	70	ns	
Chip Enable Access Time	tace	:=::	55	(70	ns	
Output Enable Access Time	toe	-	30	5 =	35	ns	
Chip Enable to Output in Low-Z	tcız*	10	7	10	19	ns	
Output Enable to Output in Low-Z	toLz*	5	#	5	Œ	ns	
Chip Disable to Output in High-Z	tcHz*	.=.	20	8. =	25	ns	
Output Disable to Output in High-Z	tonz*	-	20	.=	25	ns	
Output Hold from Address Change	tон	10	:	10	UH	ns	
LB#, UB# Access Time	tва	900B	55	1 T	70	ns	
LB#, UB# to High-Z Output	tвнz*		25	€.=	30	ns	
LB#, UB# to Low-Z Output	tBLZ*	10	-	10	S=	ns	

(2) WRITE CYCLE

PARAMETER	SYM.	AS6C1	616-55	AS6C1	UNIT	
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	twc	55		70		ns
Address Valid to End of Write	taw	50	=	60	-	ns
Chip Enable to End of Write	tcw	50	=	60	=	ns
Address Set-up Time	tas	0	1907 3-3-8	0	1500 300	ns
Write Pulse Width	twe	45	=	55	=	ns
Write Recovery Time	twr	0	=	0	*	ns
Data to Write Time Overlap	tow	25	<u>~</u>	30	-	ns
Data Hold from End of Write Time	tон	0	2001 3-24	0	3.54 3.54	ns
Output Active from End of Write	tow*	5	=	5	=	ns
Write to Output in High-Z	twnz*	-	20	-	25	ns
LB#, UB# Valid to End of Write	tew	45	<u>~</u>	60	=	ns

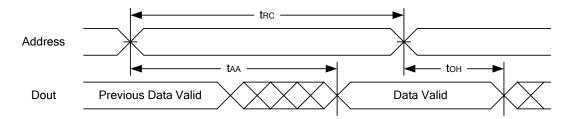
^{*}These parameters are guaranteed by device characterization, but not production tested.



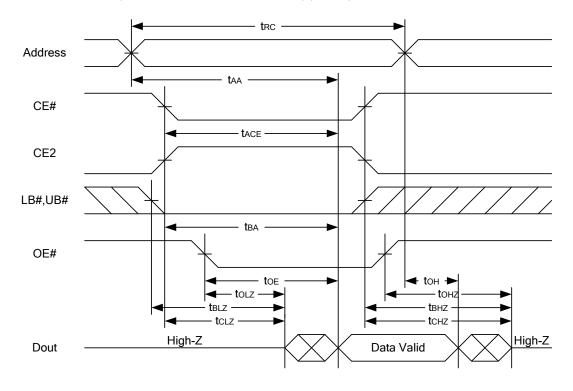
1024K X 16 BIT LOW POWER CMOS SRAM

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



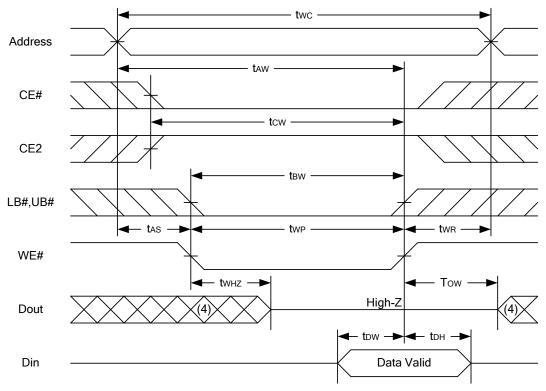
Notes:

- 1.WE#is high for read cycle
- 2.Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low
- 3.Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise tAA is the limiting parameter.
- $\frac{1}{2}$ 4.tcLz, tBLz, toLz, tCHz, tBHz and tOHz are specified with C L = 5pF. Transition is measured \pm 500mV from steady state.
- $5. At any given temperature and voltage condition, t \ \text{\tiny CHZ} \ \ is less than \ t \ \text{\tiny CLZ}, t \ \text{\tiny BHZ} \ \ is less than \ t \ \text{\tiny BLZ}, t \ \text{\tiny CHZ} \ \ is less than \ t \ \text{\tiny CLZ}.$

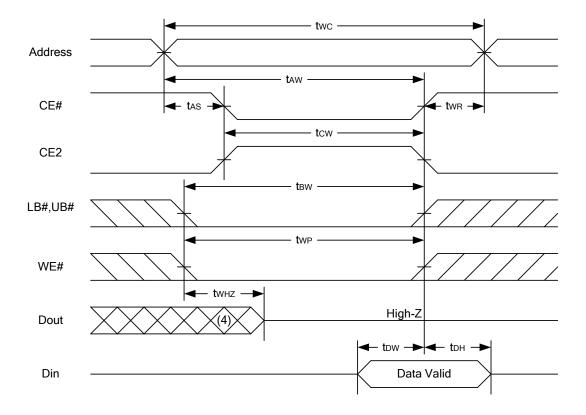


1024KX16 BITLOW POWER CMOS SRAM

WRITE CYCLE1 (WE# Controlled) (1,2,3,5,6)

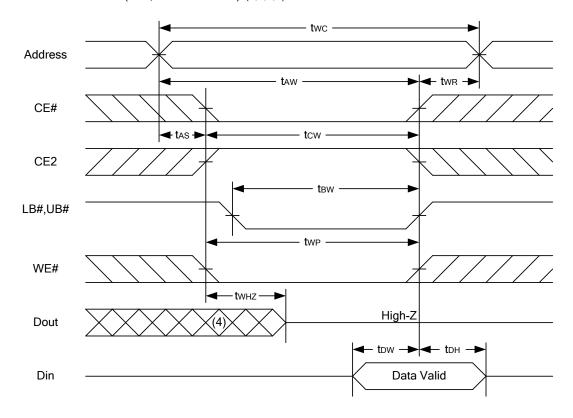


WRITE CYCLE2 (CE# and CE2 Cnotrolled) (1,2,5,6)



1024KX16 BIT LOW POWER CMOS SRAM

WRITE CYCLE 3 (LB#, UB# Controlled) (1,2,5,6)



Notes:

- 1.WE#,CE#, LB#, UB# must be high or CE2 must be low during all address transitions. 2.A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
- 3.During a WE# controlled write cycle with OE# low, twp must be greater than twHz + tpw to allow the drivers to turn off and data to be placed on the bus.
- 4. During this period, I/O pins are in the output state, and input signals must not be applied.
- 5.If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
- 6.tow and twHz are specified with C_L = 5pF. Transition is measured ±500mV from steady state.



1024KX16 BITLOW POWER CMOS SRAM

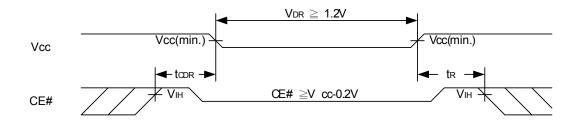
DATA RETENTION CHARACTERISTICS

PARAMETER SYMBOL		TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	CE#≥ V _{CC} - 0.2V or CE2≤0.2V	1.2	-	3.6	V
Data Retention Current		V_{CC} = 1.2V $CE\# \ge V_{CC}$ -0.2V or $CE2 \le 0.2V$ other pins at 0.2V or V_{CC} -0.2V	-	4	40	μΑ
Chip Disable to Data Retention Time	ICDD	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t RC∗	-	-	ns

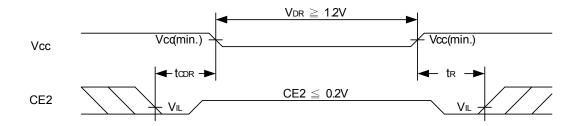
tRC∗ = Read Cycle Time

DATA RETENTION WAVEFORM

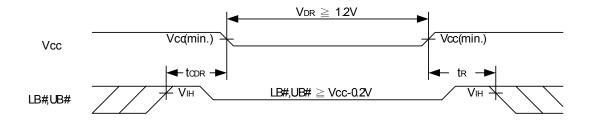
Low Vcc Data Retention Waveform (1) (CE# controlled)



Low Vcc Data Retention Waveform (2) (CE2 contribed)



Low Vcc Data Retention Waveform (3) (LB#, UB#controlled)

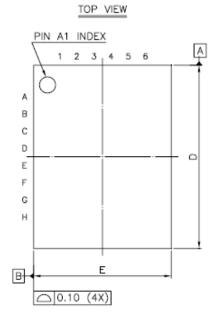


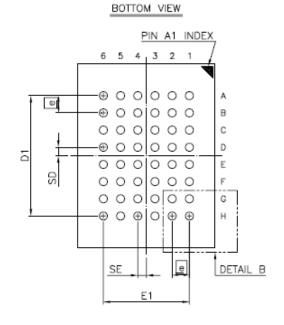


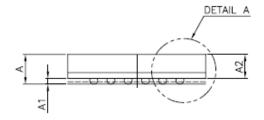
1024KX16 BITLOWPOWER CMOS SRAM

PACKAGE OUTLINE DIMENSION

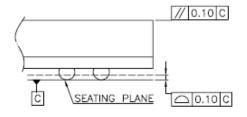
48-ball 6mm × 8mm TFBGA Package Outline Dimension





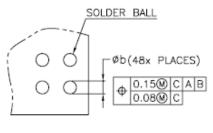


SIDE VIEW



DETAIL A

CVI	D	MENSIO (mm)	N	DIMENSION (inch)			
SYM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α		_	1.40		_	0.055	
A1	0.20	0.25	0.30	0.008	0.010	0.012	
A2		_	1.05		_	0.041	
b	0.30	0.35	0.40	0.012	0.014	0.016	
D	7.95	8.00	8.05	0.313	0.315	0.317	
D1	5	.25 BS0)	0.207 BSC			
Ε	5.95	6.00	6.05	0.234	0.236	0.238	
E1	3	.75 BS0		0	.148 BS	SC	
SE	0	.375 TY	Έ	0.015 TYP			
SD	0.375 TYP			0.015 TYP			
е	0	.75 BS0		0	.030 BS	SC	



NOTE:

- 1. CONTROLLING DIMENSION: MILLIMETER.
- 2. REFERENCE DOCUMENT : JEDEC MO-207.

DETAIL B

1024K X 16 BIT LOW POWER CMOS SRAM

Ordering Information

Alliance	Organization	VCC Range	Package	Operating Temp	Speed ns
AS6C1616-70BIN	1024K x 16	2.7 - 3.6V	48ball TFBGA	Industrial ~ -40 C – 85 C)	70
AS6C1616-55BIN	1024K x 16	2.7 - 3.6V	48ball TFBGA	Industrial ~ -40 C – 85 C)	55

Part Numbering System

AS6C	1616	-70	Х	Х	N
low power SRAM prefix	Device Number 16 = 16M 16 = x16	Access Time	Package Option 48ball TFBGA	Temperature Range I = Industrial (-40 to +85 C)	N = Lead Free RoHS compliant part

1024KX16 BITLOW POWER CMOS SRAM



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