

FEATURES

- ±2 V to ±6 V dual supply
- 2 V to 12 V single supply
- <0.1 nA leakage currents (typical)
- 45 Ω typical on resistance over full signal range
- Rail-to-rail switching operation
- Single, 8 to 1 multiplexer
- 16-lead TSSOP package
- 0.01 μA typical supply current
- TTL/CMOS compatible inputs

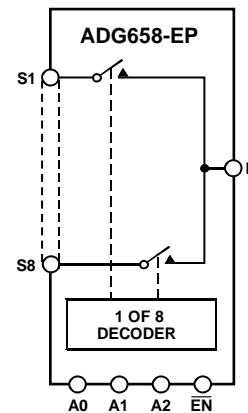
ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: -55°C to +125°C
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Communication systems
- Audio and video signal routing
- Relay replacement
- Sample-and-hold systems
- Industrial control systems

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC 1 INPUT.

Figure 1.

GENERAL DESCRIPTION

The ADG658-EP is a low voltage, CMOS analog multiplexer comprised of eight single channels. The ADG658-EP switches one of eight inputs (S1 to S8) to a common output, D, as determined by the 3-bit binary address lines A0, A1, and A2. An $\overline{\text{EN}}$ input enables or disables the device. When disabled, all channels are switched off.

The ADG658-EP is designed on an enhanced process that provides lower power dissipation yet gives high switching speeds. It can operate equally well as either a multiplexer or a demultiplexer, and has an input range that extends to the supplies. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels. All digital inputs have +0.8 V to +2.4 V logic thresholds, ensuring TTL/CMOS logic compatibility when using single +5 V or dual ±5 V supplies.

The ADG658-EP is available in a 16-lead TSSOP package.

Additional application and technical information can be found in the [ADG658](#) data sheet.

PRODUCT HIGHLIGHTS

1. Single-supply and dual-supply operation. The ADG658-EP offers high performance and is fully specified and guaranteed with ±5 V, +5 V, and +3 V supply rails.
2. Military temperature range -55°C to +125°C.
3. Low supply current, typically 0.01 μA.
4. 16-lead TSSOP package.

TABLE OF CONTENTS

| | | | |
|---------------------------------|---|--|----|
| Features | 1 | 5 V Single Supply..... | 3 |
| Enhanced Product Features | 1 | 2.7 V to 3.6 V Single Supply..... | 5 |
| Applications..... | 1 | Absolute Maximum Ratings | 6 |
| Functional Block Diagram | 1 | ESD Caution..... | 6 |
| General Description | 1 | Pin Configurations and Function Descriptions | 7 |
| Product Highlights | 1 | Typical Performance Characteristics | 8 |
| Revision History | 2 | Outline Dimensions | 10 |
| Specifications..... | 3 | Ordering Guide | 10 |
| Dual Supply | 3 | | |

REVISION HISTORY

8/2017—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

| Parameter | +25°C | -55°C to +125°C | Unit | Test Conditions/Comments |
|---|-------------|----------------------|-------------------|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | V_{SS} to V_{DD} | V | $V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$ |
| On Resistance, R_{ON} | 45 | | Ω typ | Source voltage (V_S) = $\pm 4.5\text{ V}$, source current (I_S) = 1 mA |
| | 75 | 100 | Ω max | |
| On Resistance Match Between Channels, ΔR_{ON} | 1.3 | | Ω typ | $V_S = 3.5\text{ V}$, $I_S = 1\text{ mA}$ |
| | 3 | 3.5 | Ω max | $V_{DD} = +5\text{ V}$, $V_{SS} = -5\text{ V}$ |
| On Resistance Flatness, $R_{FLAT(ON)}$ | 10 | | Ω typ | $V_S = \pm 3\text{ V}$, $I_S = 1\text{ mA}$ |
| | 16 | 18 | Ω max | |
| LEAKAGE CURRENTS | | | | |
| Source Off Leakage, I_S (OFF) | ± 0.005 | | nA typ | $V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ |
| | ± 0.2 | ± 5 | nA max | Drain voltage (V_D) = $\pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$ |
| Drain Off Leakage, I_D (OFF) | ± 0.005 | | nA typ | $V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$ |
| | ± 0.2 | ± 5 | nA max | |
| Channel On Leakage I_D , I_S (ON) | ± 0.005 | | nA typ | $V_D = V_S = \pm 4.5\text{ V}$ |
| | ± 0.2 | ± 5 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current | | | | |
| I_{INL} or I_{INH} | 0.005 | | μA typ | Input voltage (V_{IN}) = V_{INL} or V_{INH} |
| | | ± 1 | μA max | |
| Digital Input Capacitance, C_{IN} | 2 | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | |
| Transition Time, $t_{TRANSITION}$ | 80 | | ns typ | Load resistance (R_L) = 300 Ω , load capacitance (C_L) = 35 pF |
| | 115 | 165 | ns max | $V_S = 3\text{ V}$ |
| \overline{EN} On Time, $t_{ON}(\overline{EN})$ | 80 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$ |
| | 115 | 165 | ns max | $V_S = 3\text{ V}$ |
| \overline{EN} Off Time, $t_{OFF}(\overline{EN})$ | 30 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$ |
| | 45 | 55 | ns max | $V_S = 3\text{ V}$ |
| Break-Before-Make Time Delay, t_{BBM} | 50 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$ |
| | | 10 | ns min | Source 1 voltage (V_{S1}) = 3 V, source 2 voltage (V_{S2}) = 3 V |
| Charge Injection | 2 | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$ |
| | 4 | | pC max | $C_L = 1\ \text{nF}$ |
| Off Isolation | -90 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$ |
| Total Harmonic Distortion Plus Noise, THD + N | 0.025 | | % typ | $R_L = 600\ \Omega$, 2 V p-p, $f = 20\ \text{Hz}$ to 20 kHz |
| -3 dB Bandwidth | 210 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$ |
| Source Capacitance, C_S (OFF) | 4 | | pF typ | $f = 1\ \text{MHz}$ |
| Drain Capacitance, C_D (OFF) | 23 | | pF typ | $f = 1\ \text{MHz}$ |
| C_D , C_S (ON) | 28 | | pF typ | $f = 1\ \text{MHz}$ |
| POWER REQUIREMENTS | | | | |
| Positive Power Supply Current, I_{DD} | 0.01 | | μA typ | $V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ |
| | | 1 | μA max | Digital inputs = 0 V or 5.5 V |
| Negative Power Supply Current, I_{SS} | 0.01 | | μA typ | Digital inputs = 0 V or 5.5 V |
| | | 1 | μA max | |

¹ Guaranteed by design; not subject to production test.

5 V SINGLE SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

| Parameter | +25°C | -55°C to +125°C | Unit | Test Conditions/Comments |
|--|-------------|-----------------|-------------------|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 to V_{DD} | V | $V_{DD} = 4.5\text{ V}$, $V_{SS} = 0\text{ V}$ |
| On Resistance, R_{ON} | 85 | | Ω typ | $V_S = 0\text{ V to } 4.5\text{ V}$, $I_S = 1\text{ mA}$ |
| | 150 | 200 | Ω max | |
| On Resistance Match Between Channels, ΔR_{ON} | 4.5 | | Ω typ | $V_S = 3.5\text{ V}$, $I_S = 1\text{ mA}$ |
| | 8 | 10 | Ω max | |
| On Resistance Flatness, $R_{FLAT(ON)}$ | 13 | 16 | Ω typ | $V_{DD} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $V_S = 1.5\text{ V to } 4\text{ V}$, $I_S = 1\text{ mA}$ |
| LEAKAGE CURRENTS | | | | |
| Source Off Leakage, I_S (OFF) | ± 0.005 | | nA typ | $V_{DD} = 5.5\text{ V}$ |
| | ± 0.2 | ± 5 | nA max | $V_S = 1\text{ V/}4.5\text{ V}$, $V_D = 4.5\text{ V/}1\text{ V}$ |
| Drain Off Leakage, I_D (OFF) | ± 0.005 | | nA typ | $V_S = 1\text{ V/}4.5\text{ V}$, $V_D = 4.5\text{ V/}1\text{ V}$ |
| | ± 0.2 | ± 5 | nA max | |
| Channel On Leakage I_D , I_S (ON) | ± 0.005 | | nA typ | $V_S = V_D = 1\text{ V or } 4.5\text{ V}$ |
| | ± 0.2 | ± 5 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current | | | | |
| I_{INL} or I_{INH} | 0.005 | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | ± 1 | μA max | |
| Digital Input Capacitance, C_{IN} | 2 | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | |
| Transition Time, $t_{TRANSITION}$ | 120 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 200 | 300 | ns max | $V_S = 3\text{ V}$ |
| $\overline{\text{EN}}$ On Time, $t_{ON}(\overline{\text{EN}})$ | 120 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 190 | 280 | ns max | $V_S = 3\text{ V}$ |
| $\overline{\text{EN}}$ Off Time, $t_{OFF}(\overline{\text{EN}})$ | 35 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 50 | 70 | ns max | $V_S = 3\text{ V}$ |
| Break-Before-Make Time Delay, t_{BBM} | 100 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | 10 | ns min | $V_{S1} = V_{S2} = 3\text{ V}$ |
| Charge Injection | 0.5 | | pC typ | $V_S = 2.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$ |
| | 1 | | pC max | |
| Off Isolation | -90 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$ |
| -3 dB Bandwidth | 180 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ |
| Source Capacitance, C_S (OFF) | 5 | | pF typ | $f = 1\text{ MHz}$ |
| Drain Capacitance, C_D (OFF) | 29 | | pF typ | $f = 1\text{ MHz}$ |
| C_D , C_S (ON) | 30 | | pF typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | |
| Positive Power Supply Current, I_{DD} | 0.01 | | μA typ | $V_{DD} = 5.5\text{ V}$ |
| | | 1 | μA max | Digital inputs = 0V or 5.5V |

¹ Guaranteed by design; not subject to production test.

2.7 V TO 3.6 V SINGLE SUPPLY

$V_{DD} = 2.7$ to 3.6 V, $V_{SS} = 0$ V, GND = 0 V, unless otherwise noted.

Table 3.

| Parameter | +25°C | -55°C to +125°C | Unit | Test Conditions/Comments |
|---|-------------|-----------------|--------------|--|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 to V_{DD} | V | $V_{DD} = 2.7$ V, $V_{SS} = 0$ V |
| On Resistance, R_{ON} | 185 | | Ω typ | $V_S = 0$ V to 2.7 V, $I_S = 0.1$ mA |
| | 300 | 400 | Ω max | |
| On Resistance Match Between Channels, ΔR_{ON} | 2 | | Ω typ | $V_S = 1.5$ V, $I_S = 0.1$ mA |
| | 4.5 | 7 | Ω max | |
| LEAKAGE CURRENTS | | | | |
| Source Off Leakage, I_S (OFF) | ± 0.005 | | nA typ | $V_{DD} = 3.3$ V |
| | ± 0.2 | ± 5 | nA max | $V_S = 1$ V/3 V, $V_D = 3$ V/1 V |
| Drain Off Leakage, I_D (OFF) | ± 0.005 | | nA typ | $V_S = 1$ V/3 V, $V_D = 3$ V/1 V |
| | ± 0.2 | ± 5 | nA max | |
| Channel On Leakage I_D, I_S (ON) | ± 0.005 | | nA typ | $V_S = V_D = 1$ V or 3 V |
| | ± 0.2 | ± 5 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | 0.5 | V max | |
| Input Current | | | | |
| I_{INL} or I_{INH} | 0.005 | | μ A typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | ± 1 | μ A max | |
| Digital Input Capacitance, C_{IN} | 2 | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | |
| Transition Time, $t_{TRANSITION}$ | 200 | | ns typ | $R_L = 300$ Ω , $C_L = 35$ pF |
| | 370 | 490 | ns max | $V_S = 1.5$ V |
| \overline{EN} On Time, $t_{ON}(\overline{EN})$ | 230 | | ns typ | $R_L = 300$ Ω , $C_L = 35$ pF |
| | 370 | 490 | ns max | $V_S = 1.5$ V |
| \overline{EN} Off Time, $t_{OFF}(\overline{EN})$ | 50 | | ns typ | $R_L = 300$ Ω , $C_L = 35$ pF |
| | 80 | 110 | ns max | $V_S = 1.5$ V |
| Break-Before-Make Time Delay, t_{BBM} | 200 | | ns typ | $R_L = 300$ Ω , $C_L = 35$ pF |
| | | 10 | ns min | $V_{S1} = V_{S2} = 1.5$ V |
| Charge Injection | 1 | | pC typ | $V_S = 1.5$ V, $R_S = 0$ Ω , $C_L = 1$ nF |
| | 2 | | pC max | |
| Off Isolation | -90 | | dB typ | $R_L = 50$ Ω , $C_L = 5$ pF, $f = 1$ MHz |
| -3 dB Bandwidth | 160 | | MHz typ | $R_L = 50$ Ω , $C_L = 5$ pF |
| Source Capacitance, C_S (OFF) | 5 | | pF typ | $f = 1$ MHz |
| Drain Capacitance, C_D (OFF) | 29 | | pF typ | $f = 1$ MHz |
| C_D, C_S (ON) | 30 | | pF typ | $f = 1$ MHz |
| POWER REQUIREMENTS | | | | |
| Positive Power Supply Current, I_{DD} | 0.01 | | μ A typ | $V_{DD} = 3.6$ V |
| | | 1 | μ A max | Digital inputs = 0 V or 3.6 V |

¹ Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

| Parameter | Rating |
|---|---|
| V_{DD} to V_{SS} | 13 V |
| V_{DD} to GND | -0.3 V to +13 V |
| V_{SS} to GND | +0.3 V to -6.5 V |
| Analog Inputs ¹ | $V_{SS} - 0.3 \text{ V}$ to $V_{DD} + 0.3 \text{ V}$ |
| Digital Inputs ¹ | GND - 0.3 V to $V_{DD} + 0.3 \text{ V}$ or 10 mA, whichever occurs first |
| Peak Current, Sx or D (Pulsed at 1 ms, 10% duty cycle max) | 40 mA |
| Continuous Current, Sx or D | 20 mA |
| Operating Temperature Range | -55°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| θ_{JA} Thermal Impedance 16-Lead TSSOP | 150.4°C/W |
| Lead Temperature, Soldering Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |
| ESD (Human Body Model) | 4.0 kV |

¹ Overvoltages at A_x , \overline{EN} , Sx, or D are clamped by internal diodes. Current must be limited to the maximum ratings.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 5. Truth Table

| A2 | A1 | A0 | \overline{EN} | Switch Condition |
|----------------|----------------|----------------|-----------------|------------------|
| X ¹ | X ¹ | X ¹ | 1 | None |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 1 | 0 | 0 | 3 |
| 0 | 1 | 1 | 0 | 4 |
| 1 | 0 | 0 | 0 | 5 |
| 1 | 0 | 1 | 0 | 6 |
| 1 | 1 | 0 | 0 | 7 |
| 1 | 1 | 1 | 0 | 8 |

¹ X means don't care

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

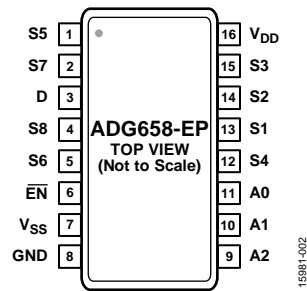


Figure 2. 16-Lead TSSOP Pin Configuration

Table 6. 16-Lead TSSOP Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|----------------------------|------------------------|--|
| 1, 2, 4, 5, 12, 13, 14, 15 | S1 to S8 | Source Terminals. Can be an input or output. |
| 3 | D | Drain Terminal. Can be an input or output. |
| 6 | $\overline{\text{EN}}$ | Active Low Digital Input. When high, device is disabled and all switches are off. When low, Ax logic inputs determine on switch. |
| 7 | V _{SS} | Most Negative Power Supply Potential. |
| 8 | GND | Ground (0 V) Reference. |
| 9, 10, 11 | A0 to A2 | Logic Control Inputs. |
| 16 | V _{DD} | Most Positive Power Supply Potential. |

TYPICAL PERFORMANCE CHARACTERISTICS

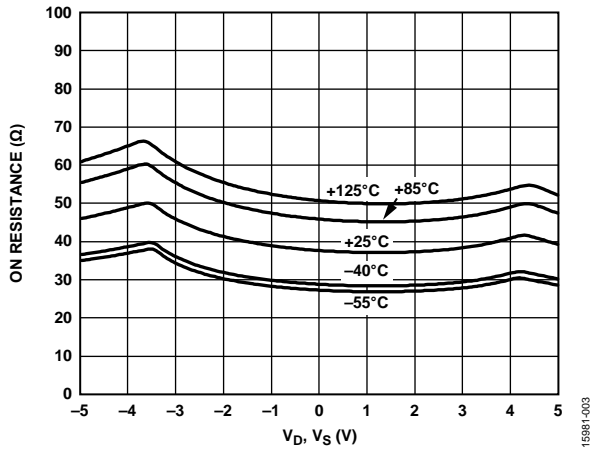


Figure 3. On Resistance vs. V_D (V_S) for Different Temperatures (Dual Supply)

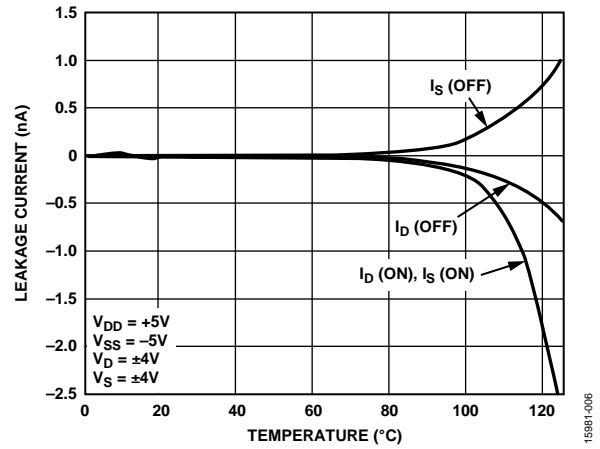


Figure 6. Leakage Current vs. Temperature (Dual Supply)

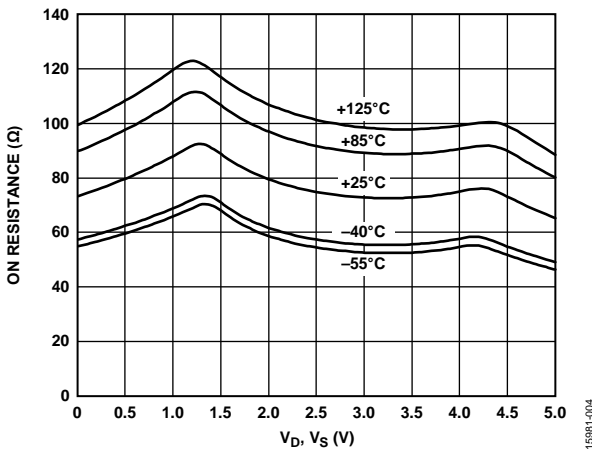


Figure 4. On Resistance vs. V_D (V_S) for Different Temperatures (Single Supply)

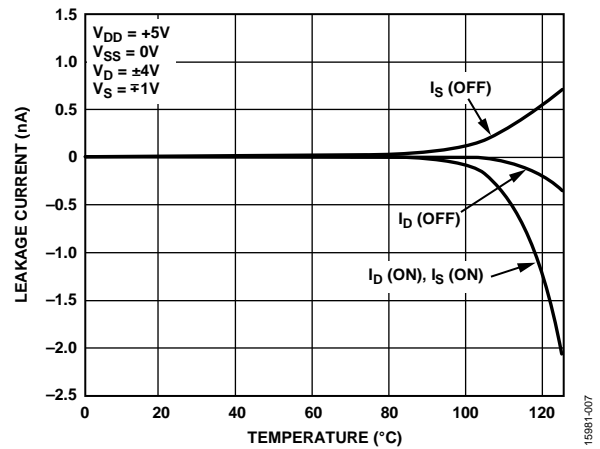


Figure 7. Leakage Current vs. Temperature (Single Supply)

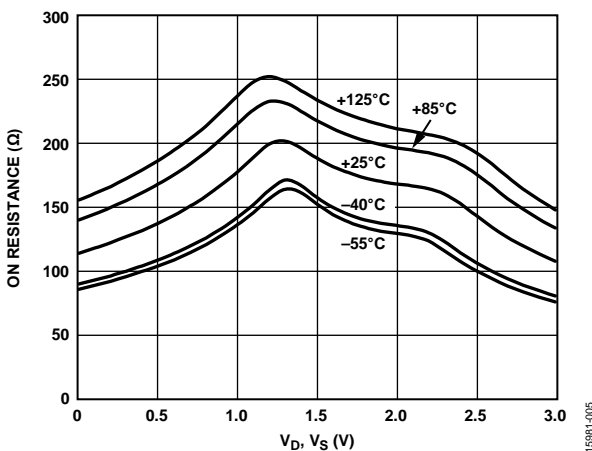


Figure 5. On Resistance vs. V_D (V_S) for Different Temperatures (Single Supply)

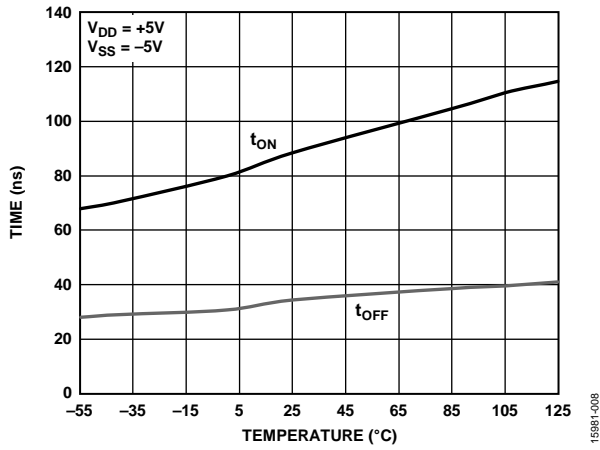


Figure 8. t_{ON}/t_{OFF} Time vs. Temperature (Dual Supply)

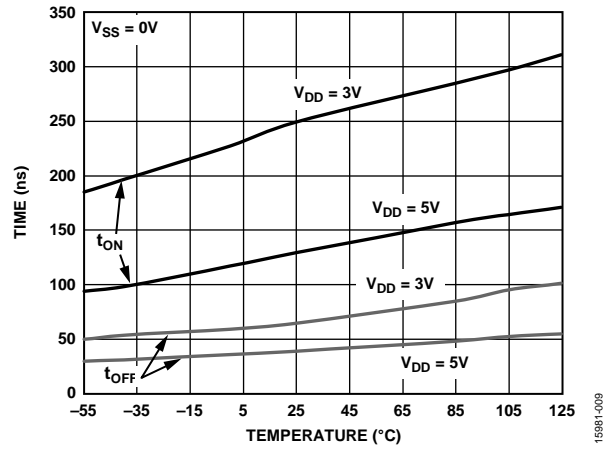
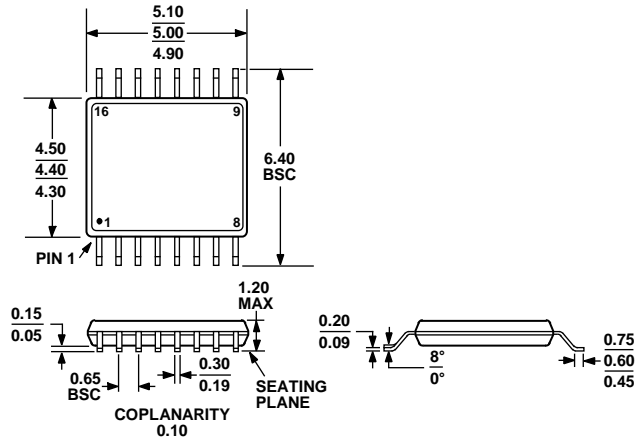


Figure 9. t_{ON}/t_{OFF} Time vs. Temperature (Single Supply)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 10. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---|----------------|
| ADG658TRUZ-EP | -55°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG658TRUZ-EP-RL7 | -55°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |

¹ Z = RoHS Compliant Part.

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