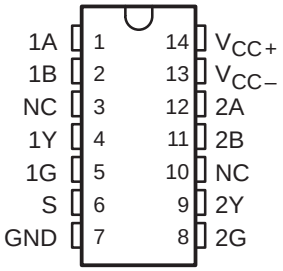
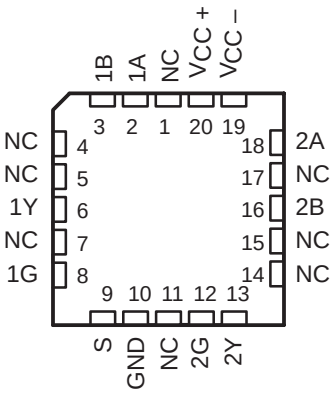
- **High Speed**
- **Standard Supply Voltage**
- **Dual Channels**
- **High Common-Mode Rejection Ratio**
- **High Input Impedance**
- **High Input Sensitivity**
- **Differential Common-Mode Input Voltage Range of ±3 V**
- **Strobe Inputs for Receiver Selection**
- **Gate Inputs for Logic Versatility**
- **TTL Drive Capability**
- **High dc Noise Margin**
- **Totem-Pole Outputs**
- **B Version Has Diode-Protected Input for Power-Off Condition**

SN55107A . . . J OR W PACKAGE
SN75107A, SN75107B, SN75108A . . . D OR N PACKAGE
(TOP VIEW)



SN55107A . . . FK PACKAGE
(TOP VIEW)

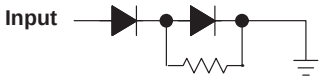


NC – No internal connection

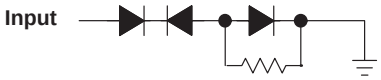
description

These circuits are TTL-compatible, high-speed line receivers. Each is a monolithic dual circuit featuring two independent channels. They are designed for general use, as well as for such specific applications as data comparators and balanced, unbalanced, and party-line transmission systems. These devices are unilaterally interchangeable with and are replacements for the SN55107, SN75107, and SN75108, but offer diode-clamped strobe inputs to simplify circuit design.

The essential difference between the A and B versions can be seen in the schematics. Input-protection diodes are in series with the collectors of the differential-input transistors of the B versions. These diodes are useful in certain party-line systems that have multiple V_{CC+} power supplies and can be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:



A Version



B Version

This would be a problem in specific systems that might have the transmission lines biased to some potential greater than 1.4 V.

The SN55107A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN75107A, SN75107B, and SN75108A are characterized for operation from 0°C to 70°C.

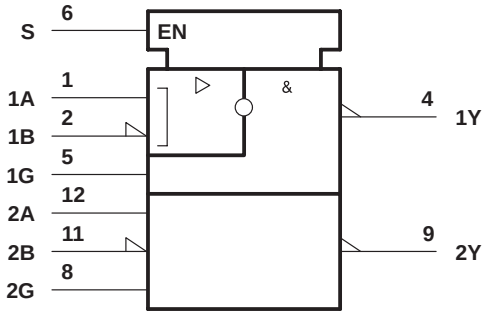
FUNCTION TABLE

DIFFERENTIAL INPUTS A – B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 25$ mV	X	X	H
-25 mV $< V_{ID} < 25$ mV	X	L	H
	L	X	H
	H	H	Indeterminate
$V_{ID} \leq -25$ mV	X	L	H
	L	X	H
	H	H	L

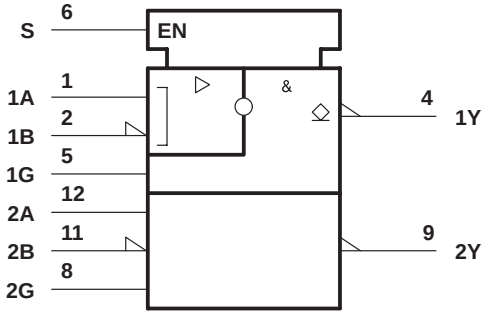
H = high level, L = low level, X = irrelevant

logic symbol†

SN55107A, SN75107A, and SN75107B

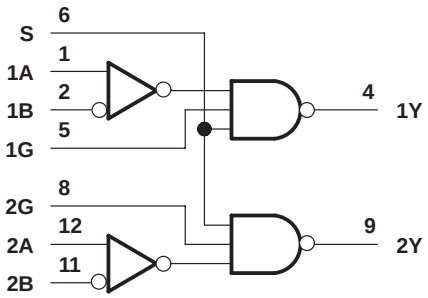


SN75108A

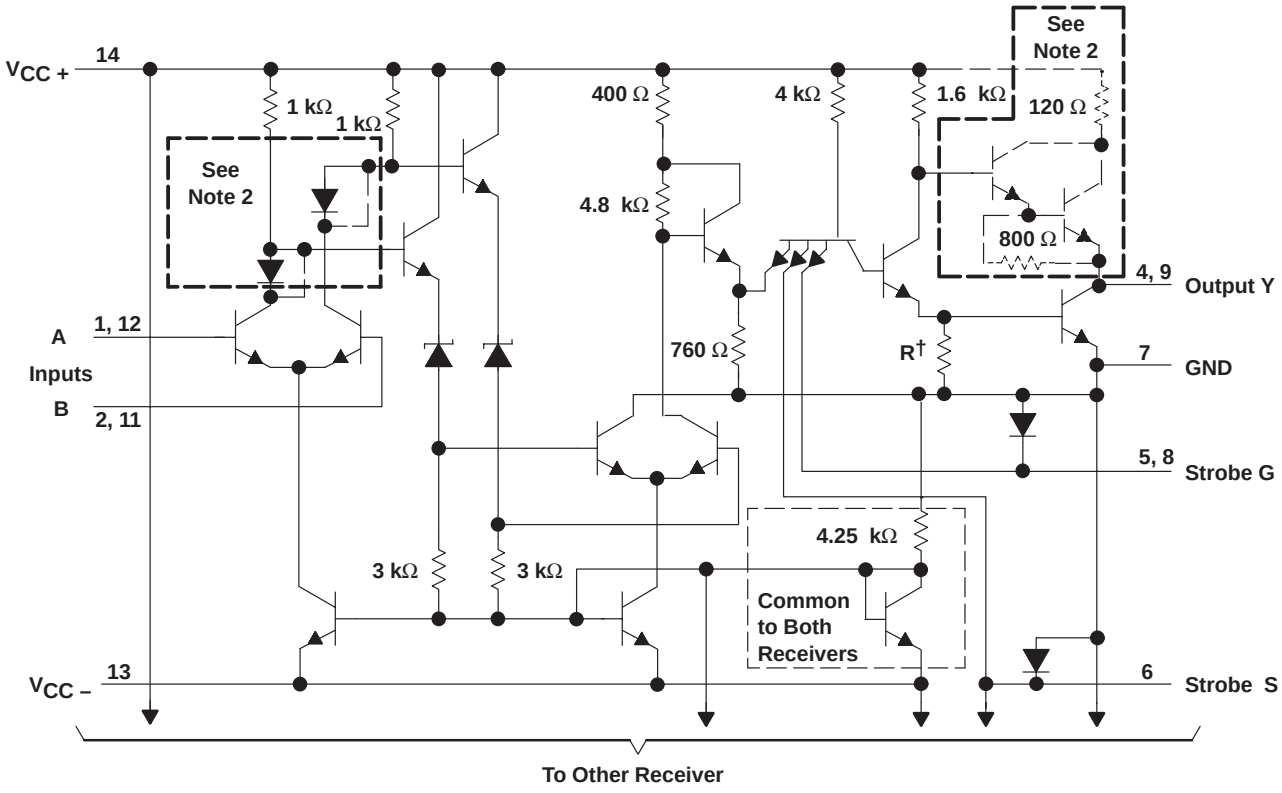


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



schematic (each receiver)



Pin numbers shown are for D, J, N, and W packages.
† R = 1 kΩ for ’107A and SN75107B, 750 Ω for SN75108A.
NOTES: 1. Resistor values shown are nominal.
2. Components shown with dashed lines in the output circuitry are applicable to the ’107A and SN75107B only. Diodes in series with the collectors of the differential input transistors are short circuited on ’107A and SN75108A.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 3) . . . . . 7 V
Supply voltage, V_{CC-} . . . . . –7 V
Differential input voltage, V_{ID} (see Note 4) . . . . . ±6 V
Common-mode input voltage, V_{IC} (see Note 5) . . . . . ±5 V
Strobe input voltage . . . . . 5.5 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 60 seconds, T_c: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or W package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 3. All voltage values, except differential voltages, are with respect to network ground terminal.
4. Differential voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
5. Common-mode input voltage is the average of the voltages at the A and B inputs.

DISSIPATION RATING TABLE

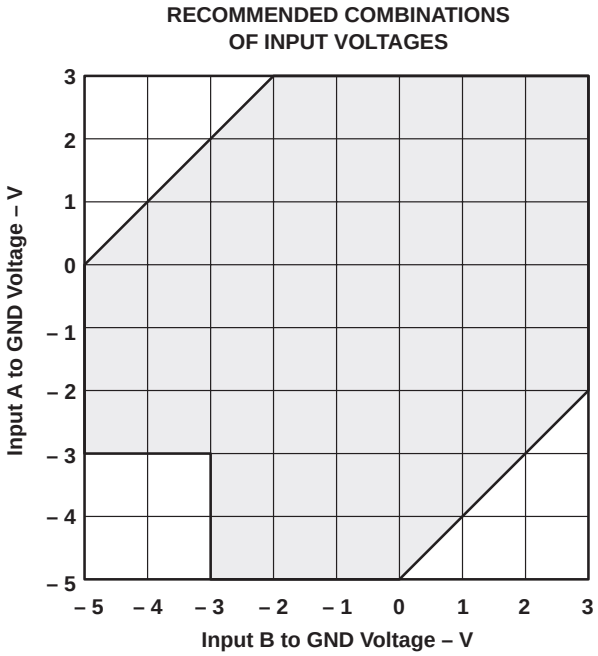
PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions (see Note 6)

	SN55107A			SN75107A, SN75107B, SN75108A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	4.5	5	5.5	4.75	5	5.25	V
Supply voltage, V_{CC-}	–4.5	–5	–5.5	–4.75	–5	–5.25	V
High-level input voltage between differential inputs, V_{IDH} (see Note 7)	0.025		5	0.025		5	V
Low-level input voltage between differential inputs, V_{IDL} (see Note 7)	–5‡		–0.025	–5‡		–0.025	V
Common-mode input voltage, V_{IC} (see Notes 7 and 8)	–3‡		3	–3‡		3	V
Input voltage, any differential input to GND (see Note 8)	–5‡		3	–5‡		3	V
High-level input voltage at strobe inputs, $V_{IH(S)}$	2		5.5	2		5.5	V
Low-level input voltage at strobe inputs, $V_{IL(S)}$	0		0.8	0		0.8	V
Low-level output current, I_{OL}			–16			–16	mA
Operating free-air temperature, T_A	–55		125	0		70	°C

‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for input voltage levels only.

NOTES: 6. When using only one channel of the line receiver, the strobe input (G) of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between –3 V and 3 V.
7. The recommended combinations of input voltages fall within the shaded area in Figure 1.
8. The common-mode voltage may be as low as –4 V provided that the more positive of the two inputs is not more negative than –3 V.



NOTE A: Recommended input-voltage combinations are in the shaded area.

Figure 1. Recommended Combinations of Input Voltages

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

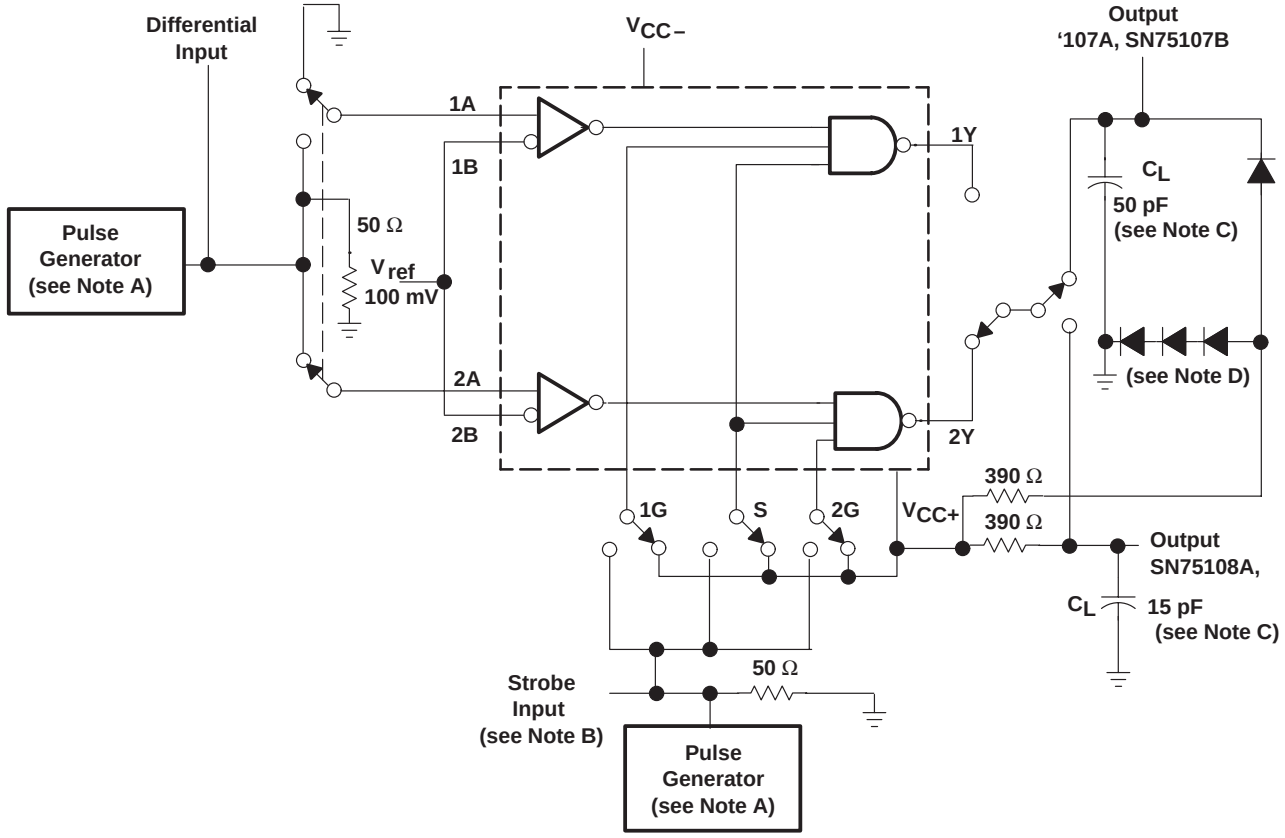
PARAMETER			TEST CONDITIONS†		'107A, SN75107B			SN75108A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-level output voltage		$V_{CC\pm}$ = MIN, V_{IDH} = 25 mV, V_{IC} = –3 V to 3 V	$V_{IL(S)}$ = 0.8 V, I_{OH} = –400 µA,	2.4						V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = MIN, V_{IDL} = –25 mV, V_{IC} = –3 V to 3 V	$V_{IH(S)}$ = 2 V, I_{OL} = 16 mA,			0.4			0.4	V
I_{IH}	High-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = 5 V		30	75		30	75	µA
		B		V_{ID} = –5 V		30	75		30	75	
I_{IL}	Low-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = –5 V			–10			–10	µA
		B		V_{ID} = 5 V			–10			–10	
I_{IH}	High-level input current into 1G or 2G		$V_{CC\pm}$ = MAX,	$V_{IH(G)}$ = 2.4 V			40			40	µA
			$V_{CC\pm}$ = MAX, $V_{IH(G)}$ = MAX V_{CC+}				1			1	mA
I_{IL}	Low-level input current into 1G or 2G		$V_{CC\pm}$ = MAX,	$V_{IL(G)}$ = 0.4 V			–1.6			–1.6	mA
I_{IH}	High-level input current into S		$V_{CC\pm}$ = MAX,	$V_{IH(S)}$ = 2.4 V			80			80	µA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				2			2	mA
I_{IL}	Low-level input current into S		$V_{CC\pm}$ = MAX,	$V_{IL(S)}$= 0.4 V			–3.2			–3.2	mA
I_{OH}	High-level output current		$V_{CC\pm}$ = MIN, V_{OH} = MAX V_{CC+}							250	µA
I_{OS}	Short-circuit output current§		$V_{CC\pm}$ = MAX		–18		–70				mA
I_{CCH+}	Supply current from V_{CC+}, outputs high		$V_{CC\pm}$ = MAX,	T_A = 25°C		18	30		18	30	mA
I_{CCH-}	Supply current from V_{CC-}, outputs high		$V_{CC\pm}$ = MAX,	T_A = 25°C		–8.4	–15		–8.4	–15	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC+} = 5 V, V_{CC-} = –5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

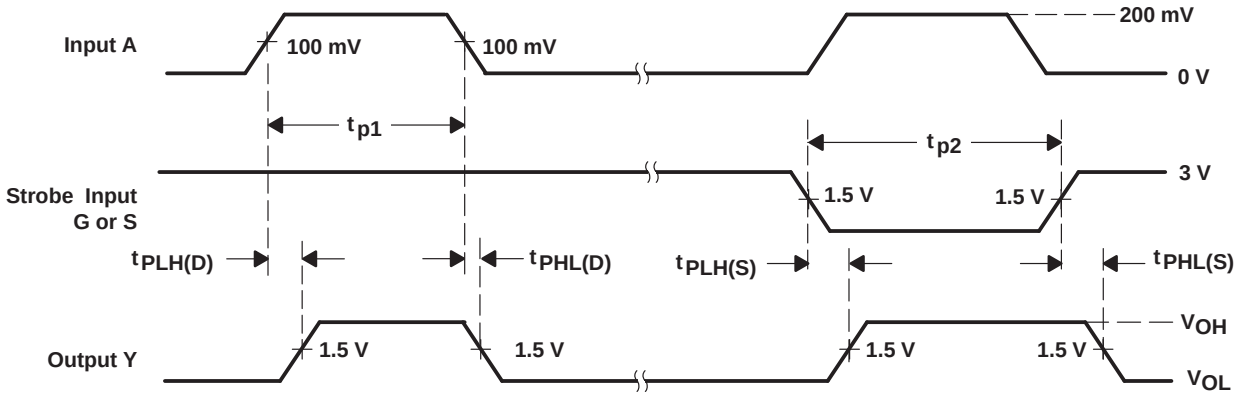
switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C, R_L = 390 Ω (see Figure 2)

PARAMETER		TEST CONDITIONS	'107A, SN75107B			SN75108A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH(D)}$	Propagation delay time, low- to high-level output, from differential inputs A and B	C_L = 50 pF		17	25				ns
		C_L = 15 pF					19	25	
$t_{PHL(D)}$	Propagation delay time, high- to low-level output, from differential inputs A and B	C_L = 50 pF		17	25				ns
		C_L = 15 pF					19	25	
$t_{PLH(S)}$	Propagation delay time, low- to high-level output, from strobe input G or S	C_L = 50 pF		10	15				ns
		C_L = 15 pF					13	20	
$t_{PHL(S)}$	Propagation delay time, high- to low-level output, from strobe input G or S	C_L = 50 pF		8	15				ns
		C_L = 15 pF					13	20	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 10 ± 5 ns, t_f = 10 ± 5 ns, t_{pd1} = 500 ns, PRR ≤ 1 MHz, t_{pd2} = 1 µs, PRR ≤ 500 kHz.
B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

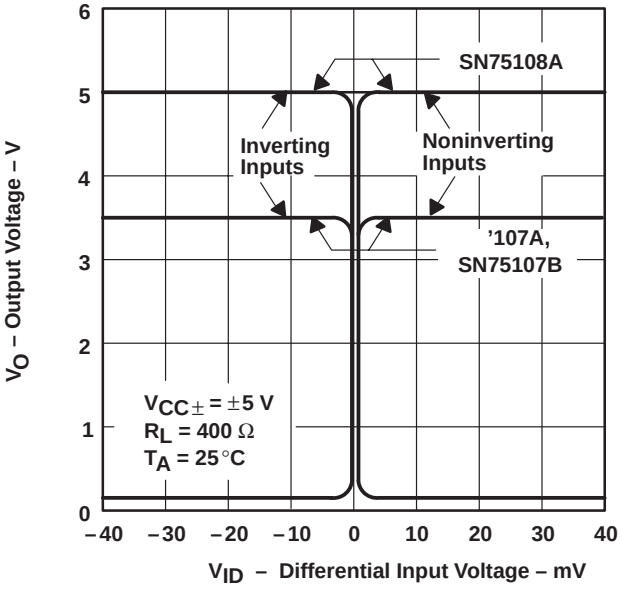


Figure 3

HIGH-LEVEL INPUT CURRENT (1A OR 2A)
vs
FREE-AIR TEMPERATURE

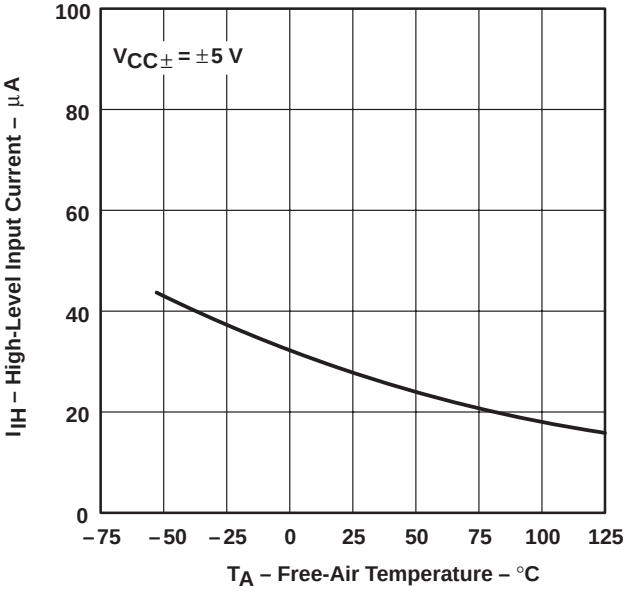


Figure 4

SUPPPLY CURRENT (OUTPUTS HIGH)
vs
FREE-AIR TEMPERATURE

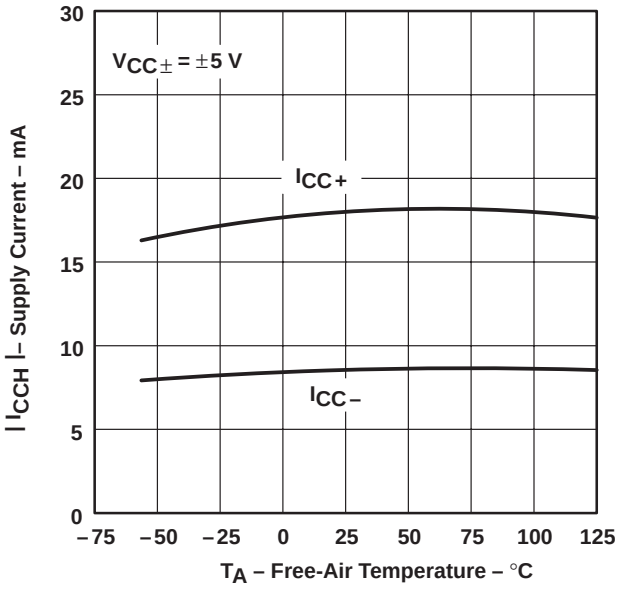


Figure 5

PROPAGATION DELAY TIME
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

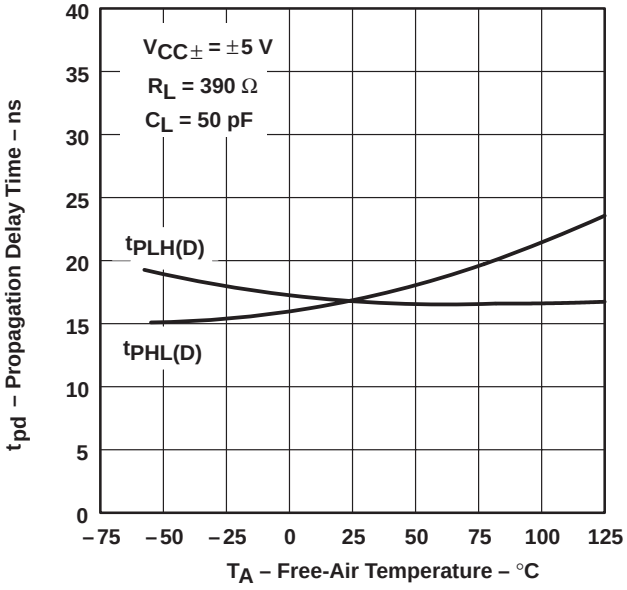


Figure 6

† Values below 0°C and above 70°C apply to SN55107A only.

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIME (LOW-TO-HIGH LEVEL)
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

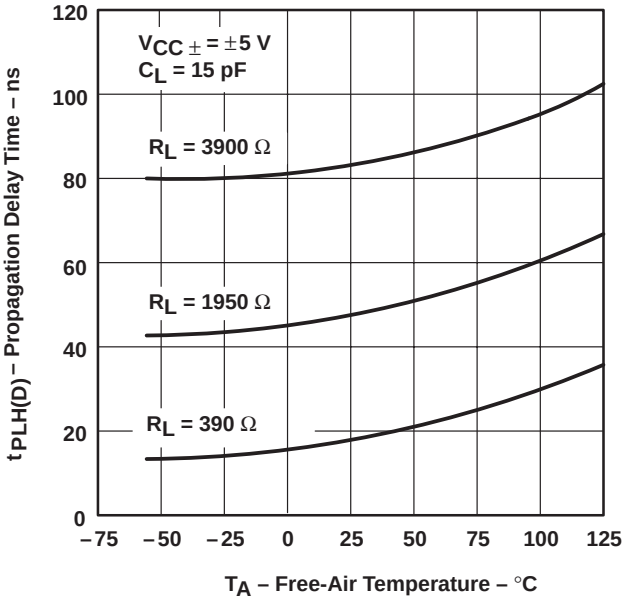


Figure 7

PROPAGATION DELAY TIME (LOW-TO-HIGH LEVEL)
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

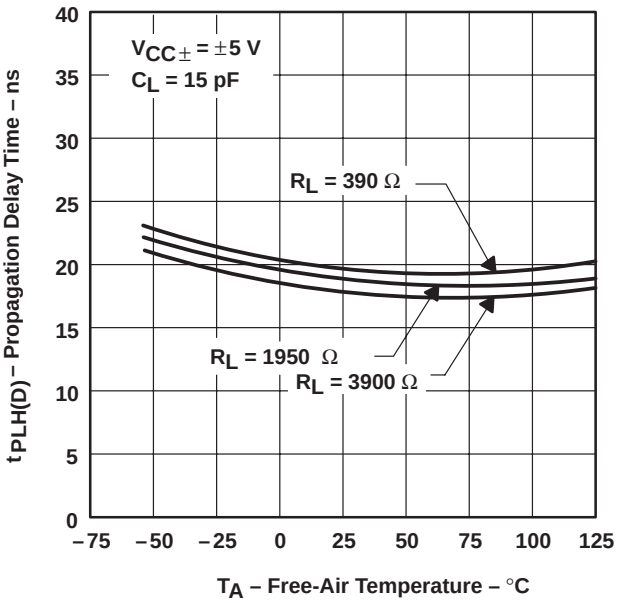


Figure 8

SN75108A
PROPAGATION DELAY TIME (STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

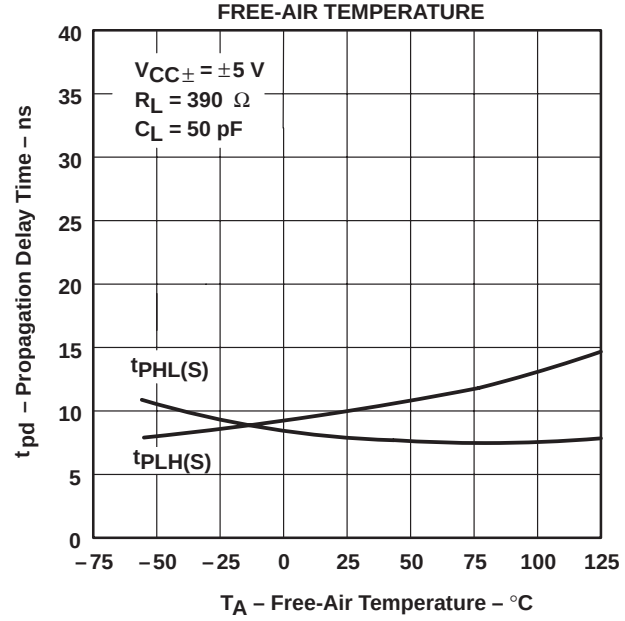


Figure 9

SN75108A
PROPAGATION DELAY TIME (STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

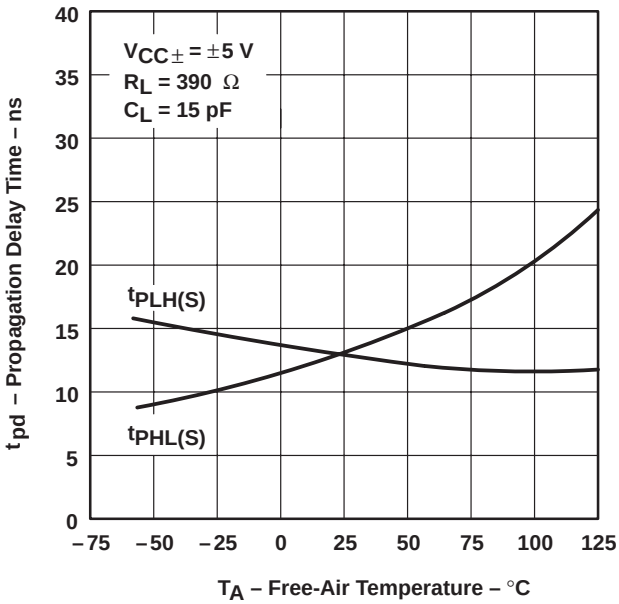


Figure 10

† Values below 0°C and above 70°C apply to SN55107A only.

APPLICATION INFORMATION

basic balanced-line transmission system

The ’107A, SN75107B, and SN75108A dual line devices are designed specifically for use in high-speed data-transmission systems that utilize balanced terminated transmission lines, such as twisted-pair lines. The system operates in the balanced mode, so noise induced on one line is also induced on the other. The noise appears common mode at the receiver input terminals, where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit; therefore, system performance is not affected by circulating ground currents.

The unique driver-output circuit allows terminated transmission lines to be driven at normal line impedances. High-speed system operation is ensured because line reflections are virtually eliminated when terminated lines are used. Crosstalk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately 30 + 1.3 L ns, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately:

$$V_{DIFF} \approx 1/2 I_{O(on)} \bullet R_T$$

High series line resistance causes degradation of the signal. However, the receivers detect signals as low as 25 mV. For normal line resistances, data can be recovered from lines of several thousand feet in length.

Line-termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may be adequate. The signal amplitude is then approximately:

$$V_{DIFF} \approx I_{O(on)} \bullet R_T$$

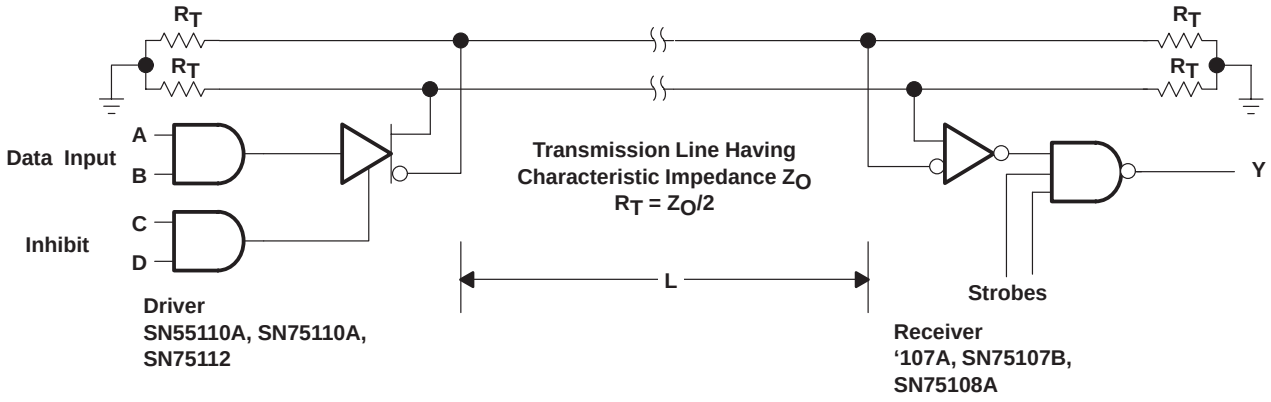


Figure 11. Typical Differential Data Line

data-bus or party-line system

The strobe feature of the receivers and the inhibit feature of the drivers allow these dual line devices to be used in data-bus or party-line systems. In these applications, several drivers and receivers can share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is time multiplexed on the transmission line. The device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.

APPLICATION INFORMATION

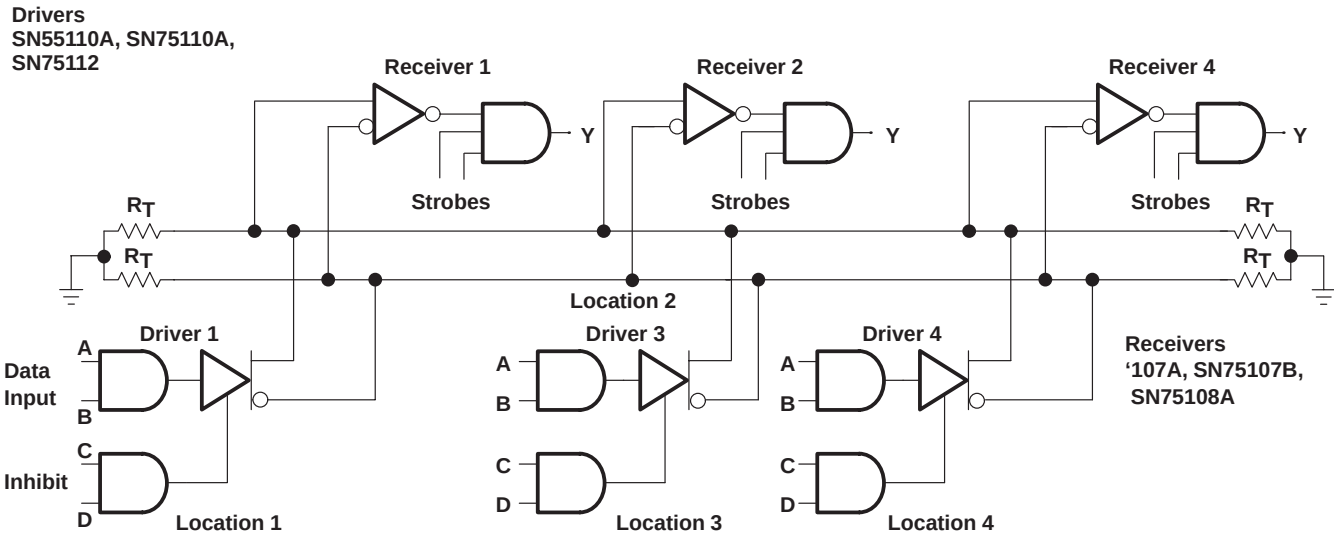


Figure 12. Typical Differential Party Line

unbalanced or single-line systems

These dual line circuits also can be used in unbalanced or single-line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environmental noise is not severe.

The receiver threshold level is established by applying a dc reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of –3 V to 3 V. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

A single-ended output from a driver can be used in single-line systems. Coaxial or shielded line is preferred for minimum noise and crosstalk problems. For large signal swings, the high output current (typically 27 mA) of the SN75112 is recommended. Drivers can be paralleled for higher current. When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

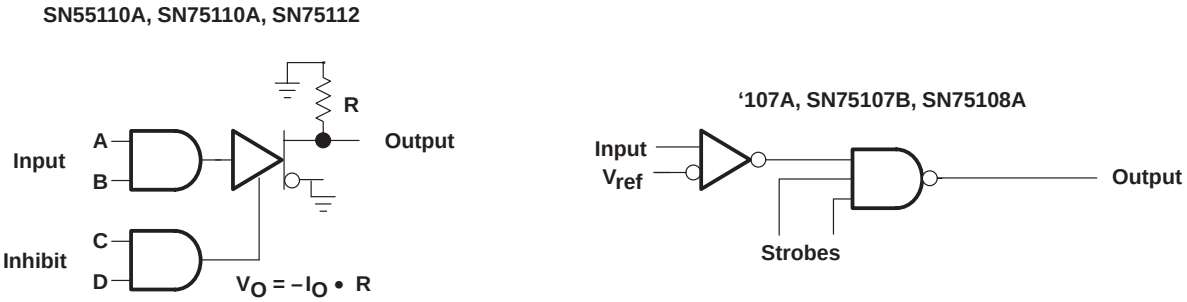


Figure 13. Single-Ended Operation

APPLICATION INFORMATION

SN75108A dot-AND output connections

The SN75108A line receiver features an open-collector-output circuit that can be connected in the dot-AND logic configuration with other similar open-collector outputs. This allows a level of logic to be implemented without additional logic delay.

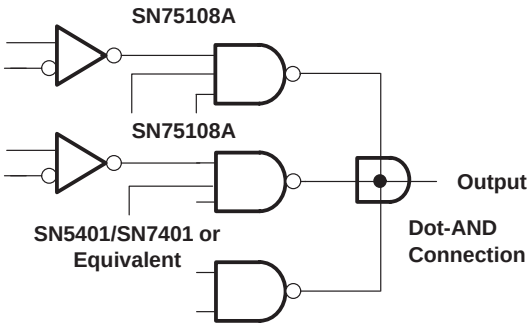


Figure 14. Dot-AND Connection

increasing common-mode input voltage range of receiver

The common-mode voltage range (CMVR) is defined as the range of voltage applied simultaneously to both input terminals that, if exceeded, does not allow normal operation of the receiver.

The recommended operating CMVR is ±3 V, making it useful in all but the noisiest environments. In extremely noisy environments, common-mode voltage can easily reach ±10 V to ±15 V if some precautions are not taken to reduce ground and power supply noise, as well as crosstalk problems. When the receiver must operate in such conditions, input attenuators should be used to decrease the system common-mode noise to a tolerable level at the receiver inputs. Differential noise is also reduced by the same ratio. These attenuators were omitted intentionally from the receiver input terminals so the designer can select resistors that are compatible with his particular application or environment. Furthermore, the use of attenuators adversely affects the input sensitivity, the propagation delay time, the power dissipation, and in some cases (depending on the selected resistor values) the input impedance; thereby reducing the versatility of the receiver.

The ability of the receiver to operate with approximately ±15 V common-mode voltage at the inputs has been checked using the circuit shown in Figure 15. Resistors R1 and R2 provide a voltage-divider network. Dividers with three different values presenting a 5-to-1 attenuation were used to operate the differential inputs at approximately ±3 V common-mode voltage. Careful matching of the two attenuators is needed to balance the overdrive at the input stage. The resistors used are shown in Table 1.

Table 1

Attenuator 1:	R1 = 2 kΩ,	R2 = 0.5 kΩ
Attenuator 2:	R1 = 6 kΩ,	R2 = 1.5 kΩ
Attenuator 3:	R1 = 12 kΩ,	R2 = 3 kΩ

APPLICATION INFORMATION

increasing common-mode input voltage range of receiver (continued)

Table 2 shows some of the typical switching results obtained under such conditions.

Table 2. Typical Propagation Delays for Receiver With Attenuator Test Circuit Shown in Figure 15

DEVICE	PARAMETERS	INPUT ATTENUATOR	TYPICAL (NS)
'107A SN75107B	t_{PLH}	1	20
		2	32
		3	42
	t_{PHL}	1	22
		2	31
		3	33
SN75108A	t_{PLH}	1	36
		2	47
		3	57
	t_{PHL}	1	29
		2	38
		3	41

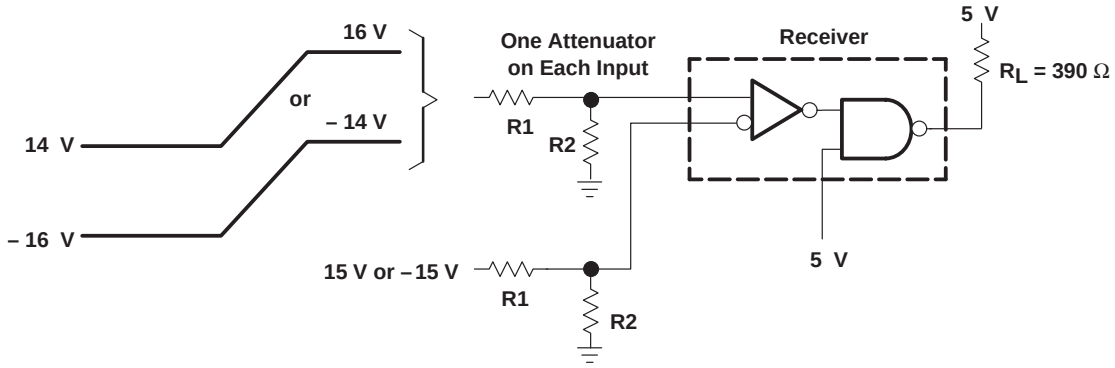
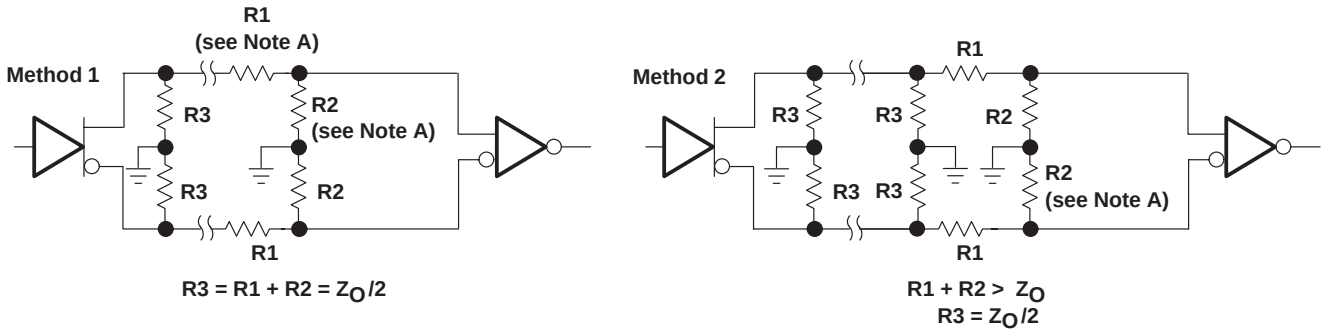


Figure 15. Common-Mode Circuit for Testing Input Attenuators With Results Shown in Table 2

Two methods of terminating a transmission line to reduce reflections are shown in Figure 16. The first method uses the resistors as the attenuation network and line termination. The second method uses two additional resistors for the line terminations.

APPLICATION INFORMATION



NOTE A: To minimize the loading, the values of R1 and R2 should be fairly large. Examples of possible values are shown in Table 1.

Figure 16. Termination Techniques

For party-line operation, method 2 should be used as shown in Figure 17.

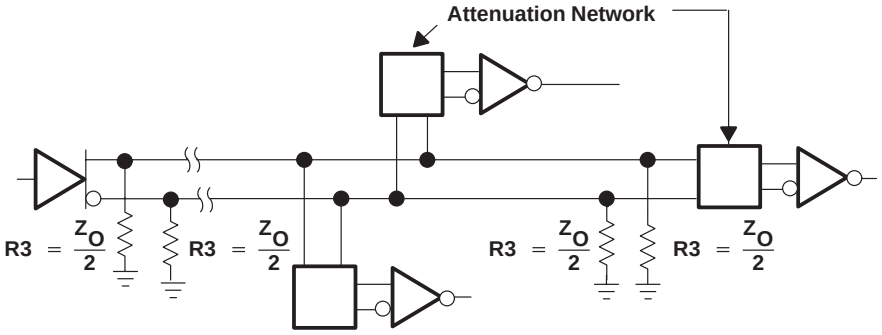


Figure 17. Party-Line Termination Technique

APPLICATION INFORMATION

furnace control using the SN75108A

The furnace control circuit in Figure 18 is an example of the possible use of the SN75108A series in areas other than what would normally be considered electronic systems. A description of the operation of this control follows. When the room temperature is below the desired level, the resistance of the room temperature sensor is high and channel 1 noninverting input is below (less positive than) the reference level set on the input differential amplifier. This situation causes a low output, operating the heat-on relay and turning on the heat. The channel 2 noninverting input is below the reference level when the bonnet temperature of the furnace reaches the desired level. This causes a low output, thus operating the blower relay. Normally the furnace is shut down when the room temperature reaches the desired level and the channel 1 output goes high, turning the heat off. The blower remains on as long as the bonnet temperature is high, even after the heat-on relay is off. There is also a safety switch in the bonnet that shuts down the furnace if the temperature there exceeds desired limits. The types of temperature-sensing devices and bias-resistor values used are determined by the particular operating conditions encountered.

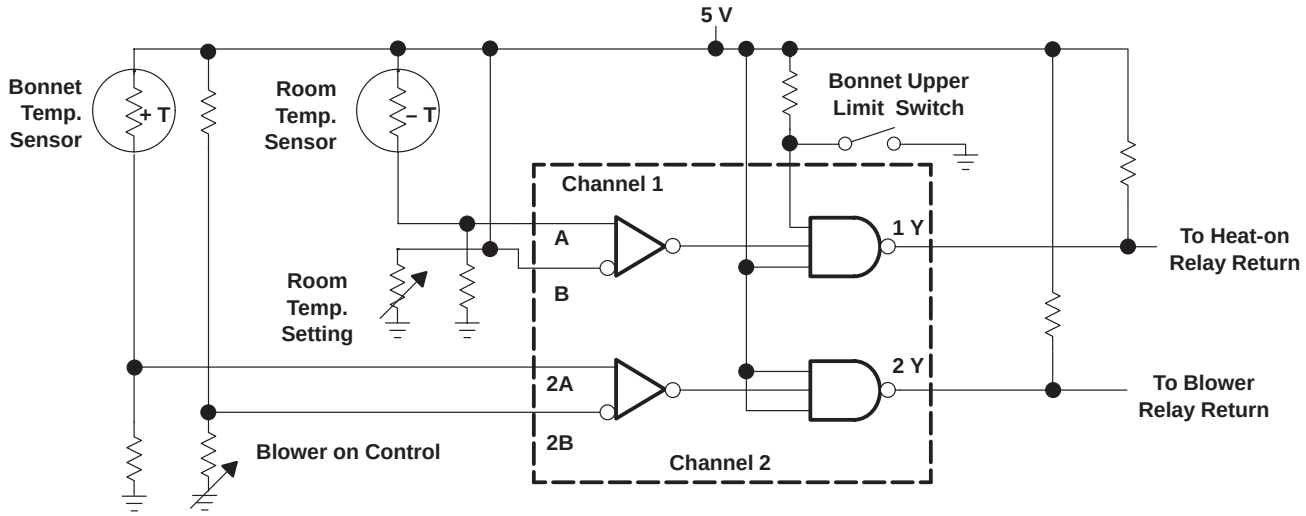


Figure 18. Furnace Control Using SN75108A

APPLICATION INFORMATION

repeaters for long lines

In some cases, the driven line may be so long that the noise level on the line reaches the common-mode limits or the attenuation becomes too large and results in poor reception. In such a case, a simple application of a receiver and a driver as repeaters [shown in Figure 19(a)] restores the signal level and allows an adequate signal level at the receiving end. If multichannel operation is desired, then proper gating for each channel must be sent through the repeater station using another repeater set as in Figure 19(b).

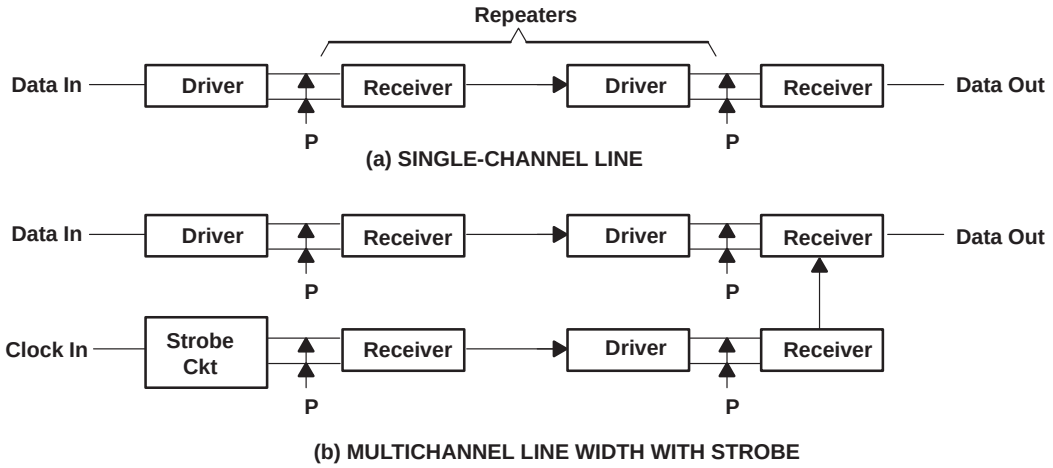


Figure 19. Receiver-Driver Repeaters

receiver as dual differential comparator

There are many applications for differential comparators, such as voltage comparison, threshold detection, controlled Schmitt triggering, and pulse-width control.

As a differential comparator, a ’107A or SN75108A can be connected to compare the noninverting input terminal with the inverting input as shown in Figure 20. The output is high or low, resulting from the A input being greater or less than the reference. The strobe inputs allow additional control over the circuit so that either output, or both, can be inhibited.

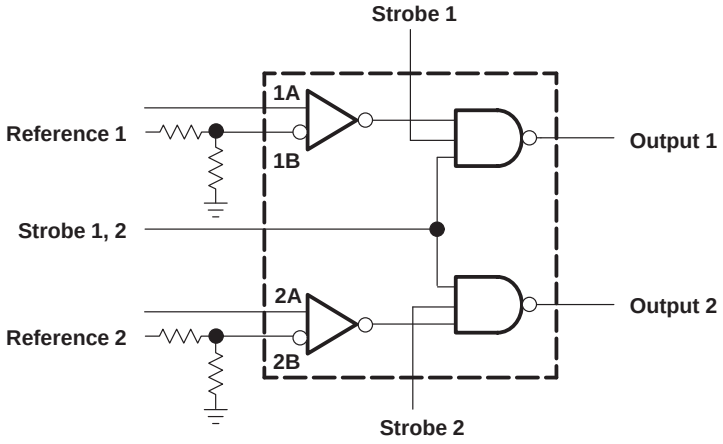
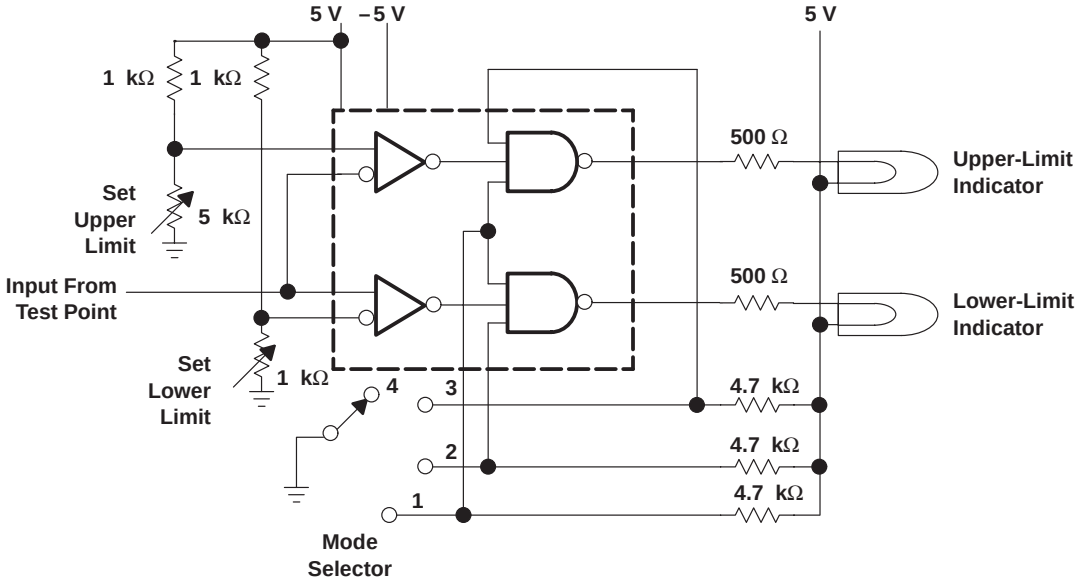


Figure 20. SN75107A Series Receiver as a Dual Differential Comparator

APPLICATION INFORMATION

window detector

The window detector circuit in Figure 21 has a large number of applications in test equipment and in determining upper limits, lower limits, or both at the same time, such as detecting whether a voltage or signal has exceeded its window limits. Illumination of the upper-limit (lower-limit) indicator shows that the input voltage is above (below) the selected upper (lower) limit. A mode selector is provided for selecting the desired test. For window detecting, the upper-and-lower-limits test position is used.



MODE SELECTOR LEGEND

POSITION	CONDITION
1	Off
2	Test for Upper Limit
3	Test for Lower Limit
4	Test for Upper and Lower Limits

Figure 21. Window Detector Using SN75108A

APPLICATION INFORMATION

temperature controller with zero-voltage switching

The circuit in Figure 22 switches an electric-resistive heater on or off by providing negative-going pulses to the gate of a triac during the time interval when the line voltage is passing through zero. The pulse generator is the 2N5447 and four diodes. This portion of the circuit provides negative-going pulses during the short time (approximately 100 μs) when the line voltage is near zero. These pulses are fed to the inverting input of one channel of the SN75108A. If the room temperature is below the desired level, the resistance of the thermistor is high and the noninverting input of channel 2 is above the reference level determined by the thermostat setting. This provides a high-level output from channel 2. This output is ANDed with the positive-going pulses from the output of channel 1, which are reinverted in the 2N5449.

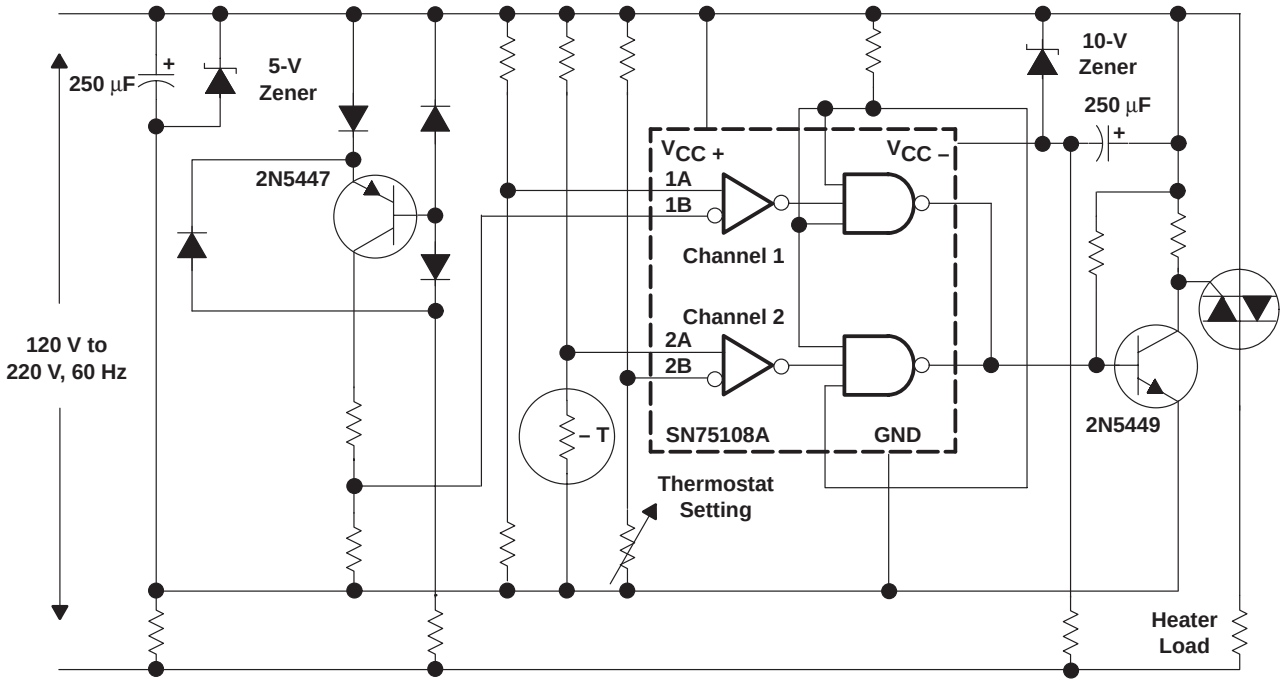


Figure 22. Zero-Voltage Switching Temperature Controller

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9690301Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9690301Q2A SNJ55107AFK	Samples
5962-9690301QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9690301QCA SNJ55107AJ	Samples
5962-9690301QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9690301QDA SNJ55107AW	Samples
JM38510/10401BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/10401BCA	Samples
M38510/10401BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/10401BCA	Samples
SN55107AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN55107AJ	Samples
SN75107AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75107A	Samples
SN75107ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75107A	Samples
SN75107AN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN75107AN	Samples
SN75107ANE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN75107AN	Samples
SN75107ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75107A	Samples
SN75107BD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75107B	Samples
SN75107BDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75107B	Samples
SN75107BDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75107B	Samples
SN75107BN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN75107BN	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75107BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75107B	Samples
SN75108AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75108A	Samples
SN75108ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75108A	Samples
SNJ55107AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9690301Q2A SNJ55 107AFK	Samples
SNJ55107AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9690301QCA SNJ55107AJ	Samples
SNJ55107AW	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9690301QDA SNJ55107AW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN55107A, SN75107A :

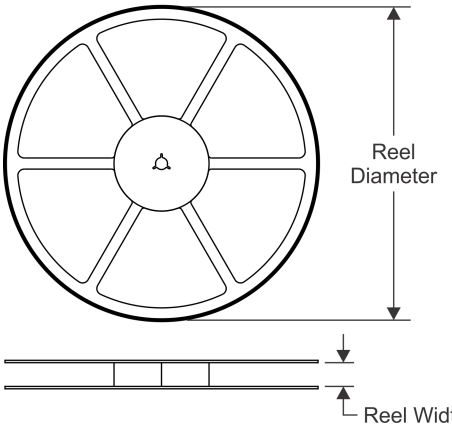
- Catalog: SN75107A
- Military: SN55107A

NOTE: Qualified Version Definitions:

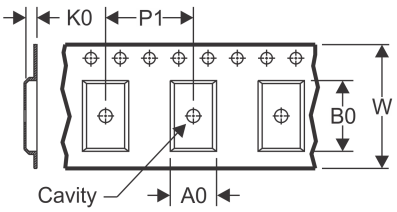
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

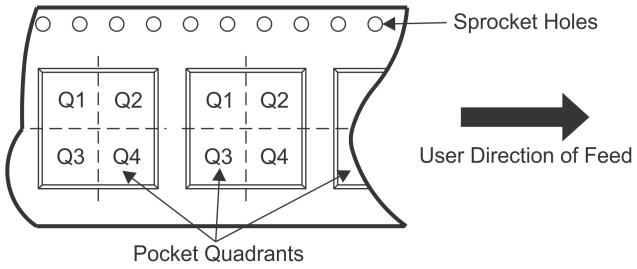


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

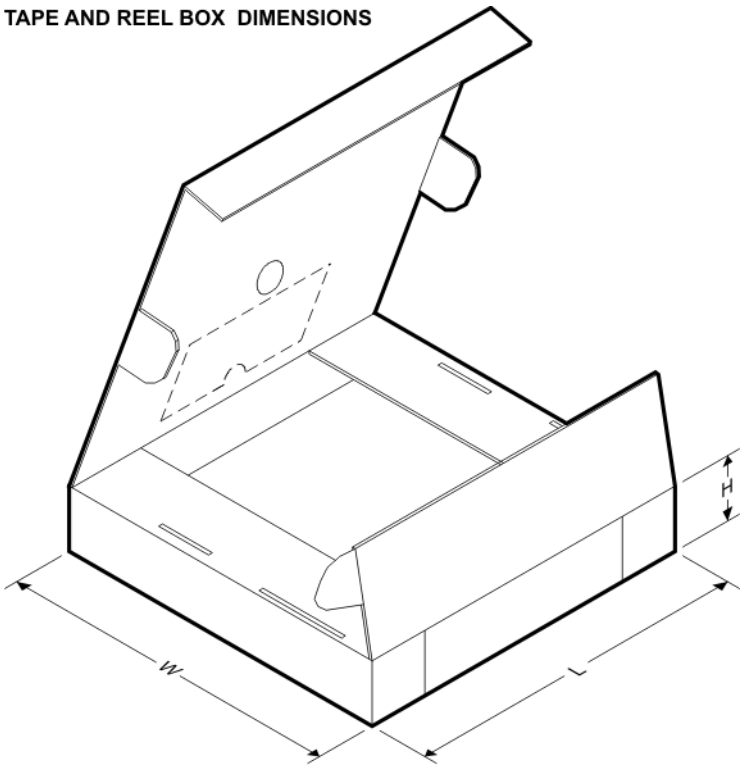
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75107ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75107ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75107BDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75107BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75108ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



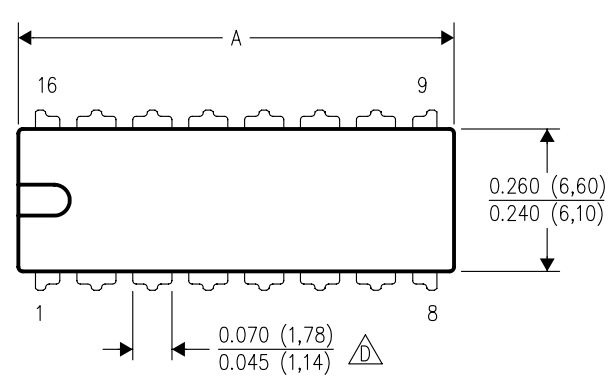
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75107ADR	SOIC	D	14	2500	367.0	367.0	38.0
SN75107ANSR	SO	NS	14	2000	367.0	367.0	38.0
SN75107BDR	SOIC	D	14	2500	367.0	367.0	38.0
SN75107BNSR	SO	NS	14	2000	367.0	367.0	38.0
SN75108ADR	SOIC	D	14	2500	367.0	367.0	38.0

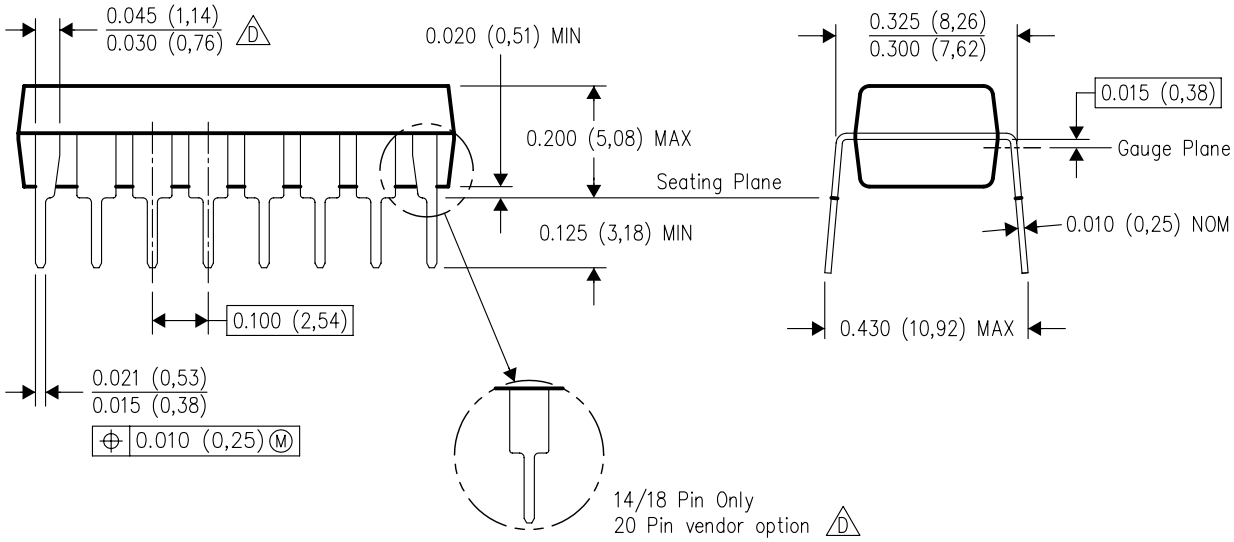
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

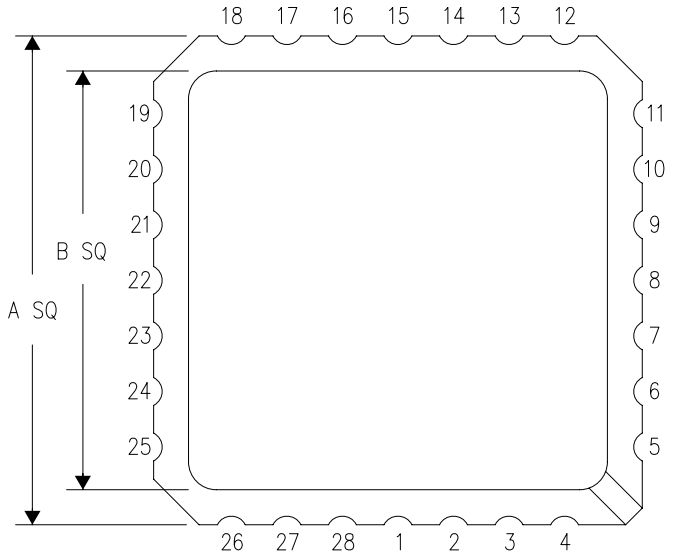


4040049/E 12/2002

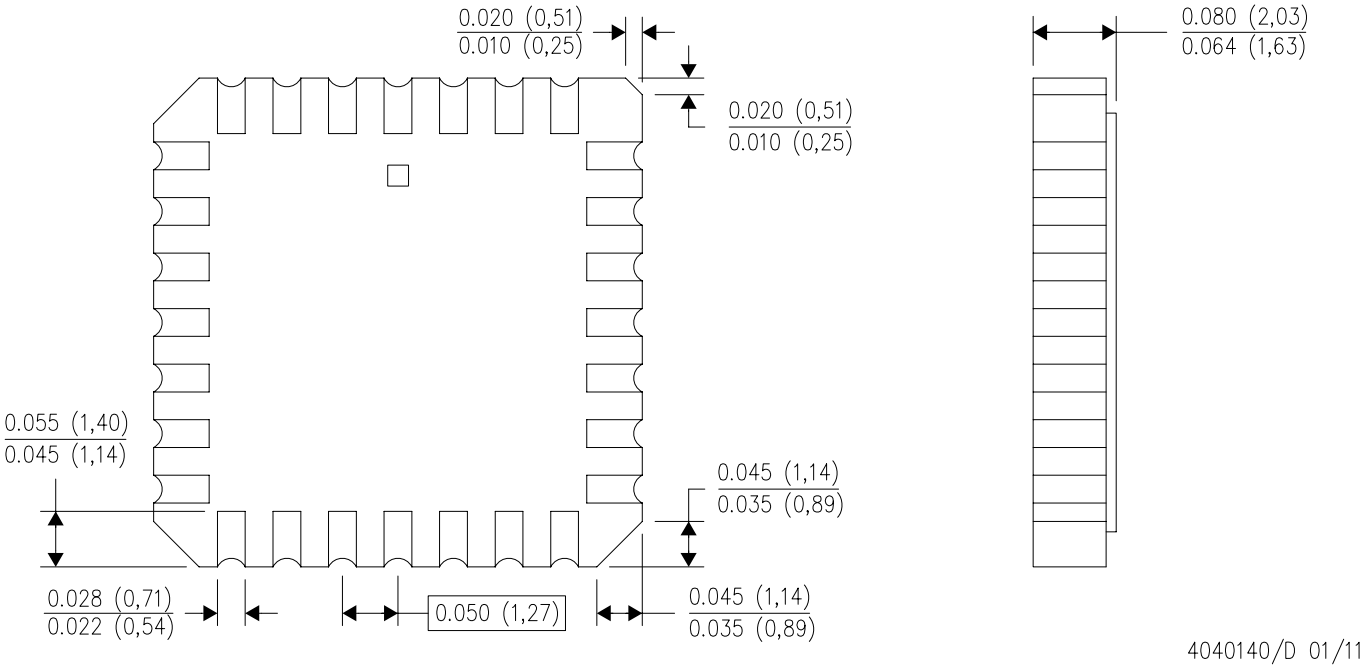
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



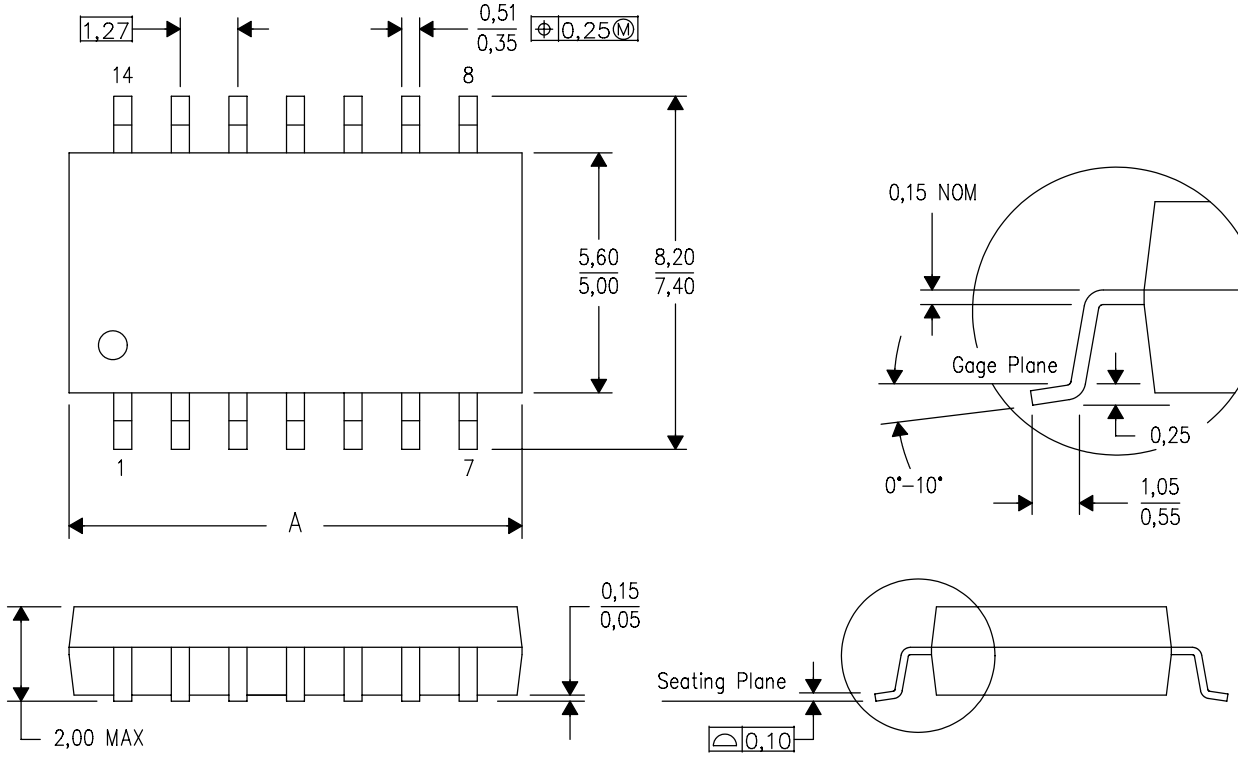
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

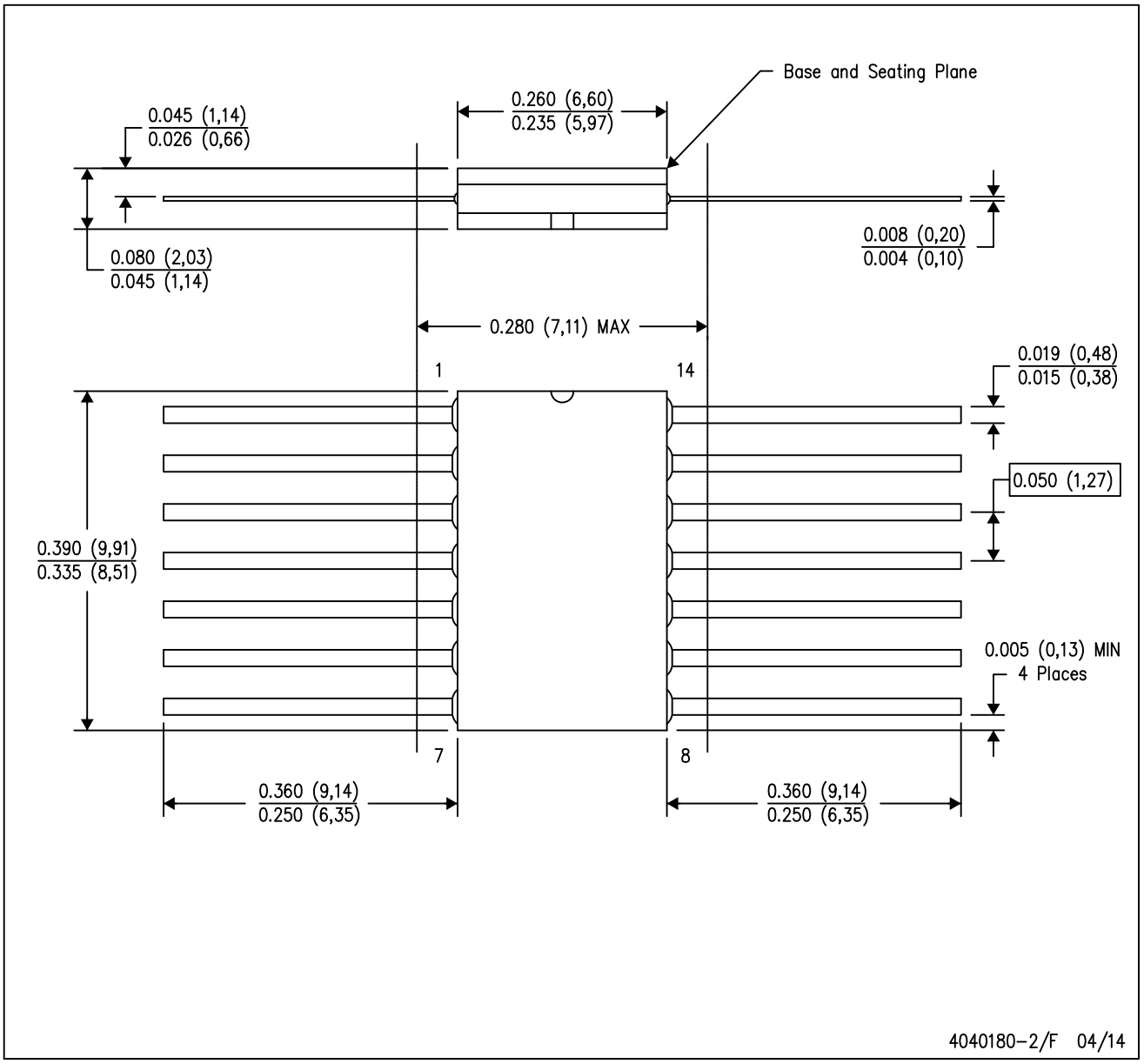


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

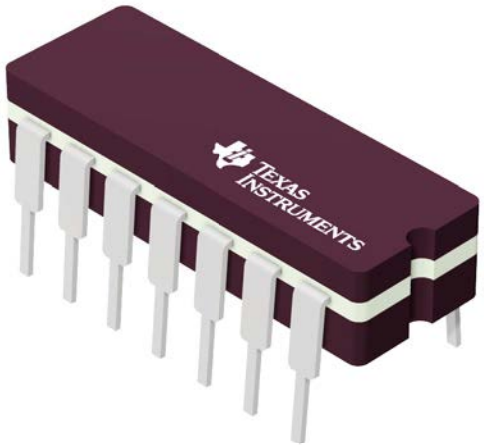


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

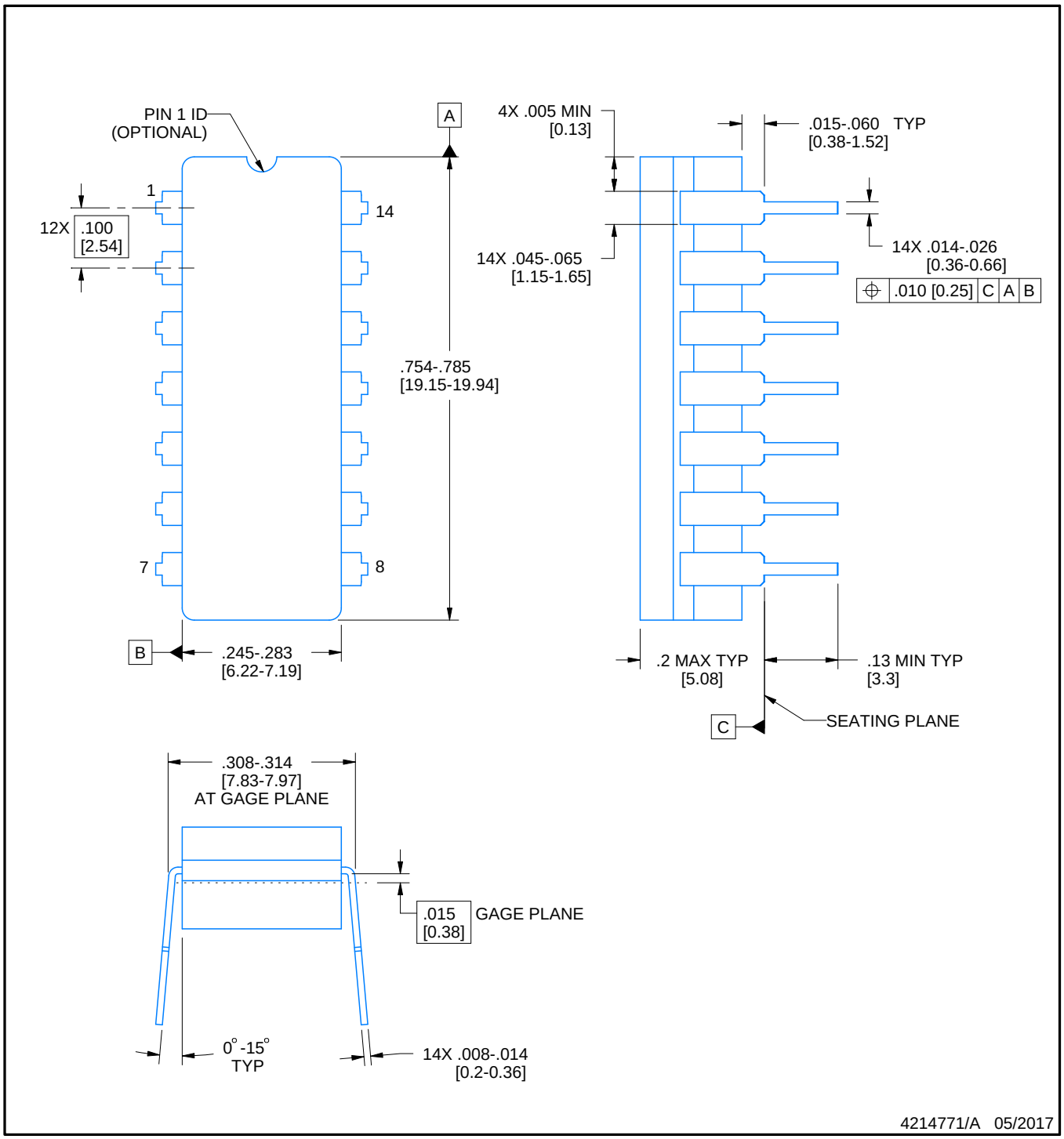
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

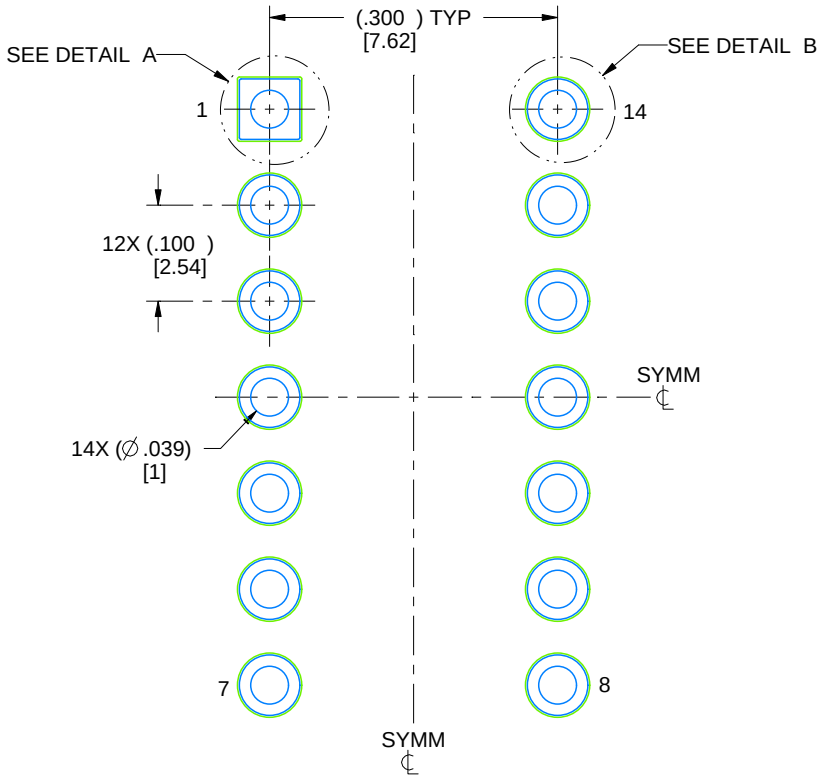
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

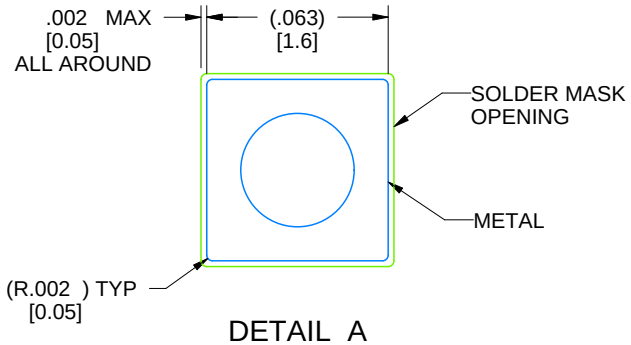
J0014A

CDIP - 5.08 mm max height

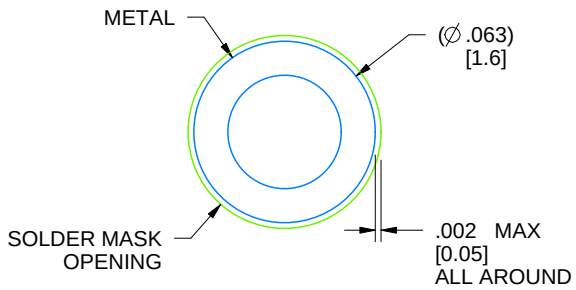
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



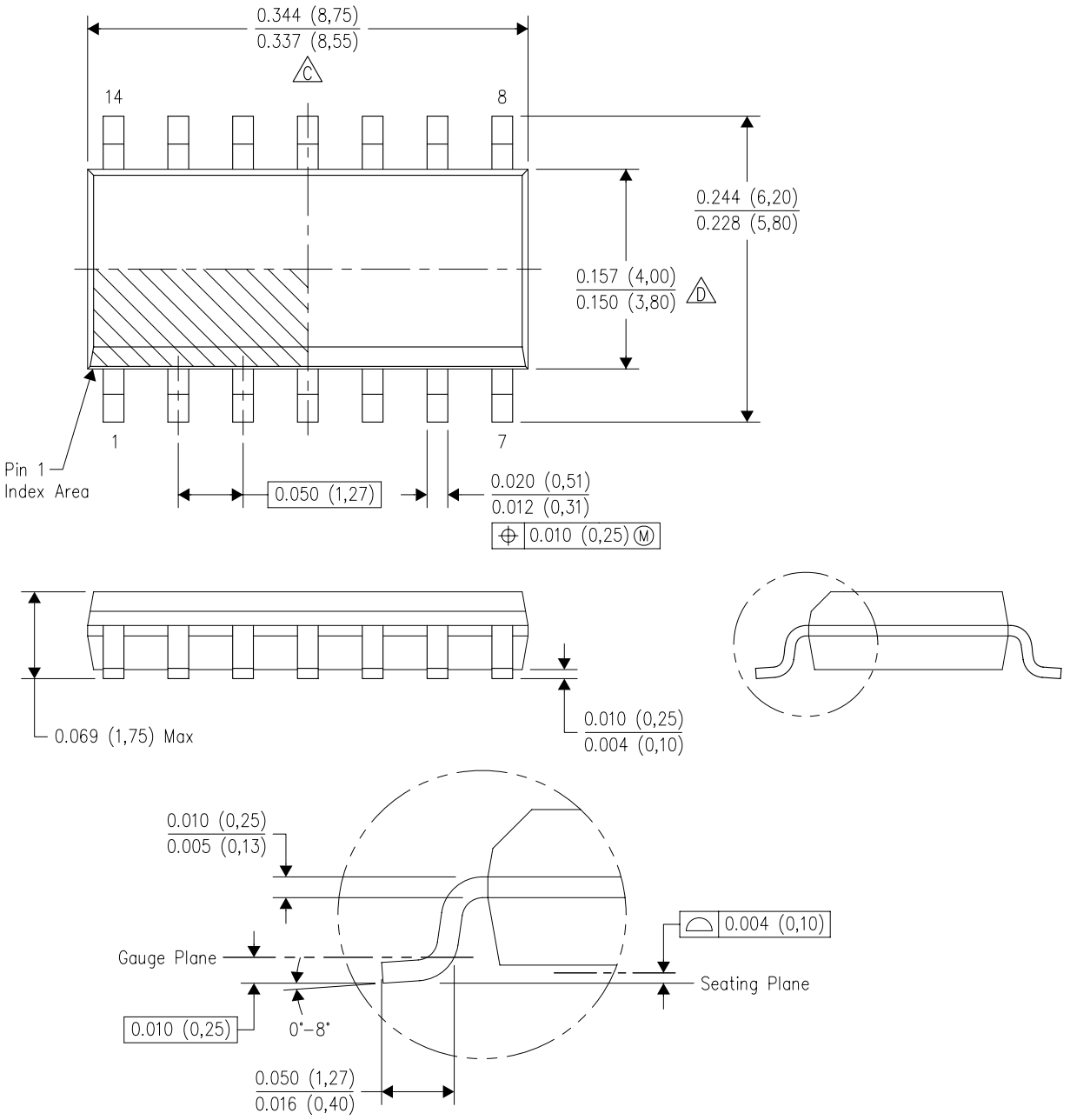
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

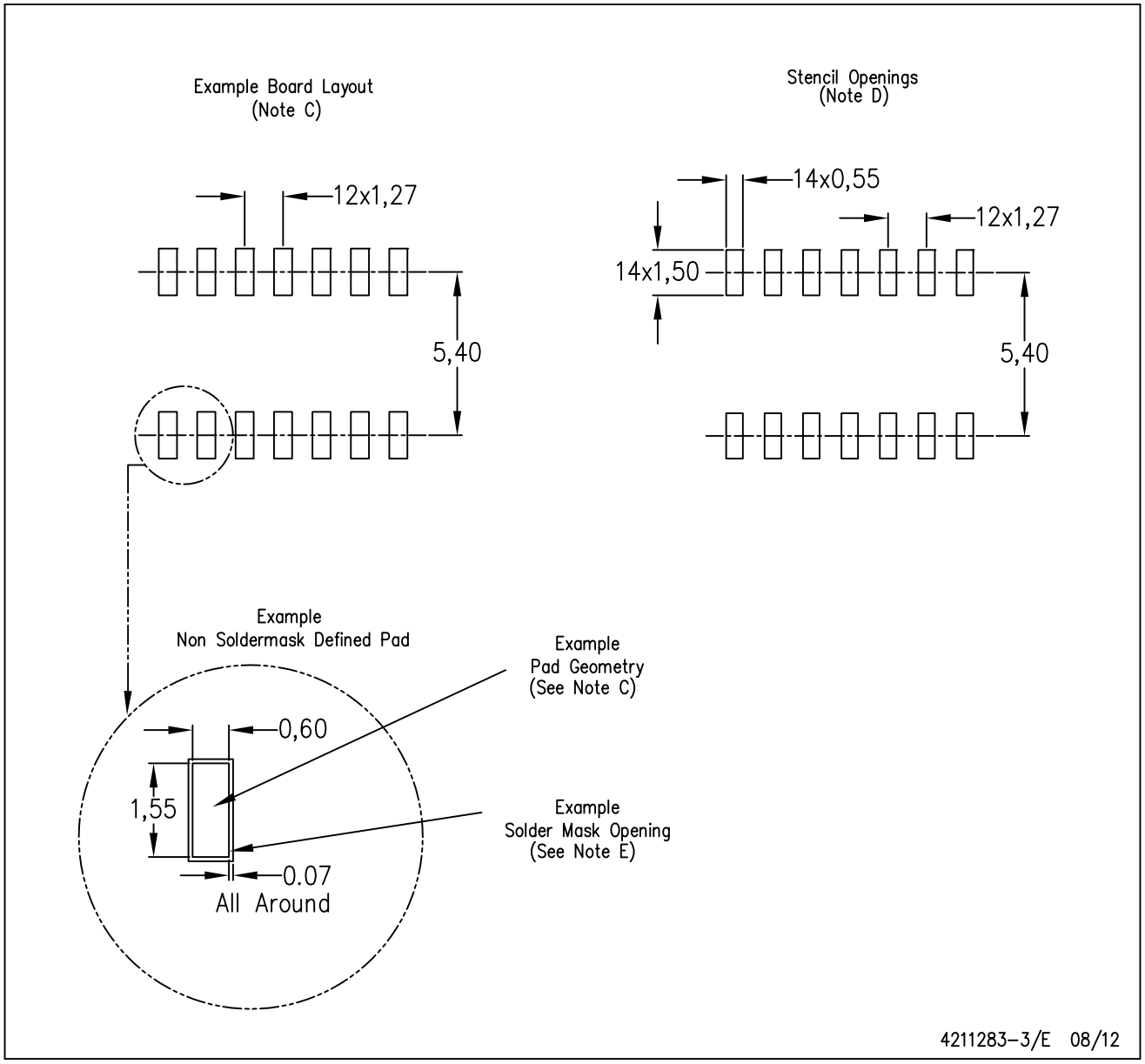
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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