Ordering number : ENA0693

LV5609V

Bi-CMOS LSI

Vertical Clock Driver for CCD

ON Semiconductor®

http://onsemi.com

Overview

The LV5609V is vertical clock driver for CCD.

Functions

- Ternary output ×2ch
- Binary output ×2ch
- SHT output ×1ch
- Output ON resistance : 30Ω typ

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = VM = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		6	V
	VH max		20	V
	VL max		-10	V
	VH-VL max		24	V
Allowable power dissipation	Pd max	with specified substrate *	0.67	W
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-40 to +125	°C

* : Specified substrate : 114.3×76.1×1.6mm³, glass epoxy board

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ratings at Ta = 25°C, V_{SS} = VM = 0V

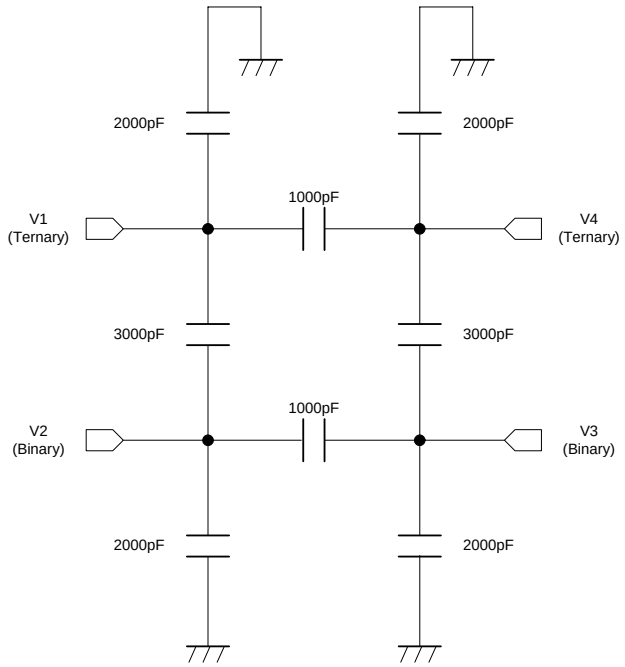
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.0	3.3	5.5	V
	VH			15	17	V
	VL		-8.5	-7.5	-4	V
	VH-VL				23.5	V
CMOS input High voltage	$V_{IN}H$		0.8V_{DD}		V_{DD}	V
CMOS input Low voltage	$V_{IN}L$		-0.1		0.4	V

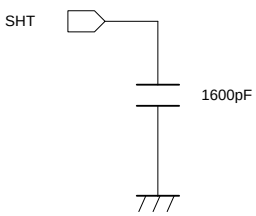
Electrical Characteristics at Ta = 25°C, V_{DD} = 3.3V, V_{SS} = 0V, VH = 15V, VL = -7.5V, VM = 0V, Unless otherwise specified

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Static current drain	I_{DD}	V_{DD} pin			1	μA
	IH	VH pin			10	μA
	IL	VL pin			1	μA
Dynamic current drain	I_{DD}	V_{DD} pin See *1 and *2.			1	mA
	IH	VH pin See *1 and *2.		2.4	4.5	mA
	IL	VL pin See *1 and *2.		3	5	mA
Output ON resistance	RL	I_O = +10mA		20	30	Ω
	RM	I_O = ±10mA		30	45	Ω
	RH	I_O = -10mA		30	40	Ω
	RSHT	I_O = -10mA		30	40	Ω
Propagation delay time	TPLM	No load			200	ns
	TPMH	No load			200	ns
	TPLH	No load			200	ns
	TPML	No load			200	ns
	TPHM	No load			200	ns
	TPHL	No load			200	ns
Rise time	TTLM	VL → VM V1, V3 See *1.			800	ns
		VL → VM V2, V4 See *1.			800	ns
	TTMH	VM → VL V1, V3 See *1.			800	ns
	TTLH	VL → VH SHT See *1.			200	ns
Fall time	TTML	VM → VL V1, V3 See *1.			800	ns
		VM → VL V2, V4 See *1.			800	ns
	TTHM	VH → VM V1, V3 See *1.			800	ns
	TTHL	VH → VL SHT See *1.			200	ns

*1 : Refer to the CCD equivalent load shown below.

*2 : Refer to the timing waveform on Page 7.

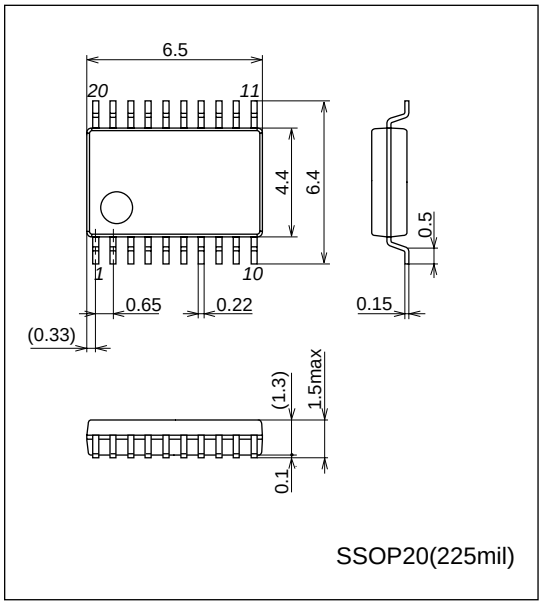


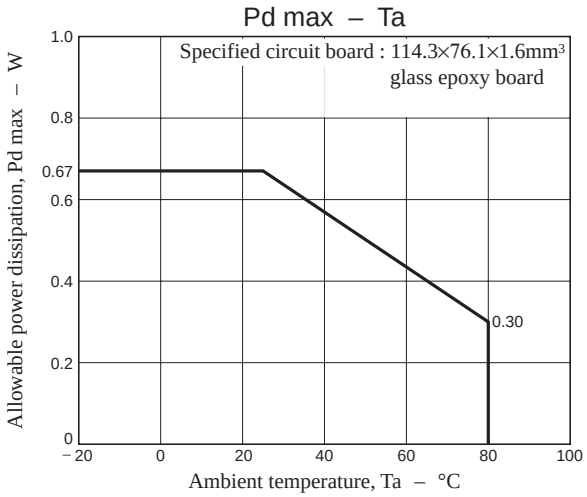


Package Dimensions

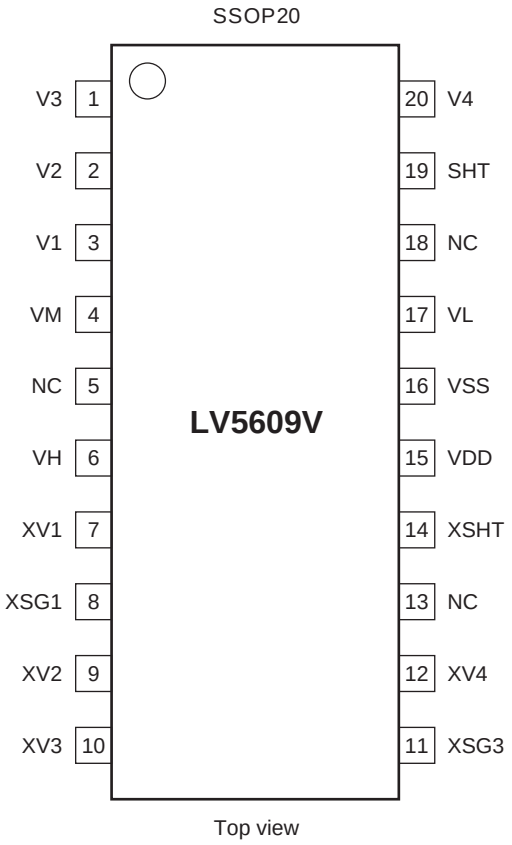
unit : mm (typ)

3179C





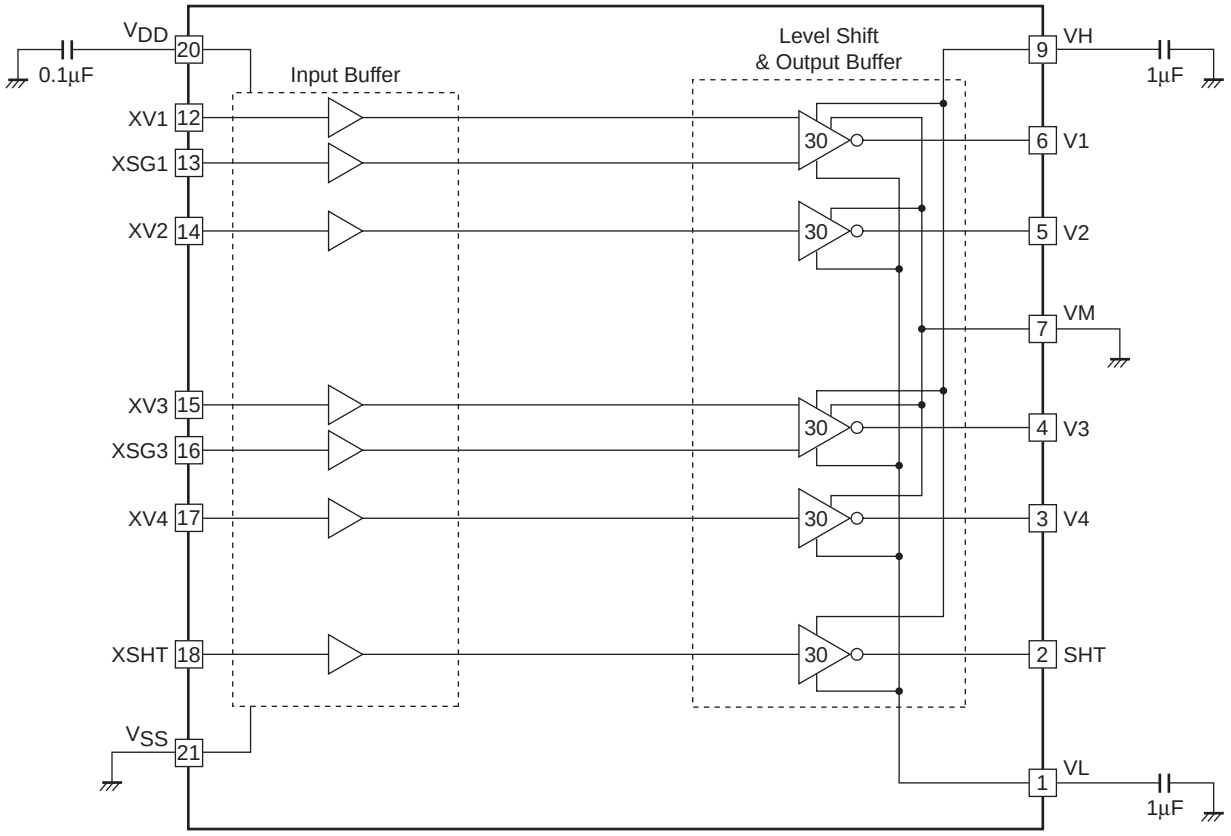
Pin Assignment



Pin Function

Pin No.	Name	Mode
1	V3	Level shift output (ternary VH, VM, VL)
2	V2	Level shift output (binary VM, VL)
3	V1	Level shift output (ternary VH, VM, VL)
4	VM	GND for output
5	NC	
6	VH	Hi power supply (15V system) for output
7	XV1	V1 transfer pulse input
8	XSG1	V1 read pulse input
9	XV2	V2 transfer pulse input
10	XV3	V3 transfer pulse input
11	XSG3	V3 read pulse input
12	XV4	V4 transfer pulse input
13	NC1	
14	XSHT	SHT pulse input
15	V_{DD}	Power supply (3.3V system) for input buffer
16	V_{SS}	GND for input buffer
17	VL	LO power supply (-7.5V system) for output
18	NC	
19	SHT	Level shift output (binary VH, VL)
20	V4	Level shift output (ternary VM, VL)

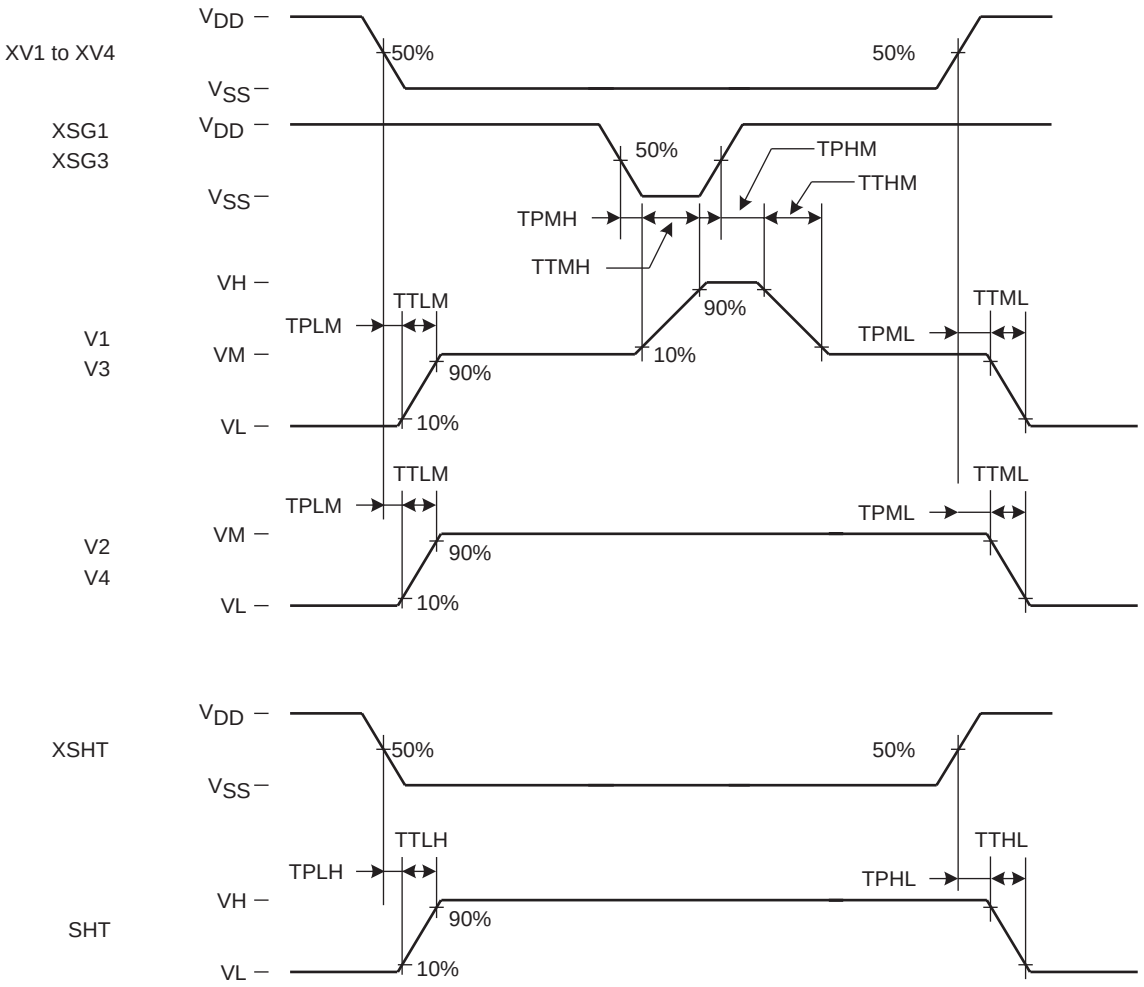
Block Diagram



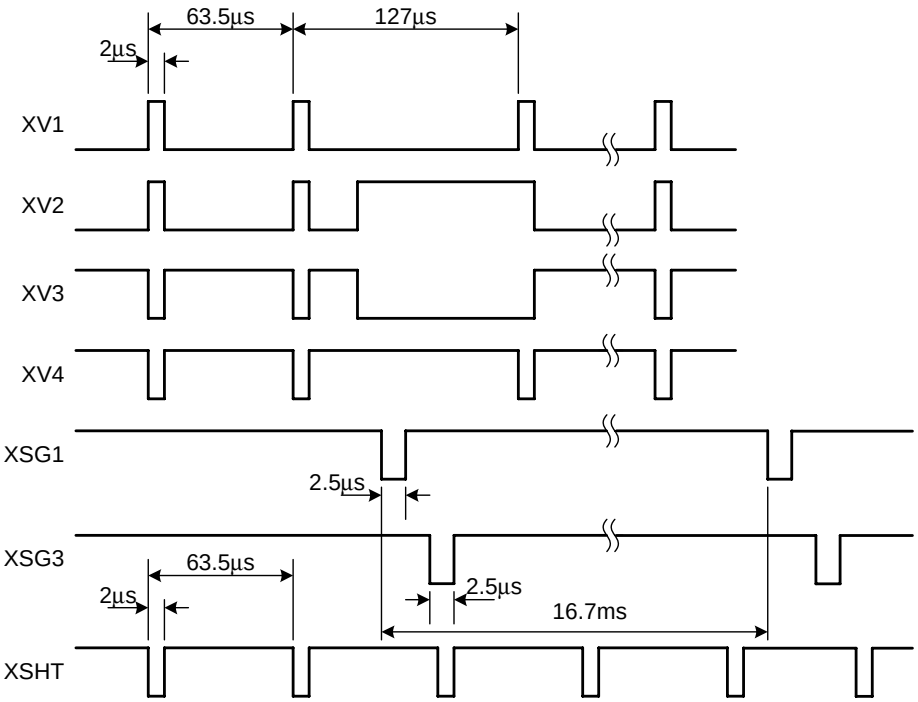
Logical Function Table

Input				Output		
XV1 XV3	XSG1 XSG3	XV2 XV4	XSHT	V1 V3	V2 V4	SHT
L	L	X	X	VH	X	X
L	H	X	X	VM	X	X
H	L	X	X	VL	X	X
H	H	X	X	VL	X	X
X	X	L	X	X	VM	X
X	X	H	X	X	VL	X
X	X	X	L	X	X	VH
X	X	X	H	X	X	VL

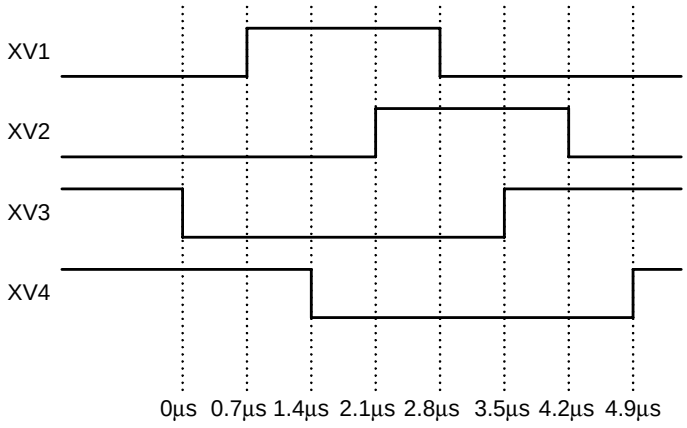
Timing Chart



CCD Equivalent Load Measurement Timing Waveform



Enlarged View of overlapped portion



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