TEXAS INSTRUMENTS

LP3872, LP3875

SNVS227H – FEBRUARY 2003 – REVISED JANUARY 2015

LP387x 1.5-A Fast Ultra-Low-Dropout Linear Regulators

1 Features

- Input Voltage Range: 2.5 V to 7 V
- Ultra Low-Dropout Voltage
- Low Ground Pin Current
- Load Regulation of 0.06%
- 10-nA Quiescent Current in Shutdown Mode
- Ensured Output Current of 1.5-A DC
- Available in DDPAK/TO-263, TO-220, and SOT-223 Packages
- Output Voltage Accuracy ± 1.5%
- $\overline{\text{ERROR}}$ Flag for Output Status
- Sense Option Improves Load Regulation
- Minimum Output Capacitor Requirements
- Overtemperature/Overcurrent Protection
- −40°C to 125°C Junction Temperature Range

2 Applications

- Microprocessor Power Supplies
- GTL, GTL+, BTL, and SSTL Bus Terminators
- Power Supplies for DSPs
- SCSI Terminators
- Post Regulators
- High Efficiency Linear Regulators
- Battery Chargers
- Other Battery-Powered Applications

3 Description

The LP387x series of fast ultra low-dropout linear regulators operate from a 2.5-V to 7-V input supply. Wide range of preset output voltage options are available. These ultra low-dropout linear regulators respond very quickly to step changes in load, which makes them suitable for low-voltage microprocessor applications. The LP3872 and LP3875 are developed on a CMOS process which allows low quiescent current operation independent of output load current. This CMOS process also allows the LP3872 and LP3875 to operate under extremely low dropout conditions.

Dropout Voltage: Ultra low-dropout voltage; typically 38 mV at 150-mA load current and 380 mV at 1.5-A load current.

Ground Pin Current: Typically 6 mA at 1.5-A load current.

Shutdown Mode: Typically 10-nA quiescent current when the $\overline{\text{SD}}$ pin is pulled low.

$\overline{\text{ERROR}}$ Flag: $\overline{\text{ERROR}}$ flag goes low when the output voltage drops 10% below nominal value (LP3872 only).

SENSE: Sense pin improves regulation at remote loads (LP3875 only).

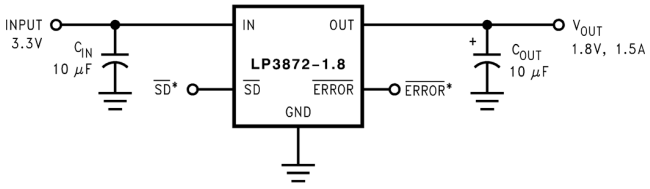
Precision Output Voltage: Multiple output voltage options are available ranging from 1.8 V to 5 V with a specified accuracy of ±1.5% at room temperature, and ±3.0% over all conditions (varying line, load, and temperature).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP3872	SOT-223 (5)	6.50 mm × 3.56 mm
	TO-263 (5)	10.16 mm × 8.42 mm
LP3875	SOT-223 (5)	6.50 mm × 3.56 mm
	TO-263 (5)	10.16 mm × 8.42 mm
	TO-220 (5)	14.986 mm × 10.16 mm

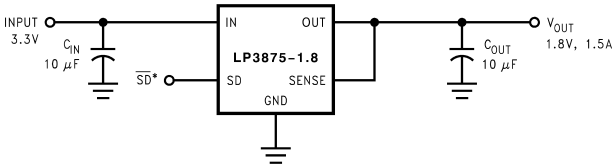
(1) For all available packages, see the orderable addendum at the end of the datasheet.

LP3872 Typical Application Circuit



*$\overline{\text{SD}}$ and $\overline{\text{ERROR}}$ pins must be pulled high through a 10-kΩ pullup resistor. Connect the $\overline{\text{ERROR}}$ pin to ground if this function is not used. See the *Shutdown Mode* and *$\overline{\text{ERROR}}$ Flag Operation* sections.

LP3875 Typical Application Circuit



*$\overline{\text{SD}}$ must be pulled high through a 10-kΩ pullup resistor. See the *Shutdown Mode* section.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (December 2014) to Revision H — **Page**

- Added Input voltage range as first Feature ... 1
- Added "(LP3872 only)" ... 1
- Added "(LP3875 only)" ... 1
- Changed all VIN and VOUT pin names to IN and OUT in drawings and text ... 1
- Changed footnotes to appear under each table ... 4
- Deleted CDM footnote ... 4
- Deleted last sentence of *Short-Circuit Protection* subsection ... 9

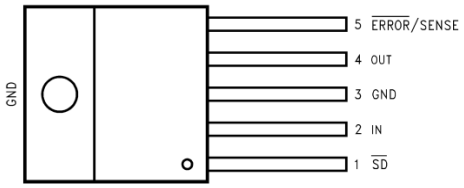
Changes from Revision F (April 2013) to Revision G — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section; update thermal values ... 1

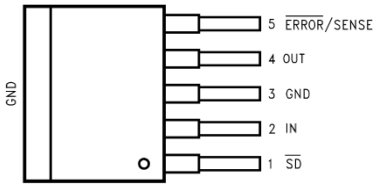
Copyright © 2003–2015, Texas Instruments Incorporated

5 Pin Configuration and Functions

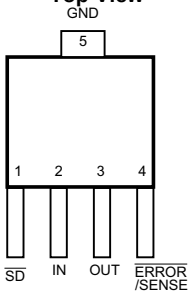
5-Pin TO-220
NDH Package
Top View



5-Pin DDPAK/TO-263
KTT Package
Top View



5-Pin SOT-223
NDC Package
Top View



Pin Functions

PIN					I/O	DESCRIPTION
NAME	NUMBER					
	LP3872		LP3875			
	TO-220 DDPAK/TO-263	SOT-223	TO-220 DDPAK/TO-263	SOT-223		
$\overline{SD}$	1	1	1	1	I	Shutdown
IN	2	2	2	2	I	Input supply
OUT	4	3	4	3	O	Output voltage
$\overline{ERROR}$	5	4	—	—	O	Error flag
SENSE	—	—	5	4	I	Remote voltage sense
GND	3	5	3	5	—	Ground

Copyright © 2003–2015, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.

	MIN	MAX	UNIT
Lead temperature (soldering, 5 sec.)		260	°C
Power dissipation[3]		Internally limited	
IN pin to GND pin voltage	−0.3	7.5	V
Shutdown ($\overline{SD}$) pin to GND pin voltage	−0.3	7.5	V
OUT pin to GND pin voltage[4], [5]	−0.3	6	V
I_{OUT}		Short-circuit protected	
$\overline{ERROR}$ pin to GND pin voltage		V_{IN}	V
SENSE pin to GND pin voltage		V_{OUT}	V
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings*[1][2] may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Internal thermal shutdown circuitry protects the device from permanent damage.
(4) If used in a dual-supply system where the regulator load is returned to a negative supply, the output must be diode-clamped to ground.
(5) The output PMOS structure contains a diode between the IN and OUT pins. This diode is normally reverse biased. This diode will get forward biased if the voltage at the output terminal is forced to be higher than the voltage at the input terminal. This diode can typically withstand 200 mA of DC current and 1 A of peak current.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
V_{IN} supply voltage [1]	2.5	7	V
Shutdown ($\overline{SD}$) voltage	−0.3	7	V
Maximum operating current (DC) I_{OUT}		1.5	A
Junction temperature	–40	125	°C

(1) The minimum operating value for V_{IN} is equal to either [$V_{OUT(NOM)}$ + $V_{DROPOUT}$] or 2.5 V, whichever is greater.

6.4 Thermal Information

THERMAL METRIC[1]		LP3872, LP3875		LP3875	UNIT
		NDC (SOT-223)	KTT (TO-263)	NDH (TO-220)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.2	40.3	32	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.2	43.4	43.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	9.9	23.1	18.6	
ψ_{JT}	Junction-to-top characterization parameter	3.4	11.5	8.8	
ψ_{JB}	Junction-to-board characterization parameter	9.7	22	18	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	1	1.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2003–2015, Texas Instruments Incorporated

6.5 Electrical Characteristics

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, I_L = 10 mA, C_{OUT} = 10 µF, V_{SD} = 2 V.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OUT}	Output voltage tolerance (3)	V_{OUT} +1 V ≤ V_{IN} ≤ 7 V, 10 mA ≤ I_L ≤ 1.5 A	–1.5%	0%	1.5%	
		V_{OUT} +1 V ≤ V_{IN} ≤ 7 V, 10 mA ≤ I_L ≤ 1.5 A, –40°C ≤ T_J ≤ 125°C	–3%		3%	
ΔV_{OL}	Output voltage line regulation (3)	V_{OUT} + 1 V ≤ V_{IN} ≤ 7 V		0.02%		
		V_{OUT} + 1 V ≤ V_{IN} ≤ 7 V, –40°C ≤ T_J ≤ 125°C		0.06%		
ΔV_O/ ΔI_{OUT}	Output voltage load regulation (3)	10 mA ≤ I_L ≤ 1.5 A		0.06%		
		10 mA ≤ I_L ≤ 1.5 A, –40°C ≤ T_J ≤ 125°C		0.12%		
V_{IN} - V_{OUT}	Dropout voltage (4)	I_L = 150 mA		38	50	mV
		I_L = 150 mA, –40°C ≤ T_J ≤ 125°C			60	
		I_L = 1.5 A		380	450	
		I_L = 1.5 A, –40°C ≤ T_J ≤ 125°C			550	
I_{GND}	Ground pin current in normal operation mode	I_L = 150 mA		5	9	mA
		I_L = 150 mA,–40°C ≤ T_J ≤ 125°C			10	
		I_L = 1.5 A		6	14	
		I_L = 1.5 A, –40°C ≤ T_J ≤ 125°C			15	
I_{GND}	Ground pin current in shutdown mode	V_{SD} ≤ 0.3 V		0.01	10	µA
		–40°C ≤ T_J ≤ 85°C			50	
$I_{O(PK)}$	Peak output current	V_{OUT} ≥ $V_{O(NOM)}$ – 4%		1.8		A
SHORT CIRCUIT PROTECTION						
I_{SC}	Short-circuit current			3.2		A
SHUTDOWN INPUT						
V_{SDT}	Shutdown threshold	Output = High		V_{IN}		V
		Output = High, –40°C ≤ T_J ≤ 125°C	2			
		Output = Low		0		
		Output = Low, –40°C ≤ T_J ≤ 125°C			0.3	
T_{dOFF}	Turnoff delay	I_L = 1.5 A		20		µs
T_{dON}	Turnon delay	I_L = 1.5 A		25		µs
I_{SD}	$\overline{SD}$ input current	V_{SD} = V_{IN}		1		nA
$\overline{ERROR}$ FLAG						
V_T	Threshold	See(5)		10%		
		See(5), –40°C ≤ T_J ≤ 125°C	5%		16%	
V_{TH}	Threshold hysteresis	See(5)		5%		
		See(5), –40°C ≤ T_J ≤ 125°C	2%		8%	
$V_{EF(Sat)}$	$\overline{ERROR}$ flag saturation	I_{sink} = 100 µA		0.02		V
		I_{sink} = 100 µA, –40°C ≤ T_J ≤ 125°C			0.1	
Td	Flag reset delay			1		µs
I_{lk}	$\overline{ERROR}$ flag pin leakage current			1		nA
I_{max}	$\overline{ERROR}$ flag pin sink current	V_{Error} = 0.5 V		1		mA

(1) Limits are specified by testing, design, or statistical correlation.
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current. The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.
(4) Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. Dropout voltage specification applies only to output voltages of 2.5 V and above. For output voltages below 2.5 V, the dropout voltage is nothing but the input to output differential, because the minimum input voltage is 2.5 V.
(5) $\overline{ERROR}$ Flag threshold and hysteresis are specified as percentage of regulated output voltage. See *$\overline{ERROR}$ Flag Operation*.

Copyright © 2003–2015, Texas Instruments Incorporated

Electrical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, I_L = 10 mA, C_{OUT} = 10 µF, V_{SD} = 2 V.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
AC PARAMETERS						
PSRR	Ripple rejection	V_{IN} = V_{OUT} + 1 V, C_{OUT} = 10 µF V_{OUT} = 3.3 V, f = 120 Hz		73		dB
		V_{IN} = V_{OUT} + 0.5 V, C_{OUT} = 10 µF V_{OUT} = 3.3 V, f = 120 Hz		57		
$\rho_{n(l/f)}$	Output noise density	f = 120 Hz		0.8		µV
e_n	Output noise voltage	BW = 10 Hz – 100 kHz, V_{OUT} = 2.5 V		150		µV (rms)
		BW = 300 Hz – 300 kH, V_{OUT} = 2.5 V		100		

6.6 Typical Characteristics

Unless otherwise specified: T_J = 25°C, C_{OUT} = 10 µF, C_{IN} = 10 µF, $\overline{SD}$ pin is tied to V_{IN}, V_{OUT} = 2.5 V, V_{IN} = $V_{O(NOM)}$ + 1 V, I_L = 10 mA

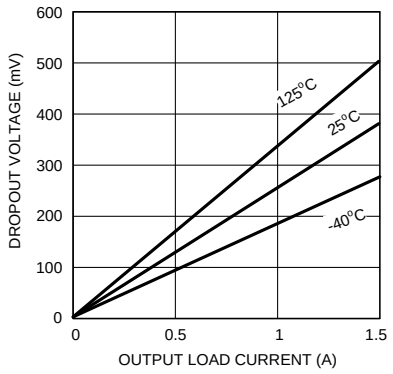


Figure 1. Dropout Voltage vs Output Load Current

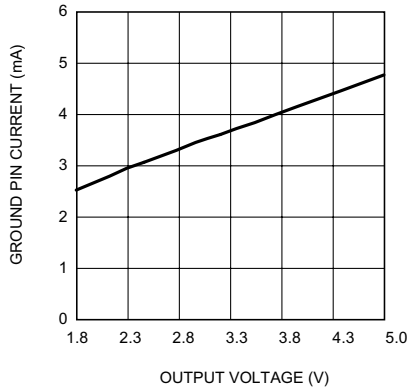


Figure 2. Ground Current vs Output Voltage
I_L = 1.5 A

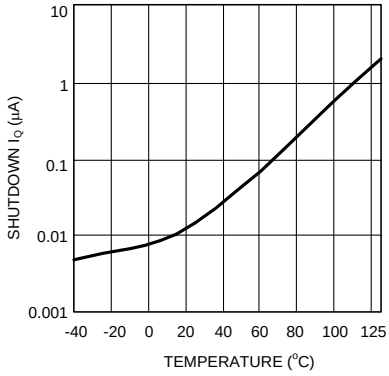


Figure 3. Shutdown I_Q vs Junction Temperature

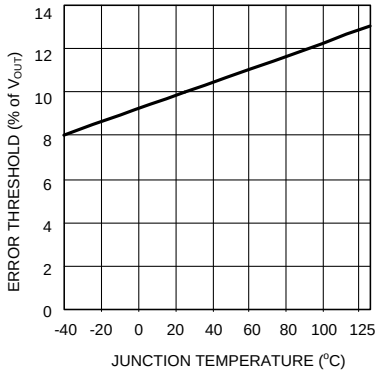


Figure 4. Errorflag Threshold vs Junction Temperature

Copyright © 2003–2015, Texas Instruments Incorporated

Typical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, C_{OUT} = 10 µF, C_{IN} = 10 µF, $\overline{SD}$ pin is tied to V_{IN}, V_{OUT} = 2.5 V, V_{IN} = $V_{O(NOM)}$ + 1 V, I_L = 10 mA

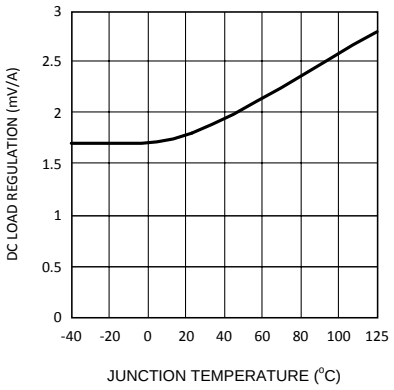


Figure 5. DC Load Reg. vs Junction Temperature

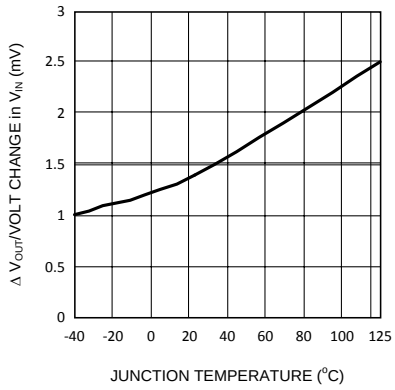


Figure 6. DC Line Regulation vs Temperature

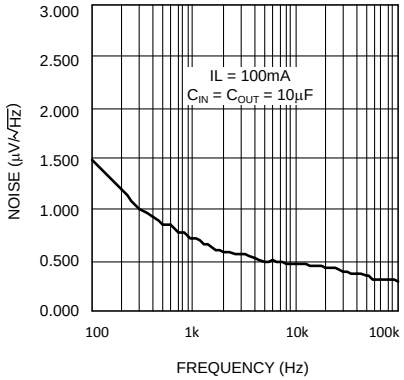


Figure 7. Noise vs Frequency

Copyright © 2003–2015, Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The LP387x linear regulators are designed to provide an ultra-low-dropout voltage with excellent transient response and load/line regulation. For battery-powered always-on type applications, the very low quiescent current of LP387x in shutdown mode helps reduce battery drain. For applications where load is not placed close to the regulator, LP3875 incorporates a voltage sense circuit to improve voltage regulation at the point of load. $\overline{\text{ERROR}}$ output pin of LP3872 can be used in the system to flag a low-voltage condition.

7.2 Functional Block Diagram

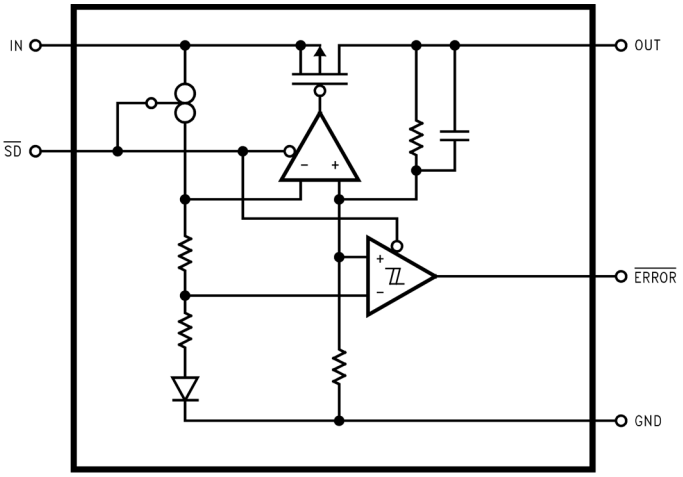


Figure 8. LP3872

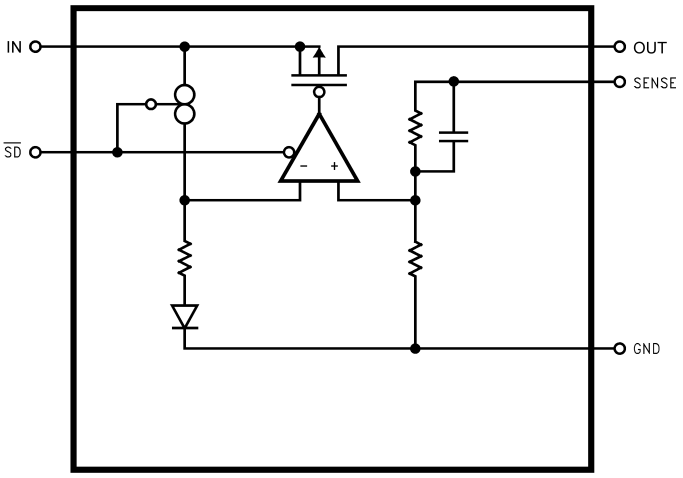


Figure 9. LP3875

7.3 Feature Description

7.3.1 Shutdown ($\overline{\text{SD}}$)

The LM387x devices have a shutdown feature that turns the device off and reduces the quiescent current to 10 nA, typical.

Copyright © 2003–2015, Texas Instruments Incorporated

Feature Description (continued)

7.3.2 Load Voltage Sense

In applications where the regulator output is not very close to the load, LP3875 can provide better remote load regulation using the SENSE pin. Figure 10 depicts the advantage of the SENSE option. LP3872 regulates the voltage at the OUT pin. Hence, the voltage at the remote load will be the regulator output voltage minus the drop across the trace resistance. For example, in the case of a 3.3-V output, if the trace resistance is 100 mΩ, the voltage at the remote load will be 3.15 V with 1.5 A of load current, I_{LOAD}. The LP3875 regulates the voltage at the sense pin. Connecting the sense pin to the remote load will provide regulation at the remote load, as shown in Figure 10. If the sense option pin is not required, the SENSE pin must be connected to the OUT pin.

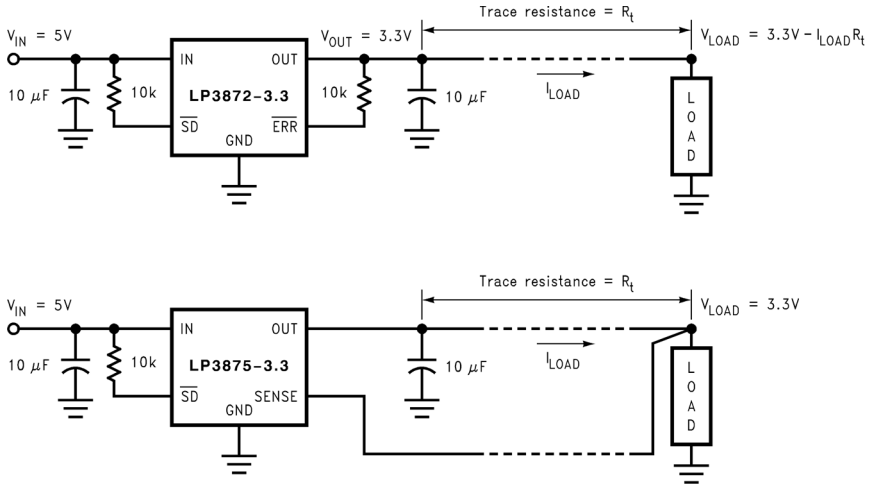


Figure 10. Improving Remote Load Regulation Using LP3875

7.3.3 Short-Circuit Protection

The LP3872 and LP3875 devices are short-circuit protected and in the event of a peak overcurrent condition, the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency.

7.3.4 Low Dropout Voltage

The LP387x devices feature an ultra-low-dropout voltage, typically 38 mV at 150-mA load current and 380 mV at 1.5-A load current.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

A CMOS Logic low level signal at the shutdown ($\overline{SD}$) pin will turn off the regulator. The $\overline{SD}$ pin must be actively terminated through a 10-kΩ pullup resistor for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pullup resistor is not required. This pin must be tied to V_{IN} if not used.

7.4.2 Active Mode

When voltage at $\overline{SD}$ pin of the LP387x device is at logic high level, the device is in normal mode of operation.

7.4.3 $\overline{ERROR}$ Flag Operation

The LP3872 and LP3875 produces a logic low signal at the $\overline{ERROR}$ Flag pin when the output drops out of regulation due to low input voltage, current limiting, or thermal limiting. This flag has a built-in hysteresis. The timing diagram in Figure 11 shows the relationship between the $\overline{ERROR}$ flag and the output voltage. In this example, the input voltage is changed to demonstrate the functionality of the $\overline{ERROR}$ Flag.

Copyright © 2003–2015, Texas Instruments Incorporated

Device Functional Modes (continued)

The internal $\overline{\text{ERROR}}$ flag comparator has an open-drain output stage. Hence, the $\overline{\text{ERROR}}$ pin should be pulled high through a pullup resistor. Although the $\overline{\text{ERROR}}$ flag pin can sink current of 1 mA, this current is energy drain from the input supply. Hence, the value of the pullup resistor should be in the range of 10 kΩ to 1 MΩ. *The $\overline{\text{ERROR}}$ pin must be connected to ground if this function is not used.* It should also be noted that when the $\overline{\text{SD}}$ pin is pulled low, the $\overline{\text{ERROR}}$ pin is forced to be invalid for reasons of saving power in shutdown mode.

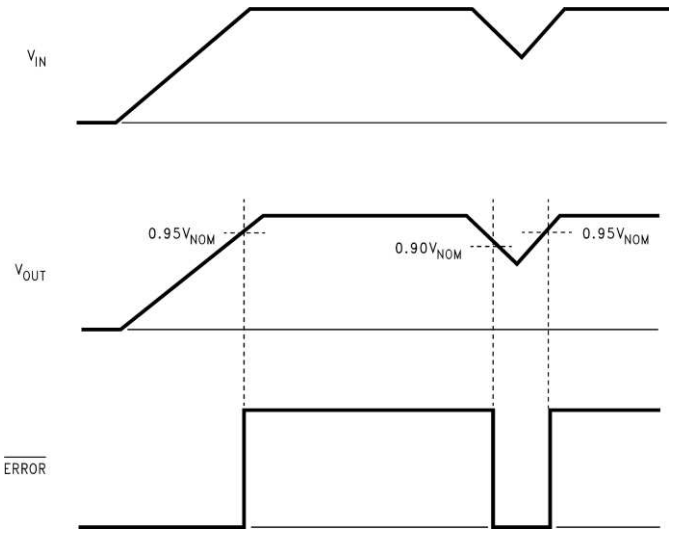


Figure 11. $\overline{\text{ERROR}}$ Flag Operation

Copyright © 2003–2015, Texas Instruments Incorporated

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP387x devices are linear regulators designed to provide high load current of up to 1.5 A, low dropout voltage, and low quiescent current in shutdown mode. Figure 12 and Figure 13 show the typical application circuit for these devices.

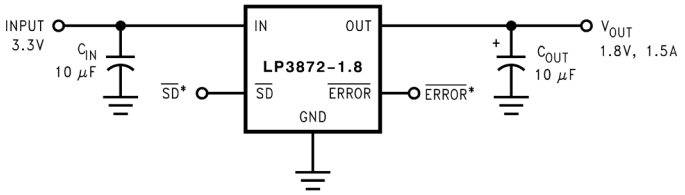
8.1.1 Dropout Voltage

The dropout voltage of a regulator is defined as the minimum input-to-output differential required to stay within 2% of the nominal output voltage. For CMOS LDOs, the dropout voltage is the product of the load current and the $R_{ds(on)}$ of the internal MOSFET.

8.1.2 Reverse Current Path

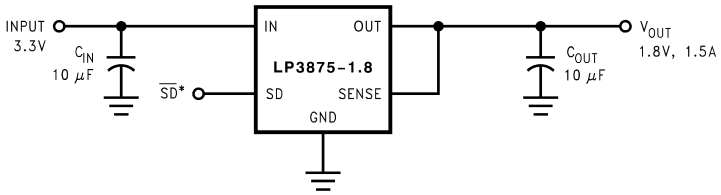
The internal MOSFET in LP3872 and LP3875 has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 200-mA continuous and 1-A peak.

8.2 Typical Application



*$\overline{SD}$ and $\overline{ERROR}$ pins must be pulled high through a 10-kΩ pullup resistor. Connect the $\overline{ERROR}$ pin to ground if this function is not used. See the *Shutdown Mode* and *$\overline{ERROR}$ Flag Operation* sections.

Figure 12. LP3872 Typical Application Circuit



*$\overline{SD}$ must be pulled high through a 10-kΩ pullup resistor. See the *Shutdown Mode* section.

Figure 13. LP3875 Typical Application Circuit

Typical Application (continued)

8.2.1 Design Requirements

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5 V to 7 V
Output voltage	1.8 V
Output current	1.5 A
Output capacitor	10 µF
Input capacitor	10 µF
Output capacitor ESR range	100 mΩ to 4 Ω

8.2.2 Detailed Design Procedure

8.2.2.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation depends on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation for the device in a given package can be calculated using Equation 1:

$$P_{D\text{-}MAX} = ((T_{J\text{-}MAX} - T_A) / R_{\theta JA}) \quad (1)$$

The actual power being dissipated in the device can be represented by Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Equation 1 and Equation 2 establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may have to be derated. $T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by Equation 3:

$$T_{A\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} - (R_{\theta JA} \times P_{D\text{-}MAX})) \quad (3)$$

Alternately, if $T_{A\text{-}MAX}$ can not be derated, the P_D value must be reduced. This can be accomplished by reducing V_{IN} in the $V_{IN} - V_{OUT}$ term as long as the minimum V_{IN} is met, or by reducing the I_{OUT} term, or by some combination of the two.

8.2.2.2 External Capacitors

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

- Input Capacitor: An input capacitor of at least 10 µF is required. Ceramic, tantalum, or Electrolytic capacitors may be used, and capacitance may be increased without limit.
- Output Capacitor: An output capacitor is required for loop stability. It must be located less than 1 cm from the device and connected directly to the output and ground pins using traces which have no other currents flowing through them (see *Layout* section).

The minimum value of output capacitance that can be used for stable full-load operation is 10 µF, but it may be increased without limit. The output capacitor must have an equivalent series resistance (ESR) value as shown in Figure 14. Tantalum capacitors are recommended for the output capacitor.

Copyright © 2003–2015, Texas Instruments Incorporated

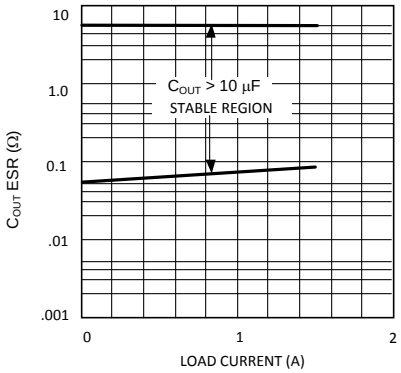


Figure 14. ESR Curve

8.2.2.3 Selecting a Capacitor

Capacitance tolerance and variation with temperature must be considered when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range. In general, a good tantalum capacitor will show very little capacitance variation with temperature, but a ceramic may not be as good (depending on dielectric type). Aluminum electrolytics also typically have large temperature variation of capacitance value.

Equally important to consider is how ESR of a capacitor changes with temperature: this is not an issue with ceramics, as their ESR is extremely low. However, it is very important in tantalum and aluminum electrolytic capacitors. Both show increasing ESR at colder temperatures, but the increase in aluminum electrolytic capacitors is so severe they may not be feasible for some applications (see *Capacitor Characteristics*).

8.2.2.4 Capacitor Characteristics

8.2.2.4.1 Ceramic

For values of capacitance in the 10-µF to 100-µF range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

X7R and X5R dielectric ceramic capacitors are strongly recommended if ceramics are used, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

8.2.2.4.2 Tantalum

Solid tantalum capacitors are recommended for use on the output because their typical ESR is very close to the ideal value required for loop compensation. They also work well as input capacitors if selected to meet the ESR requirements previously listed.

Tantalums also have good temperature stability: a good quality tantalum will typically show a capacitance value that varies less than 10-15% across the full temperature range of −40°C to 125°C. ESR will vary only about 2X going from the high to low temperature limits.

The increasing ESR at lower temperatures can cause oscillations when marginal quality capacitors are used (if the ESR of the capacitor is near the upper limit of the stability range at room temperature).

Copyright © 2003–2015, Texas Instruments Incorporated

8.2.2.4.3 Aluminum

This capacitor type offers the most capacitance for the money. The disadvantages are that they are larger in physical size, not widely available in surface mount, and have poor AC performance (especially at higher frequencies) due to higher ESR and equivalent series inductance (ESL).

Compared by size, the ESR of an aluminum electrolytic is higher than either tantalum or ceramic, and it also varies greatly with temperature. A typical aluminum electrolytic can exhibit an ESR increase of as much as 50X when going from 25°C down to −40°C.

It should also be noted that many aluminum electrolytics only specify impedance at a frequency of 120 Hz, which indicates they have poor high-frequency performance. Only aluminum electrolytics that have an impedance specified at a higher frequency (from 20 kHz to 100 kHz) should be used for the LP387x. Derating must be applied to the manufacturer's ESR specification, because it is typically only valid at room temperature.

Any applications using aluminum electrolytics should be thoroughly tested at the lowest ambient operating temperature where ESR is maximum.

8.2.2.5 Turnon Characteristics for Output Voltages Programmed to 2 V or Less

As V_{IN} increases during start-up, the regulator output will track the input until Vin reaches the minimum operating voltage (typically about 2.2 V). For output voltages programmed to 2 V or less, the regulator output may momentarily exceed its programmed output voltage during start-up. Outputs programmed to voltages above 2 V are not affected by this behavior.

8.2.2.6 RFI/EMI Susceptibility

Radio frequency interference (RFI) and electromagnetic interference (EMI) can degrade the performance of any IC because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the IC regulator.

If RFI/EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the IC.

If a load is connected to the IC output which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the IC output. Because the bandwidth of the regulator loop is less than 100 kHz, the control circuitry cannot respond to load changes above that frequency. This means the effective output impedance of the IC at frequencies above 100 kHz is determined only by the output capacitors.

In applications where the load is switching at high speed, the output of the IC may need RF isolation from the load. It is recommended that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load.

PCB layout is also critical in high noise environments, because RFI/EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from "clean" circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/EMI can cause ground bounce across the ground plane.

In multilayer PCB applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

8.2.2.7 Output Noise

Noise is specified in two ways:

- Spot Noise (or Output Noise Density): the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1-Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.
- Total Output Noise (or Broad-Band Noise): the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

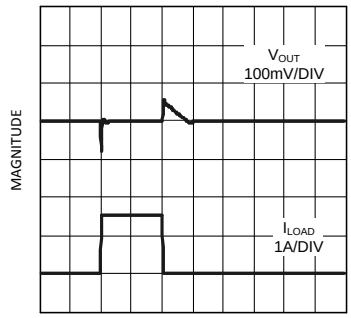
Attention should be paid to the units of measurement. Spot noise is measured in units μV/√Hz or nV/√Hz and total output noise is measured in μV(rms).

Copyright © 2003–2015, Texas Instruments Incorporated

The primary source of noise in low-dropout regulators is the internal reference. In CMOS regulators, noise has a low frequency component and a high frequency component, which depend strongly on the silicon area and quiescent current. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current). Using an optimized trade-off of ground pin current and die size, LP3872 and LP3875 achieves low noise performance and low quiescent current operation.

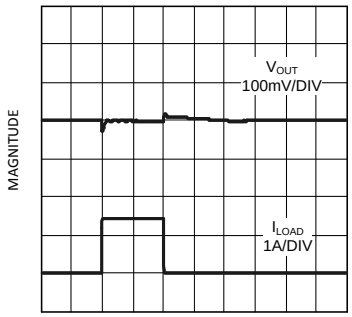
The total output noise specification for LP3872 and LP3875 is presented in *Electrical Characteristics*. The Output noise density at different frequencies is represented by a curve under typical performance characteristics.

8.2.3 Application Curves



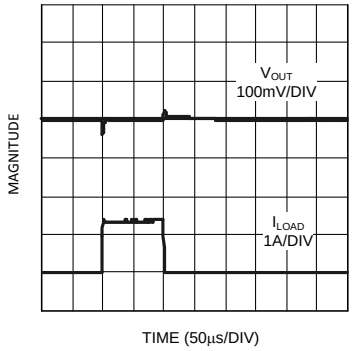
C_{IN} = C_{OUT} = 10 µF, OSCON

Figure 15. Load Transient Response



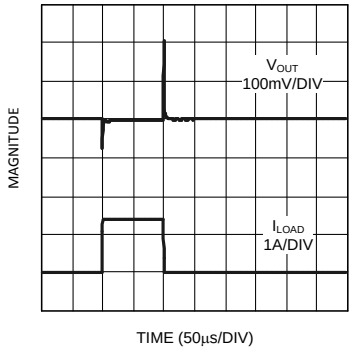
C_{IN} = C_{OUT} = 100 µF, OSCON

Figure 16. Load Transient Response



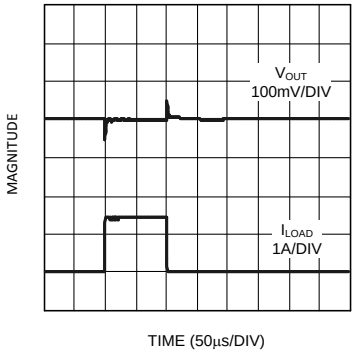
C_{IN} = C_{OUT} = 100 µF, POSCAP

Figure 17. Load Transient Response



C_{IN} = C_{OUT} = 10 µF, Tantalum

Figure 18. Load Transient Response



C_{IN} = C_{OUT} = 100 µF, Tantalum

Figure 19. Load Transient Response

9 Power Supply Recommendations

The LP397x devices are designed to operate from an input supply voltage range of 2.5 V to 7 V. The input supply should be well regulated and free of spurious noise. To ensure that the LP387x output voltage is well regulated, the input supply should be at least V_{OUT} + 0.5 V, or 2.5 V, whichever is higher. A minimum capacitor value of 10 µF is required to be within 1 cm of the IN pin.

10 Layout

10.1 Layout Guidelines

Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the input, output, and ground pins of the regulator using traces which do not have other currents flowing in them (Kelvin connect).

The best way to do this is to lay out C_{IN} and C_{OUT} near the device with short traces to the IN, OUT, and GND pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a single-point ground.

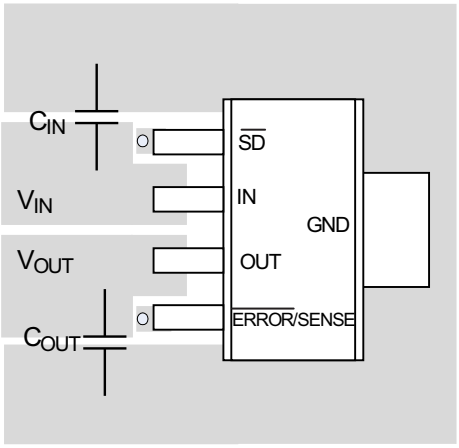
It should be noted that stability problems have been seen in applications where vias to an internal ground plane were used at the ground points of the IC and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single-point ground technique for the regulator and it's capacitors fixed the problem.

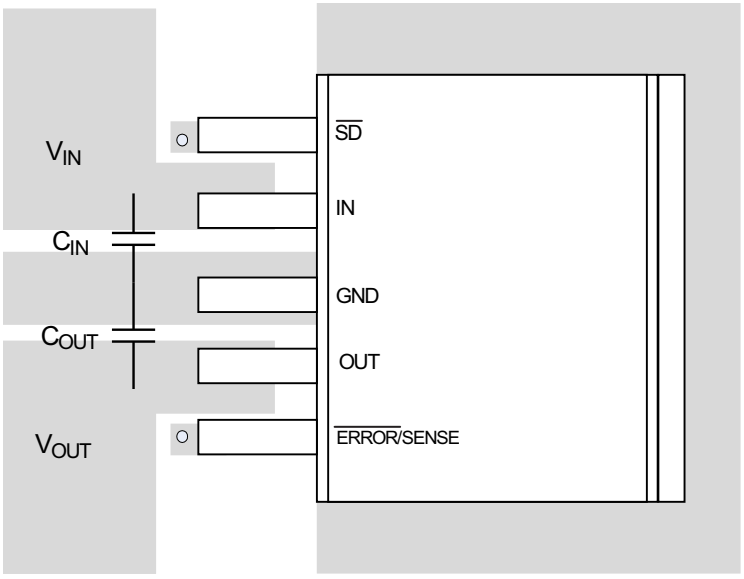
Because high current flows through the traces going into V_{IN} and coming from V_{OUT}, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

Copyright © 2003–2015, Texas Instruments Incorporated

10.2 Layout Examples

Layout Example for SOT-223 Package





Layout Example for TO-263 Package

11 Device and Documentation Support

11.1 Related Links

Table 2 below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LP3872	Click here	Click here	Click here	Click here	Click here
LP3875	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2003–2015, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3872EMP-1.8/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LHAB	Samples
LP3872EMP-2.5/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LHBB	Samples
LP3872EMP-3.3/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LHCB	Samples
LP3872EMP-5.0/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LHDB	Samples
LP3872EMPX-2.5/NOPB	ACTIVE	SOT-223	NDC	5	2000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LHBB	Samples
LP3872EMPX-3.3/NOPB	ACTIVE	SOT-223	NDC	5	2000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LHCB	Samples
LP3872ES-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	LP3872ES -1.8	Samples
LP3872ES-2.5	NRND	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LP3872ES -2.5	
LP3872ES-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	LP3872ES -2.5	Samples
LP3872ES-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	LP3872ES -3.3	Samples
LP3872ES-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	LP3872ES -5.0	Samples
LP3872ESX-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	LP3872ES -1.8	Samples
LP3872ESX-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	LP3872ES -2.5	Samples
LP3872ESX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	LP3872ES -3.3	Samples
LP3872ESX-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	LP3872ES -5.0	Samples
LP3875EMP-1.8/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LHLB	Samples
LP3875EMP-2.5/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LHNB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3875EMP-3.3/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LHPB	Samples
LP3875EMP-5.0/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LHRB	Samples
LP3875ES-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	LP3875ES -1.8	Samples
LP3875ES-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	LP3875ES -2.5	Samples
LP3875ES-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	LP3875ES -3.3	Samples
LP3875ESX-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	LP3875ES -1.8	Samples
LP3875ESX-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	LP3875ES -2.5	Samples
LP3875ESX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	LP3875ES -3.3	Samples
LP3875ET-3.3/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 125	LP3875ET -3.3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

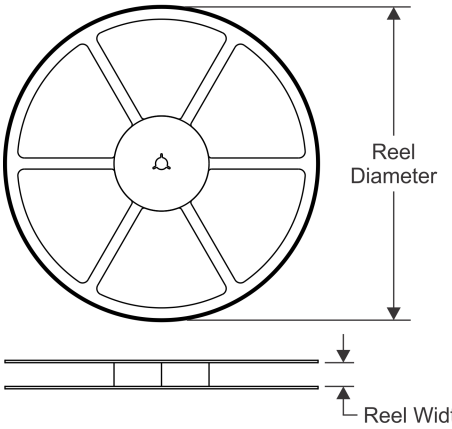
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

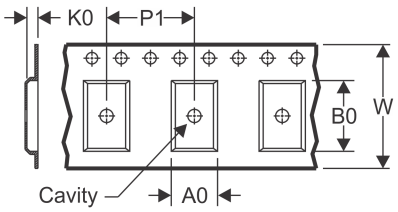
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

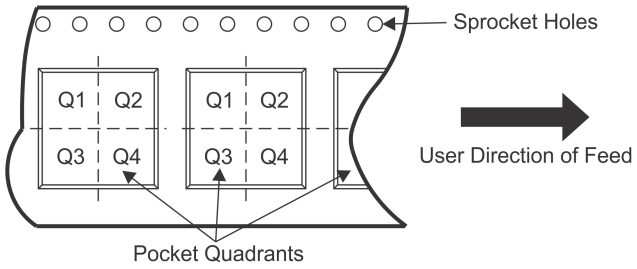


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

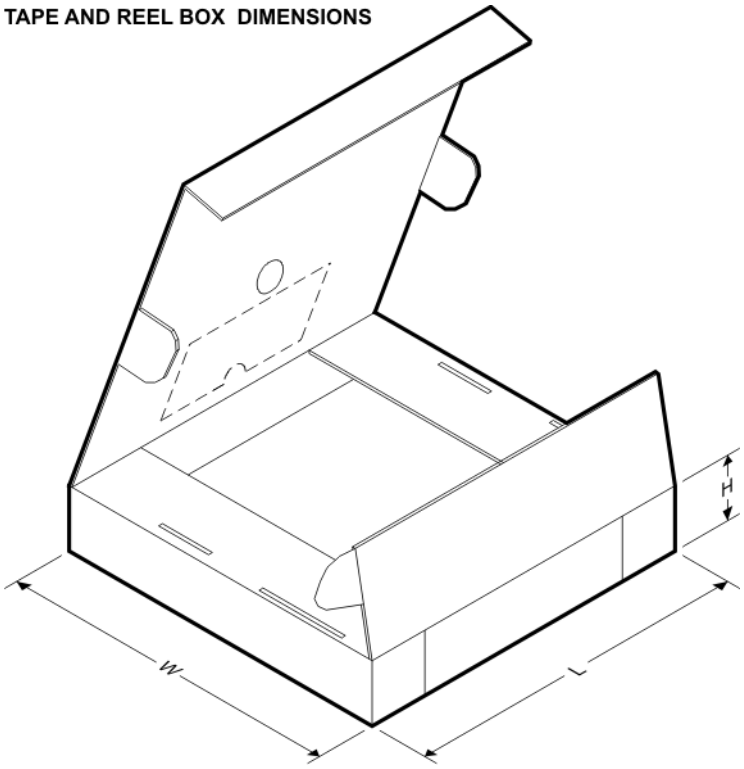


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3872EMP-1.8/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3872EMP-2.5/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3872EMP-3.3/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3872EMP-5.0/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3872EMPX-2.5/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3872EMPX-3.3/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3872ESX-1.8/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3872ESX-2.5/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3872ESX-3.3/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3872ESX-5.0/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3875EMP-1.8/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3875EMP-2.5/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3875EMP-3.3/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3875EMP-5.0/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3875ESX-1.8/NOPB	DDPAK/	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	TO-263											
LP3875ESX-2.5/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3875ESX-3.3/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

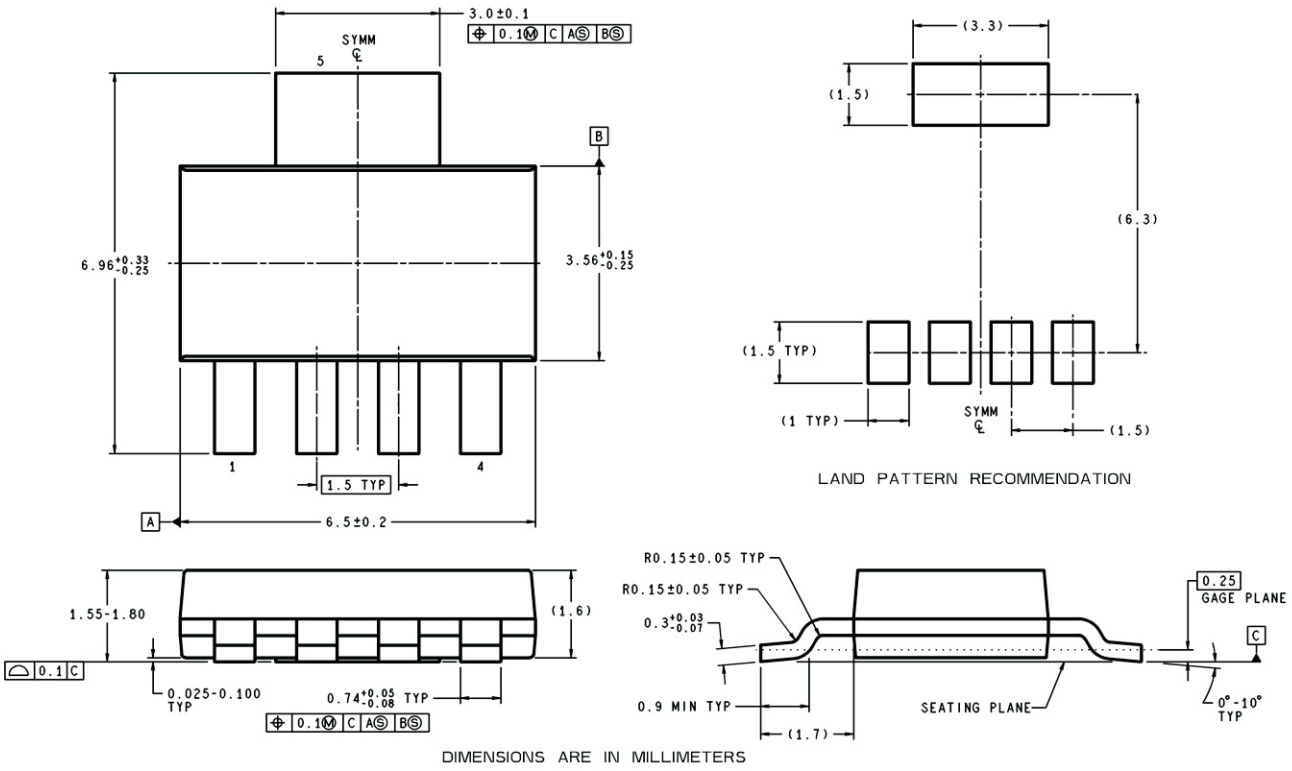


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3872EMP-1.8/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3872EMP-2.5/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3872EMP-3.3/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3872EMP-5.0/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3872EMPX-2.5/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP3872EMPX-3.3/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP3872ESX-1.8/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3872ESX-2.5/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3872ESX-3.3/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3872ESX-5.0/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3875EMP-1.8/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3875EMP-2.5/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0

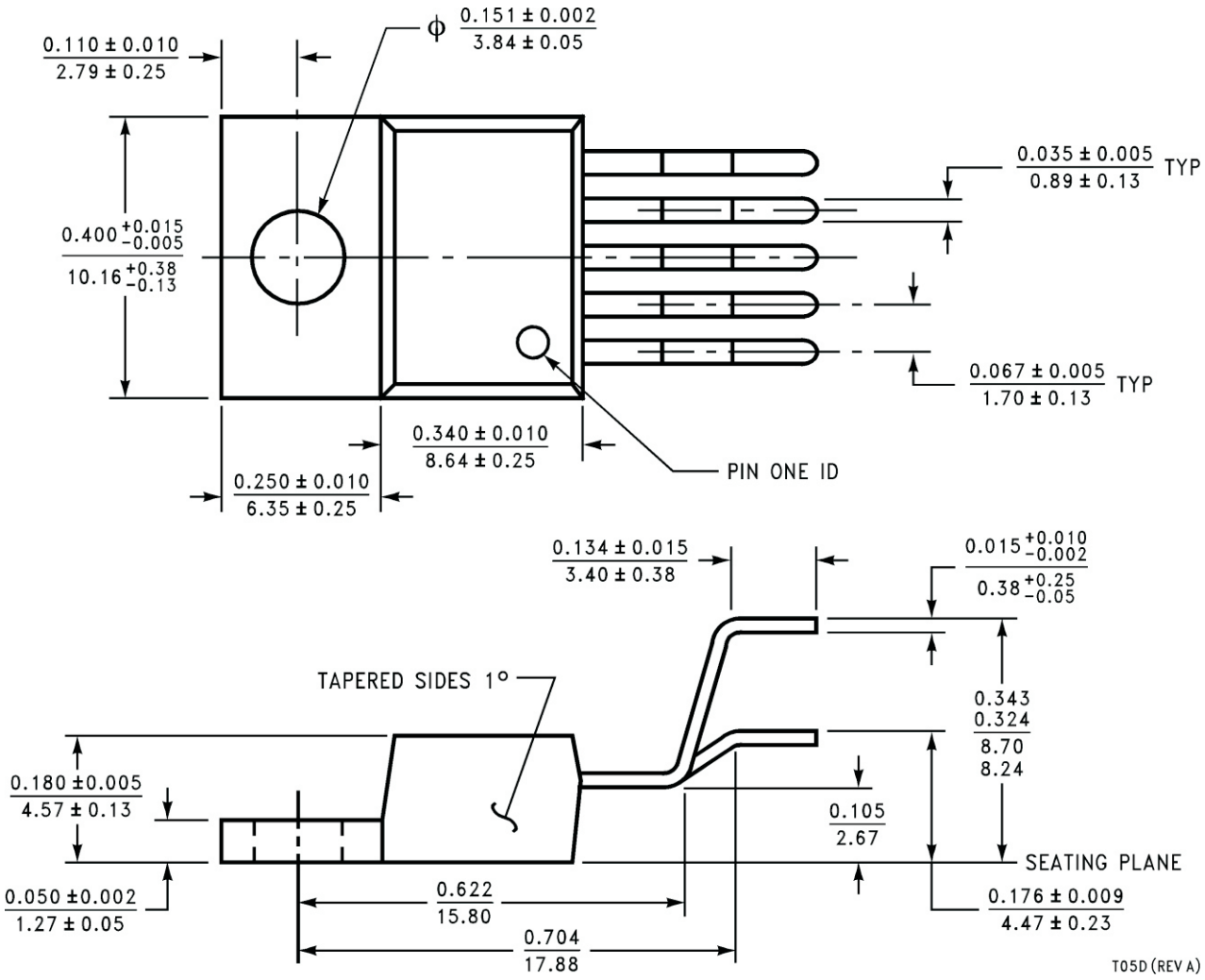
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3875EMP-3.3/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3875EMP-5.0/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3875ESX-1.8/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3875ESX-2.5/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3875ESX-3.3/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0

NDC0005A

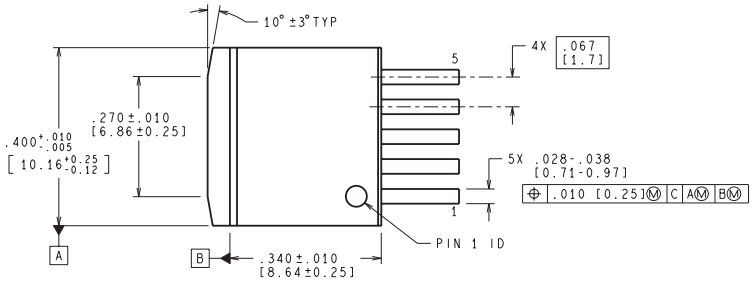


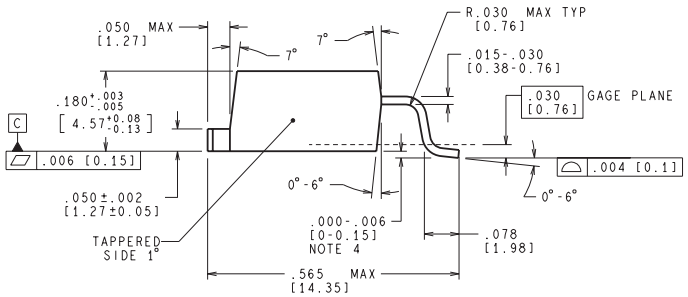
MP05A (Rev A)

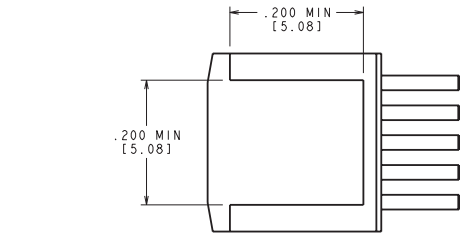
NDH0005D


0.110 ± 0.010
2.79 ± 0.25
ϕ 0.151 ± 0.002
3.84 ± 0.05
0.035 ± 0.005
0.89 ± 0.13
TYP
0.400 +0.015 −0.005
10.16 +0.38 −0.13
0.067 ± 0.005
1.70 ± 0.13
TYP
0.340 ± 0.010
8.64 ± 0.25
PIN ONE ID
0.250 ± 0.010
6.35 ± 0.25
0.134 ± 0.015
3.40 ± 0.38
0.015 +0.010 −0.002
0.38 +0.25 −0.05
TAPERED SIDES 1°
0.343
0.324
8.70
8.24
0.180 ±0.005
4.57 ± 0.13
0.105
2.67
SEATING PLANE
0.050 ±0.002
1.27 ± 0.05
0.622
15.80
0.176 ± 0.009
4.47 ± 0.23
0.704
17.88
T05D (REV A)

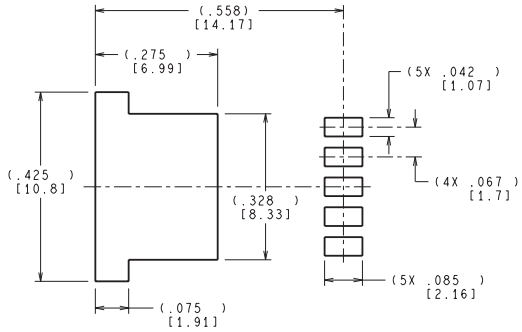
KTT0005B







BOTTOM SIDE OF PACKAGE



LAND PATTERN RECOMMENDATION

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

TS5B (Rev D)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated