EVALUATION KIT AVAILABLE

MAX17598/MAX17599

Low IQ, Wide-Input Range, Active Clamp Current-Mode PWM Controllers

General Description

The MAX17598/MAX17599 low I_Q, active clamp current-mode PWM controllers contain all the control circuitry required for the design of wide-input isolated/non-isolated forward-converter industrial power supplies. The MAX17598 is well-suited for universal input (rectified 85V AC to 265V AC) or telecom (36V DC to 72V DC) power supplies. The MAX17599 is optimized for low-voltage industrial supplies (4.5V DC to 36V DC).

The devices include an AUX driver that drives an auxiliary MOSFET (clamp switch) that helps implement the active-clamp transformer reset topology for forward converters. Such a reset topology has several advantages including reduced voltage stress on the switches, transformer size reduction due to larger allowable flux swing, and improved efficiency due to elimination of dissipative snubber circuitry. Programmable dead time between the AUX and main driver allows for zero voltage switching (ZVS).

The switching frequency is programmable from 100kHz to 1MHz for the devices with an accuracy of ±8% using an external resistor. This allows optimization of the magnetic and filter components, resulting in compact, cost-effective isolated/nonisolated power supplies. For EMI-sensitive applications, the ICs incorporate a programmable frequency-dithering scheme, enabling low-EMI spread-spectrum operation.

An input undervoltage lockout (EN/UVLO) is provided for programming input-supply start voltage, and to ensure proper operation during brownout conditions. EN/UVLO input is also used to turn on/off the ICs. Input overvoltage (OVI) protection scheme is provided to make sure that the regulator shuts down when input supply exceeds its maximum allowed value.

To control inrush current, the devices incorporate an SS pin to set the soft-start time for the regulators. Power dissipation under fault conditions is minimized by hiccup overcurrent protection (hiccup mode). Soft-stop feature provides safe discharging of the clamp capacitor when the device is turned off, and allows the controller to restart in a well-controlled manner. Additionally, negative current limit is provided in the current-sense circuitry, helping limit clamp switch current under dynamic operating conditions.

SYNC feature is provided to synchronize multiple converters to a common external clock in noise-sensitive applications. Overtemperature fault triggers thermal shutdown for reliable protection of the device. The ICs are available in a 16-pin, TQFN package with 0.5 mm lead spacing.

Benefits and Features

- **Active Clamp, Peak Current-Mode Forward PWM Controller**
- **20µA Startup Current in UVLO**
- **4.5V to 36V Input-Supply Operating Range (MAX17599)**
- **Programmable Input Undervoltage Lockout**
- **Programmable Input Overvoltage Protection**
- **Programmable 100kHz to 1MHz Switching Frequency**
- **Switching Frequency Synchronization**
- **Programmable Frequency Dithering for Low EMI Spread-Spectrum Operation**
- **Programmable Dead Time**
- **Adjustable Soft-Start**
- **Programmable Slope Compensation**
- **Fast Cycle-by-Cycle Peak-Current-Limit**
- **70ns Internal Leading-Edge Current-Sense Blanking**
- **Hiccup Mode Output Short-Circuit Protection**
- **Soft-Stop for Well-Controlled Clamp Capacitor Discharge**
- **Negative Clamp-Switch Current Limit**
- **3mm x 3mm, Lead-Free 16-Pin TQFN**
- **-40°C to +125°C Operating Temperature Range**

Applications

Telecom and Datacom Power Supplies

Isolated Battery Chargers

Servers and Embedded Computing

Industrial Power Supplies

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX17598.related.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-6179; Rev 2; 4/14

ABSOLUTE MAXIMUM RATINGS

V_{IN} (MAX17599 only) ..... -0.3V to +40V
V_{DRV} to SGND
(MAX17598 Only) ..... -0.3V to +16V
(MAX17599 Only) ..... -0.3V to +6V
EN/UVLO to SGND ..... -0.3V to (V_{IN} + 0.3V)
NDRV, AUXDRV to PGND ..... -0.3V to (V_{DRV} + 0.3V)
OVI, RT, DITHER, COMP, SS, FB,
SLOPE, DT to SGND ..... -0.3V to +6V
CS to SGND ..... -0.8V to +6V
PGND to SGND ..... -0.3V to +0.3V

Maximum Input/Output Current (Continuous)
V_{IN}, V_{DRV} 100mA
NDRV (pulsed for less than 100ns) ..... +0.9A/-1.5A
AUXDRV (pulsed for less than 100ns) ..... +0.3A/-0.7A
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 20.8mW/°C above 70°C) 1666mW
Operating Temperature Range ..... -40°C to +125°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 7°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 48°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V (for MAX17598, bring V_{IN} up to 21V for startup), V_{CS} = V_{DITHER} = V_{FB} = V_{OVI} = V_{SGND} = V_{PGND} = 0V, $V_{EN/UVLO}$ = +2V, AUXDRV = NDRV = SS = COMP = SLOPE = unconnected, R_{RT} = 25kΩ, R_{DT} = 10kΩ, C_{VIN} = 1µF, C_{VDRV} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})							
V_{IN} Voltage Range	V_{IN}	MAX17598		8		29	V
		MAX17599		4.5		36	
V_{IN} Bootstrap UVLO Wakeup	V_{IN-UVR}	IN rising	MAX17598	18.5	20	21.5	V
			MAX17599	3.8	4.1	4.4	
V_{IN} Bootstrap UVLO Shutdown Level	V_{IN-UVF}	IN falling	MAX17598	6.5	7	7.5	V
			MAX17599	3.6	3.9	4.2	
V_{IN} Supply Startup Current (under UVLO)	$I_{IN-STARTUP}$	V_{IN} < UVLO			20	32	µA
V_{IN} Supply Shutdown Current	I_{IN-SH}	V_{EN} = 0V			20	32	µA
V_{IN} Supply Current	I_{IN-SW}	Switching, f_{SW} = 400kHz			2		mA
V_{IN} Clamp Voltage	V_{INC}	V_{EN} = 0V, I_{IN} = 2mA sinking (MAX17598) (Note 3)		30	33	36	V
ENANBLE (EN)							
EN Threshold	V_{ENR}	V_{EN} rising		1.16	1.21	1.26	V
	V_{ENF}	V_{EN} falling		1.1	1.15	1.20	
EN Input Leakage Current	I_{EN}	V_{EN} = 1.5V, T_A = +25°C		-100		+100	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V (for MAX17598, bring V_{IN} up to 21V for startup), V_{CS} = V_{DITHER} = V_{FB} = V_{OVI} = V_{SGND} = V_{PGND} = 0V, $V_{EN/UVLO}$ = +2V, AUXDRV = NDRV = SS = COMP = SLOPE = unconnected, R_{RT} = 25kΩ, R_{DT} = 10kΩ, C_{VIN} = 1µF, C_{VDRV} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL LDO (V_{DRV})						
V_{DRV} Output Voltage Range	V_{VDRV}	8V < V_{IN} < 15V and 0mA < I_{VDRV} < 50mA (MAX17598)	7.1	7.4	7.7	V
		6V < V_{IN} < 15V and 0mA < I_{VDRV} < 50mA (MAX17599)	4.7	4.9	5.1	
V_{DRV} Current Limit	$I_{VDRV-MAX}$		70	100		mA
V_{DRV} Dropout	$V_{VDRV-DO}$	V_{IN} = 4.5V, I_{VDRV} = 20mA (MAX17599)	4.2			V
OVERVOLTAGE PROTECTION (OVI)						
OVI Overvoltage Threshold	V_{OVIR}	V_{OVI} rising	1.16	1.21	1.26	V
	V_{OVIF}	V_{OVI} falling	1.1	1.15	1.2	
OVI Masking Delay	t_{OVI-MD}			2		µs
OVI Input Leakage Current	I_{OVI}	V_{OVI} = 1V, T_A = +25°C	-100		+100	nA
OSCILLATOR (RT)						
NDRV Switching Frequency Range	f_{SW}		100		1000	kHz
NDRV Switching Frequency Accuracy			-8		+8	%
Maximum Duty Cycle	D_{MAX}	f_{SW} = 400KHz, R_{DT} = 10kΩ	71	72.5	74	%
SYNCHRONIZATION (DITHER/SYNC)						
Synchronization Logic-High Input	$V_{IH-SYNC}$		3			V
Synchronization Pulse Width				50		ns
Synchronization Frequency Range	f_{SYNC}		1.1 x f_{SW}		1.3 x f_{SW}	
DITHERING RAMP GENERATOR (DITHER/SYNC)						
Charging Current			45	50	55	µA
Discharging Current			43	50	57	µA
Ramp-High Trip Point				2		V
Ramp-Low Trip Point				0.4		

ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SOFT-START/SOFT-STOP (SS)							
Soft-Start Charging Current	I_{SSCH}			9	10	11	µA
Soft-Stop Discharging Current	$I_{SSDISCH}$			4.4	5	5.6	µA
SS Bias Voltage	V_{SS}			1.19	1.21	1.23	V
SS Discharge Threshold	$V_{SSDISCH}$	Soft-stop completion			0.15		V
NDRV DRIVER (NDRV)							
Pulldown Impedance	R_{NDRV-N}	I_{NDRV} (sinking) = 100mA			1.37	3	Ω
Pullup Impedance	R_{NDRV-P}	I_{NDRV} (sourcing) = 50mA			4.26	8.5	Ω
Peak Sink Current		C_{NDRV} = 10nF			1.5		A
Peak Source Current		C_{NDRV} = 10nF			0.9		A
Fall Time	t_{NDRV-F}	C_{NDRV} = 1nF			10		ns
Rise Time	t_{NDRV-R}	C_{NDRV} = 1nF			20		ns
AUXDRV DRIVER (AUXDRV)							
Pulldown Impedance	$R_{AUXDRV-N}$	I_{AUXDRV} (sinking) = 100mA			3.35	7	Ω
Pullup Impedance	$R_{AUXDRV-P}$	I_{AUXDRV} (sourcing) = 50mA			9.78	19	Ω
Peak Sink Current		C_{AUXDRV} = 10nF			0.7		A
Peak Source Current		C_{AUXDRV} = 10nF			0.3		A
Fall Time	$t_{AUXDRV-F}$	C_{AUXDRV} = 1nF			16		ns
Rise Time	$t_{AUXDRV-R}$	C_{AUXDRV} = 1nF			32		ns
DEAD TIME (DT)							
NDRV to AUXDRV Delay (Dead Time)	t_{DT}	NDRV↓ to AUXDRV↓	R_{DT} = 10kΩ		25		ns
			R_{DT} = 100kΩ		250		
		AUXDRV↑ to NDRV↑	R_{DT} = 10kΩ		25		
			R_{DT} = 100kΩ		250		
CURRENT-LIMIT COMPARATOR (CS)							
Cycle-by-Cycle Peak-Current-Limit Threshold	$V_{CS-PEAK}$			290	305	320	mV
Cycle-by-Cycle Runaway-Current-Limit Threshold	V_{CS-RUN}			340	360	380	mV
Cycle-by-Cycle Reverse-Current-Limit Threshold	V_{CS-REV}			-122	-102	-82	mV

ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Sense Leading-Edge Blanking Time	$t_{CS-BLANK}$	From NDRV↑ edge		70		ns
Current-Sense-Blanking Time for Reverse-Current Limit	$t_{CS-BLANK-Rev}$	From AUXDRV↓ edge		70		ns
Propagation Delay from Comparator Input to NDRV	t_{PDCS}	From CS rising (10mV overdrive) to NDRV falling (excluding leading-edge blanking)		40		ns
Number of Consecutive Peak-Current-Limit Events to HICCUP	$N_{HICCUP-P}$			8		event
Number of Runaway Current-Limit Events to HICCUP	$N_{-HICCUP-R}$			1		event
Overcurrent Hiccup Timeout				32,768		cycle
Minimum On-Time	t_{ON-MIN}		90	130	170	ns
SLOPE COMPENSATION (SLOPE)						
Slope Bias Current	I_{SLOPE}		9	10	11	µA
Slope Resistor Range	R_{SLOPE}		25		200	kΩ
Slope Compensation Ramp		R_{SLOPE} = 100kΩ	140	165	190	mV/µs
Default Slope Compensation Ramp		V_{SLOPE} < 0.2V or 4V < V_{SLOPE}		50		mV/µs
PWM COMPARATOR						
Comparator Offset Voltage	V_{PWM-OS}	V_{COMP}, when V_{CS} = 0V	1.65	1.81	2	V
Current-Sense Gain	A_{CS-PWM}	ΔV_{COMP} /ΔV_{CS}	1.75	1.97	2.15	V/V
Comparator Propagation Delay	t_{PWM}	Change in V_{CS} = 10mV (including internal lead-edge blanking)		110		ns
ERROR AMPLIFIER						
FB Reference Voltage	V_{REF}	V_{FB}, when I_{COMP} = 0V and V_{COMP} = 1.8V	1.19	1.21	1.23	V
FB Input Bias Current	I_{FB}	V_{FB} = 1.5V, T_A = +25°C	-100		+100	nA
Open-Loop Voltage Gain	A_{EAMP}			90		dB
Transconductance	Gm		1.5	1.8	2.1	mS

ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Transconductance Bandwidth	BW	Open-loop (gain = 1), -3dB frequency°		10		MHz
Source Current		V_{COMP} = 1.8V, V_{FB} = 1V	80	120	210	µA
Sink Current		V_{COMP} = 1.8V, V_{FB} = 1.75V	80	120	210	µA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		Temperature rising		160		°C
Thermal Shutdown Hysteresis				20		°C

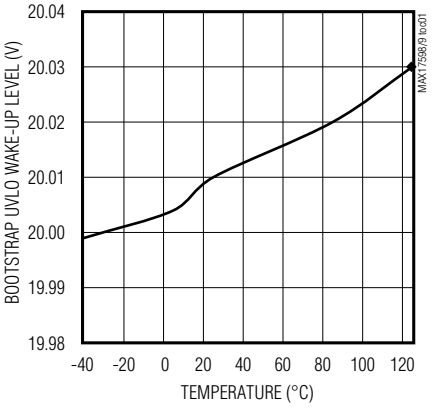
Note 2: All devices are 100% production tested at +25°C. Limits over temperature are guaranteed by design.

Note 3: The MAX17598 is intended for use in universal input power supplies. The internal clamp circuit at IN is used to prevent the bootstrap capacitor from charging to a voltage beyond the absolute maximum rating of the device when EN is low (shutdown mode). Externally limit the maximum current to IN (hence to clamp) to 2mA (max) when EN is low.

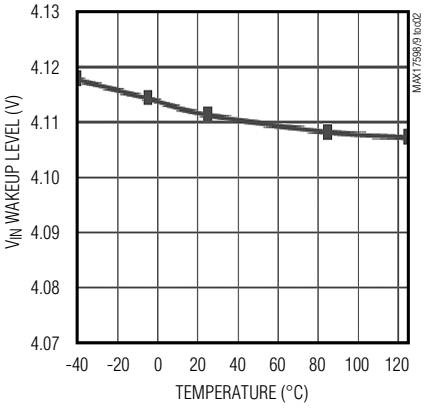
Typical Operating Characteristics

(V_{IN} = 15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{VIN} = 1µF, C_{VDRV} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted.)

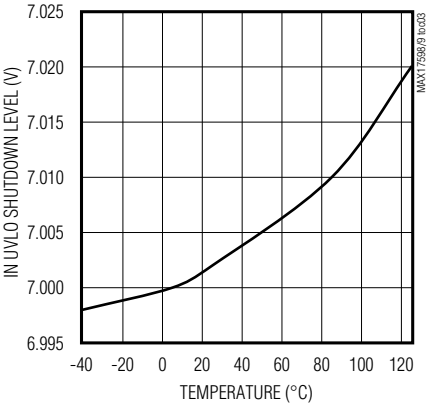
BOOTSTRAP UVLO WAKE-UP LEVEL vs. TEMPERATURE (MAX17598)



V_{IN} WAKEUP LEVEL vs. TEMPERATURE (MAX17599)



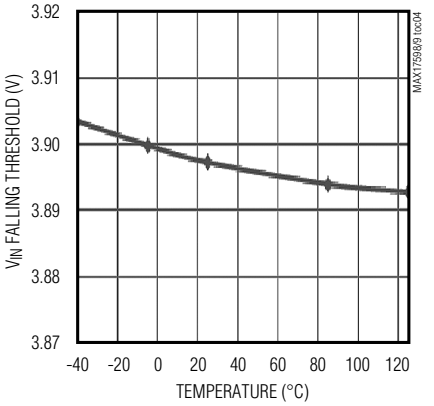
IN UVLO SHUTDOWN LEVEL vs. TEMPERATURE (MAX17598)



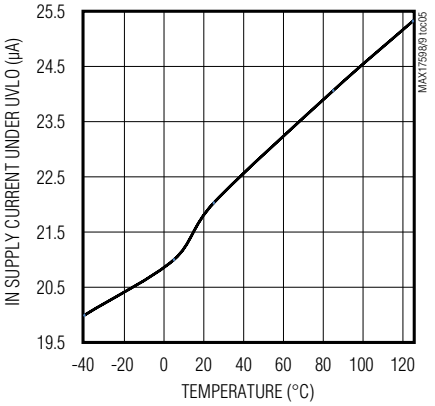
Typical Operating Characteristics (continued)

(V_{IN} = 15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{VIN} = 1µF, C_{VDRV} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted.)

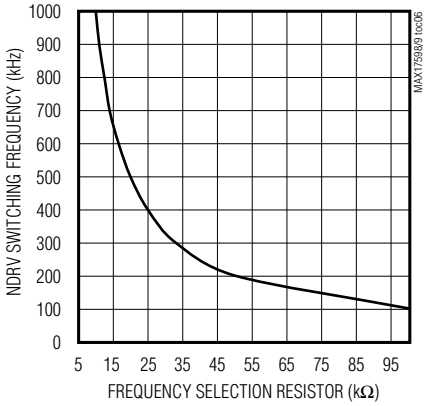
V_{IN} FALLING THRESHOLD vs. TEMPERATURE (MAX17599)



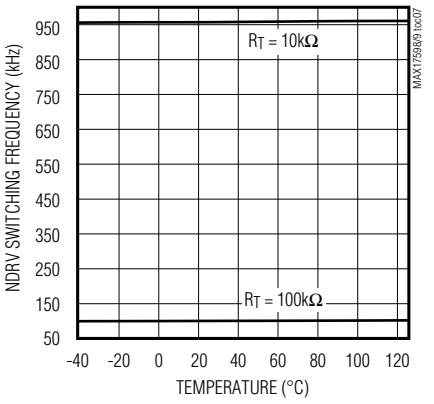
IN SUPPLY CURRENT UNDER UVLO vs. TEMPERATURE



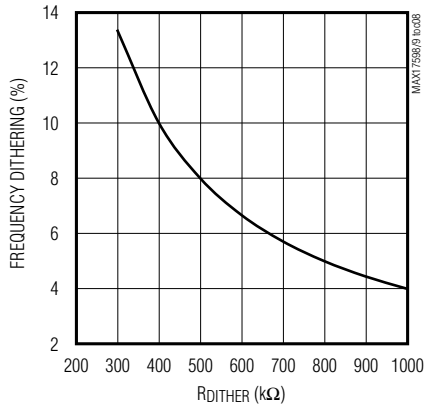
NDRV SWITCHING FREQUENCY vs. RESISTOR



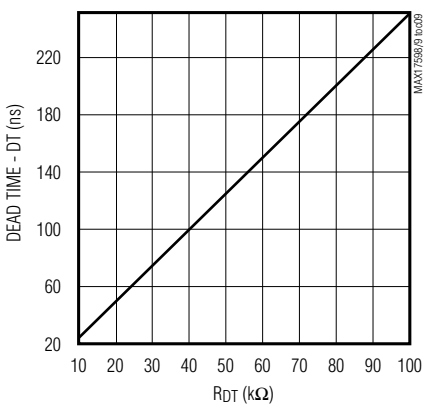
NDRV SWITCHING FREQUENCY vs. TEMPERATURE



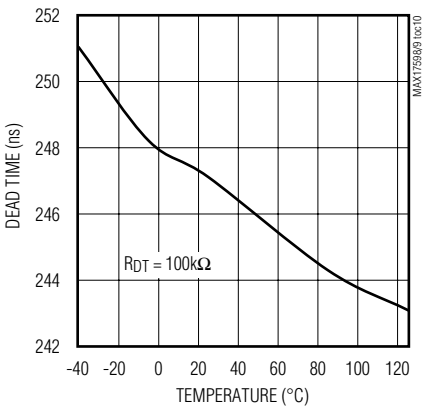
FREQUENCY DITHERING vs. R_{DITHER}



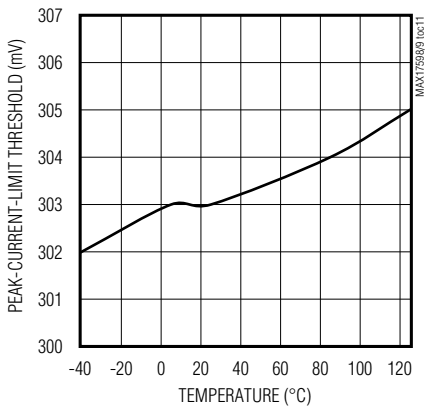
DEAD TIME vs. R_{DT}



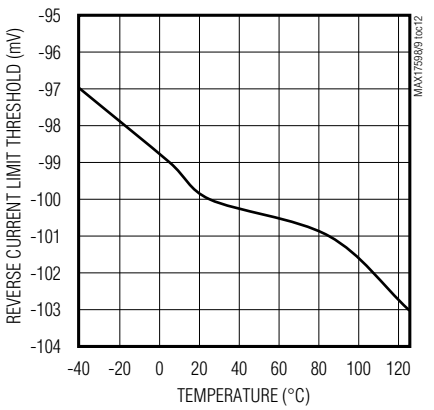
DEAD TIME vs. TEMPERATURE



PEAK-CURRENT-LIMIT THRESHOLD vs. TEMPERATURE



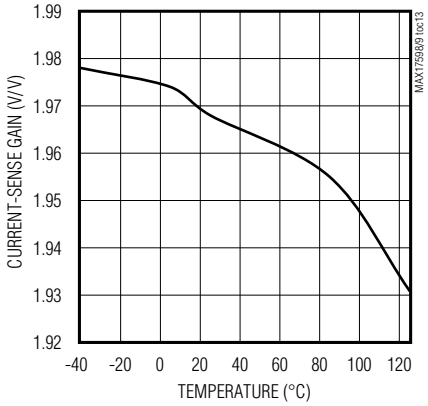
REVERSE CURRENT LIMIT THRESHOLD vs. TEMPERATURE



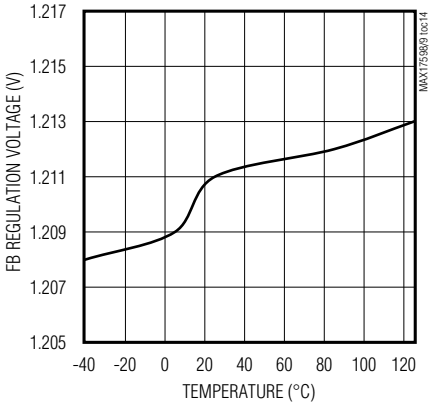
Typical Operating Characteristics (continued)

(V_{IN} = 15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{VIN} = 1µF, C_{VDRV} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted.)

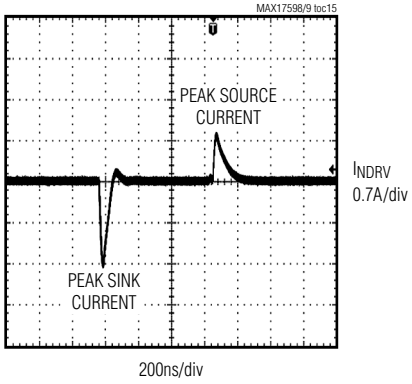
CURRENT-SENSE GAIN vs. TEMPERATURE



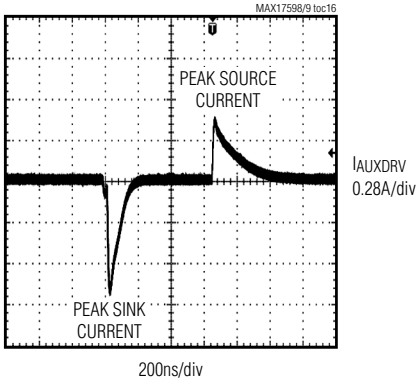
FB REGULATION VOLTAGE vs. TEMPERATURE



NDRV PEAK SOURCE AND SINK CURRENTS

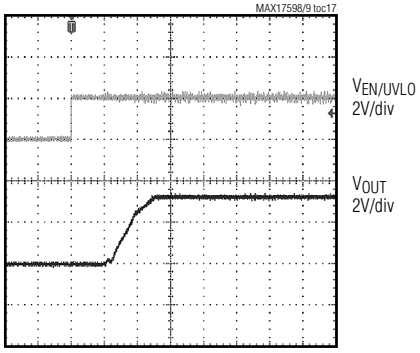


AUXDRV PEAK SOURCE AND SINK CURRENTS

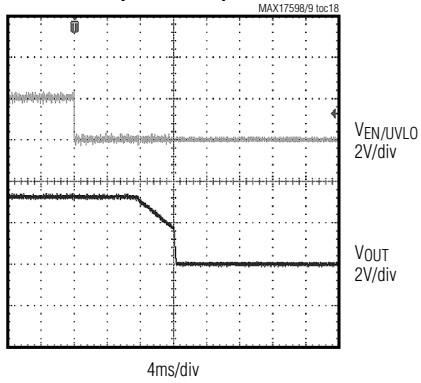


Typical Operating Characteristics (continued)

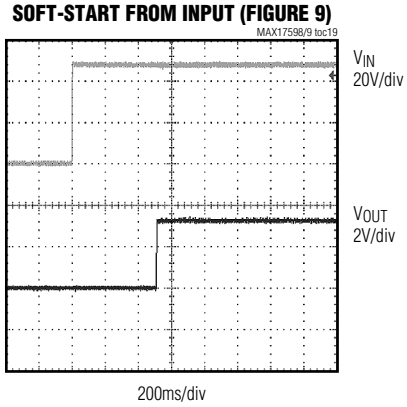
ENABLE STARTUP WAVEFORM (DUTY-CYCLE SOFT-START)



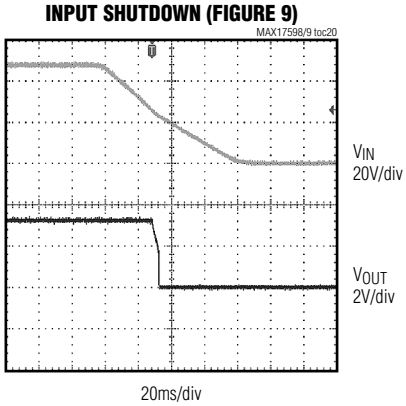
ENABLE SHUTDOWN WAVEFORM (SOFT-STOP)



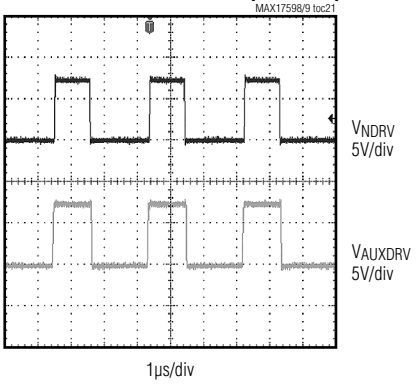
SOFT-START FROM INPUT (FIGURE 9)



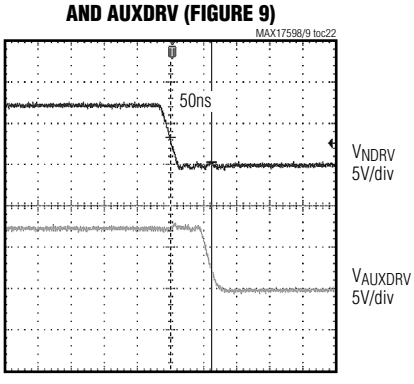
INPUT SHUTDOWN (FIGURE 9)



NDRV AND AUXDRV SIGNALS (FIGURE 9)

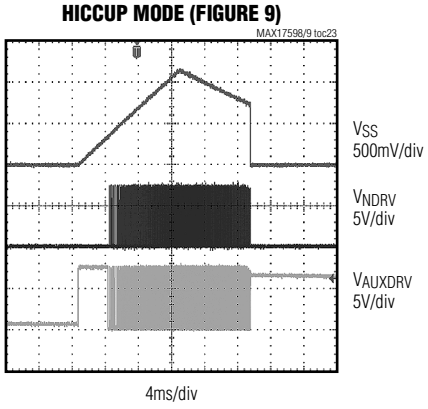


DEAD TIME BETWEEN NDRV AND AUXDRV (FIGURE 9)

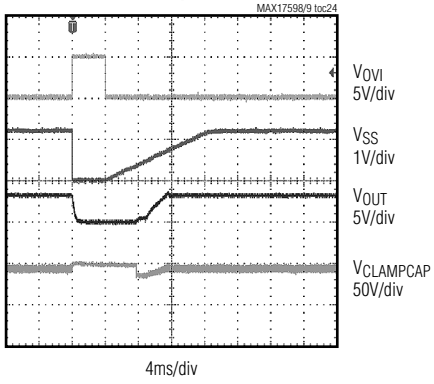


Typical Operating Characteristics (continued)

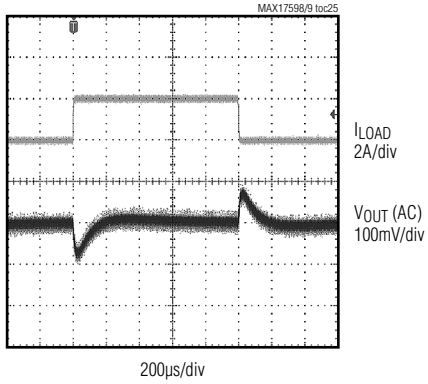
SS, NDRV AND AUXDRV IN HICCUP MODE (FIGURE 9)



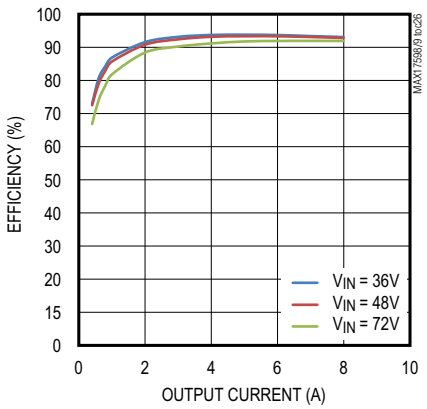
MOMENTARY OVI OPERATION (FIGURE 9)



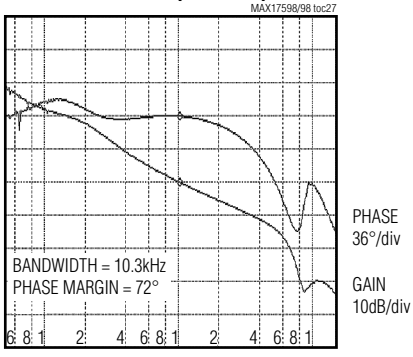
LOAD TRANSIENT RESPONSE (FIGURE 9)



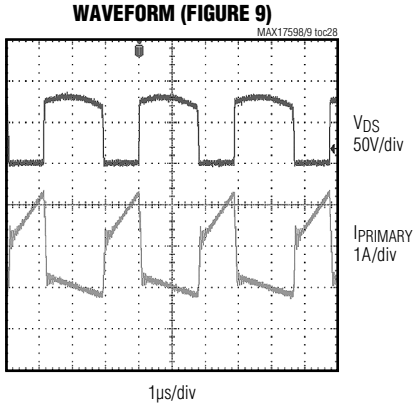
EFFICIENCY CURVES



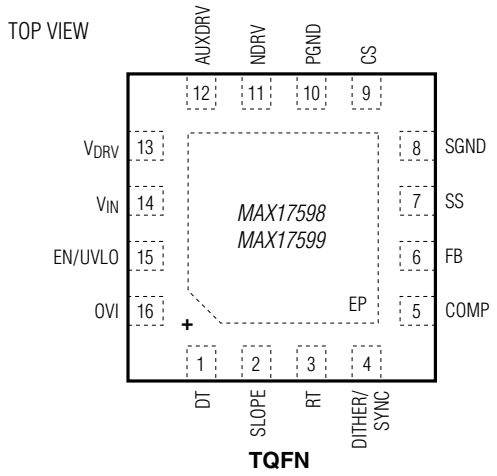
BODE PLOT (FIGURE 9)



ACTIVE CLAMP SWITCHING WAVEFORM (FIGURE 9)



Pin Configuration



TQFN

Pin Description

PIN	NAME	FUNCTION
1	DT	Dead-Time Programming Resistor Connection. Connect resistor from DT to GND to set the desired dead time between the NDRV and AUXDRV signals. See the *Dead Time* section to calculate the resistor value for a particular dead time.
2	SLOPE	Slope Compensation Programming Input. A resistor RSLOPE connected from SLOPE to SGND programs the amount of internal slope compensation. Shorting this pin to SGND sets a default slope compensation of 50mV/µs.
3	RT	Switching Frequency Programming Resistor Connection. Connect resistor from RT to SGND to set the PWM switching frequency.
4	DITHER/SYNC	Frequency Dithering Programming or Synchronization Connection. For spread-spectrum frequency operation, connect a capacitor from DITHER to SGND and a resistor from DITHER to RT. To synchronize the internal oscillator to the externally applied frequency, connect DITHER/SYNC to the synchronization pulse.
5	COMP	Transconductance Amplifier Output. Connect the frequency compensation network between COMP and SGND in nonisolated applications and between COMP and FB pins in isolated applications.
6	FB	Transconductance Error Amplifier Inverting Input
7	SS	Soft-Start/Soft-Stop Capacitor Pin for Forward/Flyback Regulator. Connect a capacitor from SS to SGND to set the soft-start/soft-stop time interval.
8	SGND	Signal Ground. Connect SGND to the signal ground plane.
9	CS	Current-Sense Input. Current-sense connection for average current-sense and cycle-by-cycle current limit. Peak current limit trip voltage is 350mV (typ).
10	PGND	Power Ground. Connect PGND to the power ground plane.

Pin Description (continued)

PIN	NAME	FUNCTION
11	NDRV	External Switching NMOS Gate-Driver Output
12	AUXDRV	PMOS Active-Clamp-Switch Gate-Driver Output. AUXDRV can also be used to drive a pulse transformer for synchronous flyback application.
13	V_{DRV}	Linear Regulator Output and Driver Input. Connect a 1µF bypass capacitor from V_{DRV} to PGND as close as possible to the IC.
14	V_{IN}	Internal V_{DRV} Regulator Input. Connect V_{IN} to the input voltage source. Bypass V_{IN} to PGND with a 0.1µF minimum ceramic capacitor.
15	EN/UVLO	Enable/Undervoltage Lockout Pin. To externally program the UVLO threshold of the input supply, connect a resistive divider among input supply, EN/UVLO, and SGND.
16	OVI	Overvoltage Comparator Input. Connect a resistive divider among the input supply, OVI, and SGND to set the input overvoltage threshold.
—	EP	Exposed Pad

Detailed Description

The MAX17598/MAX17599 low I_Q active-clamp current-mode PWM controllers contain all the control circuitry required for design of wide-input isolated/nonisolated forward converter industrial power supplies. The MAX17598 has a rising UVLO threshold of 20V with a 13V hysteresis, and is therefore well-suited for universal input (rectified 85V AC to 265V AC) or telecom (36V DC to 72V DC) power supplies. The MAX17599 features a 4.1V rising UVLO with a 200mV hysteresis and is optimized for low-voltage industrial supplies (4.5V DC to 36V DC).

The devices include an AUX driver that drives an auxiliary MOSFET (clamp switch) that helps implement the active-clamp transformer reset topology for forward converters. Such a reset topology has several advantages, including reduced voltage stress on the switches, transformer size reduction due to larger allowable flux swing, and improved efficiency due to elimination of dissipative snubber circuitry. Programmable dead time between the AUX and main driver allows for zero voltage switching (ZVS).

Input Voltage Range

The MAX17598 has different rising and falling undervoltage lockout (UVLO) thresholds on the V_{IN} pin than those of the MAX17599. The thresholds for the MAX17598 are optimized for implementing power-supply startup schemes typically used for off-line AC/DC and telecom DC-DC power supplies that are typically encountered in industrial applications. As such, the MAX17598 has no limitation on the maximum input voltage, as long as the external components are rated suitably, and the maximum operating voltages of the MAX17598 are respected. The MAX17598 can be successfully used in universal input (85V to 265V AC) rectified bus applications, rectified 3-phase DC bus applications, and telecom (36V to 72V DC) applications.

The V_{IN} pin of the MAX17599 has a maximum operating voltage of 36V. The MAX17599 implements rising and falling thresholds on the V_{IN} pin that assume power-supply startup schemes, typical of lower voltage DC-DC applications down to an input voltage of 4.5V DC. Thus isolated/non-isolated active-clamp converters with supply-voltage range of 4.5V to 36V can be implemented with the MAX17599. See *Startup Operation* section for more details on power-supply startup schemes for MAX17598/MAX17599.

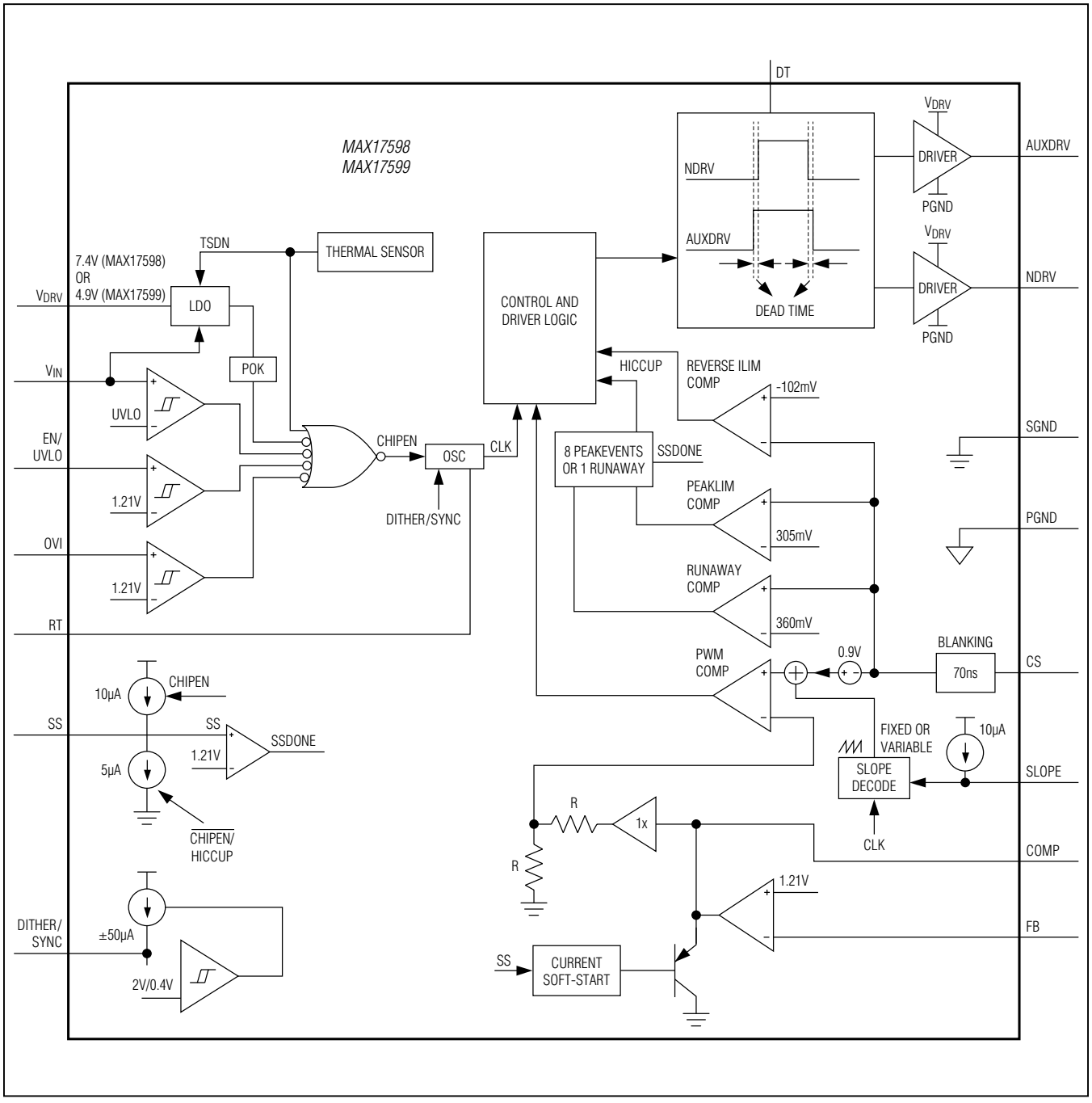


Figure 1. Block Diagram

Linear Regulator (V_{DRV})

The MAX17598/MAX17599 have an internal linear regulator that is powered from the V_{IN} pin. The output of the linear regulator is connected to the V_{DRV} pin, and should be decoupled with a 1µF capacitor to ground for stable operation. The V_{DRV} converter output supplies the MOSFET drivers internal to the MAX17598/MAX17599. The V_{DRV} voltage is regulated at 7.4V (typ) in the MAX17598, and at 4.9V (typ) in the MAX17599. The maximum operating voltage of the IN pin is 29V for the MAX17598 and 36V for the MAX17599.

Maximum Duty Cycle (Dmax)

The MAX17598/MAX17599 operate at a maximum duty cycle of 72.5% (typ). When the SLOPE pin is left OPEN, the ICs have the necessary amount of slope compensation to provide stable, jitter-free current-mode control operation in applications where the operating duty cycle is less than 50%. Slope compensation is necessary for stable operation of current-mode controlled converters at duty cycles greater than 50%, in addition to the loop compensation required for small signal stability. The MAX17598/MAX17599 implement a SLOPE pin for this purpose. See the *Slope Compensation Programming* section for more details.

Applications Information

Startup Voltage and Input Overvoltage Protection Setting (EN/UVLO, OVI)

The EN/UVLO pin in the MAX17598/MAX17599 serves as an enable/disable input, as well as an accurate programmable undervoltage lockout (UVLO) pin. The MAX17598/MAX17599 do not commence startup operations unless the EN/UVLO pin voltage exceeds 1.21V (typ). The MAX17598/MAX17599 turn off if the EN/UVLO pin voltage falls below 1.15V (typ). A resistor divider from the input DC bus to ground maybe used to divide down and apply a fraction of the input DC voltage to the EN/UVLO pin as shown in Figure 2. The values of the resistor divider can be selected so that the EN/UVLO pin voltage exceeds the 1.21V (typ) turn on threshold at the desired input DC bus voltage. The same resistor divider can be modified with an additional resistor, R_{OVI}, to implement input overvoltage protection, in addition to the EN/UVLO functionality as shown in Figure 2. When the voltage at the OVI pin exceeds 1.21V (typ), the MAX17598/MAX17599 stop switching. Switching resumes with soft-start operation, only if the voltage at the OVI pin falls below 1.15V (typ). The OVI feature is easily disabled by tying the pin to ground. For given values of startup DC input voltage (V_{START}) and input overvoltage protection voltage (V_{OVI}), the resistor values for the divider can be calculated as follows, assuming a 24.9kΩ resistor for R_{OVI}. R_{SUM} represents the series combination of several resistors that might be needed in high-voltage DC bus applications (MAX17598) or a single resistor in low-voltage DC-DC applications (MAX17599).

$$R_{EN} = 24.9 \times \left[\frac{V_{OVI}}{V_{START}} - 1\right] k\Omega,$$

where V_{START} and V_{OVI} are in volts.

$$R_{SUM} = \left[24.9 + R_{EN}\right] \times \left[\frac{V_{START}}{1.21} - 1\right] k\Omega,$$

where R_{EN} is in kΩ. R_{SUM} might need to be implemented as equal multiple resistors in series (R_{DC1}, R_{DC2}, R_{DC3}) so that voltage across each resistor is limited to its maximum operating voltage.

$$R_{DC1} = R_{DC2} = R_{DC3} = \frac{R_{SUM}}{3} k\Omega.$$

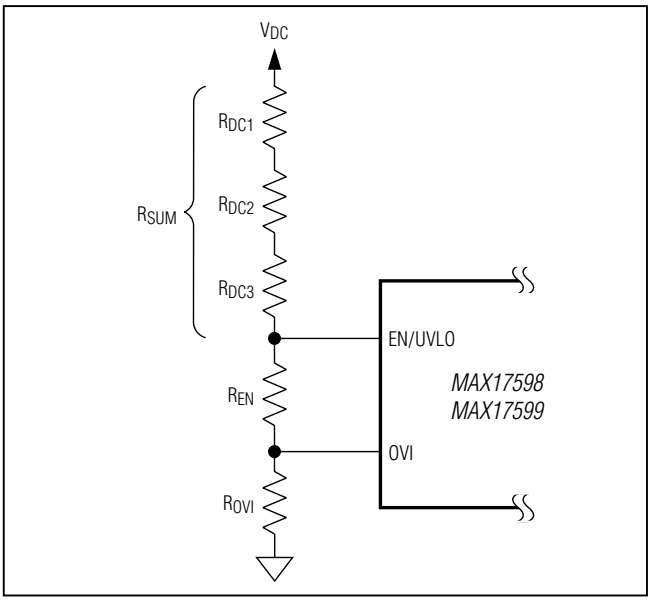


Figure 2. Programming EN/UVLO, OVI

Startup Operation

The MAX17598 is optimized for implementing active-clamp converters operating either from a rectified AC input or in a 36V DC to 72V_{DC} telecom application. A cost-effective RC startup circuit can be used in such applications. In this startup method (Figure 3), when the input DC voltage is applied, the startup resistor R_{START} charges the startup capacitor C_{START}, causing the voltage at the V_{IN} pin to increase towards the rising V_{IN} UVLO threshold (20V typical). During this time, the MAX17598 draws a low startup current of 20µA (typ) through the startup resistor R_{START}. When the voltage at V_{IN} reaches the rising IN UVLO threshold, the MAX17598 commences all internal operations and drives the external MOSFETs connected to NDRV and AUXDRV. In this condition, the MAX17598 draws 2mA (typ) current in from C_{START}, in addition to the current required to switch the gates of the external MOSFETs Q1and Q2. Since this current cannot be supported by the current through R_{START}, the voltage on C_{START} starts to drop. When suitably configured as shown in Figure 3, the converter operates to generate an output voltage (V_{BIAS}) that is bootstrapped to the V_{IN} pin. If the voltage V_{BIAS} exceeds 7V before the voltage on C_{START} falls below 7V (typ), then the V_{IN} voltage is sustained by V_{BIAS}, thus allowing the MAX17598 to continue to operate with energy from V_{BIAS}. The large hysteresis (13V typical) of the MAX17598 allows for a small startup capacitor (C_{START}). The low startup current (20µA typical) allows the use of a large startup resistor (R_{START}), thus reducing power dissipation at higher DC bus voltages. The startup resistor R_{START} might need to be implemented as equal, multiple resistors in series (R_{IN1}, R_{IN2} and R_{IN3}) to share the applied high DC voltage in offline applications so that the voltage across each resistor is limited to the maximum continuous operating voltage rating. R_{START} and C_{START} can be calculated as follows:

$$C_{START} = 0.09\left[\begin{array}{c}7.4\times C_{VDRV} + 0.04\times I_{IN}\times C_{SS}\\ +\left(I_{IN}+\frac{Q_{GATE}\times f_{sw}}{10^6}\right)t_{SS}\end{array}\right]\mu F$$

where I_{IN} is the supply current drawn at the IN pin in mA, Q_{GATE} is the sum of the gate charges of the external MOSFETs Q1 and Q2 in nC, f_{sw} is the switching frequency of the converter in Hz, t_{SS} is the soft-start time programmed for the converter in ms. C_{VDRV} is cummulative capacitor used at DRV node in µF, and C_{SS} is soft-start capacitor in nF. See the *Soft-Start* section.

$$R_{START} = \frac{(V_{START} - 10)\times 50}{[1 + C_{START}]}k\Omega,$$

where C_{START} is the startup capacitor in µF.

The IN UVLO rising threshold of the MAX17599 is set to 4.1V with a hysteresis of 200mV, and is optimized for low-voltage DC-DC applications in the range of 4.5V DC to 36V DC. The IN pin is rated for a maximum operating input voltage of 36V DC and can directly be connected to the input DC supply.

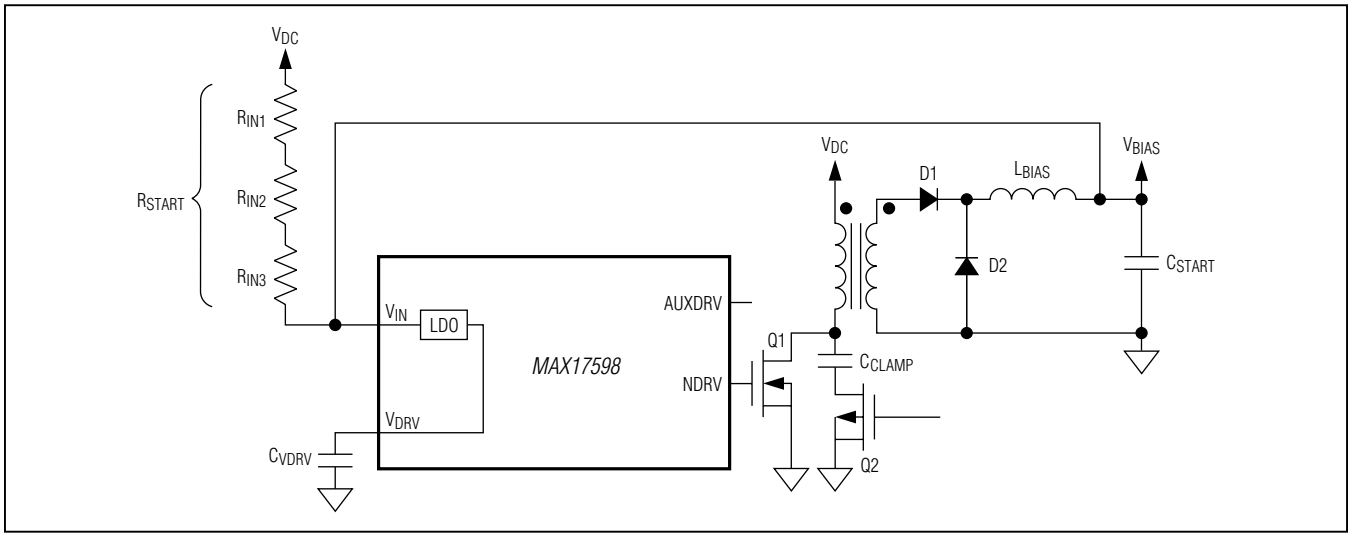


Figure 3. RC-Based Startup Circuit

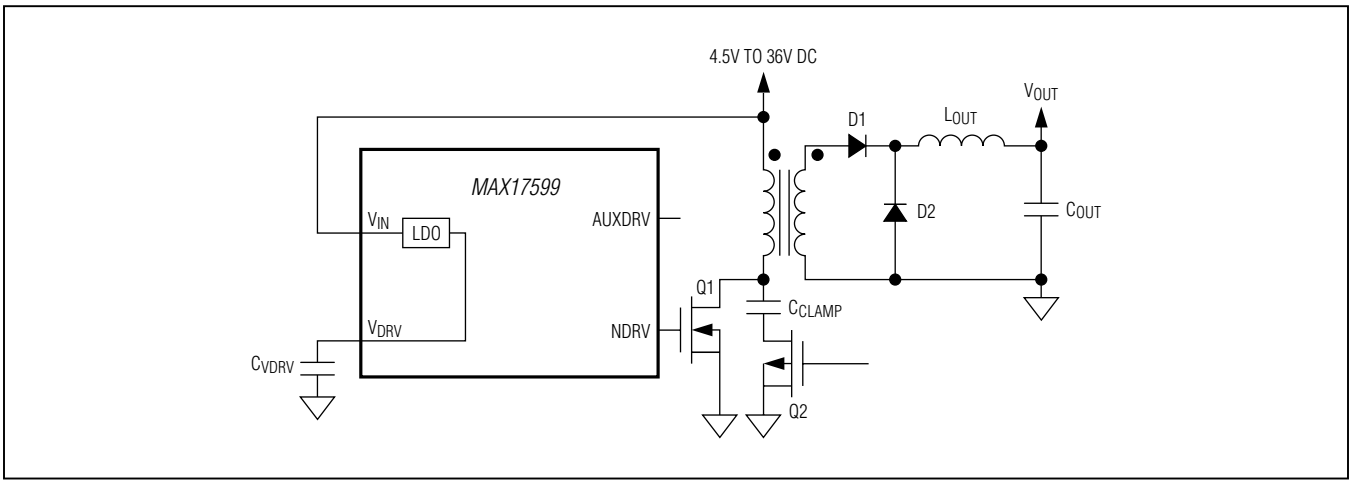


Figure 4. Typical Startup Circuit with IN Connected Directly to DC Input

Soft-Start and Soft-Stop

In a current-mode isolated active clamp forward converter, the COMP voltage programs the peak current in the primary, and thus the secondary-side inductor current as well. The MAX17598/MAX17599 implement a soft-start scheme that controls the COMP pin of the device at turn on. A useful benefit of this feature is the elimination of need for secondary-side soft-start circuitry in such isolated applications. In the absence of secondary-side soft-start circuitry, the secondary-side error amplifier can cause the output voltage to rapidly reach the regulation value, thus causing inrush current and output voltage overshoot. The MAX17598/MAX17599 avoid this issue by applying a soft-start to the COMP pin. Thus the regulator's primary and secondary currents are ramped up in a well-controlled manner resulting in a current-mode soft-start operation.

Soft-start period of MAX17598/MAX17599 can be programmed by selecting the value of capacitor connected from SS pin to GND. The capacitor C_{SS} can be calculated as follows:

$$C_{SS} = \frac{10 \times t_{SS}}{V_{COMP} - 1.81} nF$$

where t_{SS} is in ms, V_{COMP} is steady-state COMP voltage ($V_{COMP,MAX}$ = 2.6V).

A soft-stop feature ramps down the output voltage when the device is turned off, and provides safe discharging of the clamp capacitor, thus allowing the controller to restart in a well-controlled manner. Additionally, a negative current limit is provided in the current-sense circuitry that helps limit the clamp switch current under dynamic operating conditions, such as momentary input overvoltage charging from a precharged output capacitor. The soft-stop duration is twice that of the programmed soft-start period.

Programming Slope Compensation

Since the MAX17598/MAX17599 operate at a maximum duty cycle of 72.5% (typ), slope compensation is required to prevent subharmonic instability that occurs naturally in continuous-conduction mode, peak current mode-controlled converters operating at duty cycles greater than 50%. A minimum amount of slope signal is added to the sensed current signal, even for converters operating below 50% duty to provide stable, jitter-free operation. The SLOPE pin allows the user to program the necessary slope compensation by setting the value of the resistor R_{SLOPE} connected from SLOPE pin to ground.

$$R_{SLOPE} = \frac{S_E - 8}{1.55} k\Omega$$

where S_E, the slope is expressed in mV per microseconds.

For the default minimum slope compensation of 50mV/µs (typ), the SLOPE pin should be connected to SGND or left unconnected.

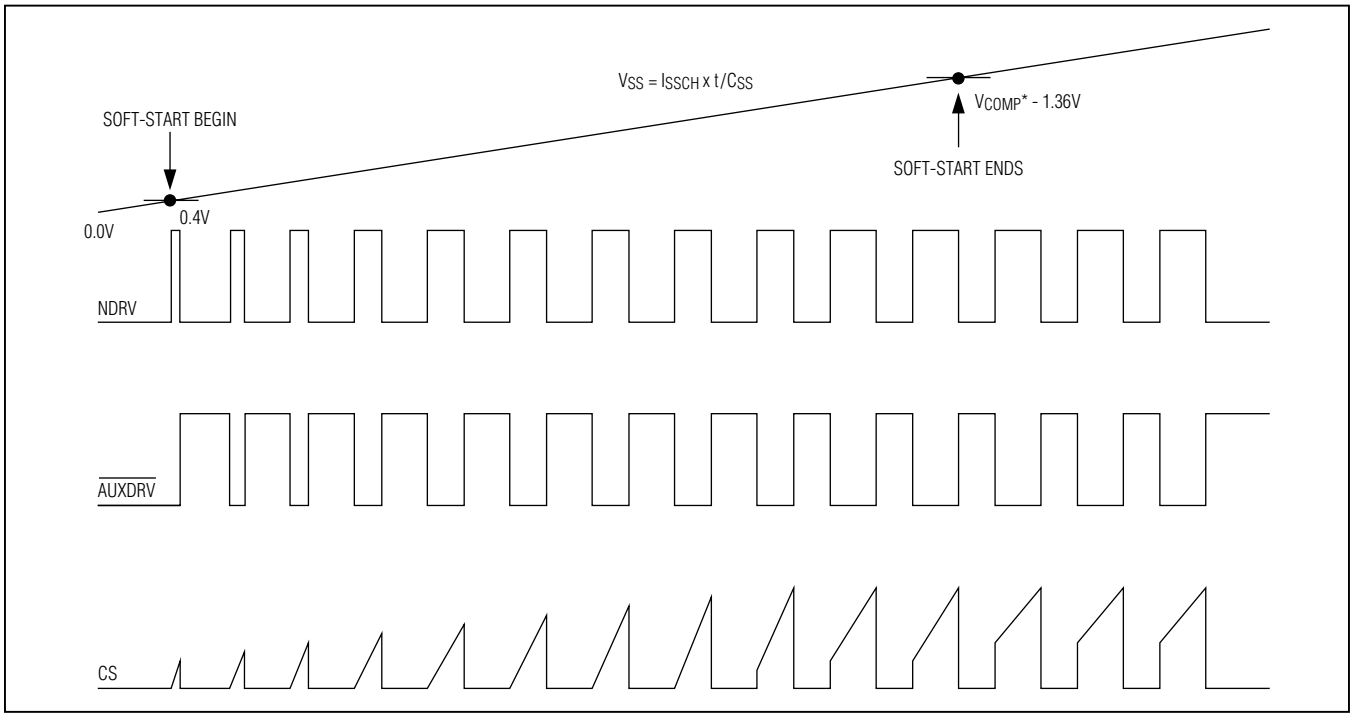


Figure 5. Duty Cycle Soft-Start

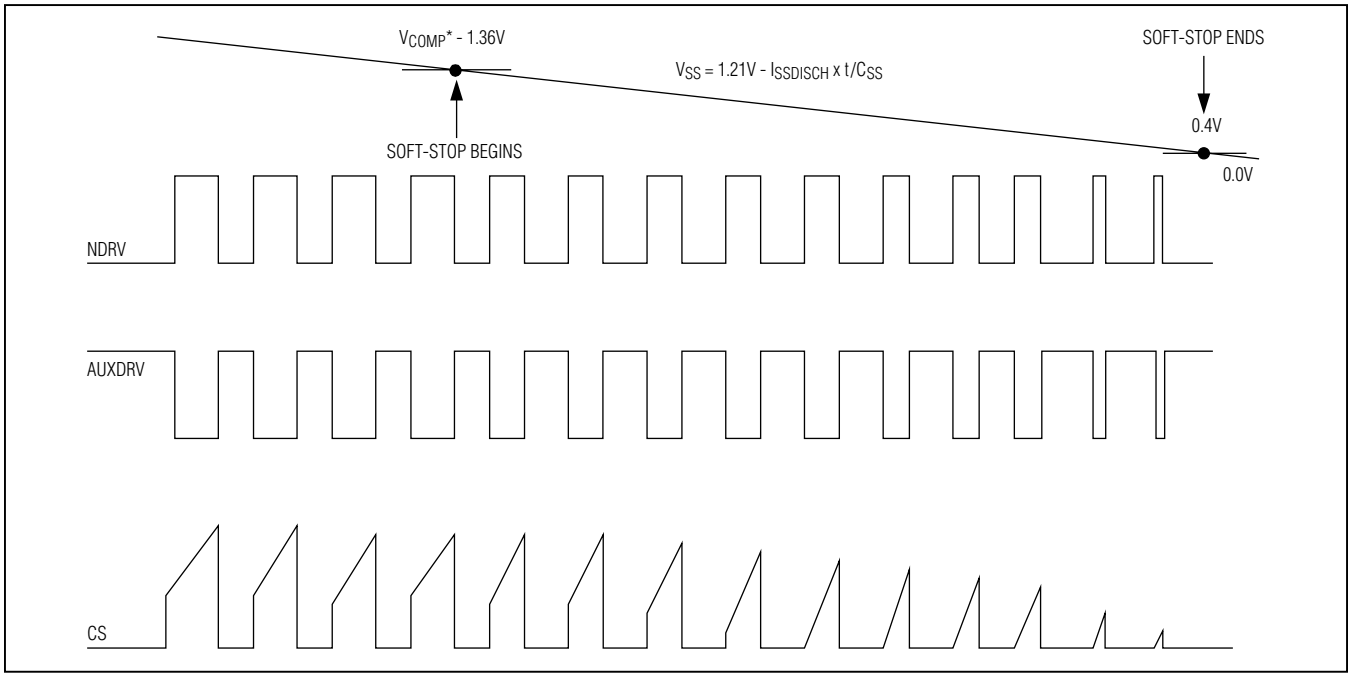


Figure 6. Duty Cycle or Current Soft-Stop

**V_{COMP} is steady-state COMP voltage.*

n-Channel MOSFET Gate Driver

The NDRV output drives an external n-channel MOSFET. NDRV can source/sink in excess of 900mA/1500mA peak current. Therefore, select a MOSFET that yields acceptable conduction and switching losses.

p-Channel MOSFET Gate Driver

The AUXDRV output drives an external p-channel MOSFET with the aid of a level shifter, as shown in the *Typical Application Circuits*. AUXDRV can source/sink in excess of 300mA/700mA peak current. Therefore, select a MOSFET that yields acceptable conduction and switching losses. The external PMOSFET used must be able to withstand the maximum clamp voltage.

Dead Time

Dead time between the main and AUX output edges allow ZVS to occur, minimizing switching losses and improving efficiency. The dead time (t_{DT}) is applied to both leading and trailing edges of the main and AUX outputs as shown in Figure 7. Connect a resistor between DT and GND to set t_{DT} to any value between 25ns and 250ns. RDT in kΩ, is calculated as:

$$R_{DT} = 0.4 \times t_{DT}\ k\Omega,$$

where t_{DT} is in ns.

Oscillator/Switching Frequency

The ICs' switching frequency is programmable between 100kHz and 1MHz with a resistor R_{RT} connected between RT and GND. Use the following formula to determine the appropriate value of R_{RT} needed to generate the desired output switching frequency (f_{SW}):

$$R_{RT} = \frac{1 \times 10^{10}}{f_{SW}}$$

where f_{SW} is the desired switching frequency.

Peak-Current-Limit

The current-sense resistor (R_{CS}), connected between the source of the n-channel MOSFET and PGND, sets the current limit. The source end of current-sense resistor connects to CS pin of MAX17598/MAX17599. The signal thus obtained is used by the devices, both for current-mode control and peak-current limiting purposes. The current-limit comparator has a voltage trip level ($V_{CS-PEAK}$) of 305mV, and is independent of slope compensation applied to stabilize the converter. The following equation is used to calculate the value of R_{CS}:

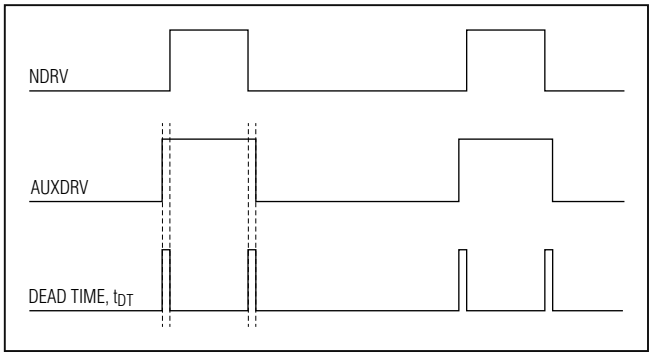


Figure 7. Dead Time Between AUXDRV and NDRV

$$R_{CS} = \frac{305mV}{1.2 \times I_{PRI\_PEAK}}$$

where I_{PRI_PEAK} is the peak current in the primary side of the transformer, which also flows through the main n-channel MOSFET. When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (NDRV) terminates the current on-cycle within 40ns (typ).

The devices implement 70ns of internal leading-edge blanking to ignore leading-edge current spikes encountered in practice due to parasitics. Use a small RC network for additional filtering of the leading-edge spike on the sense waveform when needed. Set the corner frequency of the RC filter network at 5 to 10 times the switching frequency.

For a given peak-current-limit setting, the runaway current limit is typically 20% higher. The peak current-limit-triggered hiccup operation is disabled until the end of soft-start, while the runaway current-limit-triggered hiccup operation is always enabled.

Negative Peak Current Limit

The MAX17598/MAX17599 protect against excessive negative currents through the clamp switch, primary of the transformer and the clamp capacitor under dynamic operating conditions. The devices limit negative current by monitoring the voltage across R_{CS}, while the AUXDRV output is low and the p-Channel FET is on. The typical negative-current-limit threshold is set at -102mV (1/3 of the positive-peak-current-limit threshold).

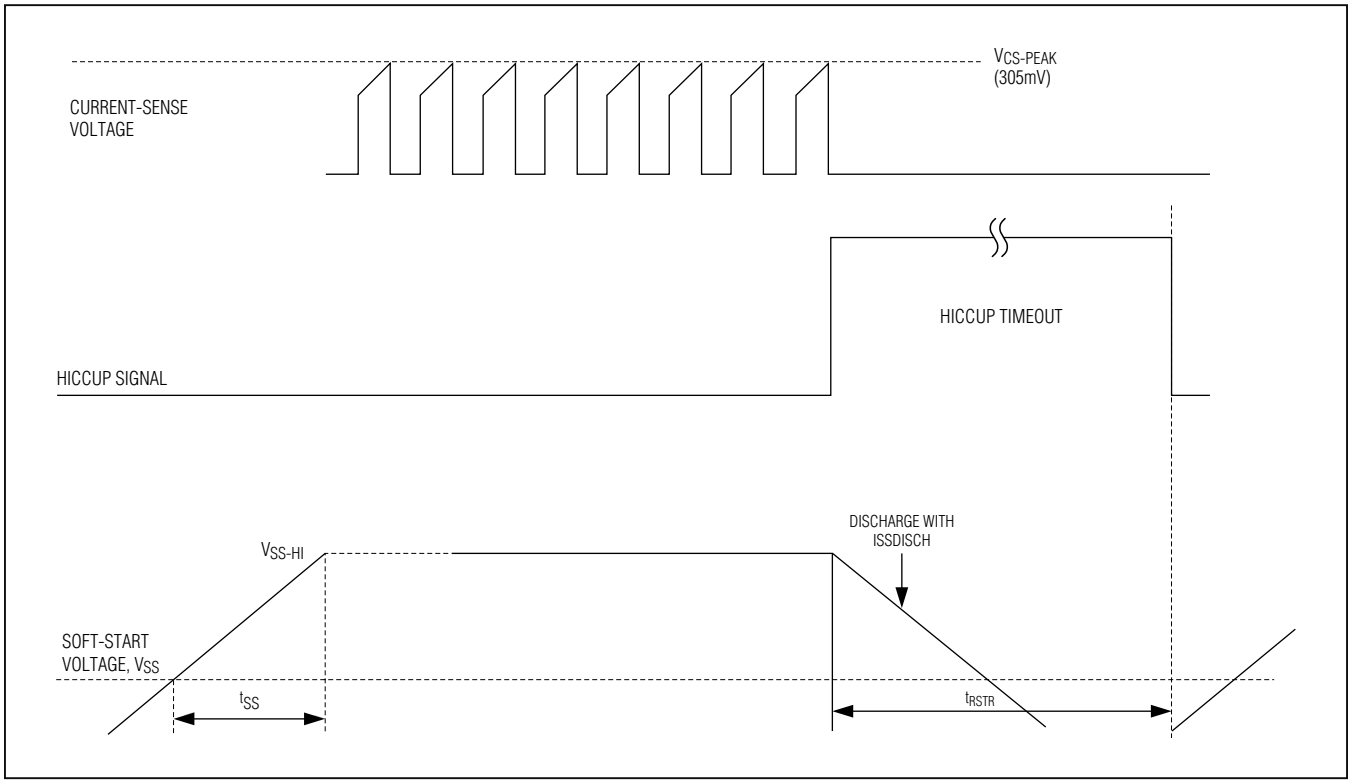


Figure 8. Hiccup-Mode Timing Diagram

Output Short-Circuit Protection with Hiccup Mode

When the MAX17598/MAX17599 detect eight consecutive peak-current-limit events, both NDRV and AUXDRV driver outputs are turned off (hiccup is followed by soft-stop) for a restart period, t_{RSTR}. After t_{RSTR}, the device turns on again with a soft-start. The duration of the restart period is 32678 clock cycles, and therefore depends on the switching frequency setting. The device also features a runaway current limit setting at 120% (typ) of the peak current limit. This feature is useful under short-circuit faults in forward converters with synchronous rectifiers that occur during minimum on-time conditions at high input voltages. Under these conditions, the primary peak current tends to build up and staircase beyond the peak current limit setting due to insufficient discharging of the output inductor. One single event of a runaway current limit forces the MAX17598/MAX17599 into hiccup mode operation. Figure 8 shows the behavior of the device prior and during hiccup mode.

Oscillator Synchronization

The internal oscillator can be synchronized to an external clock by applying the clock to SYNC/DITHER directly. The external clock frequency can be set anywhere between 1.1x to 1.3x the internal clock frequency. Using an external clock increases the maximum duty cycle by a factor equal to f_{SYNC}/f_{SW}.

Frequency Dithering for Spread-Spectrum Applications (Low EMI)

The switching frequency of the converter can be dithered in a range of ±10% by connecting a capacitor from DITHER/SYNC to GND, and a resistor from DITHER to RT as shown in the *Typical Applications Circuit*. This results in lower EMI.

A current source at SYNC/DITHER charges the capacitor C_{DITHER} to 2V with 50µA. Upon reaching this trip point, it discharges C_{DITHER} to 0.4V with 50µA. The charging and discharging of the capacitor generates a triangular waveform on SYNC/DITHER with peak levels at 0.4V and 2V. C_{DITHER} is calculated as:

$$C_{DITHER} = \frac{15.625}{f_{TRI}} nF$$

where f_{TRI} is in kHz.

Typically, f_{TRI} should be set close to 1kHz. The resistor R_{DITHER} connected from SYNC/DITHER to RT determines the amount of dither as follows:

$$\%DITHER = \frac{R_{RT}}{R_{DITHER}}$$

where %DITHER is the amount of dither expressed as a percentage of the switching frequency. Setting R_{DITHER} to 10 x R_{RT} generates ±10% dither.

Layout Recommendations

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents in high-frequency switching power converters. This implies that the loop areas for forward- and return-pulsed currents in various parts of the circuit should be minimized. Additionally, small current loop areas reduce radiated EMI. Similarly, the heatsink of the MOSFET presents a dV/dt source. Therefore, the surface area of the MOSFET heatsink should be minimized as much as possible.

Ground planes must be kept as intact as possible. The ground plane for the power section of the converter should be kept separate from the analog ground plane, except for a connection at the least-noisy section of the power ground plane, typically the return of the input filter capacitor. The negative terminal of the filter capacitor, the ground return of the power switch, and current-sensing resistor must be close together. PCB layout also affects the thermal performance of the design. A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the part for efficient heat dissipation. For a sample layout that ensures first pass success, please refer to the MAX17598/MAX17599 Evaluation Kit layouts available at **www.maximintegrated.com**. For universal AC input designs, follow all applicable safety regulations. Offline power supplies can require UL, VDE, and other similar agency approvals.

Typical Application Circuits

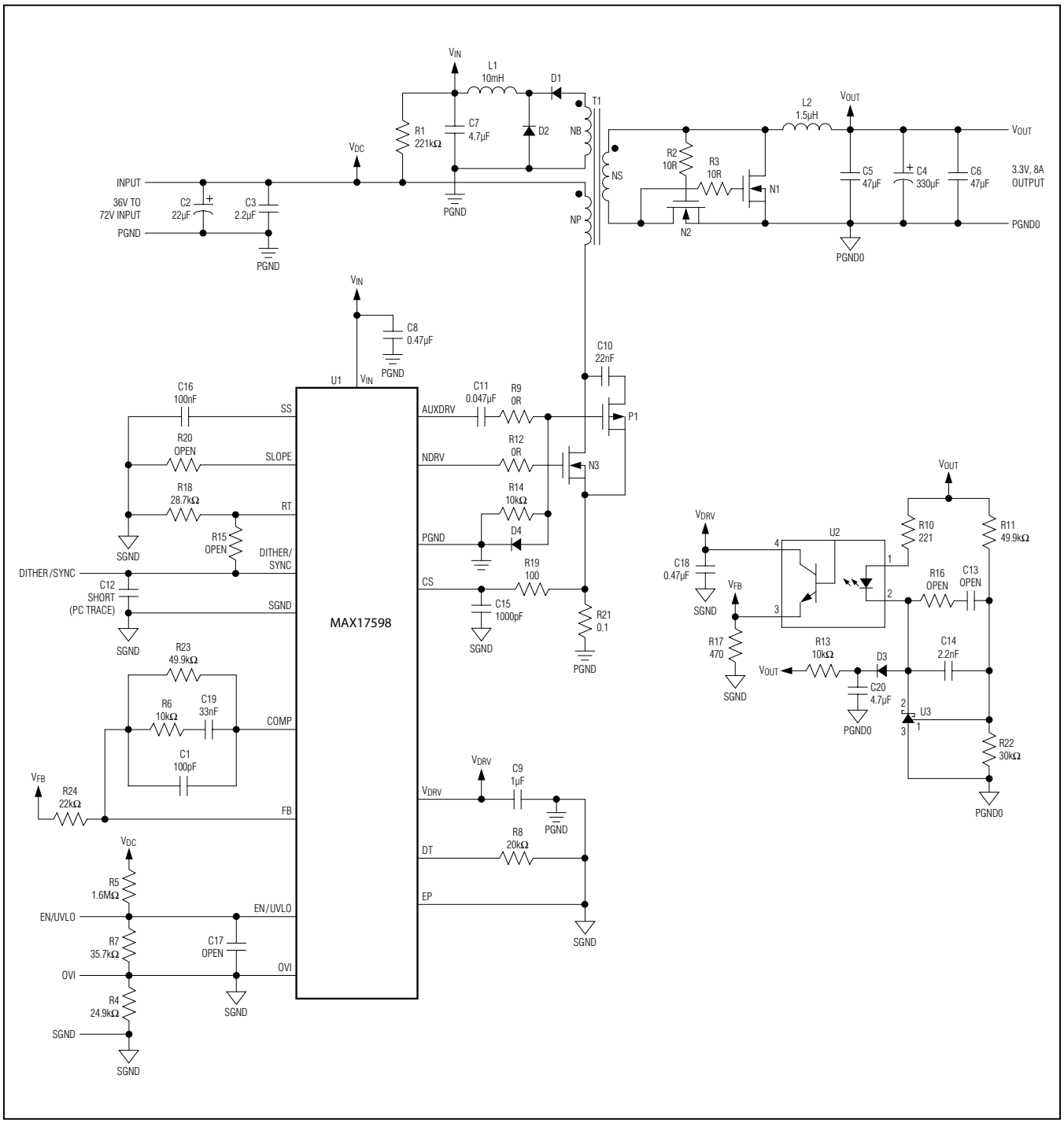


Figure 9. Typical Application Circuit (Telecom Power Supplies)

Typical Application Circuits (continued)

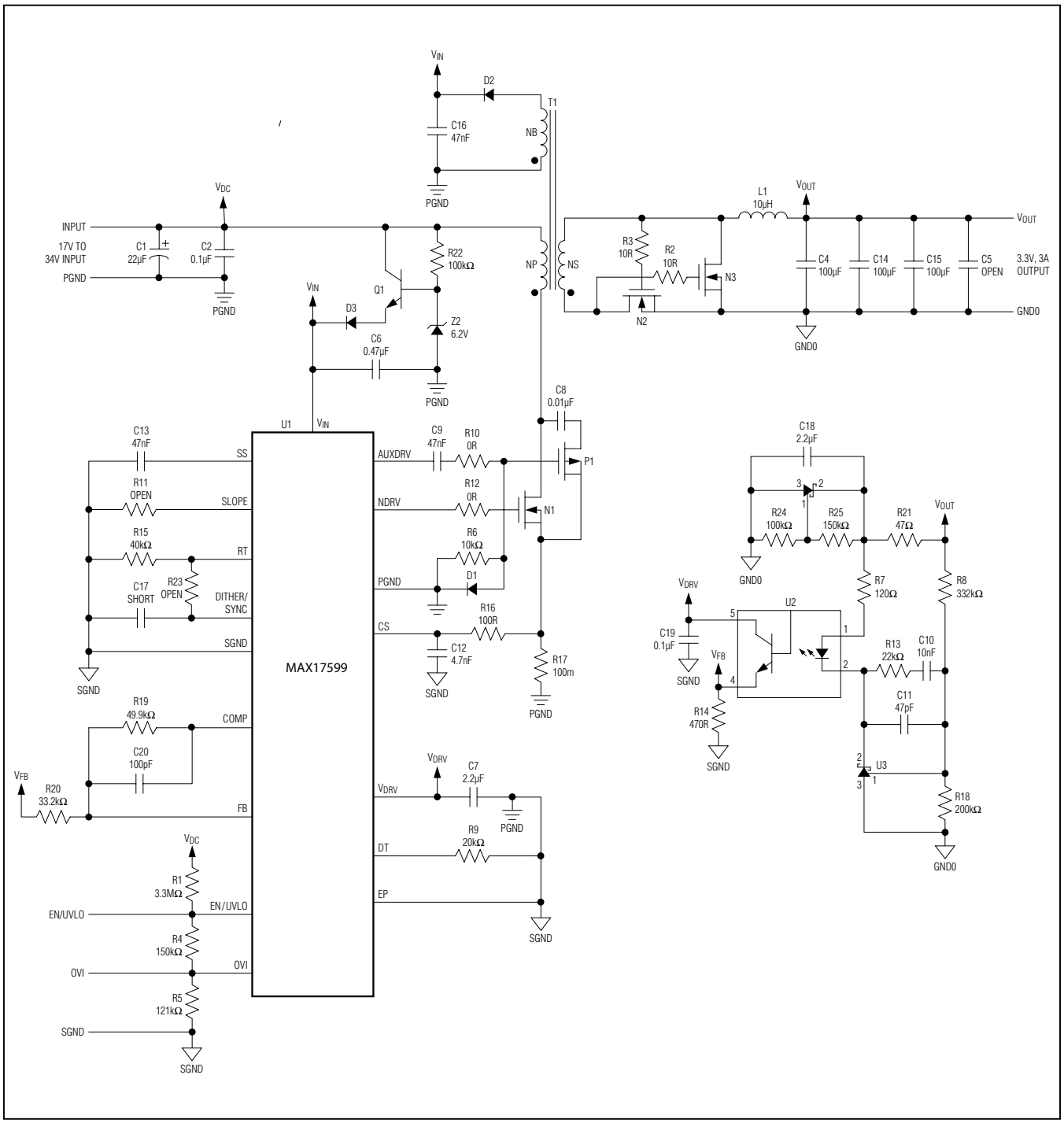


Figure 10. Typical Application Circuit (Power Supply for Low-Voltage DC-DC Applications)

Ordering Information

PART	TEMP RANGE	PIN PACKAGE	FUNCTIONALITY	UVLO, IN CLAMP	Dmax
MAX17598ATE+	-40°C to +125°C	16 TQFN	Active-clamp, peak-current-mode, offline PWM controller	20V, Yes	70%
MAX17599ATE+	-40°C to +125°C	16 TQFN	Active-clamp, peak-current-mode, PWM DC-DC controller	4V, No	70%

+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN	T1633+4	21-0136	90-0032

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/12	Initial release	—
1	3/13	Updated *General Description*, *Benefits and Features*, *Absolute Maximum Ratings*, *Electrical Characteristics*, *Typical Operating Characteristics*, *Pin Description*, *Detailed Description* sections, and Figures 1, 3–6, 8–10	1–23
2	4/14	R2 and R3 components values updated.	21-22

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