MSP430FG461x, MSP430CG461x Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- Low supply-voltage range: 1.8 V to 3.6 V
- Ultra-low power consumption
  - Active mode: 400 µA at 1 MHz, 2.2 V
  - Standby mode: 1.3 µA
  - Off mode (RAM retention): 0.22 µA
- Five power-saving modes
- Wakeup from standby mode in less than 6 µs
- 16-bit RISC architecture, extended memory, 125-ns instruction cycle time
- Three-channel internal DMA
- 12-bit analog-to-digital converter (ADC) with internal reference, sample-and-hold and autoscan feature
- Three configurable operational amplifiers
- Dual 12-bit digital-to-analog converters (DACs) with synchronization
- 16-bit Timer_A with three capture/compare registers
- 16-bit Timer_B with seven capture/compare-with-shadow registers
- On-chip comparator
- Supply voltage supervisor and monitor with programmable level detection
- Serial communication interface (USART1), select asynchronous UART or synchronous SPI by software
- Universal serial communication interface
  - Enhanced UART supports automatic baud-rate detection
  - IrDA encoder and decoder
  - Synchronous SPI
  - I^{2}C
- Serial onboard programming, programmable code protection by security fuse
- Brownout detector
- Basic timer with real-time clock (RTC) feature
- Integrated LCD driver up to 160 segments with regulated charge pump
- Device Comparison summarizes the available family members
  - MSP430FG4616, MSP430FG4616, 92KB+256B of flash or ROM, 4KB of RAM
  - MSP430FG4617, MSP430CG4617, 92KB+256B of flash or ROM, 8KB of RAM
  - MSP430FG4618, MSP430CG4618, 116KB+256B of flash or ROM, 8KB of RAM
  - MSP430FG4619, MSP430CG4619, 120KB+256B of flash or ROM, 4KB of RAM

1.2 Applications

- Portable medical applications
- E-meter applications

1.3 Description

The TI MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in less than 6 µs.

The MSP430xG461x series are microcontroller configurations with two 16-bit timers, a high-performance 12-bit ADC, dual 12-bit DACs, three configurable operational amplifiers, one universal serial communication interface (USCI), one universal synchronous/asynchronous communication interface (USART), DMA, 80 I/O pins, and a segment liquid crystal display (LCD) driver with regulated charge pump.

For complete module descriptions, see the *MSP430x4xx Family User's Guide*.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE(2)
MSP430FG4619IPZ	LQFP (100)	14 mm × 14 mm
MSP430FG4619IZCA	nFBGA (113)	7 mm × 7 mm
MSP430FG4619IZQW(3)	MicroStar Junior™ BGA (113)	7 mm × 7 mm

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.

(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 8.

(3) All orderable part numbers in the ZQW (MicroStar Junior BGA) package have been changed to a status of Last Time Buy. Visit the Product life cycle page for details on this status.

1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram.

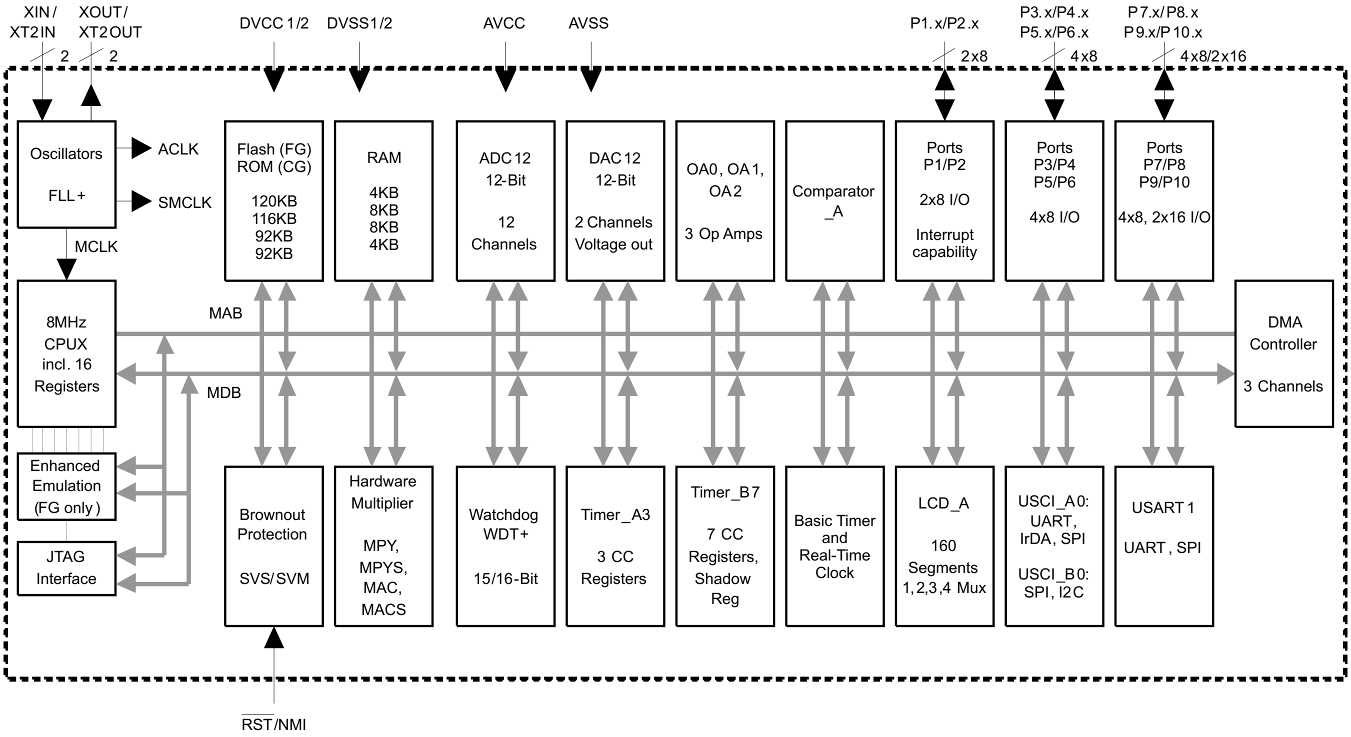


Figure 1-1. Functional Block Diagram

Table of Contents

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from June 20, 2015 to May 4, 2020	Page
• Throughout the document, added the ZCA package	1
• Changed the status of all orderable part numbers in the ZQW package	2

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Device Comparison (1) (2)

DEVICE	FLASH (KB)	ROM (KB)	RAM (KB)	EEM	Timer_A	Timer_B	ADC12 (Channels)	OP AMP	DAC12 (Channels)	COMP_A (Channels)	USART	USCI	I/O	PACKAGE
MSP430FG4619	120	–	4	1	TA3	TB7	12	3	2	2	1	A0, B0	80	PZ 100 ZCA 113 ZQW 113
MSP430FG4618	116	–	8	1	TA3	TB7	12	3	2	2	1	A0, B0	80	PZ 100 ZCA 113 ZQW 113
MSP430FG4617	92	–	8	1	TA3	TB7	12	3	2	2	1	A0, B0	80	PZ 100 ZCA 113 ZQW 113
MSP430FG4616	92	–	4	1	TA3	TB7	12	3	2	2	1	A0, B0	80	PZ 100 ZCA 113 ZQW 113
MSP430CG4619	–	120	4	–	TA3	TB7	12	3	2	2	1	A0, B0	80	PZ 100 ZQW 113 (3)
MSP430CG4618	–	116	8	–	TA3	TB7	12	3	2	2	1	A0, B0	80	PZ 100 ZQW 113 (3)
MSP430CG4617	–	92	8	–	TA3	TB7	12	3	2	2	1	A0, B0	80	PZ 100 ZQW 113 (3)
MSP430CG4616	–	92	4	–	TA3	TB7	12	3	2	2	1	A0, B0	80	PZ 100 ZQW 113 (3)

(1) For the most current device, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) All orderable part numbers in the ZQW (MicroStar Junior BGA) package have been changed to a status of Last Time Buy. Visit the Product life cycle page for details on this status.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout for the 100-pin PZ package.

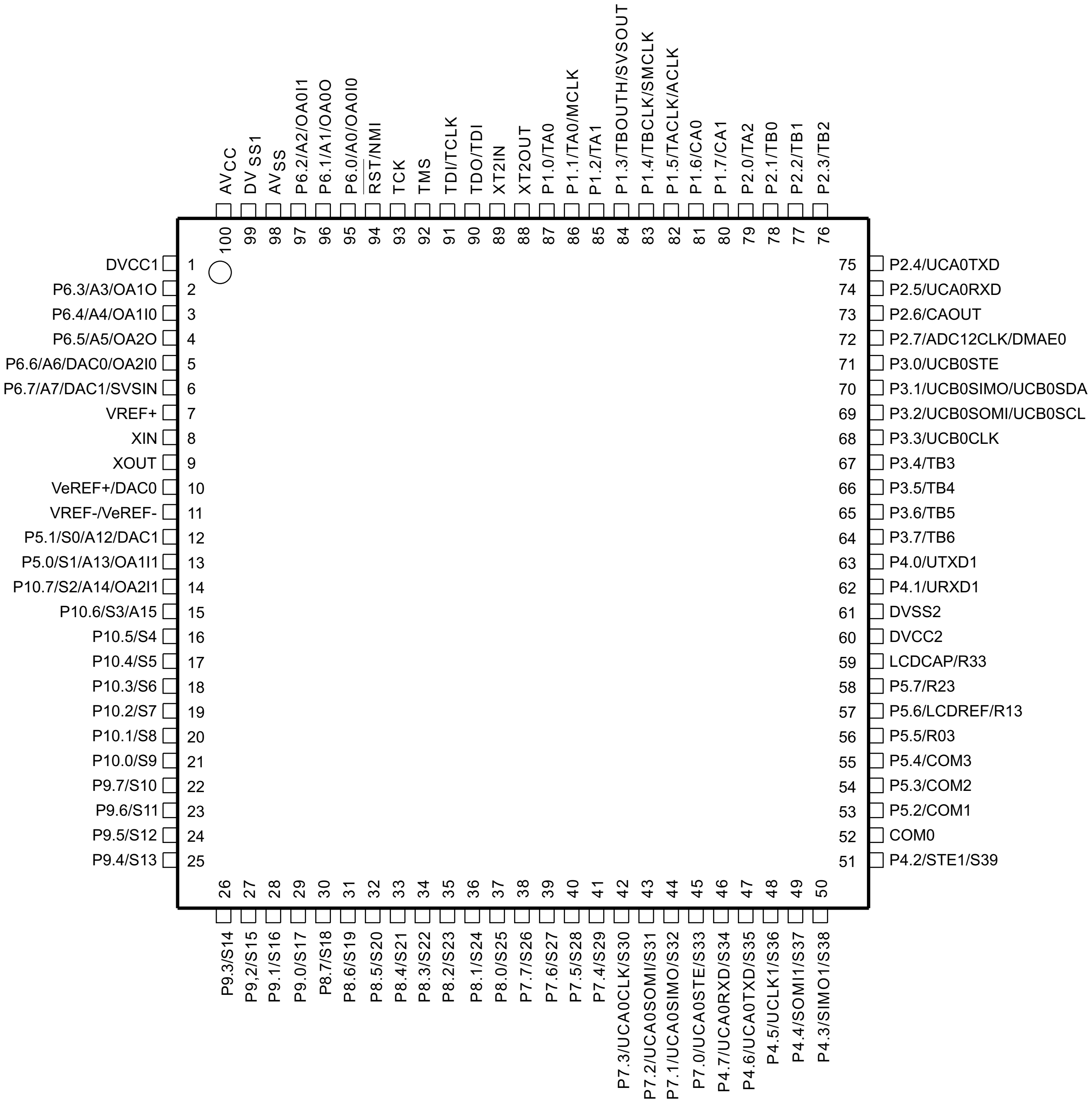
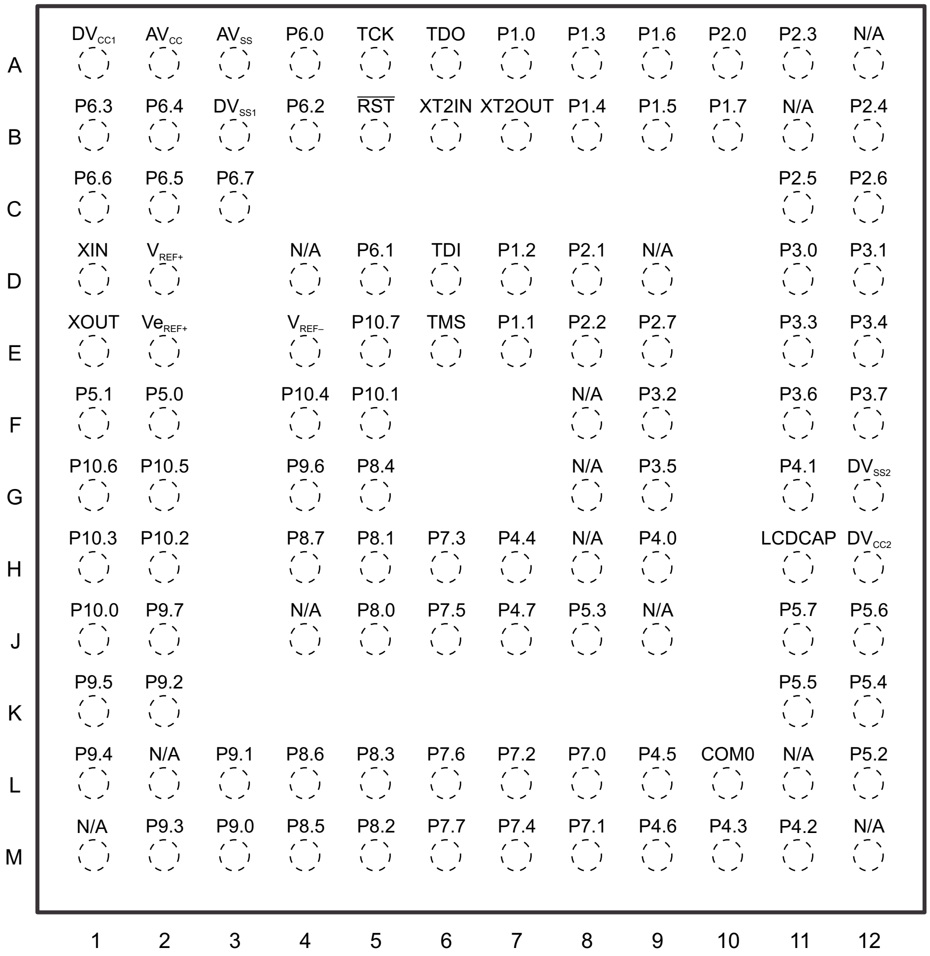


Figure 4-1. 100-Pin PZ Package (Top View)

Figure 4-2 shows the pinout for the 113-pin ZCA and ZQW packages. This figure shows only the default pin assignments; for all pin assignments, see Table 4-1.



	1	2	3	4	5	6	7	8	9	10	11	12
A	DV_{CC1}	AV_{CC}	AV_{SS}	P6.0	TCK	TDO	P1.0	P1.3	P1.6	P2.0	P2.3	N/A
B	P6.3	P6.4	DV_{SS1}	P6.2	$\overline{RST}$	XT2IN	XT2OUT	P1.4	P1.5	P1.7	N/A	P2.4
C	P6.6	P6.5	P6.7								P2.5	P2.6
D	XIN	V_{REF+}		N/A	P6.1	TDI	P1.2	P2.1	N/A		P3.0	P3.1
E	XOUT	Ve_{REF+}		V_{REF-}	P10.7	TMS	P1.1	P2.2	P2.7		P3.3	P3.4
F	P5.1	P5.0		P10.4	P10.1			N/A	P3.2		P3.6	P3.7
G	P10.6	P10.5		P9.6	P8.4			N/A	P3.5		P4.1	DV_{SS2}
H	P10.3	P10.2		P8.7	P8.1	P7.3	P4.4	N/A	P4.0		LCDCAP	DV_{CC2}
J	P10.0	P9.7		N/A	P8.0	P7.5	P4.7	P5.3	N/A		P5.7	P5.6
K	P9.5	P9.2									P5.5	P5.4
L	P9.4	N/A	P9.1	P8.6	P8.3	P7.6	P7.2	P7.0	P4.5	COM0	N/A	P5.2
M	N/A	P9.3	P9.0	P8.5	P8.2	P7.7	P7.4	P7.1	P4.6	P4.3	P4.2	N/A

N/A = Not Assigned. All unassigned ball locations on the ZCA or ZQW package should be electrically tied to the ground supply. The shortest ground return path to the device should be established to ball location B3, DV_{SS1}.

Figure 4-2. 113-Pin ZCA and ZQW Packages (Top View)

4.2 Signal Descriptions

Table 4-1 describes the signals for all device variants and package options.

Table 4-1. Signal Descriptions

SIGNAL NAME	PIN NO.		I/O	DESCRIPTION
	PZ	ZCA, ZQW		
DV_{CC1}	1	A1		Digital supply voltage, positive terminal
P6.3 A3 OA1O	2	B1	I/O	General-purpose digital I/O Analog input A3 for 12-bit ADC OA1 output
P6.4 A4 OA1I0	3	B2	I/O	General-purpose digital I/O Analog input A4 for 12-bit ADC OA1 input multiplexer on + terminal and – terminal
P6.5 A5 OA2O	4	C2	I/O	General-purpose digital I/O Analog input A5 for 12-bit ADC OA2 output
P6.6 A6 DAC0 OA2I0	5	C1	I/O	General-purpose digital I/O Analog input A6 for 12-bit ADC DAC12.0 output OA2 input multiplexer on + terminal and – terminal
P6.7 A7 DAC1 SVSIN	6	C3	I/O	General-purpose digital I/O Analog input A7 for 12-bit ADC DAC12.1 output Analog input to brownout, supply voltage supervisor
V_{REF+}	7	D2	O	Output of positive terminal of the reference voltage in the ADC
XIN	8	D1	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	E1	O	Output terminal of crystal oscillator XT1
Ve_{REF+} DAC0	10	E2	I/O	Input for an external reference voltage to the ADC DAC12.0 output
V_{REF} Ve_{REF-}	11	E4	I	Internal reference voltage, negative terminal for the ADC reference voltage External applied reference voltage, negative terminal for the ADC reference voltage
P5.1 S0(1) A12 DAC1	12	F1	I/O	General-purpose digital I/O LCD segment output 0 Analog input A12 for 12-bit ADC DAC12.1 output
P5.0 S1(1) A13 OA1I1	13	F2	I/O	General-purpose digital I/O LCD segment output 1 Analog input A13 for 12-bit ADC OA1 input multiplexer on + terminal and – terminal
P10.7 S2(1) A14 OA2I1	14	E5	I/O	General-purpose digital I/O LCD segment output 2 Analog input A14 for 12-bit ADC OA2 input multiplexer on + terminal and – terminal
P10.6 S3(1) A15	15	G1	I/O	General-purpose digital I/O LCD segment output 3 Analog input A15 to 12-bit ADC

(1) Segments S0 through S3 are disabled when the LCD charge pump feature is enabled (LCDCPEN = 1) and, therefore, cannot be used together with the LCD charge pump. On the MSP430xG461x devices only, S0 through S3 are also disabled if VLCDEXT = 1. This setting is typically used to apply an external LCD voltage supply to the LCDCAP terminal. For these devices, set LCDCPEN = 0, VLCDEXT = 0, and VLCDx > 0 to enable an external LCD voltage supply to be applied to the LCDCAP terminal.

Table 4-1. Signal Descriptions (continued)

SIGNAL NAME	PIN NO.		I/O	DESCRIPTION
	PZ	ZCA, ZQW		
P10.5 S4	16	G2	I/O	General-purpose digital I/O LCD segment output 4
P10.4 S5	17	F4	I/O	General-purpose digital I/O LCD segment output 5
P10.3 S6	18	H1	I/O	General-purpose digital I/O LCD segment output 6
P10.2 S7	19	H2	I/O	General-purpose digital I/O LCD segment output 7
P10.1 S8	20	F5	I/O	General-purpose digital I/O LCD segment output 8
P10.0 S9	21	J1	I/O	General-purpose digital I/O LCD segment output 9
P9.7 S10	22	J2	I/O	General-purpose digital I/O LCD segment output 10
P9.6 S11	23	G4	I/O	General-purpose digital I/O LCD segment output 11
P9.5 S12	24	K1	I/O	General-purpose digital I/O LCD segment output 12
P9.4 S13	25	L1	I/O	General-purpose digital I/O LCD segment output 13
P9.3 S14	26	M2	I/O	General-purpose digital I/O LCD segment output 14
P9.2 S15	27	K2	I/O	General-purpose digital I/O LCD segment output 15
P9.1 S16	28	L3	I/O	General-purpose digital I/O LCD segment output 16
P9.0 S17	29	M3	I/O	General-purpose digital I/O LCD segment output 17
P8.7 S18	30	H4	I/O	General-purpose digital I/O LCD segment output 18
P8.6 S19	31	L4	I/O	General-purpose digital I/O LCD segment output 19
P8.5 S20	32	M4	I/O	General-purpose digital I/O LCD segment output 20
P8.4 S21	33	G5	I/O	General-purpose digital I/O LCD segment output 21
P8.3 S22	34	L5	I/O	General-purpose digital I/O LCD segment output 22
P8.2 S23	35	M5	I/O	General-purpose digital I/O LCD segment output 23
P8.1 S24	36	H5	I/O	General-purpose digital I/O LCD segment output 24
P8.0 S25	37	J5	I/O	General-purpose digital I/O LCD segment output 25
P7.7 S26	38	M6	I/O	General-purpose digital I/O LCD segment output 26

Table 4-1. Signal Descriptions (continued)

SIGNAL NAME	PIN NO.		I/O	DESCRIPTION
	PZ	ZCA, ZQW		
P7.6 S27	39	L6	I/O	General-purpose digital I/O LCD segment output 27
P7.5 S28	40	J6	I/O	General-purpose digital I/O LCD segment output 28
P7.4 S29	41	M7	I/O	General-purpose digital I/O LCD segment output 29
P7.3 UCA0CLK S30	42	H6	I/O	General-purpose digital I/O External clock input – USCI_A0 in UART or SPI mode, Clock output – USCI_A0 in SPI mode LCD segment 30
P7.2 UCA0SOMI S31	43	L7	I/O	General-purpose digital I/O Slave out/master in of USCI_A0 in SPI mode LCD segment output 31
P7.1 UCA0SIMO S32	44	M8	I/O	General-purpose digital I/O Slave in/master out of USCI_A0 in SPI mode LCD segment output 32
P7.0 UCA0STE S33	45	L8	I/O	General-purpose digital I/O Slave transmit enable – USCI_A0 in SPI mode LCD segment output 33
P4.7 UCA0RXD S34	46	J7	I/O	General-purpose digital I/O Receive data in – USCI_A0 in UART or IrDA mode LCD segment output 34
P4.6 UCA0TXD S35	47	M9	I/O	General-purpose digital I/O Transmit data out – USCI_A0 in UART or IrDA mode LCD segment output 35
P4.5 UCLK1 S36	48	L9	I/O	General-purpose digital I/O External clock input – USART1 in UART or SPI mode, Clock output – USART1 in SPI MODE LCD segment output 36
P4.4 SOMI1 S37	49	H7	I/O	General-purpose digital I/O Slave out/master in of USART1 in SPI mode LCD segment output 37
P4.3 SIMO1 S38	50	M10	I/O	General-purpose digital I/O Slave in/master out of USART1 in SPI mode LCD segment output 38
P4.2 STE1 S39	51	M11	I/O	General-purpose digital I/O Slave transmit enable – USART1 in SPI mode LCD segment output 39
COM0	52	L10	O	Common output, COM0 for LCD backplanes
P5.2 COM1	53	L12	I/O	General-purpose digital I/O Common output, COM1 for LCD backplanes
P5.3 COM2	54	J8	I/O	General-purpose digital I/O Common output, COM2 for LCD backplanes
P5.4 COM3	55	K12	I/O	General-purpose digital I/O Common output, COM3 for LCD backplanes

Table 4-1. Signal Descriptions (continued)

SIGNAL NAME	PIN NO.		I/O	DESCRIPTION
	PZ	ZCA, ZQW		
P5.5 R03	56	K11	I/O	General-purpose digital I/O Input port of lowest analog LCD level (V5)
P5.6 LCDREF R13	57	J12	I/O	General-purpose digital I/O External reference voltage input for regulated LCD voltage Input port of third most positive analog LCD level (V4 or V3)
P5.7 R23	58	J11	I/O	General-purpose digital I/O Input port of second most positive analog LCD level (V2)
LCDCAP R33	59	H11	I	LCD capacitor connection Input/output port of most positive analog LCD level (V1)
DV_{CC2}	60	H12		Digital supply voltage, positive terminal
DV_{SS2}	61	G12		Digital supply voltage, negative terminal
P4.1 URXD1	62	G11	I/O	General-purpose digital I/O Receive data in – USART1 in UART mode
P4.0 UTXD1	63	H9	I/O	General-purpose digital I/O Transmit data out – USART1 in UART mode
P3.7 TB6	64	F12	I/O	General-purpose digital I/O Timer_B7 CCR6. Capture: CCI6A/CCI6B input, compare: Out6 output
P3.6 TB5	65	F11	I/O	General-purpose digital I/O Timer_B7 CCR5. Capture: CCI5A/CCI5B input, compare: Out5 output
P3.5 TB4	66	G9	I/O	General-purpose digital I/O Timer_B7 CCR4. Capture: CCI4A/CCI4B input, compare: Out4 output
P3.4 TB3	67	E12	I/O	General-purpose digital I/O Timer_B7 CCR3. Capture: CCI3A/CCI3B input, compare: Out3 output
P3.3 UCB0CLK	68	E11	I/O	General-purpose digital I/O External clock input – USCI_B0 in UART or SPI mode, Clock output – USCI_B0 in SPI mode
P3.2 UCB0SOMI UCB0SCL	69	F9	I/O	General-purpose digital I/O Slave out/master in of USCI_B0 in SPI mode I^2C clock – USCI_B0 in I^2C mode
P3.1 UCB0SIMO UCB0SDA	70	D12	I/O	General-purpose digital I/O Slave in/master out of USCI_B0 in SPI mode I^2C data – USCI_B0 in I^2C mode
P3.0 UCB0STE	71	D11	I/O	General-purpose digital I/O Slave transmit enable – USCI_B0 in SPI mode
P2.7 ADC12CLK DMAE0	72	E9	I/O	General-purpose digital I/O Conversion clock for 12-bit ADC DMA channel 0 external trigger
P2.6 CAOUT	73	C12	I/O	General-purpose digital I/O Comparator_A output
P2.5 UCA0RXD	74	C11	I/O	General-purpose digital I/O Receive data in – USCI_A0 in UART or IrDA mode
P2.4 UCA0TXD	75	B12	I/O	General-purpose digital I/O Transmit data out – USCI_A0 in UART or IrDA mode
P2.3 TB2	76	A11	I/O	General-purpose digital I/O Timer_B7 CCR2. Capture: CCI2A/CCI2B input, compare: Out2 output

Table 4-1. Signal Descriptions (continued)

SIGNAL NAME	PIN NO.		I/O	DESCRIPTION
	PZ	ZCA, ZQW		
P2.2 TB1	77	E8	I/O	General-purpose digital I/O Timer_B7 CCR1. Capture: CCI1A/CCI1B input, compare: Out1 output
P2.1 TB0	78	D8	I/O	General-purpose digital I/O Timer_B7 CCR0. Capture: CCI0A/CCI0B input, compare: Out0 output
P2.0 TA2	79	A10	I/O	General-purpose digital I/O Timer_A Capture: CCI2A input, compare: Out2 output
P1.7 CA1	80	B10	I/O	General-purpose digital I/O Comparator_A input
P1.6 CA0	81	A9	I/O	General-purpose digital I/O Comparator_A input
P1.5 TACLK ACLK	82	B9	I/O	General-purpose digital I/O Timer_A, clock signal TACLK input ACLK output (divided by 1, 2, 4, or 8)
P1.4 TBCLK SMCLK	83	B8	I/O	General-purpose digital I/O Input clock TBCLK – Timer_B7 Submain system clock SMCLK output
P1.3 TBOUTH SVSOUT	84	A8	I/O	General-purpose digital I/O Switch all PWM digital output ports to high impedance – Timer_B7 TB0 to TB6 SVS: output of SVS comparator
P1.2 TA1	85	D7	I/O	General-purpose digital I/O Timer_A, Capture: CCI1A input, compare: Out1 output
P1.1 TA0 MCLK	86	E7	I/O	General-purpose digital I/O Timer_A. Capture: CCI0B input. Note: TA0 is only an input on this pin. BSL receive. MCLK output
P1.0 TA0	87	A7	I/O	General-purpose digital I/O Timer_A. Capture: CCI0A input, compare: Out0 output. BSL transmit.
XT2OUT	88	B7	O	Output terminal of crystal oscillator XT2
XT2IN	89	B6	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
TDO TDI	90	A6	I/O	Test data output port. TDO/TDI data output. Programming data input terminal
TDI TCLK	91	D6	I	Test data input Test clock input. The device protection fuse is connected to TDI/TCLK.
TMS	92	E6	I	Test mode select. TMS is used as an input port for device programming and test.
TCK	93	A5	I	Test clock. TCK is the clock input port for device programming and test.
RST NMI	94	B5	I	Reset input Nonmaskable interrupt input port
P6.0 A0 OA0I0	95	A4	I/O	General-purpose digital I/O Analog input A0 for 12-bit ADC OA0 input multiplexer on + terminal and – terminal
P6.1 A1 OA0O	96	D5	I/O	General-purpose digital I/O Analog input A1 for 12-bit ADC OA0 output
P6.2 A2 OA0I1	97	B4	I/O	General-purpose digital I/O Analog input A2 for 12-bit ADC OA0 input multiplexer on + terminal and – terminal

Table 4-1. Signal Descriptions (continued)

SIGNAL NAME	PIN NO.		I/O	DESCRIPTION
	PZ	ZCA, ZQW		
AVSS	98	A3		Analog supply voltage, negative terminal. Supplies SVS, brownout, oscillator, Comparator_A, port 1
DV_{SS1}	99	B3		Digital supply voltage, negative terminal
AV_{CC}	100	A2		Analog supply voltage, positive terminal. Supplies SVS, brownout, oscillator, Comparator_A, port 1. Do not power up before powering DV_{CC1} and DV_{CC2}.
Not Assigned	–	A12, B11, D4, D9, F8, G8, H8, J4, J9, L2, L11, M1, M12	–	All unassigned ball locations on the ZCA and ZQW packages should be electrically tied to the ground supply. The shortest ground return path to the device should be established to ball location B3, DV_{SS1}.

5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}		–0.3	4.1	V
Voltage applied to any pin(2)		–0.3	V_{CC} + 0.3	V
Diode current at any device terminal			±2	mA
Storage temperature, T_{stg}	Unprogrammed device	–55	105	°C
	Programmed device	–40	85	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are referenced to V_{SS}.The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During program execution(1) ($AV_{CC} = DV_{CC1/2} = V_{CC}$)		1.8		3.6	V
		During flash memory programming (FG461x) ($AV_{CC} = DV_{CC1/2} = V_{CC}$)(1)		2.7		3.6	
		During program execution, SVS enabled and PORON = 1(1) ($AV_{CC} = DV_{CC1/2} = V_{CC}$)(2)		2		3.6	
V_{SS}	Supply voltage ($AV_{SS} = DV_{SS1/2} = V_{SS}$)			0		0	V
T_A	Operating free-air temperature range			–40		85	°C
$f_{(LFXT1)}$	Crystal frequency(3)	LF selected, XTS_FLL = 0(3)	Watch crystal		32.768		kHz
		XT1 selected, XTS_FLL = 1	Ceramic resonator	450		8000	
		XT1 selected, XTS_FLL = 1	Crystal	1000		8000	
$f_{(XT2)}$	Crystal frequency		Ceramic resonator	450		8000	kHz
			Crystal	1000		8000	
$f_{(System)}$	Processor frequency (signal MCLK)		V_{CC} = 1.8 V	DC		3	MHz
			V_{CC} = 2.0 V	DC		4.6	
			V_{CC} = 3.6 V	DC		8	

(1) TI recommends powering AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.

(2) The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing the supply voltage. POR is going inactive when the supply voltage is raised above the minimum supply voltage plus the hysteresis of the SVS circuitry.

(3) In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

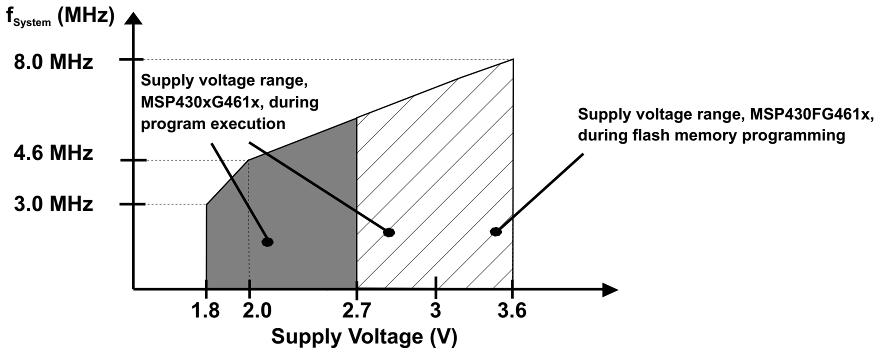


Figure 5-1. Frequency vs Supply Voltage

5.4 Supply Current Into AV_{CC} + DV_{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITION		MIN	TYP	MAX	UNIT
$I_{(AM)}$	Active mode[1] [2] $f_{(MCLK)} = f_{(SMCLK)} = 1$ MHz, $f_{(ACLK)} = 32768$ Hz, XTS = 0, SELM = (0, 1), (FG461x: program executes from flash)	CG461x	T_A = –40°C to 85°C	V_{CC} = 2.2 V		280	370	µA
				V_{CC} = 3 V		470	580	
		FG461x	T_A = –40°C to 85°C	V_{CC} = 2.2 V		400	480	
				V_{CC} = 3 V		600	740	
$I_{(LPM0)}$	Low power mode (LPM0)[1] [2]		T_A = –40°C to 85°C	V_{CC} = 2.2 V		45	70	µA
				V_{CC} = 3 V		75	110	
$I_{(LPM2)}$	Low-power mode (LPM2), $f_{(MCLK)} = f_{(SMCLK)} = 0$ MHz, $f_{(ACLK)} = 32768$ Hz, SCG0 = 0[3] [2]		T_A = –40°C to 85°C	V_{CC} = 2.2 V		11	20	µA
				V_{CC} = 3 V		17	24	
$I_{(LPM3)}$	Low-power mode (LPM3), $f_{(MCLK)} = f_{(SMCLK)} = 0$ MHz, $f_{(ACLK)} = 32768$ Hz, SCG0 = 1, Basic Timer1 enabled, ACLK selected, LCD_A enabled, LCDCPEN = 0, (static mode, $f_{LCD} = f_{(ACLK)}/32$)[3] [4] [2]		T_A = –40°C	V_{CC} = 2.2 V		1.3	4.0	µA
			T_A = 25°C			1.3	4.0	
			T_A = 60°C			2.22	6.5	
			T_A = 85°C			6.5	15.0	
			T_A = –40°C	V_{CC} = 3 V		1.9	5.0	
			T_A = 25°C			1.9	5.0	
			T_A = 60°C			2.5	7.5	
			T_A = 85°C			7.5	18.0	
$I_{(LPM3)}$	Low-power mode (LPM3), $f_{(MCLK)} = f_{(SMCLK)} = 0$ MHz, $f_{(ACLK)} = 32768$ Hz, SCG0 = 1, Basic Timer1 enabled, ACLK selected, LCD_A enabled, LCDCPEN = 0, (4-mux mode; $f_{LCD} = f_{(ACLK)}/32$)[3] [4] [2]		T_A = –40°C	V_{CC} = 2.2 V		1.5	5.5	µA
			T_A = 25°C			1.5	5.5	
			T_A = 60°C			2.8	7.0	
			T_A = 85°C			7.2	17.0	
			T_A = –40°C	V_{CC} = 3 V		2.5	6.5	
			T_A = 25°C			2.5	6.5	
			T_A = 60°C			3.2	8.0	
			T_A = 85°C			8.5	20.0	
$I_{(LPM4)}$	Low-power mode (LPM4), $f_{(MCLK)} = 0$ MHz, $f_{(SMCLK)} = 0$ MHz, $f_{(ACLK)} = 0$ Hz, SCG0 = 1[3] [2]		T_A = –40°C	V_{CC} = 2.2 V		0.13	1.0	µA
			T_A = 25°C			0.22	1.0	
			T_A = 60°C			0.9	2.5	
			T_A = 85°C			4.3	12.5	
			T_A = –40°C	V_{CC} = 3 V		0.13	1.6	
			T_A = 25°C			0.3	1.6	
			T_A = 60°C			1.1	3.0	
			T_A = 85°C			5.0	15.0	

(1) Timer_B is clocked by $f_{(DCOCLK)} = f_{(DCO)} = 1$ MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Current for brownout included.
(3) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(4) The LPM3 currents are characterized with a Micro Crystal CC4V-T1A (9 pF) crystal and OSCCAPx = 1h.

Current consumption of active mode versus system frequency, FG version:

$$I_{(AM)} = I_{(AM)\ [1\ MHz]} \times f_{(System)}\ [MHz]$$

Current consumption of active mode versus supply voltage, FG version:

$$I_{(AM)} = I_{(AM)\ [3\ V]} + 200\ \mu A/V \times (V_{CC} - 3\ V)$$

5.5 Thermal Characteristics

PARAMETER		PACKAGE	VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance, still air(1)	ZQW (BGA)	42	°C/W
$\theta_{JC,TOP}$	Junction-to-case (top) thermal resistance(2)		10	°C/W
θ_{JB}	Junction-to-board thermal resistance(3)		12	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		12	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.3	°C/W
θ_{JA}	Junction-to-ambient thermal resistance, still air(1)	PZ (PQFP-100)	43.5	°C/W
$\theta_{JC,TOP}$	Junction-to-case (top) thermal resistance(2)		6.2	°C/W
θ_{JB}	Junction-to-board thermal resistance(3)		21.8	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		21.2	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.2	°C/W

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

5.6 Schmitt-Trigger Inputs – Ports P1 to P10, $\overline{\text{RST}}$/NMI, JTAG (TCK, TMS, TDI/TCLK,TDO/TDI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1	1.55	V
		V_{CC} = 3 V	1.5	1.98	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4	0.9	V
		V_{CC} = 3 V	0.9	1.3	
V_{hys}	Input voltage hysteresis (V_{IT+} – V_{IT-})	V_{CC} = 2.2 V	0.3	1.1	V
		V_{CC} = 3 V	0.5	1	

5.7 Inputs Px.x, TAx, TBX

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag (1)	2.2 V	62		ns
			3 V	50		
$t_{(cap)}$	Timer_A, Timer_B capture timing	TA0, TA1, TA2 TB0, TB1, TB2, TB3, TB4, TB5, TB6	2.2 V	62		ns
			3 V	50		
$f_{(TAext)}$ $f_{(TBext)}$	Timer_A or Timer_B clock frequency externally applied to pin	TACLK, TBCLK INCLK $t_{(H)} = t_{(L)}$	2.2 V		8	MHz
			3 V		10	
$f_{(TAint)}$ $f_{(TBint)}$	Timer A or Timer B clock frequency	SMCLK or ACLK signal selected	2.2 V		8	MHz
			3 V		10	

(1) The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.

5.8 Leakage Current – Ports P1 to P10(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$I_{lkg(Px.y)}$	Leakage current, Port Px	V(Px.y) (2) (1 ≤ × ≤ 10, 0 ≤ y ≤ 7)	V_{CC} = 2.2 V, 3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The port pin must be selected as input.

5.9 Outputs – Ports P1 to P10

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –1.5 mA, V_{CC} = 2.2 V (1)	V_{CC} – 0.25	V_{CC}	V
		$I_{OH(max)}$ = –6 mA, V_{CC} = 2.2 V (2)	V_{CC} – 0.6	V_{CC}	
		$I_{OH(max)}$ = –1.5 mA, V_{CC} = 3 V (1)	V_{CC} – 0.25	V_{CC}	
		$I_{OH(max)}$ = –6 mA, V_{CC} = 3 V (2)	V_{CC} – 0.6	V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA, V_{CC} = 2.2 V (1)	V_{SS}	V_{SS} + 0.25	V
		$I_{OL(max)}$ = 6 mA, V_{CC} = 2.2 V (2)	V_{SS}	V_{SS} + 0.6	
		$I_{OL(max)}$ = 1.5 mA, V_{CC} = 3 V (1)	V_{SS}	V_{SS} + 0.25	
		$I_{OL(max)}$ = 6 mA, V_{CC} = 3 V (2)	V_{SS}	V_{SS} + 0.6	

(1) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
(2) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

5.10 Output Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(Px.y)}$	(1 ≤ × ≤ 10, 0 ≤ y ≤ 7)	C_L = 20 F, I_L = ±1.5 mA	V_{CC} = 2.2 V	DC		10	MHz
			V_{CC} = 3 V	DC		12	
$f_{(MCLK)}$ $f_{(SMCLK)}$	P1.1/TA0/MCLK P1.4/TBCLK/SMCLK	C_L = 20 pF	V_{CC} = 2.2 V			10	MHz
$f_{(ACLK)}$	P1.5/TACLK/ACLK		V_{CC} = 3 V	DC		12	
$t_{(Xdc)}$	Duty cycle of output frequency	P1.5/TACLK/ACLK, C_L = 20 pF, V_{CC} = 2.2 V, 3 V	$f_{(ACLK)} = f_{(LFXT1)} = f_{(XT1)}$	40%		60%	
			$f_{(ACLK)} = f_{(LFXT1)} = f_{(LF)}$	30%		70%	
			$f_{(ACLK)} = f_{(LFXT1)}$		50%		
		P1.1/TA0/MCLK, C_L = 20 pF, V_{CC} = 2.2 V, 3 V	$f_{(MCLK)} = f_{(XT1)}$	40%		60%	
			$f_{(MCLK)} = f_{(DCOCLK)}$	50% – 15 ns	50%	50%+ 15 ns	
		P1.4/TBCLK/SMCLK, C_L = 20 pF, V_{CC} = 2.2 V, 3 V	$f_{(SMCLK)} = f_{(XT2)}$	40%		60%	
			$f_{(SMCLK)} = f_{(DCOCLK)}$	50% – 15 ns	50%	50% + 15 ns	

5.11 Typical Characteristics – Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

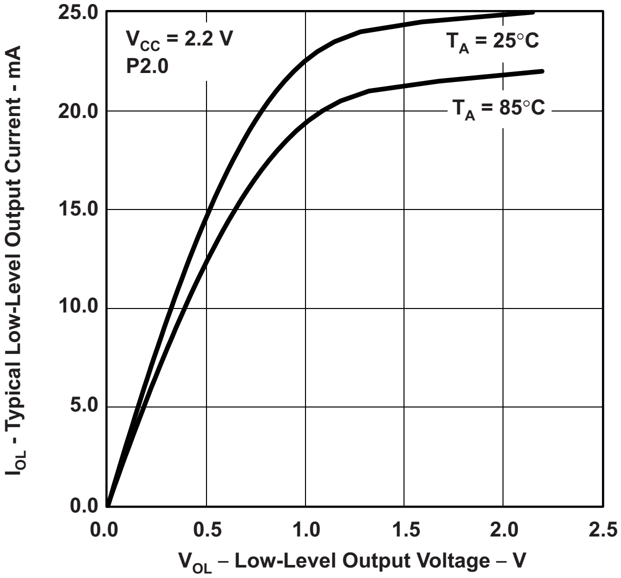


Figure 5-2. Typical Low-Level Output Current vs Typical Low-Level Output Current

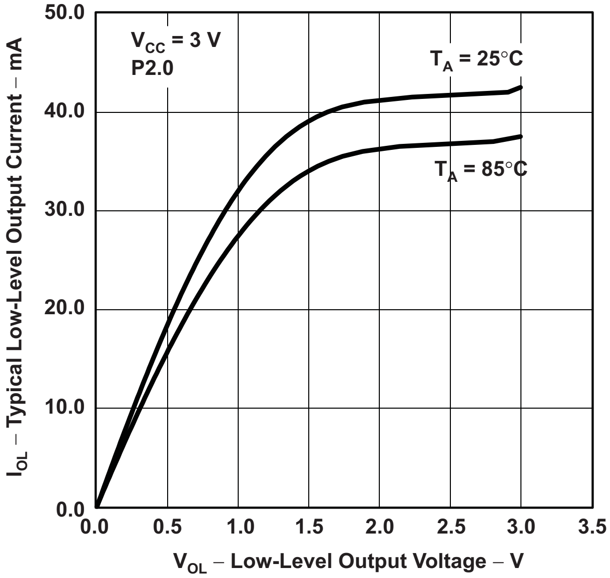


Figure 5-3. Typical Low-Level Output Current vs Typical Low-Level Output Current

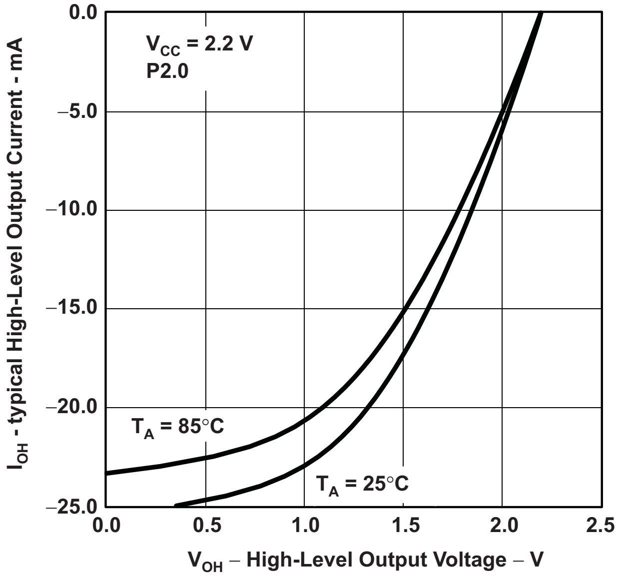


Figure 5-4. Typical High-Level Output Current vs Typical High-Level Output Current

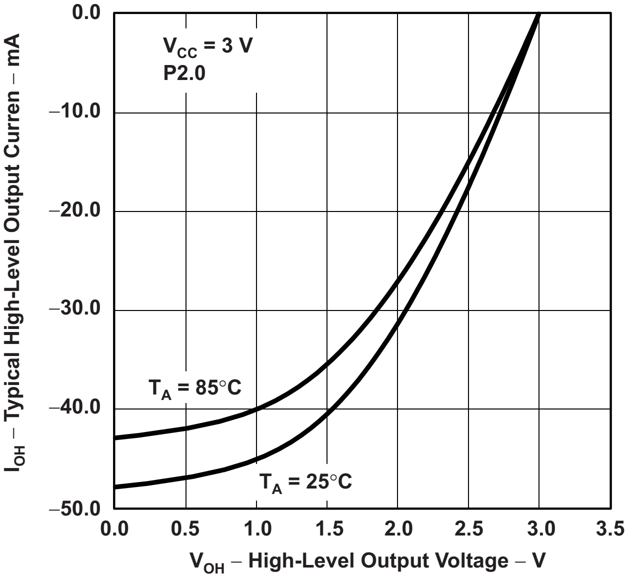


Figure 5-5. Typical High-Level Output Current vs Typical High-Level Output Current

5.12 Wake-up Timing From LPM3

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{d(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 2.2 V, 3 V		6	µs
		f = 2 MHz			6	
		f = 3 MHz			6	

5.13 RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VRAMh	CPU halted (1)	1.6		V

(1) This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

5.14 LCD_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(LCD)}$	Supply voltage (1)	Charge pump enabled (LCDCPEN = 1, VLCDx > 0000)		2.2		3.6	V
$I_{CC(LCD)}$	Supply current (1)	$V_{LCD(typ)}$ = 3 V, LCDCPEN = 1, VLCDx= 1000, all segments on, f_{LCD} = f_{ACLK}/32, no LCD connected (2), T_A = 25°C	2.2 V		3		µA
C_{LCD}	Capacitor on LCDCAP (3) (4)	Charge pump enabled (LCDCPEN = 1, VLCDx > 0000)		4.7			µF
f_{LCD}	LCD frequency					1.1	kHz
V_{LCD}	LCD voltage (4)	VLCDx = 0000			V_{CC}		V
		VLCDx = 0001			2.60		
		VLCDx = 0010			2.66		
		VLCDx = 0011			2.72		
		VLCDx = 0100			2.78		
		VLCDx = 0101			2.84		
		VLCDx = 0110			2.90		
		VLCDx = 0111			2.96		
		VLCDx = 1000			3.02		
		VLCDx = 1001			3.08		
		VLCDx = 1010			3.14		
		VLCDx = 1011			3.20		
		VLCDx = 1100			3.26		
		VLCDx = 1101			3.32		
		VLCDx = 1110			3.38		
		VLCDx = 1111			3.44	3.60	
R_{LCD}	LCD driver output impedance	V_{LCD}= 3 V, CPEN = 1, VLCDx = 1000, I_{LOAD} = ±10 µA	2.2 V			10	kΩ

(1) Refer to the supply current specifications $I_{(LPM3)}$ for additional current specifications with the LCD_A module active.
(2) Connecting an actual display increases the current consumption depending on the size of the LCD.
(3) Enabling the internal charge pump with an external capacitor smaller than the minimum specified might damage the device.
(4) Segments S0 through S3 are disabled when the LCD charge pump feature is enabled (LCDCPEN = 1) and, therefore, cannot be used together with the LCD charge pump. On the MSP430xG461x devices only, S0 through S3 are also disabled if VLCDEXT = 1. This setting is typically used to apply an external LCD voltage supply to the LCDCAP terminal. For these devices, set LCDCPEN = 0, VLCDEXT = 0, and VLCDx > 0 to enable an external LCD voltage supply to be applied to the LCDCAP terminal.

5.15 Comparator_A(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(CC)}$		CAON = 1, CARSEL = 0, CAREF = 0	2.2 V		25	40	µA
			3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = (1, 2, 3), No load at P1.6/CA0 and P1.7/CA1	2.2 V		30	50	µA
			3 V		45	71	
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{cc} \text{ node}}{V_{cc}}$	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P1.6/CA0 and P1.7/CA1	2.2 V, 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5 } V_{cc} \text{ node}}{V_{cc}}$	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P1.6/CA0 and P1.7/CA1	2.2 V, 3 V	0.47	0.48	0.5	
$V_{(RefVT)}$		PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P1.6/CA0 and P1.7/CA1, T_A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
V_{IC}	Common-mode input voltage range	CAON = 1	2.2 V, 3 V	0		V_{CC} – 1	V
$V_p – V_S$	Offset voltage(2)		2.2 V, 3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON = 1	2.2 V, 3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 0	2.2 V	160	210	300	ns
			3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 1	2.2 V	1.4	1.9	3.4	µs
			3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 0	2.2 V	130	210	300	ns
			3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 1	2.2 V	1.4	1.9	3.4	µs
			3 V	0.9	1.5	2.6	

(1) The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
(2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

5.16 Typical Characteristics – Comparator_A

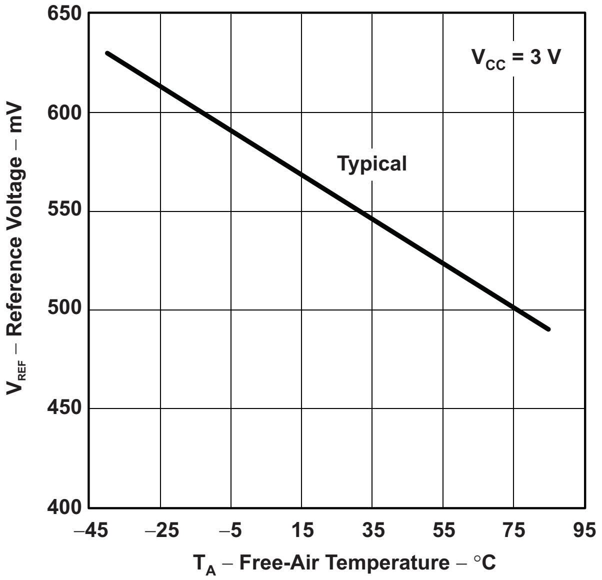


Figure 5-6. Reference Voltage vs Free-Air Temperature

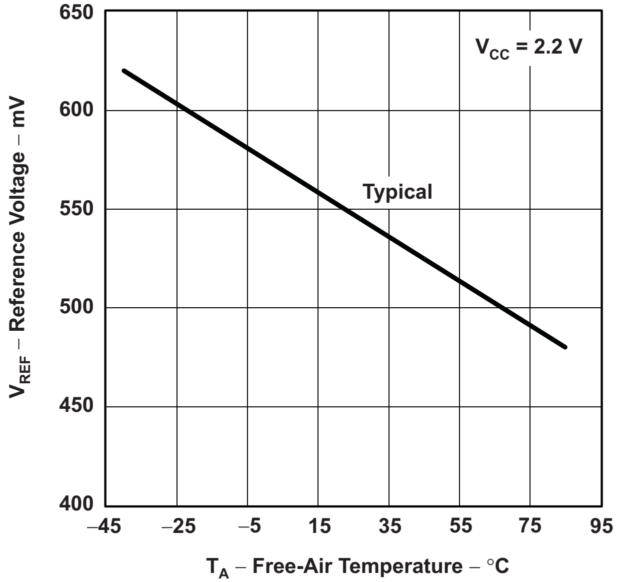


Figure 5-7. Reference Voltage vs Free-Air Temperature

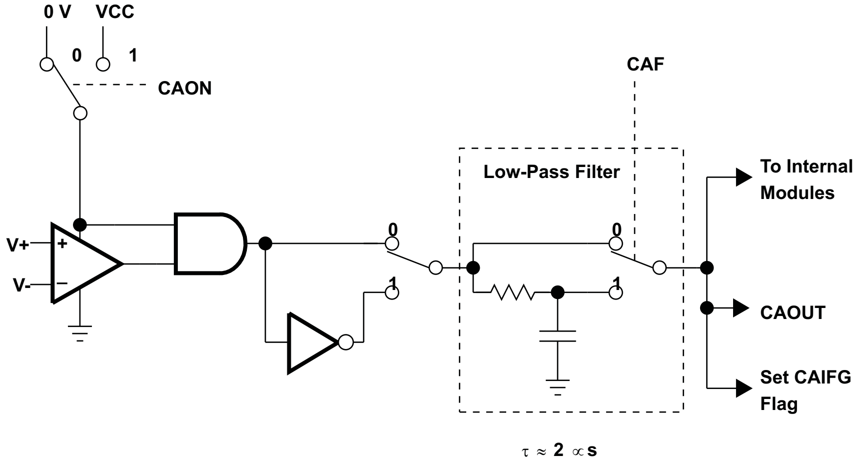


Figure 5-8. Block Diagram of Comparator_A Module

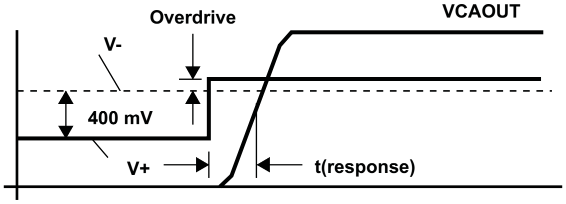


Figure 5-9. Overdrive Definition

5.17 POR, BOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout(2) (3)				2000	µs
$V_{CC(start)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 5-10)		0.7 × $V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 5-10 through Figure 5-12)			1.79	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 5-10)	70	130	210	mV
$t_{(reset)}$		Pulse duration needed at RST/NMI pin to accepted reset internally, V_{CC} = 2.2 V, 3 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data.
(2) The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)} \le 1.89$ V.
(3) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide* (SLAU056) for more information on the brownout and SVS circuit.

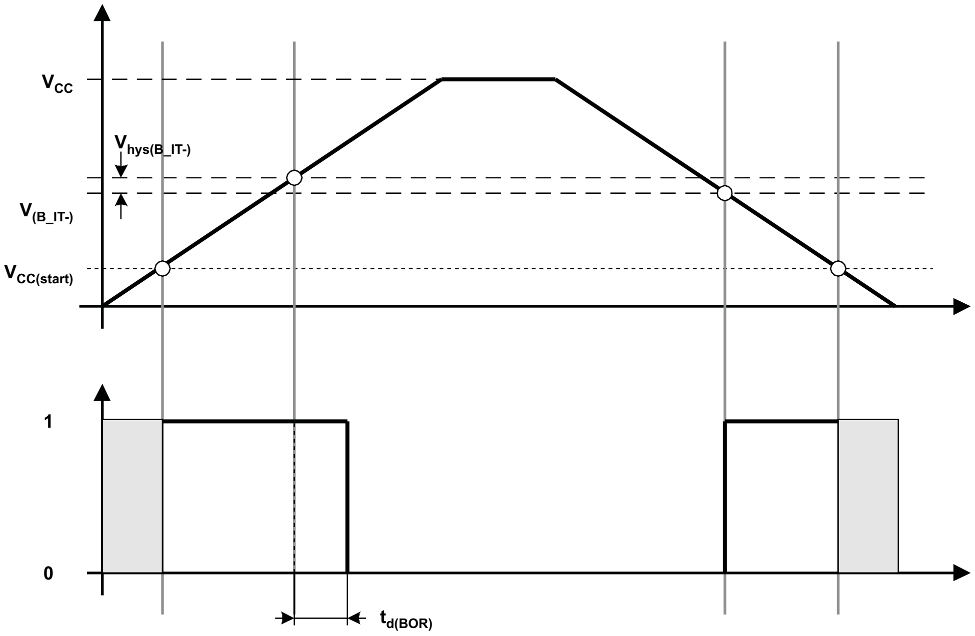


Figure 5-10. POR, BOR vs Supply Voltage

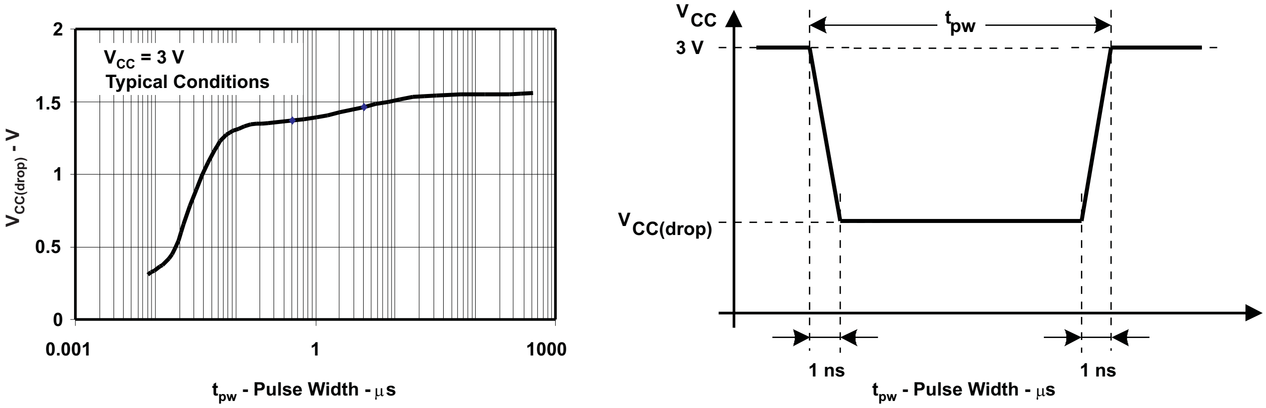


Figure 5-11. $V_{CC(drop)}$ Level with a Square Voltage Drop to Generate a POR or BOR Signal

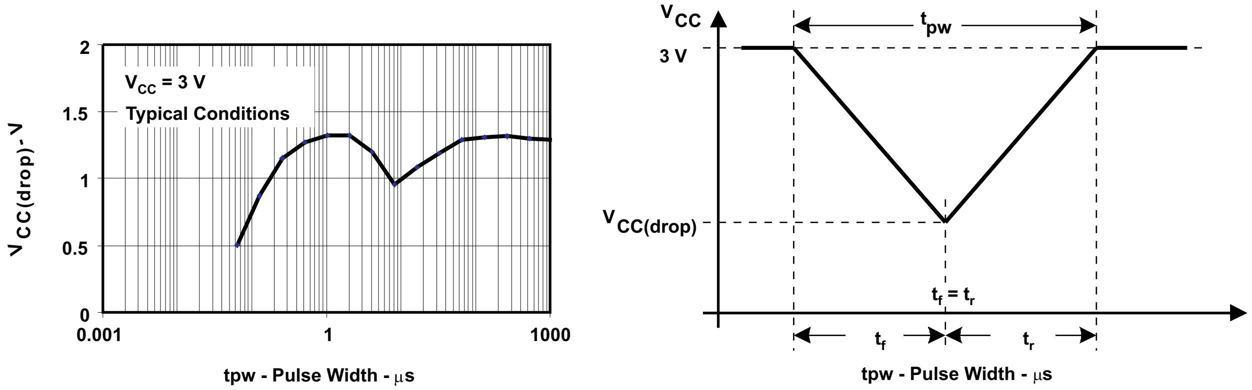


Figure 5-12. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR or BOR Signal

5.18 SVS (Supply Voltage Supervisor and Monitor)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(SVSR)}$	$dV_{CC}/dt > 30$ V/ms (see Figure 5-13)		5		150	µs
	$dV_{CC}/dt \leq 30$ V/ms				2000	
$t_{d(SVSon)}$	SVS on, switch from VLD = 0 to VLD ≠ 0, V_{CC} = 3 V			150	300	µs
t_{settle}	VLD ≠ 0 (1)				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \leq 3$ V/s (see Figure 5-13)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	$V_{CC}/dt \leq 3$ V/s (see Figure 5-13)	VLD = 1	70	120	155	mV
		VLD = 2 to 14	$V_{(SVS\_IT-)}$ × 0.001		$V_{(SVS\_IT-)}$ × 0.016	
	$V_{CC}/dt \leq 3$ V/s (see Figure 5-13), external voltage applied on A7	VLD = 15	4.4		20	mV
$V_{(SVS\_IT-)}$	$V_{CC}/dt \leq 3$ V/s (see Figure 5-13)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.23	
		VLD = 3	2.05	2.2	2.35	
		VLD = 4	2.14	2.3	2.46	
		VLD = 5	2.24	2.4	2.58	
		VLD = 6	2.33	2.5	2.69	
		VLD = 7	2.46	2.65	2.84	
		VLD = 8	2.58	2.8	2.97	
		VLD = 9	2.69	2.9	3.10	
		VLD = 10	2.83	3.05	3.26	
		VLD = 11	2.94	3.2	3.39	
		VLD = 12	3.11	3.35	3.58 (2)	
		VLD = 13	3.24	3.5	3.73 (2)	
		VLD = 14	3.43	3.7 (2)	3.96 (2)	
	$V_{CC}/dt \leq 3$ V/s (see Figure 5-13), external voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (3)	VLD ≠ 0, V_{CC} = 2.2 V, 3 V			10	15	µA

(1) t_{settle} is the settling time that the comparator output needs to have a stable level after VLD is switched from VLD ≠ 0 to a different VLD value from 2 to 15. The overdrive is assumed to be > 50 mV.
(2) The recommended operating voltage range is limited to 3.6 V.
(3) The current consumption of the SVS module is not included in the I_{CC} current consumption data.

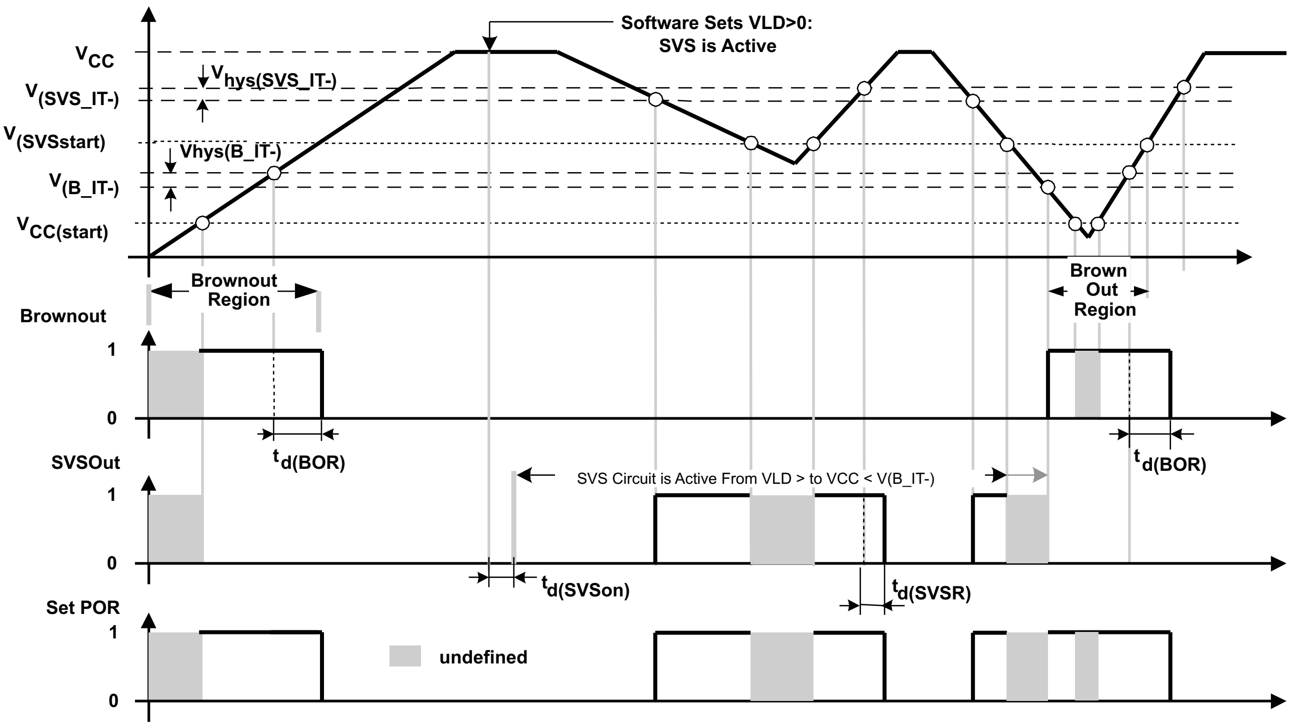


Figure 5-13. SVS Reset (SVSR) vs Supply Voltage

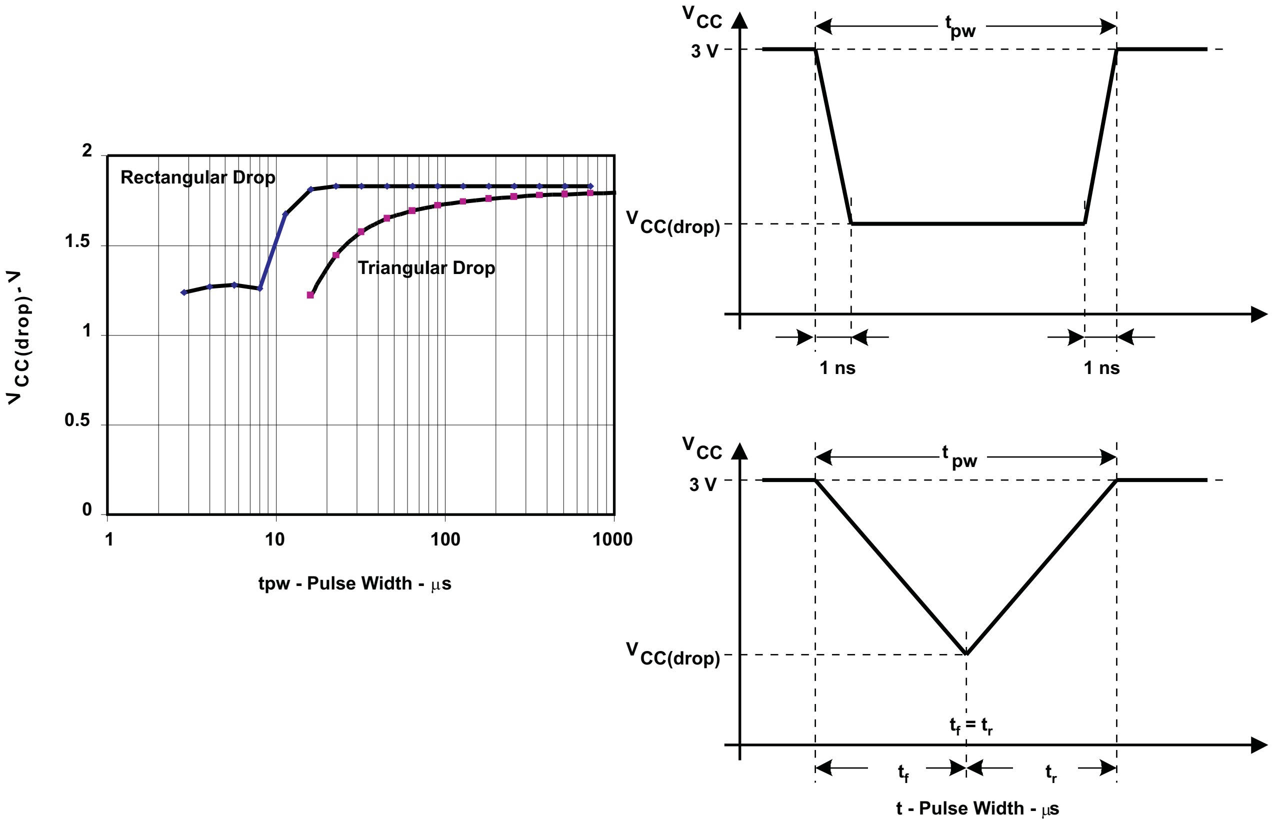


Figure 5-14. $V_{CC(drop)}$ with a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal

5.19 DCO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0	2.2 V, 3 V		1		MHz
$f_{(DCO = 2)}$	FN_8 = FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1	2.2 V	0.3	0.65	1.25	MHz
		3 V	0.3	0.7	1.3	
$f_{(DCO = 27)}$	FN_8 = FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1	2.2 V	2.5	5.6	10.5	MHz
		3 V	2.7	6.1	11.3	
$f_{(DCO = 2)}$	FN_8 = FN_4 = FN_3 = FN_2 = 1, DCOPLUS = 1	2.2 V	0.7	1.3	2.3	MHz
		3 V	0.8	1.5	2.5	
$f_{(DCO = 27)}$	FN_8 = FN_4 = FN_3 = FN_2 = 1, DCOPLUS = 1	2.2 V	5.7	10.8	18	MHz
		3 V	6.5	12.1	20	
$f_{(DCO = 2)}$	FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1	2.2 V	1.2	2	3	MHz
		3 V	1.3	2.2	3.5	
$f_{(DCO = 27)}$	FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1	2.2 V	9	15.5	25	MHz
		3 V	10.3	17.9	28.5	
$f_{(DCO = 2)}$	FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	1.8	2.8	4.2	MHz
		3 V	2.1	3.4	5.2	
$f_{(DCO = 27)}$	FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	13.5	21.5	33	MHz
		3 V	16	26.6	41	
$f_{(DCO = 2)}$	FN_8 = 1, FN_4 = 1 = FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	2.8	4.2	6.2	MHz
		3 V	4.2	6.3	9.2	
$f_{(DCO = 27)}$	FN_8 = 1, FN_4 = 1 = FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	21	32	46	MHz
		3 V	30	46	70	
S_n	Step size between adjacent DCO taps: $S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$ (see Figure 5-16 for taps 21 to 27)	1 < TAP ≤ 20	1.06		1.11	
		TAP = 27	1.07		1.17	
D_t	Temperature drift, $N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0	2.2 V	–0.2	–0.3	–0.4	%/°C
		3 V	–0.2	–0.3	–0.4	
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0		0	5	15	%/V

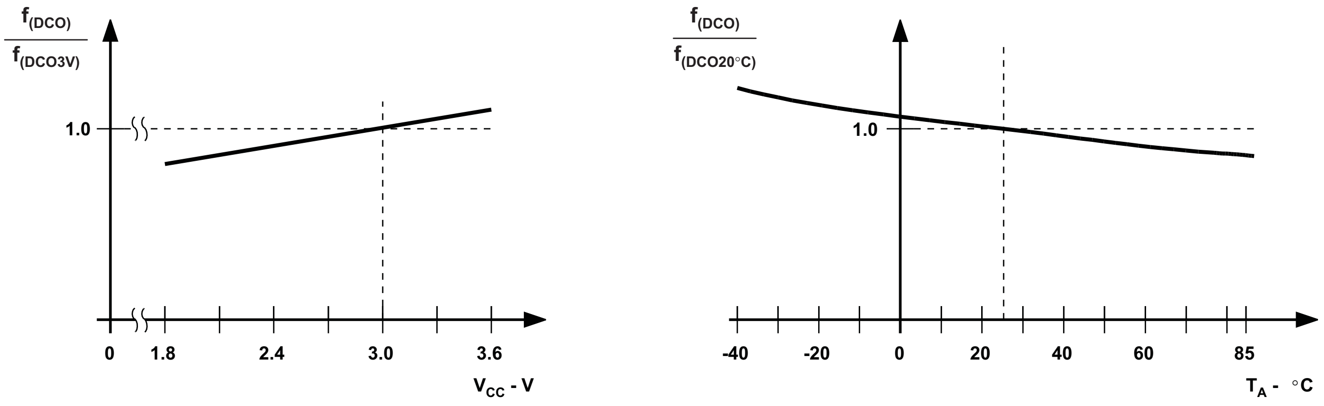


Figure 5-15. DCO Frequency vs Supply Voltage V_{CC} and vs Ambient Temperature

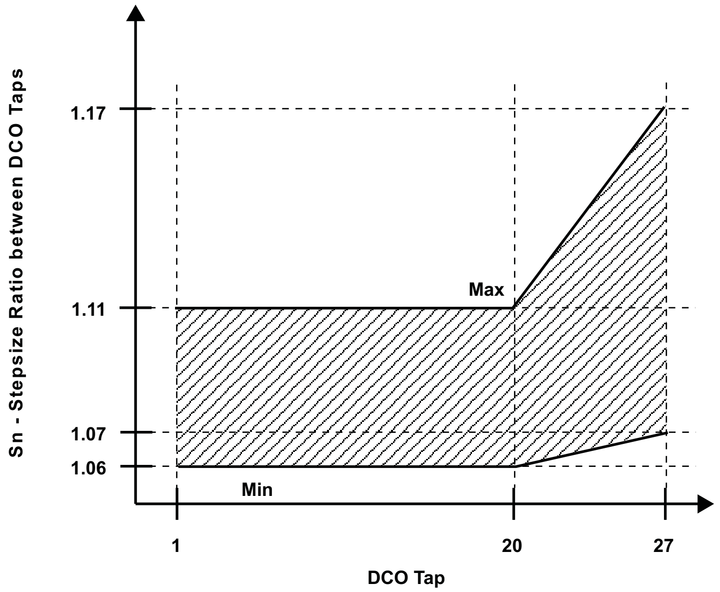


Figure 5-16. DCO Tap Step Size

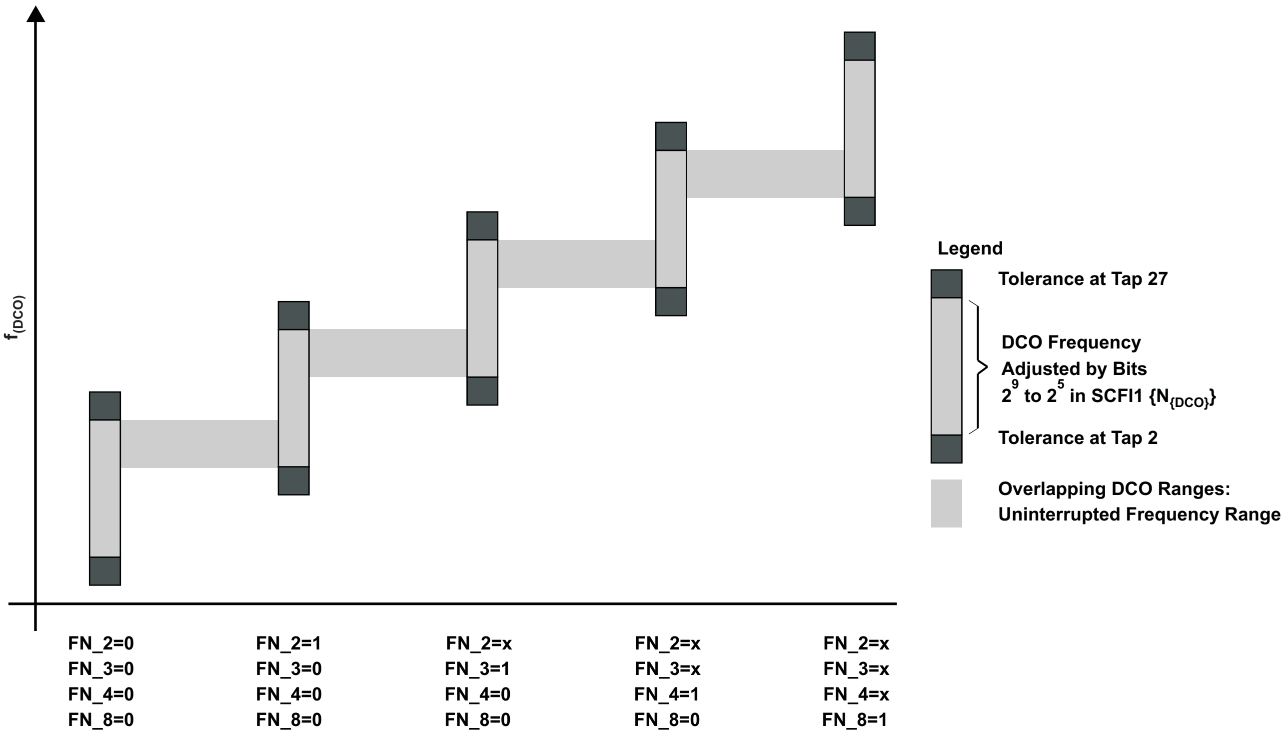


Figure 5-17. Five Overlapping DCO Ranges Controlled by FN_x Bits

5.20 Crystal Oscillator, LFXT1 Oscillator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{XIN}	Integrated input capacitance(3)	OSCCAPx = 0h, V_{CC} = 2.2 V, 3 V		0		pF
		OSCCAPx = 1h, V_{CC} = 2.2 V, 3 V		10		
		OSCCAPx = 2h, V_{CC} = 2.2 V, 3 V		14		
		OSCCAPx = 3h, V_{CC} = 2.2 V, 3 V		18		
C_{XOUT}	Integrated output capacitance(3)	OSCCAPx = 0h, V_{CC} = 2.2 V, 3 V		0		pF
		OSCCAPx = 1h, V_{CC} = 2.2 V, 3 V		10		
		OSCCAPx = 2h, V_{CC} = 2.2 V, 3 V		14		
		OSCCAPx = 3h, V_{CC} = 2.2 V, 3 V		18		
V_{IL}	Low-level input voltage at XIN	V_{CC} = 2.2 V, 3 V(4)	V_{SS}		0.2 × V_{CC}	V
V_{IH}	High-level input voltage at XIN	V_{CC} = 2.2 V, 3 V(4)	0.8 × V_{CC}		V_{CC}	V

(1) The parasitic capacitance from the package and board may be estimated to be 2 pF. The effective load capacitor for the crystal is (C_{XIN} × C_{XOUT}) / (C_{XIN}+ C_{XOUT}). This is independent of XTS_FLL.
(2) To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines should be observed.
  - Keep the trace between the MCU and the crystal as short as possible.
  - Design a good ground plane around the oscillator pins.
  - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
  - If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
  - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(3) TI recommends external capacitance for precision real-time clock applications; OSCCAPx = 0h.
(4) Applies only when using an external logic-level clock source. XTS_FLL must be set. Not applicable when using a crystal or resonator.

5.21 Crystal Oscillator, XT2 Oscillator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{XT2IN}	Integrated input capacitance	V_{CC} = 2.2 V, 3 V		2		pF
C_{XT2OUT}	Integrated output capacitance	V_{CC} = 2.2 V, 3 V		2		pF
V_{IL}	Input levels at XT2IN		V_{SS}		0.2 × V_{CC}	V
V_{IH}		V_{CC} = 2.2 V, 3 V(2)	0.8 × V_{CC}		V_{CC}	V

(1) The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
(2) Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

5.22 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ±10%				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)		2.2 V, 3 V			1	MHz
t_{τ}	UART receive deglitch time UART(1)		2.2 V	50	150	600	ns
			3 V	50	100	600	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

5.23 USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-18 and Figure 5-19)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK Duty cycle = 50% ±10%			f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		2.2 V	110		ns
			3 V	75		
$t_{HD,MI}$	iSOMI input data hold time		2.2 V	0		ns
			3 V	0		
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V		30	ns
			3 V		20	

5.24 USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-20 and Figure 5-21)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time STE low to clock		2.2 V, 3 V		50		ns
$t_{STE,LAG}$	STE lag time Last clock to STE high		2.2 V, 3 V	10			ns
$t_{STE,ACC}$	STE access time STE low to SOMI data out		2.2 V, 3 V		50		ns
$t_{STE,DIS}$	STE disable time STE high to SOMI high impedance		2.2 V, 3 V		50		ns
$t_{SU,SI}$	SIMO input data setup time		2.2 V	20			ns
			3 V	15			
$t_{HD,SI}$	SIMO input data hold time		2.2 V	10			ns
			3 V	10			
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		75	110	ns
			3 V		50	75	

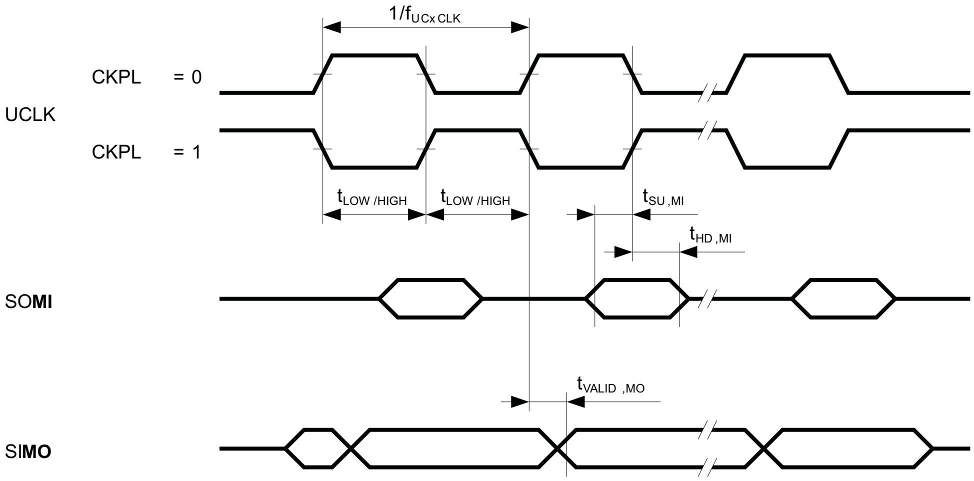


Figure 5-18. SPI Master Mode, CKPH = 0

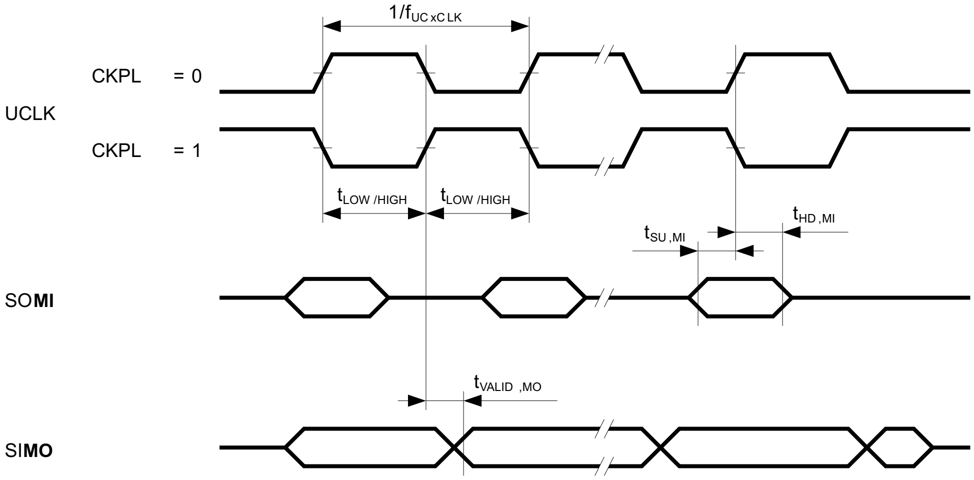


Figure 5-19. SPI Master Mode, CKPH = 1

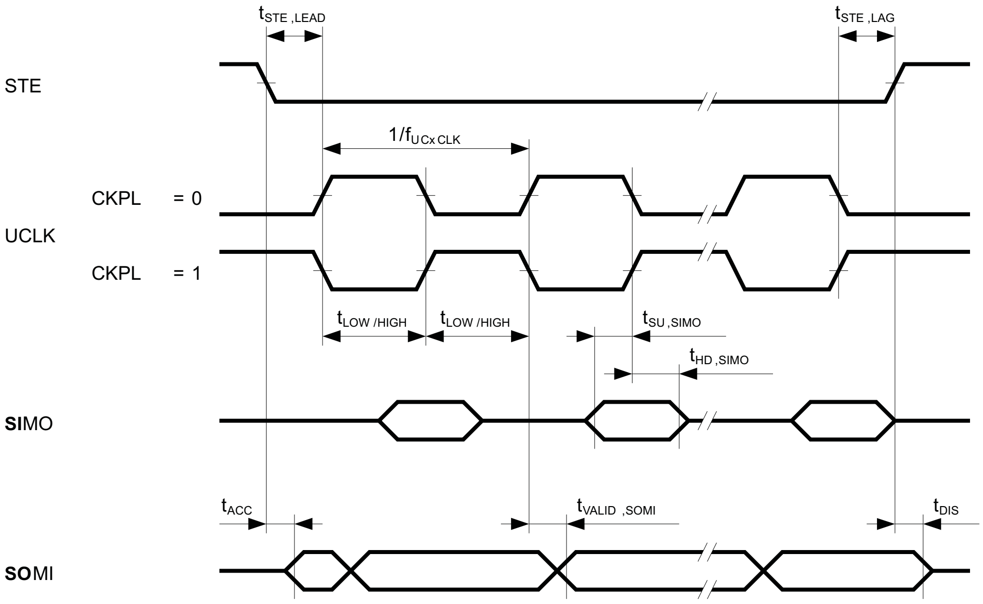


Figure 5-20. SPI Slave Mode, CKPH = 0

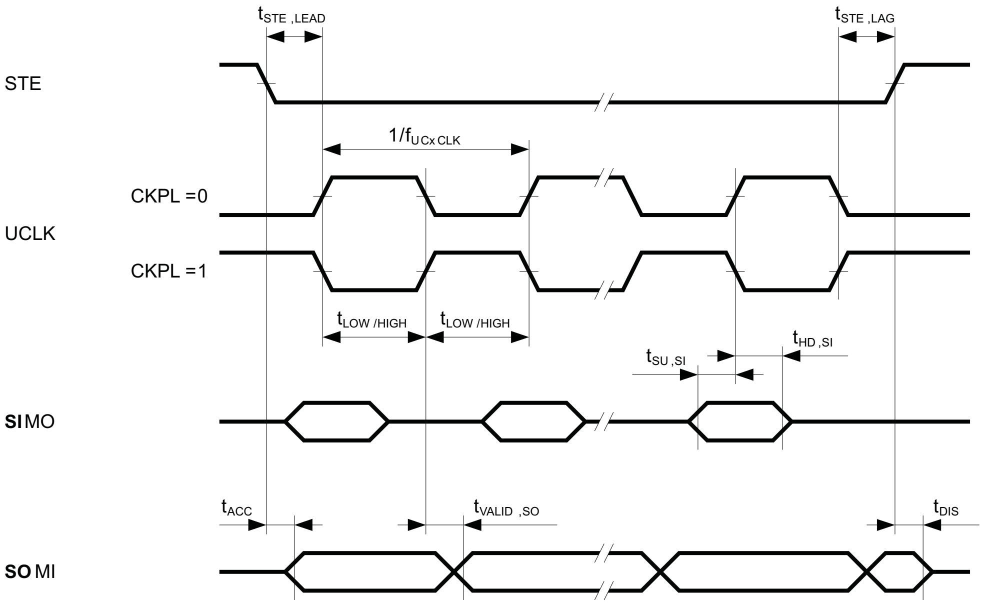


Figure 5-21. SPI Slave Mode, CKPH = 1

5.25 USCI (I^{2}C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-22)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty Cycle = 50% ±10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4			µs
		f_{SCL} > 100 kHz	2.2 V, 3 V	0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.7			µs
		f_{SCL} > 100 kHz	2.2 V, 3 V	0.6			
$t_{HD,DAT}$	Data hold time		2.2 V, 3 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V, 3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		2.2 V, 3 V	4			µs
t_{SP}	Pulse duration of spikes suppressed by input filter		2.2 V	50	150	600	ns
			3 V	50	100	600	

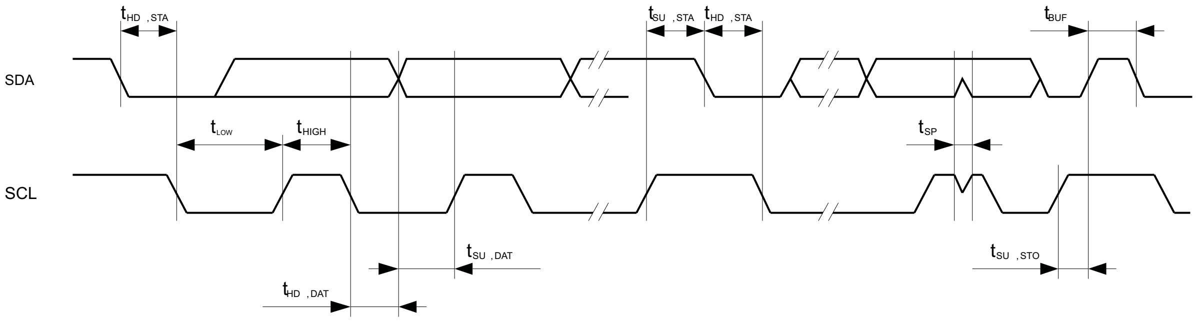


Figure 5-22. I^{2}C Mode Timing

5.26 USART1

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(\tau)}$	USART1 deglitch time	V_{CC} = 2.2 V, SYNC = 0, UART mode	200	430	800	ns
		V_{CC} = 3 V, SYNC = 0, UART mode	150	280	500	

(1) The signal applied to the USART1 receive signal (terminal) (URXD1) must meet the timing requirements of $t_{(\tau)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses that meet the minimum-timing condition of $t_{(\tau)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD1 line.

5.27 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(P6.x/Ax)}$	Analog input voltage range(2)	All external Ax terminals, Analog inputs selected in ADC12MCTLx register, P6Sel.x = 1, $V_{(AVSS)} \leq V_{Ax} \leq V_{(AVCC)}$		0		V_{AVCC}	V
I_{ADC12}	Operating supply current into AV_{CC} terminal(3)	$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0	V_{CC} = 2.2 V		0.65	1.3	mA
			V_{CC} = 3 V		0.8	1.6	
I_{REF+}	Operating supply current into AV_{CC} terminal(4)	$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 1	V_{CC} = 3 V		0.5	0.8	mA
		$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 0	V_{CC} = 2.2 V		0.5	0.8	
			V_{CC} = 3 V		0.5	0.8	
C_I	Input capacitance	Only one terminal can be selected at one time, Ax	V_{CC} = 2.2 V			40	pF
R_I	Input MUX ON resistance	$0 \text{ V} \leq V_{Ax} \leq V_{AVCC}$	V_{CC} = 3 V			2000	Ω

(1) The leakage current is defined in the leakage current table with Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC12}.
(4) The internal reference current is supplied from terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

5.28 12-Bit ADC, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Ve_{REF+}	Positive external reference voltage input	$Ve_{REF+} > V_{REF-}/Ve_{REF-}$ (2)		1.4		V_{AVCC}	V
V_{REF-}/Ve_{REF-}	Negative external reference voltage input	$Ve_{REF+} > V_{REF-}/Ve_{REF-}$ (3)		0		1.2	V
$(Ve_{REF+} - V_{REF-}/Ve_{REF-})$	Differential external reference voltage input	$Ve_{REF+} > V_{REF-}/Ve_{REF-}$ (4)		1.4		V_{AVCC}	V
I_{VeREF+}	Input leakage current	$0 \text{ V} \leq Ve_{REF+} \leq V_{AVCC}$	V_{CC} = 2.2 V, 3 V			±1	µA
$I_{VREF-/VeREF-}$	Input leakage current	$0 \text{ V} \leq Ve_{REF-} \leq V_{AVCC}$	V_{CC} = 2.2 V, 3 V			±1	µA

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

5.29 12-Bit ADC, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF+}	Positive built in reference voltage output	REF2_5V = 1 for 2.5 V, I_{VREF+}max ≤ I_{VREF+} ≤ I_{VREF+}min	V_{CC} = 3 V	2.4	2.5	2.6	V
		REF2_5V = 0 for 1.5 V, I_{VREF+}max ≤ I_{VREF+} ≤ I_{VREF+}min	V_{CC} = 2.2 V, 3 V	1.44	1.5	1.56	
$AV_{CC(min)}$	AV_{CC} minimum voltage, Positive built in reference active	REF2_5V = 0, I_{VREF+}max ≤ I_{VREF+} ≤ I_{VREF+}min		2.2			V
		REF2_5V = 1, I_{VREF+}min ≥ I_{VREF+} ≥ –0.5 mA		2.8			
		REF2_5V = 1, I_{VREF+}min ≥ I_{VREF+} ≥ – 1 mA		2.9			
I_{VREF+}	Load current out of V_{REF+} terminal		V_{CC} = 2.2 V	0.01		–0.5	mA
			V_{CC} = 3 V	0.01		–1	
$I_{L(VREF+)}$	Load-current regulation, V_{REF+} terminal	I_{VREF+} = 500 µA ±100 µA, Analog input voltage ≈ 0.75 V, REF2_5V = 0	V_{CC} = 2.2 V			±2	LSB
			V_{CC} = 3 V			±2	
		I_{VREF+} = 500 µA ±100 µA, Analog input voltage ≈ 1.25 V, REF2_5V = 1	V_{CC} = 3 V			±2	
$I_{DL(VREF+)}$	Load current regulation, VREF+ terminal	I_{VREF+} = 100 µA → 900 µA, C_{VREF+} = 5 µF, Ax ≈ 0.5 × V_{REF+}, Error of conversion result ≤ 1 LSB	V_{CC} = 3 V			20	ns
C_{VREF+}	Capacitance at pin V_{REF+} (1)	REFON = 1, 0 mA ≤ I_{VREF+} ≤ I_{VREF+}max	V_{CC} = 2.2 V, 3 V	5	10		µF
T_{REF+}	Temperature coefficient of built-in reference	I_{VREF+} is a constant in the range of 0 mA ≤ I_{VREF+} ≤ 1 mA	V_{CC} = 2.2 V, 3 V			±100	ppm/°C
t_{REFON}	Settling time of internal reference voltage (see Figure 5-23) (2)	I_{VREF+} = 0.5 mA, C_{VREF+} = 10 µF, V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V				17	ms

(1) The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins V_{REF+} and AV_{SS} and V_{REF-}/Ve_{REF-} and AV_{SS}: 10-µF tantalum and 100-nF ceramic.

(2) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load.

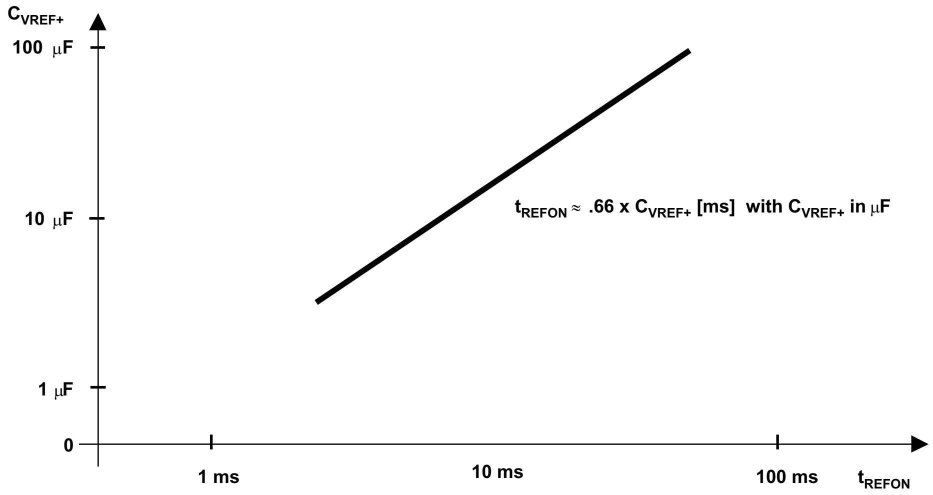


Figure 5-23. Typical Settling Time of Internal Reference t_{REFON} vs External Capacitor on V_{REF+}

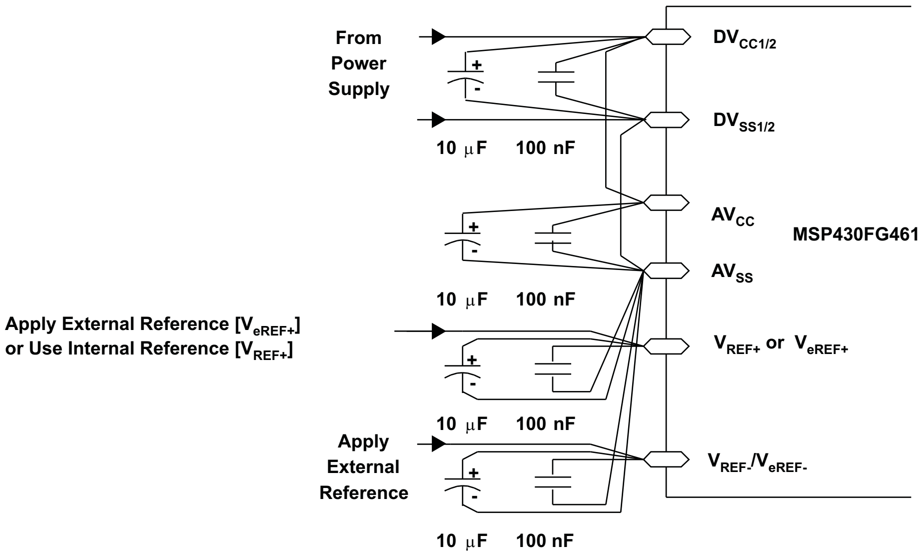


Figure 5-24. Supply Voltage and Reference Voltage Design V_{REF-}/Ve_{REF-} External Supply

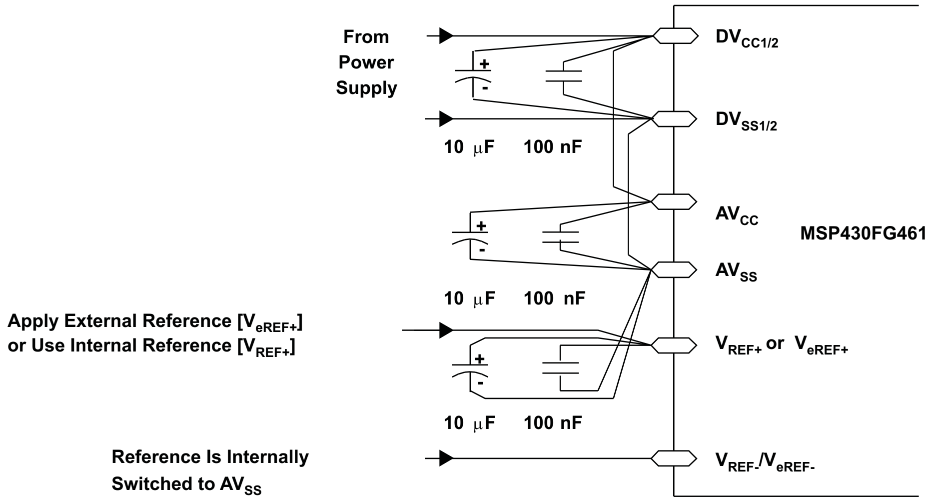


Figure 5-25. Supply Voltage and Reference Voltage Design $V_{REF-}/Ve_{REF-} = AV_{SS}$, Internally Connected

5.30 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$		For specified performance of ADC12 linearity parameters	2.2 V, 3 V	0.45	5	6.3	MHz
$f_{ADC12OSC}$	Internal ADC12 oscillator	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V, 3 V	3.7	5	6.3	MHz
$t_{CONVERT}$	Conversion time	C_{VREF+} ≥ 5 µF, Internal oscillator, $f_{ADC12OSC}$ = 3.7 MHz to 6.3 MHz	2.2 V, 3 V	2.06		3.51	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0		13 × ADC12DIV × 1/$f_{ADC12CLK}$			
$t_{ADC12ON}$	Turnon settling time of the ADC	(1)				100	ns
t_{Sample}	Sampling time	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30pF, τ = [RS +RI] × C_I (2)	3 V	1220			ns
			2.2 V	1400			

(1) The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

(2) Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns where n = ADC resolution = 12, R_S = external source resistance.

5.31 12-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error	1.4 V ≤ (Ve_{REF+} – $V_{REF–}$/$Ve_{REF–}$) min ≤ 1.6 V	2.2 V, 3 V			±2	LSB
		1.6 V < (Ve_{REF+} – $V_{REF–}$/$Ve_{REF–}$) min ≤ [V_{AVCC}]				±1.7	
E_D	Differential linearity error	(Ve_{REF+} – $V_{REF–}$/$Ve_{REF–}$) min ≤ (Ve_{REF+} – $V_{REF–}$/$Ve_{REF–}$), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V			±1	LSB
E_O	Offset error	(Ve_{REF+} – $V_{REF–}$/$Ve_{REF–}$) min ≤ (Ve_{REF+} – $V_{REF–}$/$Ve_{REF–}$), Internal impedance of source RS < 100 Ω, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±2	±4	LSB
E_G	Gain error	(Ve_{REF+} – $V_{REF–}$/$Ve_{REF–}$)min ≤ (Ve_{REF+} – $V_{REF–}$/$Ve_{REF–}$), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±1.1	±2	LSB
E_T	Total unadjusted error	(Ve_{REF+} -– $V_{REF–}$/$Ve_{REF–}$)min ≤ (Ve_{REF+} –$V_{REF–}$/$Ve_{REF–}$), CVREF+ = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±2	±5	LSB

5.32 12-Bit ADC, Temperature Sensor and Built-In V_{MID}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal(1)	REFON = 0, INCH = 0Ah, ADC12ON = N/A, T_A = 25°C	2.2 V		40	120	µA
			3 V		60	160	
V_{SENSOR}	(2)	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V, 3 V		986		mV
TC_{SENSOR}		ADC12ON = 1, INCH = 0Ah	2.2 V, 3 V		3.55 ±3%		mV/°C
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected(3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3 V	30			
I_{VMID}	Current into divider at channel 11(4)	ADC12ON = 1, INCH = 0Bh	2.2 V			N/A(4)	µA
			3 V			N/A(4)	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, $V_{MID} \approx 0.5 \times V_{AVCC}$	2.2 V		1.1	1.1 ±0.04	V
			3 V		1.5	1.50 ±0.04	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected(5)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

(1) The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON = 1), or (ADC12ON = 1 AND INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
(2) The temperature sensor offset can be as much as ±20°C. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$
(4) No additional current is needed. The V_{MID} is used during sampling.
(5) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

5.33 12-Bit DAC, Supply Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS}$ = 0 V		2.20		3.60	V
I_{DD}	Supply current, single DAC channel(1) (2)	DAC12AMPx = 2, DAC12IR = 0, DAC12_xDAT = 0800h	2.2 V, 3 V		50	110	µA
		DAC12AMPx = 2, DAC12IR = 1, DAC12_xDAT = 0800h, $Ve_{REF+} = V_{REF+} = AV_{CC}$			50	110	
		DAC12AMPx = 5, DAC12IR = 1, DAC12_xDAT = 0800h, $Ve_{REF+} = V_{REF+} = AV_{CC}$			200	440	
		DAC12AMPx = 7, DAC12IR = 1, DAC12_xDAT = 0800h, $Ve_{REF+} = V_{REF+} = AV_{CC}$			700	1500	
PSRR	Power-supply rejection ratio(3)(4)	DAC12_xDAT = 800h, V_{REF} = 1.5 V, ΔAV_{CC} = 100 mV	2.2 V		70		dB
		DAC12_×DAT = 800h, V_{REF} = 1.5 V or 2.5 V, ΔAV_{CC} = 100 mV	3 V				

(1) No load at the output pin, DAC12_0 or DAC12_1, assuming that the control bits for the shared pins are set properly.
(2) Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
(3) PSRR = $20 \times \log\{\Delta AV_{CC}/\Delta V_{DAC12\_xOUT}\}$.
(4) V_{REF} is applied externally. The internal reference is not used.

5.34 12-Bit DAC, Linearity Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-26)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
	Resolution	12-bit monotonic		12			bits
INL	Integral nonlinearity(1)	V_{ref} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V		±2.0	±8.0	LSB
		V_{ref} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V				
DNL	Differential nonlinearity(1)	V_{ref} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V		±0.4	±1.0	LSB
		V_{ref} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V				
E_O	Offset voltage without calibration(1) (2)	V_{ref} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V			±21	mV
		V_{ref} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V				
	Offset voltage with calibration(1) (2)	V_{ref} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V			±2.5	
		V_{ref} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V				
$d_{E(O)}/d_T$	Offset error temperature coefficient(1)		2.2 V, 3 V		±30		µV/°C
E_G	Gain error(1)	V_{REF} = 1.5 V	2.2 V			±3.5	%FSR
		V_{REF} = 2.5 V	3 V				
$d_{E(G)}/d_T$	Gain temperature coefficient(1)		2.2 V, 3 V		10		ppm of FSR/°C
t_{Offset_Cal}	Time for offset calibration(3)	DAC12AMPx = 2	2.2 V, 3 V			100	ms
		DAC12AMPx = 3, 5				32	
		DAC12AMPx = 4, 6, 7				6	

(1) Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients “a” and “b” of the first order equation: y = a + b × x. $V_{DAC12\_xOUT} = E_O + (1 + E_G) \times (Ve_{REF+}/4095) \times DAC12\_xDAT$, DAC12IR = 1.
(2) The offset calibration works on the output operational amplifier. Offset calibration is triggered by setting bit DAC12CALON.
(3) The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. TI recommends that the DAC12 module be configured before initiating calibration. Port activity during calibration may effect accuracy and is not recommended.

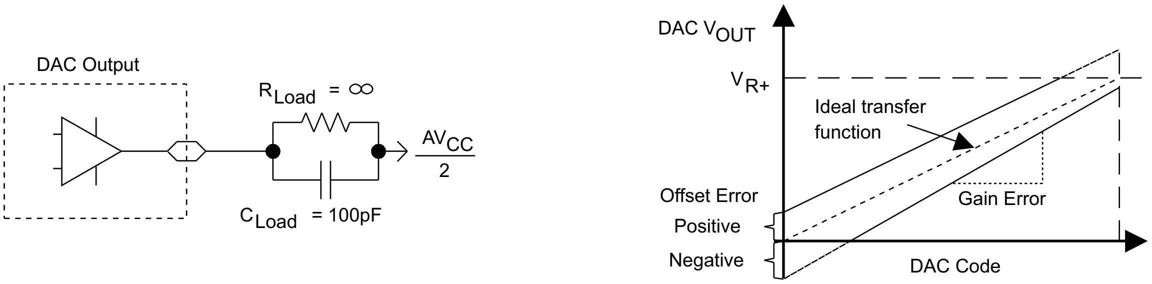


Figure 5-26. Linearity Test Load Conditions and Gain and Offset Definition

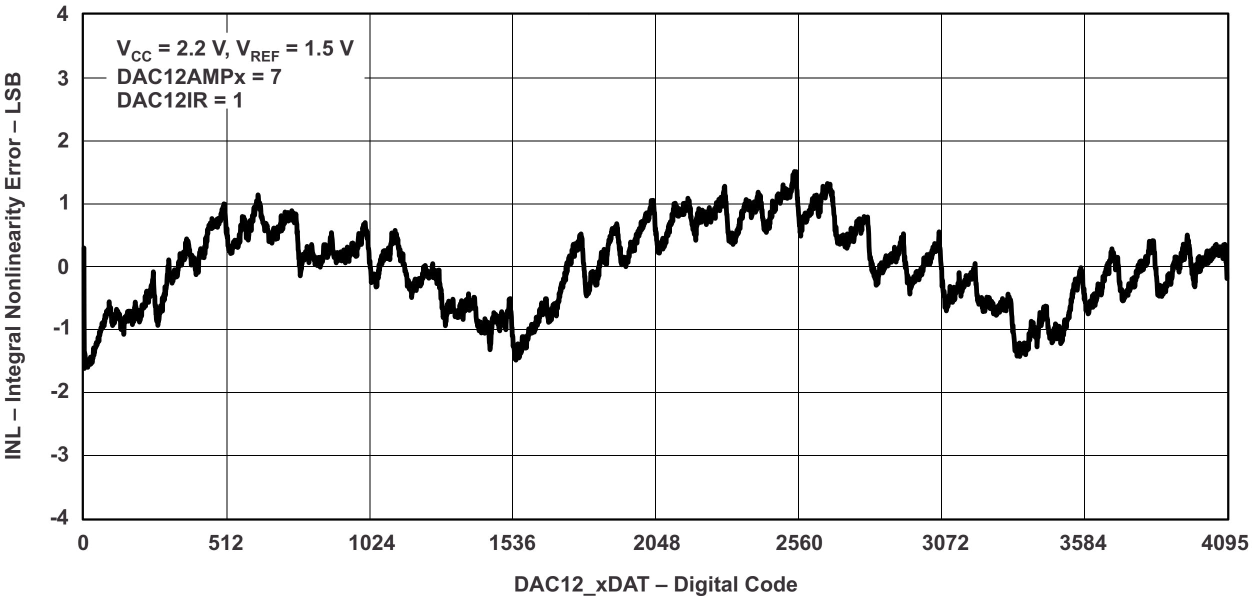


Figure 5-27. Typical INL Error vs Digital Input Data

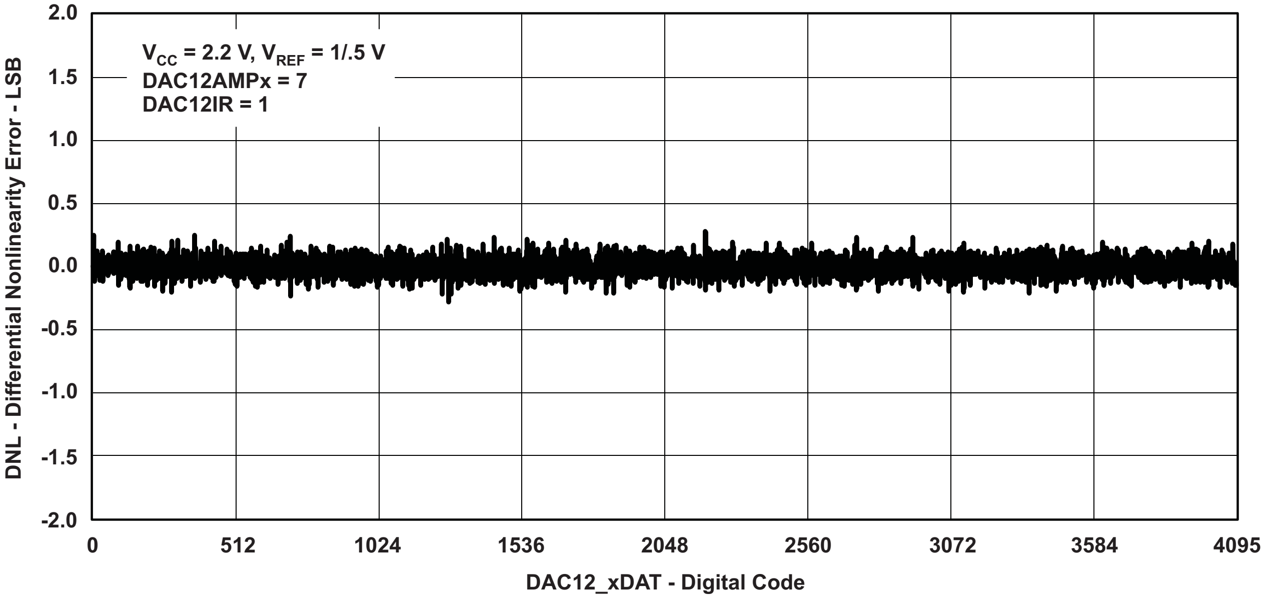


Figure 5-28. Typical DNL Error vs Digital Input Data

5.35 12-Bit DAC, Output Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_O	Output voltage range (see Figure 5-29)(1)	No load, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2 V, 3 V	0		0.005	V
		No load, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC} – 0.05		AV_{CC}	
		R_{Load} = 3 kΩ, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7		0		0.1	
		R_{Load} = 3 kΩ, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC} – 0.13		AV_{CC}	
$C_{L(DAC12)}$	Max DAC12 load capacitance		2.2 V, 3 V			100	pF
$I_{L(DAC12)}$	Max DAC12 load current		2.2 V	–0.5		+0.5	mA
			3 V	–1.0		+1.0	
$R_{O/P(DAC12)}$	Output resistance (see Figure 5-29)	R_{Load} = 3 kΩ, $V_{O/P(DAC12)}$ < 0.3 V, DAC12AMPx = 2, DAC12_xDAT = 0h	2.2 V, 3 V		150	250	Ω
		R_{Load} = 3 kΩ, $V_{O/P(DAC12)} > AV_{CC}$ – 0.3 V, DAC12_xDAT = 0FFFh			150	250	
		R_{Load} = 3 kΩ, 0.3 V ≤ $V_{O/P(DAC12)} \le AV_{CC}$ – 0.3 V			1	4	

(1) Data is valid after the offset calibration of the output amplifier.

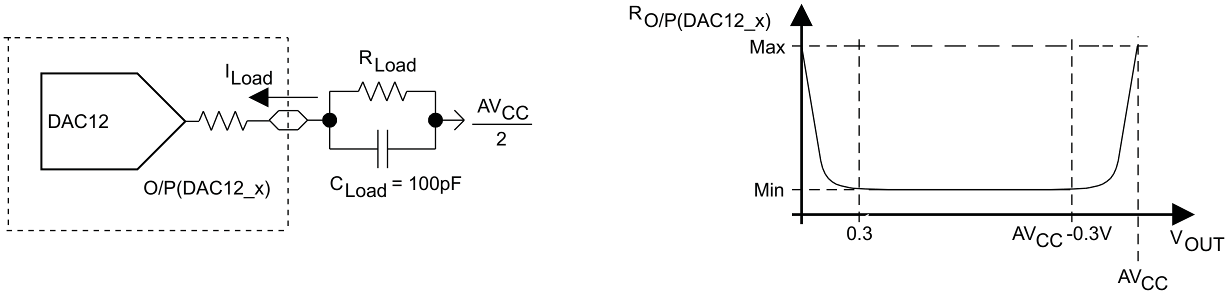


Figure 5-29. DAC12_x Output Resistance Tests

5.36 12-Bit DAC, Reference Input Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Ve_{REF+}	Reference input voltage range	DAC12IR = 0(1) (2)	2.2 V, 3 V		$AV_{CC}/3$	AV_{CC} + 0.2	V
		DAC12IR = 1(3) (4)			AV_{CC}	AV_{CC} + 0.2	
$Ri_{(VREF+)}$, $(Ri_{(VeREF+)})$	Reference input resistance	DAC12_0 IR = DAC12_1 IR = 0	2.2 V, 3 V	20			MΩ
		DAC12_0 IR = 1, DAC12_1 IR = 0		40	48	56	kΩ
		DAC12_0 IR = 0, DAC12_1 IR = 1					
		DAC12_0 IR = DAC12_1 IR = 1, DAC12_0 SREFx = DAC12_1 SREFx(5)		20	24	28	

(1) For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).
(2) The maximum voltage applied at reference input voltage terminal $Ve_{REF+} = [AV_{CC} - V_{E(O)}] / [3 \times (1 + E_G)]$.
(3) For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV_{CC}).
(4) The maximum voltage applied at reference input voltage terminal $Ve_{REF+} = [AV_{CC} - V_{E(O)}] / (1 + E_G)$.
(5) When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel reducing the reference input resistance.

5.37 12-Bit DAC, Dynamic Specifications

V_{ref} = V_{CC}, DAC12IR = 1, over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-30 and Figure 5-31)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
t_{ON}	DAC12 on time	DAC12_xDAT = 800h, $Error_{V(O)}$ < ±0.5 LSB[1] (see Figure 5-30)	DAC12AMPx = 0 → {2, 3, 4}	2.2 V, 3 V		60	120	µs
			DAC12AMPx = 0 → {5, 6}			15	30	
			DAC12AMPx = 0 → 7			6	12	
$t_{S(FS)}$	Settling time, full scale	DAC12_xDAT = 80h→F7Fh→80h	DAC12AMPx = 2	2.2 V, 3 V		100	200	µs
			DAC12AMPx = 3,5			40	80	
			DAC12AMPx = 4, 6, 7			15	30	
$t_{S(C-C)}$	Settling time, code to code	DAC12_xDAT = 3F8h→408h→3F8h BF8h→C08h→BF8h	DAC12AMPx = 2	2.2 V, 3 V		5		µs
			DAC12AMPx = 3,5			2		
			DAC12AMPx = 4, 6, 7			1		
SR	Slew rate	DAC12_xDAT = 80h→F7Fh→80h[2]	DAC12AMPx = 2	2.2 V, 3 V	0.05	0.12		V/µs
			DAC12AMPx = 3,5		0.35	0.7		
			DAC12AMPx = 4, 6, 7		1.5	2.7		
	Glitch energy, full-scale	DAC12_xDAT = 80h→F7Fh→80h	DAC12AMPx = 2	2.2 V, 3 V		600		nV-s
			DAC12AMPx = 3,5			150		
			DAC12AMPx = 4, 6, 7			30		

(1) R_{Load} and C_{Load} connected to AV_{SS} (not $AV_{CC}/2$) in Figure 5-30.
(2) Slew rate applies to output voltage steps ≥ 200 mV.

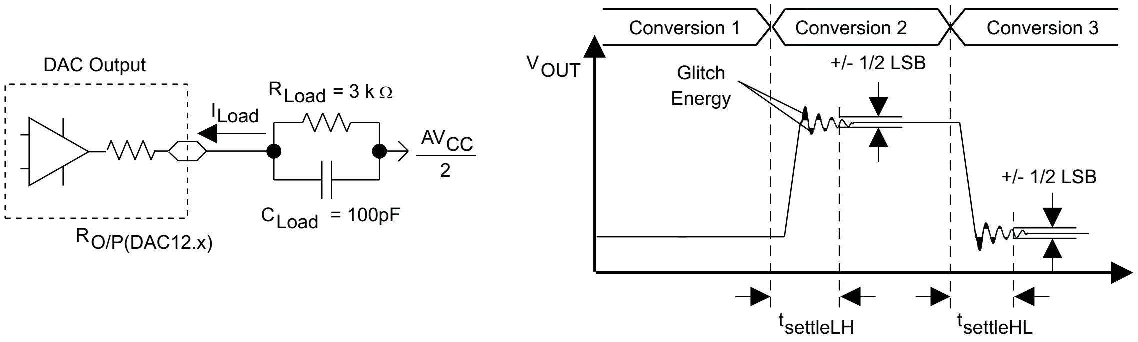


Figure 5-30. Settling Time and Glitch Energy Testing

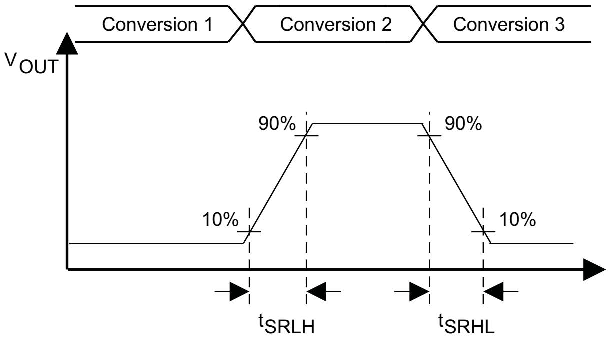


Figure 5-31. Slew Rate Testing

5.38 12-Bit DAC, Dynamic Specifications Continued

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$BW_{–3dB}$	3-dB bandwidth, V_{DC} = 1.5 V, V_{AC} = 0.1 VPP (see Figure 5-32)	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2 V, 3 V	40			kHz
		DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		180			
		DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		550			
	Channel-to-channel crosstalk (see Figure 5-33)(1)	DAC12_0DAT = 800h, No Load, DAC12_1DAT = 80h↔F7Fh, R_{Load} = 3 kΩ f_{DAC12_1OUT} = 10 kHz at 50/50 duty cycle	2.2 V, 3 V		–80		dB
		DAC12_0DAT = 80h↔F7Fh, R_{Load} = 3 kΩ, DAC12_1DAT = 800h, No Load, f_{DAC12_0OUT} = 10 kHz at 50/50 duty cycle			–80		

(1) R_{LOAD} = 3 kΩ, C_{LOAD} = 100 pF

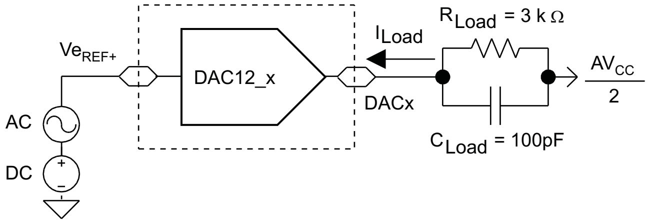


Figure 5-32. Test Conditions for 3-dB Bandwidth Specification

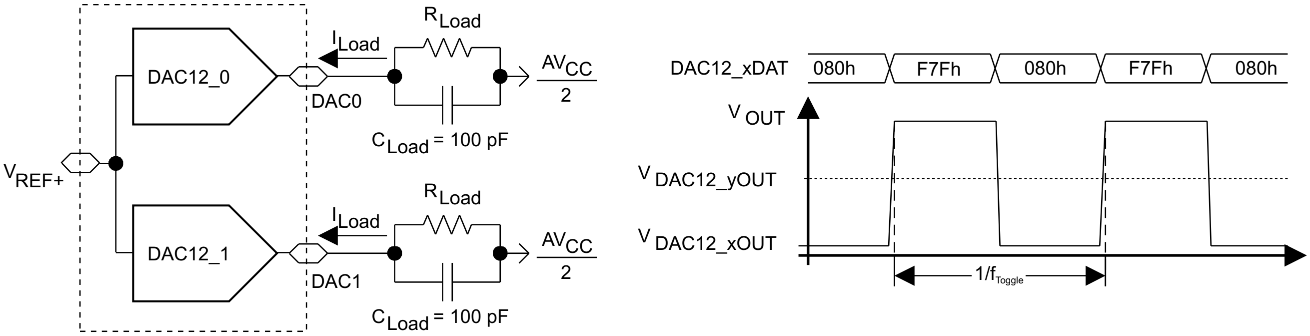


Figure 5-33. Crosstalk Test Conditions

5.39 Operational Amplifier OA, Supply Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			2.2		3.6	V
I_{CC}	Supply current[1]	Fast Mode, OARRIP = 1 (rail-to-rail mode off)	2.2 V, 3 V		180	290	µA
		Medium Mode, OARRIP = 1 (rail-to-rail mode off)			110	190	
		Slow Mode, OARRIP = 1 (rail-to-rail mode off)			50	80	
		Fast Mode, OARRIP = 0 (rail-to-rail mode on)			300	490	
		Medium Mode, OARRIP = 0 (rail-to-rail mode on)			190	350	
		Slow Mode, OARRIP = 0 (rail-to-rail mode on)			90	190	
PSRR	Power supply rejection ratio	Noninverting	2.2 V, 3 V		70		dB

(1) P6SEL.x = 1 for each corresponding pin when used in OA input or OA output mode.

5.40 Operational Amplifier OA, Input/Output Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{I/P}$	Voltage supply, I/P	OARRIP = 1 (rail-to-rail mode off)			–0.1		V_{CC} – 1.2	V
		OARRIP = 0 (rail-to-rail mode on)			–0.1		V_{CC} + 0.1	
I_{lkg}	Input leakage current, I/P[1] [2]	T_A = –40 to +55°C			–5	±0.5	5	nA
		T_A = +55 to +85°C			–20	±5	20	
V_n	Voltage noise density, I/P	Fast Mode	$f_{V(I/P)}$ = 1 kHz			50		$nV/\sqrt{HZ}$
		Medium Mode				80		
		Slow Mode				140		
		Fast Mode	$f_{V(I/P)}$ = 10 kHz			30		
		Medium Mode				50		
		Slow Mode				65		
V_{IO}	Offset voltage, I/P			2.2 V, 3 V			±10	mV
	Offset temperature drift, I/P	[3]		2.2 V, 3 V		±10		µV/°C
	Offset voltage drift with supply, I/P	0.3 V ≤ V_{IN} ≤ V_{CC} – 0.3 V ΔV_{CC} ≤ ±10%, T_A = 25°C		2.2 V, 3 V			±1.5	mV/V
V_{OH}	High-level output voltage, O/P	Fast Mode, I_{SOURCE} ≤ –500 µA		2.2 V	V_{CC} – 0.2		V_{CC}	V
		Slow Mode, I_{SOURCE} ≤ –150 µA		3 V	V_{CC} – 0.1		V_{CC}	
V_{OL}	Low-level output voltage, O/P	Fast Mode, I_{SOURCE} ≤ +500 µA		2.2 V	V_{SS}		0.2	V
		Slow Mode, I_{SOURCE} ≤ +150 µA		3 V	V_{SS}		0.1	
$R_{O/P\ (OAx)}$	Output resistance (see Figure 5-34)[4]	R_{Load} = 3 kΩ, C_{Load} = 50 pF, OARRIP = 0 (rail-to-rail mode on), $V_{O/P(OAx)}$ < 0.2 V		2.2 V, 3 V		150	250	Ω
		R_{Load} = 3 kΩ, C_{Load} = 50 pF, OARRIP = 0 (rail-to-rail mode on), $V_{O/P(OAx)}$ > AV_{CC} – 0.2 V				150	250	
		R_{Load} = 3 kΩ, C_{Load} = 50 pF, OARRIP = 0 (rail-to-rail mode on), 0.2 V ≤ $V_{O/P(OAx)}$ ≤ AV_{CC} – 0.2 V				0.1	4	
CMRR	Common-mode rejection ratio	Noninverting		2.2 V, 3 V		70		dB

(1) ESD damage can degrade input current leakage.
(2) The input bias current is overridden by the input leakage current.
(3) Calculated using the box method.
(4) Specification valid for voltage-follower OAx configuration.

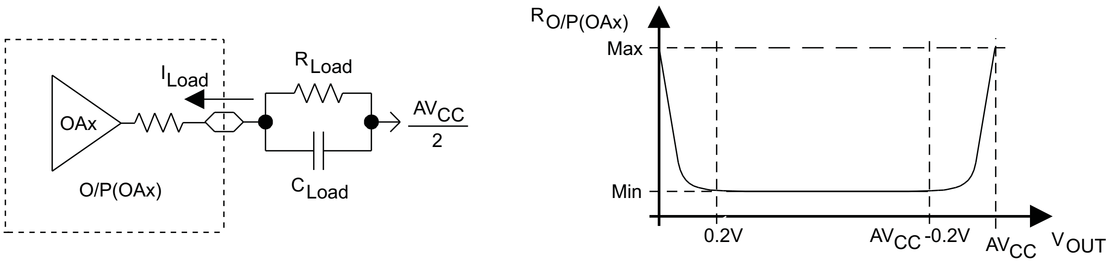


Figure 5-34. OAx Output Resistance Tests

5.41 Operational Amplifier OA, Dynamic Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
SR	Slew rate	Fast Mode			1.2		V/µs
		Medium Mode			0.8		
		Slow Mode			0.3		
	Open-loop voltage gain				100		dB
φm	Phase margin	C_L = 50 pF			60		deg
	Gain margin	C_L = 50 pF			20		dB
GBW	Gain-bandwidth product (see Figure 5-35 and Figure 5-36)	Noninverting, Fast Mode, R_L = 47 kΩ, C_L = 50 pF	2.2 V, 3 V		2.2		MHz
		Noninverting, Medium Mode, R_L = 300 kΩ, C_L = 50 pF			1.4		
		Noninverting, Slow Mode, R_L = 300 kΩ, C_L = 50 pF			0.5		
$t_{en(on)}$	Enable time on	t_{on}, Noninverting, Gain = 1	2.2 V, 3 V		10	20	µs
$t_{en(off)}$	Enable time off		2.2 V, 3 V			1	µs

5.42 Operational Amplifier OA, Typical Characteristics

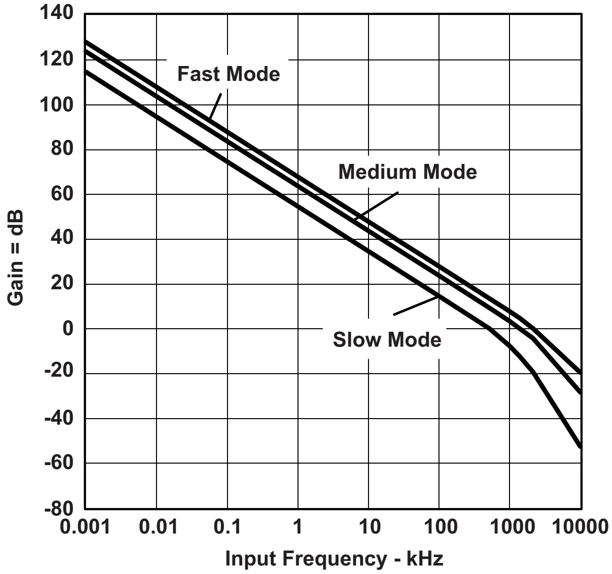


Figure 5-35. Typical Open-Loop Gain vs Frequency

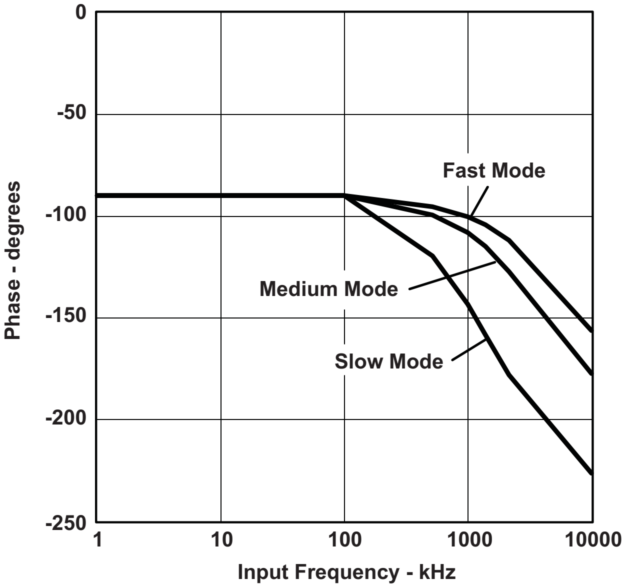


Figure 5-36. Typical Phase vs Frequency

5.43 Operational Amplifier OA Feedback Network, Noninverting Amplifier Mode (OAFCx = 4)

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
G	Gain	OAFBRx = 0	2.2 V, 3 V	0.996	1.00	1.002	
		OAFBRx = 1		1.329	1.334	1.340	
		OAFBRx = 2		1.987	2.001	2.016	
		OAFBRx = 3		2.64	2.667	2.70	
		OAFBRx = 4		3.93	4.00	4.06	
		OAFBRx = 5		5.22	5.33	5.43	
		OAFBRx = 6		7.76	7.97	8.18	
		OAFBRx = 7		15.0	15.8	16.6	
THD	Total harmonic distortion and nonlinearity	All gains	2.2 V		–60		dB
			3 V		–70		
t_{Settle}	Settling time (1)	All power modes	2.2 V, 3 V		7	12	µs

(1) The settling time specifies the time until an ADC result is stable. This includes the minimum required sampling time of the ADC. The settling time of the amplifier itself might be faster.

5.44 Operational Amplifier OA Feedback Network, Inverting Amplifier Mode (OAFCx = 6)(1)

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
G	Gain	OAFBRx = 1	2.2 V, 3 V	–0.371	–0.335	–0.298	
		OAFBRx = 2		–1.031	–1.002	–0.972	
		OAFBRx = 3		–1.727	–1.668	–1.609	
		OAFBRx = 4		–3.142	–3.00	–2.856	
		OAFBRx = 5		–4.581	–4.33	–4.073	
		OAFBRx = 6		–7.529	–6.97	–6.379	
		OAFBRx = 7		–17.040	–14.8	–12.279	
THD	Total harmonic distortion and nonlinearity	All gains	2.2 V		–60		dB
			3 V		–70		
t_{Settle}	Settling time (2)	All power modes	2.2 V, 3 V		7	12	µs

(1) This includes the two OA configuration "inverting amplifier with input buffer". Both OAs need to be set to the same power mode, OAPMx.
(2) The settling time specifies the time until an ADC result is stable. This includes the minimum required sampling time of the ADC. The settling time of the amplifier itself might be faster.

5.45 Flash Memory (FG461x Devices Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.7		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from DVCC during program		2.7 V, 3.6 V		3	5	mA
I_{ERASE}	Supply current from DVCC during erase	(1)	2.7 V, 3.6 V		3	7	mA
$I_{GMERASE}$	Supply current from DVCC during global mass erase	(2)	2.7 V, 3.6 V		6	14	mA
t_{CPT}	Cumulative program time	(3)	2.7 V, 3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.7 V, 3.6 V	20			ms
	Program and erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	(4)			30		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				25		
$t_{Block, 1-63}$	Block program time for each additional byte or word				18		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				10593		
$t_{Global Mass Erase}$	Global mass erase time				10593		
$t_{Seg Erase}$	Segment erase time				4819		

(1) Lower 64KB or upper 64KB flash memory erased.
(2) All flash memory erased.
(3) The cumulative program time must not be exceeded during a block-write operation. This parameter is only relevant if the block write feature is used.
(4) These values are hardwired into the flash controller state machine (t_{FTG} = 1/f_{FTG}).

5.46 JTAG Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency	(1)	2.2 V	0		5	MHz
			3 V	0		10	
$R_{Internal}$	Internal pullup resistance on TMS, TCK, TDI/TCLK	(2)	2.2 V, 3 V	25	60	90	kΩ

(1) f_{TCK} may be restricted to meet the timing requirements of the module selected.
(2) TMS, TDI/TCLK, and TCK pullup resistors are implemented in all versions.

5.47 JTAG Fuse(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C	2.5		V
V_{FB}	Voltage level on TDI/TCLK for fuse-blow (FG461x)		6	7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) After the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

6 Detailed Description

6.1 CPU

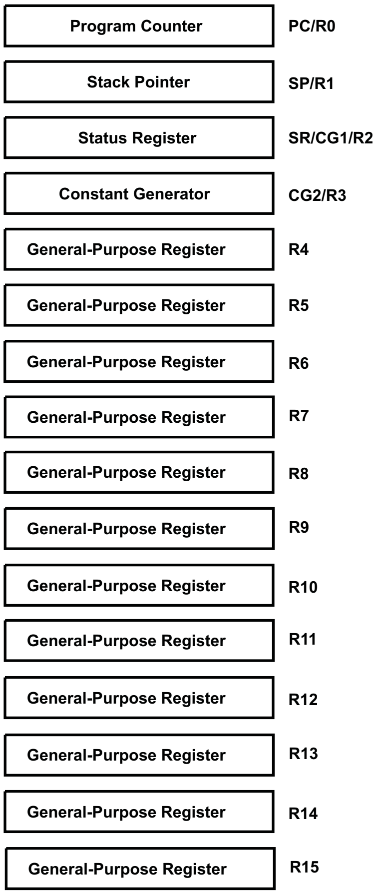
The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The MSP430xG461x device family uses the MSP430X CPU and is completely backwards compatible with the MSP430 CPU. For a complete description of the MSP430X CPU, refer to the *MSP430x4xx Family User's Guide* (SLAU056).



6.2 Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. Table 6-1 shows examples of the three types of instruction formats; the address modes are listed in Table 6-2.

Table 6-1. Instruction Word Formats

FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC→ (TOS), R8 → PC
Relative jump, un/conditional	JNE	Jump-on-equal bit = 0

Table 6-2. Address Mode Descriptions

ADDRESS MODE	S (1)	D (1)	SYNTAX	EXAMPLE	OPERATION
Register	•	•	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	•	•	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)→ M(6+R6)
Symbolic (PC relative)	•	•	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	•	•	MOV & MEM, & TCDAT		M(MEM) → M(TCDAT)
Indirect	•		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	•		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2→ R10
Immediate	•		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) NOTE: S = source D = destination

6.3 Operating Modes

These devices have one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
  - FLL+ loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL+ loop control is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL+ loop control and DCOCLK are disabled
  - DCO DC generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO DC generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO DC generator is disabled
  - Crystal oscillator is stopped

6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 6-3. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Flash Memory	WDTIFG KEYV (1) (2)	Reset	0FFFEh	31, highest
NMI Oscillator Fault Flash Memory Access Violation	NMIIFG (1) (3) OFIFG (1) (3) ACCVIFG (1) (4)(2)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	30
Timer_B7	TBCCR0 CCIFG0 (4)	Maskable	0FFFAh	29
Timer_B7	TBCCR1 CCIFG1 to TBCCR6 CCIFG6, TBIFG (1)(4)	Maskable	0FFF8h	28
Comparator_A	CAIFG	Maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	Maskable	0FFF4h	26
USCI_A0, USCI_B0 Receive	UCA0RXIFG, UCB0RXIFG (1)	Maskable	0FFF2h	25
USCI_A0, USCI_B0 Transmit	UCA0TXIFG, UCB0TXIFG (1)	Maskable	0FFF0h	24
ADC12	ADC12IFG (1) (4)	Maskable	0FFEEh	23
Timer_A3	TACCR0 CCIFG0 (4)	Maskable	0FFECh	22
Timer_A3	TACCR1 CCIFG1 and TACCR2 CCIFG2, TAIFG (1) (4)	Maskable	0FFEAh	21
I/O Port P1 (Eight Flags)	P1IFG.0 to P1IFG.7 (1) (4)	Maskable	0FFE8h	20
USART1 Receive	URXIFG1	Maskable	0FFE6h	19
USART1 Transmit	UTXIFG1	Maskable	0FFE4h	18
I/O Port P2 (Eight Flags)	P2IFG.0 to P2IFG.7 (1) (4)	Maskable	0FFE2h	17
Basic Timer 1, RTC	BTIFG	Maskable	0FFE0h	16
DMA	DMA0IFG, DMA1IFG, DMA2IFG (1) (4)	Maskable	0FFDEh	15
DAC12	DAC12.0IFG, DAC12.1IFG (1) (4)	Maskable	0FFDCh	14
Reserved	Reserved (5)		0FFDAh	13
			⋮	⋮
			0FFC0h	0, lowest

---

(1) Multiple source flags
(2) Access and key violations, KEYV and ACCVIFG, only applicable to FG devices.
(3) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh). (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(4) Interrupt flags are located in the module.
(5) The interrupt vectors at addresses 0FFDAh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

6.5 Special Function Registers (SFRs)

The MSP430 SFRs are in the lowest address space and are organized as byte mode registers. SFRs should be accessed with byte instructions.

Legend

rw	Bit can be read and written.
rw-0, rw-1	Bit can be read and written. It is Reset or Set by PUC.
rw-(0), rw-(1)	Bit can be read and written. It is Reset or Set by POR.
▨	SFR bit is not present in device

6.5.1 Interrupt Enable 1 and 2

Address	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0h	▨	▨	**ACCVIE**	**NMIIE**	▨	▨	**OFIE**	**WDTIE**
			rw*0	**rw*0**			**rw*0**	**rw*0**

WDTIE	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured as a general-purpose timer.
OFIE	Oscillator fault-interrupt enable
NMIIE	Nonmaskable interrupt enable
ACCVIE	Flash access violation interrupt enable

Address	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
01h	**BTIE**	▨	**UTXIE1**	**URXIE1**	**UCB0TXIE**	**UCB0RXIE**	**UCA0TXIE**	**UCA0RXIE**
	rw*0		**rw*0**	**rw*0**	**rw*0**	**rw*0**	**rw*0**	**rw*0**

UCA0RXIE	USCI_A0 receive-interrupt enable
UCA0TXIE	USCI_A0 transmit-interrupt enable
UCB0RXIE	USCI_B0 receive-interrupt enable
UCB0TXIE	USCI_B0 transmit-interrupt enable
URXIE1	USART1 UART and SPI receive-interrupt enable
UTXIE1	USART1 UART and SPI transmit-interrupt enable
BTIE	Basic timer interrupt enable

6.5.2 Interrupt Flag Register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG			OFIFG	WDTIFG
				rw*0			rw*1	rw*(0)

WDTIFG	Set on watchdog timer overflow (in watchdog mode) or security key violation Reset on V_{CC} power-on or a reset condition at the $\overline{\text{RST}}$/NMI pin in reset mode
OFIFG	Flag set on oscillator fault
NMIIFG	Set by the $\overline{\text{RST}}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h	BTIFG		UTXIFG1	URXIFG1	UCB0TXIFG	UCB0RXIFG	UCA0TXIFG	UCA0RXIFG
	rw*0		rw*1	rw*0	rw*0	rw*0	rw*0	rw*0

UCA0RXIFG	USCI_A0 receive-interrupt flag
UCA0TXIFG	USCI_A0 transmit-interrupt flag
UCB0RXIFG	USCI_B0 receive-interrupt flag
UCB0TXIFG	USCI_B0 transmit-interrupt flag
URXIFG0	USART1: UART and SPI receive flag
UTXIFG0	USART1: UART and SPI transmit flag
BTIFG	Basic timer flag

6.5.3 Module Enable Registers 1 and 2

Address	7	6	5	4	3	2	1	0
04h								

URXE1	USART1: UART mode receive enable
UTXE1	USART1: UART mode transmit enable
USPIE1	USART1: SPI mode transmit and receive enable

Address	7	6	5	4	3	2	1	0
05h			UTXE1	URXE1 USPIE1				
			rw*0	rw*0				

URXE1	USART1: UART mode receive enable
UTXE1	USART1: UART mode transmit enable
USPIE1	USART1: SPI mode transmit and receive enable

6.6 Memory Organization

Table 6-4 summarizes the memory organization for the FG461x devices, and Table 6-5 summarizes the memory organization for the CG461x devices.

Table 6-4. MSP430FG461x Memory Organization

			MSP430FG4616	MSP430FG4617	MSP430FG4618	MSP430FG4619
Memory		Size	92KB	92KB	116KB	120KB
Main: interrupt vector		Flash	0FFFFh-0FFC0h	0FFFFh-0FFC0h	0FFFFh-0FFC0h	0FFFFh-0FFC0h
Main: code memory		Flash	018FFFh-002100h	019FFFh-003100h	01FFFFh-003100h	01FFFFh-002100h
RAM	Total	Size	4KB	8KB	8KB	4KB
			020FFh-01100h	030FFh-01100h	030FFh-01100h	020FFh-01100h
	Extended	Size	2KB	6KB	6KB	2KB
			020FFh-01900h	030FFh-01900h	030FFh-01900h	020FFh-01900h
	Mirrored	Size	2KB	2KB	2KB	2KB
			018FFh-01100h	018FFh-01100h	018FFh-01100h	018FFh-01100h
Information memory		Size	256 Byte	256 Byte	256 Byte	256 Byte
		Flash	010FFh-01000h	010FFh-01000h	010FFh-01000h	010FFh-01000h
Boot memory		Size	1KB	1KB	1KB	1KB
		ROM	0FFFFh-0C00h	0FFFFh-0C00h	0FFFFh-0C00h	0FFFFh-0C00h
RAM		Size	2KB	2KB	2KB	2KB
(Mirrored at 018FFh-01100h)			09FFh-0200h	09FFh-0200h	09FFh-0200h	09FFh-0200h
Peripherals		16 bit	01FFh-0100h	01FFh-0100h	01FFh-0100h	01FFh-0100h
		8 bit	0FFh-010h	0FFh-010h	0FFh-010h	0FFh-010h
		8-bit SFR	0Fh-00h	0Fh-00h	0Fh-00h	0Fh-00h

Table 6-5. MSP430CG461x Memory Organization

			MSP430CG4616	MSP430CG4617	MSP430CG4618	MSP430CG4619
Memory		Size	92KB	92KB	116KB	120KB
Main: interrupt vector		ROM	0FFFFh-0FFC0h	0FFFFh-0FFC0h	0FFFFh-0FFC0h	0FFFFh-0FFC0h
Main: code memory		ROM	018FFFh-002100h	019FFFh-003100h	01FFFFh-003100h	01FFFFh-002100h
RAM	Total	Size	4KB	8KB	8KB	4KB
			020FFh-01100h	030FFh-01100h	030FFh-01100h	020FFh-01100h
	Extended	Size	2KB	6KB	6KB	2KB
			020FFh-01900h	030FFh-01900h	030FFh-01900h	020FFh-01900h
	Mirrored	Size	2KB	2KB	2KB	2KB
			018FFh-01100h	018FFh-01100h	018FFh-01100h	018FFh-01100h
Information memory		Size	256 Byte	256 Byte	256 Byte	256 Byte
		ROM	010FFh-01000h	010FFh-01000h	010FFh-01000h	010FFh-01000h
Boot memory		Size	1KB	1KB	1KB	1KB
(Optional on CG)		ROM	0FFFFh-0C00h	0FFFFh-0C00h	0FFFFh-0C00h	0FFFFh-0C00h
RAM		Size	2KB	2KB	2KB	2KB
(Mirrored at 018FFh-01100h)			09FFh-0200h	09FFh-0200h	09FFh-0200h	09FFh-0200h
Peripherals		16 bit	01FFh-0100h	01FFh-0100h	01FFh-0100h	01FFh-0100h
		8 bit	0FFh-010h	0FFh-010h	0FFh-010h	0FFh-010h
		8-bit SFR	0Fh-00h	0Fh-00h	0Fh-00h	0Fh-00h

6.7 Bootstrap Loader (BSL)

The BSL lets users program the flash memory or RAM using a UART serial interface. Access to the MCU memory through the BSL is protected by user-defined password. A bootstrap loader security key is provided at address 0FFBEh to disable the BSL completely or to disable the erasure of the flash if an invalid password is supplied. The BSL is optional for ROM-based devices. For complete description of the features of the BSL and its implementation, see the application report *Features of the MSP430 Bootstrap Loader* (SLAA089).

BSLKEY	DESCRIPTION
00000h	Erasure of flash disabled if an invalid password is supplied
0AA55h	BSL disabled
any other value	BSL enabled

BSL FUNCTION	PZ, ZCA, ZQW PACKAGE PINS
Data Transmit	87/A7 – P1.0
Data Receiver	86/E7 – P1.1

6.8 Flash Memory

The flash memory can be programmed by the JTAG port, the bootstrap loader, or in system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0-n. Segments A and B are also called information memory.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory before the first use.

6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be handled using all instructions. For complete module descriptions, refer to the *MSP430x4xx Family User's Guide*.

6.9.1 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12 conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode without having to awaken to move data to or from a peripheral.

6.9.2 Oscillator and System Clock

The clock system in the MSP430xG461x family of devices is supported by the FLL+ module, which includes support for a 32768-Hz watch crystal oscillator, an internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low power consumption. The FLL+ features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turnon clock source and stabilizes in less than 6 µs. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high-frequency crystal
- Main clock (MCLK), the system clock used by the CPU
- Submain clock (SMCLK), the subsystem clock used by the peripheral modules
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8

6.9.3 Brownout, Supply Voltage Supervisor (SVS)

The brownout circuit provides the proper internal reset signal to the device during power-on and power-off. The SVS circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must make sure the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

6.9.4 Digital I/O

There are ten 8-bit I/O ports implemented—ports P1 through P10:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions
- Ports P7/P8 and P9/P10 can be accessed word-wise as ports PA and PB, respectively.

6.9.5 Basic Timer1 and Real-Time Clock

The Basic Timer1 has two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Basic Timer1 is extended to provide an integrated real-time clock (RTC). An internal calendar compensates for months with less than 31 days and includes leap-year correction.

6.9.6 LCD_A Drive With Regulated Charge Pump

The LCD_A driver generates the segment and common signals required to drive a segment LCD display. The LCD_A controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. Furthermore it is possible to control the level of the LCD voltage and, thus, contrast by software.

6.9.7 Watchdog Timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.9.8 Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3-pin or 4-pin), I^{2}C, and asynchronous communication protocols like UART, enhanced UART with automatic baudrate detection, and IrDA.

The USCI_A0 module provides support for SPI (3-pin or 4-pin), UART, enhanced UART and IrDA.

The USCI_B0 module provides support for SPI (3-pin or 4-pin) and I^{2}C.

6.9.9 USART1

The hardware universal synchronous/asynchronous receive transmit (USART) peripheral module is used for serial data communication. The USART supports synchronous SPI (3-pin or 4-pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

6.9.10 Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs 16×16, 16×8, 8×16, and 8×8 bit operations. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

6.9.11 Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-6. Timer_A3 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUT SIGNAL	OUTPUT PIN NUMBER
PZ, ZCA, ZQW					PZ, ZCA, ZQW
82/B9 - P1.5	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
82/B9 - P1.5	$\overline{\text{TACLK}}$	INCLK			
87/A7 - P1.0	TA0	CCI0A	CCR0	TA0	87/A7 - P1.0
86/E7 - P1.1	TA0	CCI0B			
	DV$_{SS}$	GND			
	DV$_{CC}$	V$_{CC}$			
85/D7 - P1.2	TA1	CCI1A	CCR1	TA1	85/D7 - P1.2
	CAOUT (internal)	CCI1B			ADC12 (internal)
	DV$_{SS}$	GND			
	DV$_{CC}$	V$_{CC}$			
79/A10 - P2.0	TA2	CCI2A	CCR2	TA2	79/A10 - P2.0
	ACLK (internal)	CCI2B			
	DV$_{SS}$	GND			
	DV$_{CC}$	V$_{CC}$			

6.9.12 Timer_B7

Timer_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer_B7 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-7. Timer_B7 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUT SIGNAL	OUTPUT PIN NUMBER
PZ, ZCA, ZQW					PZ, ZCA, ZQW
83/B8 - P1.4	TBCLK	TBCLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
83/B8 - P1.4	$\overline{\text{TBCLK}}$	INCLK			
78/D8 - P2.1	TB0	CCI0A	CCR0CCR0	TB0TB0	78/D8 - P2.1
78/D8 - P2.1	TB0	CCI0B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
77/E8 - P2.2	TB1	CCI1A	CCR1	TB1	77/E8 - P2.2
77/E8 - P2.2	TB1	CCI1B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
76/A11 - P2.3	TB2	CCI2A	CCR2	TB2	76/A11 - P2.3
76/A11 - P2.3	TB2	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
67/E12 - P3.4	TB3	CCI3A	CCR3	TB3	67/E12 - P3.4
67/E12 - P3.4	TB3	CCI3B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
66/G9 - P3.5	TB4	CCI4A	CCR4	TB4	66/G9 - P3.5
66/G9 - P3.5	TB4	CCI4B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
65/F11 - P3.6	TB5	CCI5A	CCR5	TB5	65/F11 - P3.6
65/F11 - P3.6	TB5	CCI5B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
64/F12 - P3.7	TB6	CCI6A	CCR6	TB6	64/F12 - P3.7
	ACLK (internal)	CCI6B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

6.9.13 Comparator_A

The primary function of the comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

6.9.14 ADC12

The ADC12 module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

6.9.15 DAC12

The DAC12 module is a 12-bit R-ladder voltage-output DAC. The DAC12 can be used in 8-bit or 12-bit mode and can be used in conjunction with the DMA controller. When multiple DAC12 modules are present, they may be grouped together for synchronous operation.

6.9.16 OA

The MSP430xG461x has three configurable low-current general-purpose operational amplifiers. Each OA input and output terminal is software-selectable and offer a flexible choice of connections for various applications. The OA op amps primarily support front-end analog signal conditioning before analog-to-digital conversion.

Table 6-8. OA Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER
PZ						PZ
95 - P6.0	OA0I0	OA0I0	OA0	OA0OUT	OA0O	96 - P6.1
97 - P6.2	OA0I1	OA0I1			OA0O	ADC12 (internal)
	DAC12_0OUT (internal)	DAC12_0OUT				
	DAC12_1OUT (internal)	DAC12_1OUT				
3- P6.4	OA1I0	OA1I0	OA1	OA1OUT	OA1O	2- P6.3
13 - P5.0	OA1I1	OA1I1			OA1O	13- P5.0
	DAC12_0OUT (internal)	DAC12_0OUT			OA1O	ADC12 (internal)
	DAC12_1OUT (internal)	DAC12_1OUT				
5- P6.6	OA2I0	OA2I0	OA2	OA2OUT	OA2O	4- P6.5
14 - P10.7	OA2I1	OA2I1			OA2O	14 - P10.7
	DAC12_0OUT (internal)	DAC12_0OUT			OA2O	ADC12 (internal)
	DAC12_1OUT (internal)	DAC12_1OUT				

6.9.17 Peripheral File Map

Table 6-9 lists the registers and addresses for peripherals with word access. Table 6-10 lists the registers and addresses for peripherals with byte access.

Table 6-9. Peripherals With Word Access

MODULE	REGISTER NAME	ACRONYM	ADDRESS
Watchdog+	Watchdog timer control	WDTCTL	0120h
Timer_B7	Capture/compare register 6	TBCCR6	019Eh
	Capture/compare register 5	TBCCR5	019Ch
	Capture/compare register 4	TBCCR4	019Ah
	Capture/compare register 3	TBCCR3	0198h
	Capture/compare register 2	TBCCR2	0196h
	Capture/compare register 1	TBCCR1	0194h
	Capture/compare register 0	TBCCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control 6	TBCCTL6	018Eh
	Capture/compare control 5	TBCCTL5	018Ch
	Capture/compare control 4	TBCCTL4	018Ah
	Capture/compare control 3	TBCCTL3	0188h
	Capture/compare control 2	TBCCTL2	0186h
	Capture/compare control 1	TBCCTL1	0184h
	Capture/compare control 0	TBCCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
Timer_A3	Capture/compare register 2	TACCR2	0176h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 0	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control 2	TACCTL2	0166h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 0	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Hardware Multiplier	Sum extend	SUMEXT	013Eh
	Result high word	RESHI	013Ch
	Result low word	RESLO	013Ah
	Second operand	OP2	0138h
	Multiply signed + accumulate/operand1	MACS	0136h
	Multiply + accumulate/operand1	MAC	0134h
	Multiply signed/operand1	MPYS	0132h
	Multiply unsigned/operand1	MPY	0130h
Flash (FG devices only)	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
DMA	DMA module control 0	DMACTL0	0122h
	DMA module control 1	DMACTL1	0124h
	DMA interrupt vector	DMAIV	0126h
DMA Channel 0	DMA channel 0 control	DMA0CTL	01D0h
	DMA channel 0 source address	DMA0SA	01D2h
	DMA channel 0 destination address	DMA0DA	01D6h
	DMA channel 0 transfer size	DMA0SZ	01DAh
DMA Channel 1	DMA channel 1 control	DMA1CTL	01DCh
	DMA channel 1 source address	DMA1SA	01DEh
	DMA channel 1 destination address	DMA1DA	01E2h
	DMA channel 1 transfer size	DMA1SZ	01E6h
DMA Channel 2	DMA channel 2 control	DMA2CTL	01E8h
	DMA channel 2 source address	DMA2SA	01EAh
	DMA channel 2 destination address	DMA2DA	01EEh
	DMA channel 2 transfer size	DMA2SZ	01F2h

Table 6-9. Peripherals With Word Access (continued)

MODULE	REGISTER NAME	ACRONYM	ADDRESS
ADC12 See also Table 6-10	Conversion memory 15	ADC12MEM15	015Eh
	Conversion memory 14	ADC12MEM14	015Ch
	Conversion memory 13	ADC12MEM13	015Ah
	Conversion memory 12	ADC12MEM12	0158h
	Conversion memory 11	ADC12MEM11	0156h
	Conversion memory 10	ADC12MEM10	0154h
	Conversion memory 9	ADC12MEM9	0152h
	Conversion memory 8	ADC12MEM8	0150h
	Conversion memory 7	ADC12MEM7	014Eh
	Conversion memory 6	ADC12MEM6	014Ch
	Conversion memory 5	ADC12MEM5	014Ah
	Conversion memory 4	ADC12MEM4	0148h
	Conversion memory 3	ADC12MEM3	0146h
	Conversion memory 2	ADC12MEM2	0144h
	Conversion memory 1	ADC12MEM1	0142h
	Conversion memory 0	ADC12MEM0	0140h
	Interrupt-vector-word register	ADC12IV	01A8h
	Inerrupt-enable register	ADC12IE	01A6h
	Inerrupt-flag register	ADC12IFG	01A4h
	Control register 1	ADC12CTL1	01A2h
	Control register 0	ADC12CTL0	01A0h
DAC12	DAC12_1 data	DAC12_1DAT	01CAh
	DAC12_1 control	DAC12_1CTL	01C2h
	DAC12_0 data	DAC12_0DAT	01C8h
	DAC12_0 control	DAC12_0CTL	01C0h
Port PA	Port PA selection	PASEL	03Eh
	Port PA direction	PADIR	03Ch
	Port PA output	PAOUT	03Ah
	Port PA input	PAIN	038h
Port PB	Port PB selection	PBSEL	00Eh
	Port PB direction	PBDIR	00Ch
	Port PB output	PBOUT	00Ah
	Port PB input	PBIN	008h

Table 6-10. Peripherals With Byte Access

MODULE	REGISTER NAME	ACRONYM	ADDRESS
OA2	Operational Amplifier 2 control register 1 Operational Amplifier 2 control register 0	OA2CTL1 OA2CTL0	0C5h 0C4h
OA1	Operational Amplifier 1 control register 1 Operational Amplifier 1 control register 0	OA1CTL1 OA1CTL0	0C3h 0C2h
OA0	Operational Amplifier 0 control register 1 Operational Amplifier 0 control register 0	OA0CTL1 OA0CTL0	0C1h 0C0h
LCD_A	LCD Voltage Control 1 LCD Voltage Control 0 LCD Voltage Port Control 1 LCD Voltage Port Control 0 LCD memory 20 : LCD memory 16 LCD memory 15 : LCD memory 1 LCD control and mode	LCDAVCTL1 LCDAVCTL0 LCDAPCTL1 LCDAPCTL0 LCDM20 : LCDM16 LCDM15 : LCDM1 LCDCTL	0AFh 0AEh 0ADh 0ACh 0A4h : 0A0h 09Fh : 091h 090h
ADC12 (Memory control registers require byte access)	ADC memory-control register 15 ADC memory-control register 14 ADC memory-control register 13 ADC memory-control register 12 ADC memory-control register 11 ADC memory-control register 10 ADC memory-control register 9 ADC memory-control register 8 ADC memory-control register 7 ADC memory-control register 6 ADC memory-control register 5 ADC memory-control register 4 ADC memory-control register 3 ADC memory-control register 2 ADC memory-control register 1 ADC memory-control register 0	ADC12MCTL15 ADC12MCTL14 ADC12MCTL13 ADC12MCTL12 ADC12MCTL11 ADC12MCTL10 ADC12MCTL9 ADC12MCTL8 ADC12MCTL7 ADC12MCTL6 ADC12MCTL5 ADC12MCTL4 ADC12MCTL3 ADC12MCTL2 ADC12MCTL1 ADC12MCTL0	08Fh 08Eh 08Dh 08Ch 08Bh 08Ah 089h 088h 087h 086h 085h 084h 083h 082h 081h 080h
USART1	Transmit buffer Receive buffer Baud rate Baud rate Modulation control Receive control Transmit control USART control	U1TXBUF U1RXBUF U1BR1 U1BR0 U1MCTL U1RCTL U1TCTL U1CTL	07Fh 07Eh 07Dh 07Ch 07Bh 07Ah 079h 078h
USCI	USCI I2C Slave Address USCI I2C Own Address USCI Synchronous Transmit Buffer USCI Synchronous Receive Buffer USCI Synchronous Status USCI I2C Interrupt Enable USCI Synchronous Bit Rate 1 USCI Synchronous Bit Rate 0 USCI Synchronous Control 1 USCI Synchronous Control 0 USCI Transmit Buffer USCI Receive Buffer USCI Status USCI Modulation Control USCI Baud Rate 1 USCI Baud Rate 0 USCI Control 1 USCI Control 0 USCI IrDA Receive Control USCI IrDA Transmit Control USCI LIN Control	UCBI2CSA UCBI2COA UCBTXBUF UCBRXBUF UCBSTAT UCBI2CIE UCBBR1 UCBBR0 UCBCTL1 UCBCTL0 UCATXBUF UCARXBUF UCASTAT UCAMCTL UCABR1 UCABR0 UCACTL1 UCACTL0 UCAIRRCTL UCAIRTCTL UCAABCTL	011Ah 0118h 06Fh 06Eh 06Dh 06Ch 06Bh 06Ah 069h 068h 067h 066h 065h 064h 063h 062h 061h 060h 05Fh 05Eh 05Dh
Comparator_A	Comparator_A port disable Comparator_A control 2 Comparator_A control 1	CAPD CACTL2 CACTL1	05Bh 05Ah 059h

Table 6-10. Peripherals With Byte Access (continued)

MODULE	REGISTER NAME	ACRONYM	ADDRESS
BrownOUT, SVS	SVS control register (Reset by brownout signal)	SVSCTL	056h
FLL+Clock	FLL+ Control 1	FLL_CTL1	054h
	FLL+ Control 0	FLL_CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h
RTC (Basic Timer 1)	Real Time Clock Year High Byte	RTCYEARH	04Fh
	Real Time Clock Year Low Byte	RTCYEARL	04Eh
	Real Time Clock Month	RTCMON	04Dh
	Real Time Clock Day of Month	RTCDAY	04Ch
	Basic Timer1 Counter 2	BTCNT2	047h
	Basic Timer1 Counter 1	BTCNT1	046h
	Real Time Counter 4	RTCNT4	045h
	(Real Time Clock Day of Week)	(RTCDOW)	044h
	Real Time Counter 3	RTCNT3	043h
	(Real Time Clock Hour)	(RTCHOUR)	042h
	Real Time Counter 2	RTCNT2	041h
	(Real Time Clock Minute)	(RTCMIN)	040h
	Real Time Counter 1	RTCNT1	
	(Real Time Clock Second)	(RTCSEC)	
	Real Time Clock Control	RTCCTL	
	Basic Timer1 Control	BTCTL	
Port P10	Port P10 selection	P10SEL	00Fh
	Port P10 direction	P10DIR	00Dh
	Port P10 output	P10OUT	00Bh
	Port P10 input	P10IN	009h
Port P9	Port P9 selection	P9SEL	00Eh
	Port P9 direction	P9DIR	00Ch
	Port P9 output	P9OUT	00Ah
	Port P9 input	P9IN	008h
Port P8	Port P8 selection	P8SEL	03Fh
	Port P8 direction	P8DIR	03Dh
	Port P8 output	P8OUT	03Bh
	Port P8 input	P8IN	039h
Port P7	Port P7 selection	P7SEL	03Eh
	Port P7 direction	P7DIR	03Ch
	Port P7 output	P7OUT	03Ah
	Port P7 input	P7IN	038h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h

Table 6-10. Peripherals With Byte Access (continued)

MODULE	REGISTER NAME	ACRONYM	ADDRESS
Port P1	Port P1 selection Port P1 interrupt enable Port P1 interrupt-edge select Port P1 interrupt flag Port P1 direction Port P1 output Port P1 input	P1SEL P1IE P1IES P1IFG P1DIR P1OUT P1IN	026h 025h 024h 023h 022h 021h 020h
Special functions	SFR module enable 2 SFR module enable 1 SFR interrupt flag 2 SFR interrupt flag 1 SFR interrupt enable 2 SFR interrupt enable 1	ME2 ME1 IFG2 IFG1 IE2 IE1	005h 004h 003h 002h 001h 000h

6.10 Input/Output Schematics

6.10.1 Port P1, P1.0 to P1.5, Input/Output With Schmitt Trigger

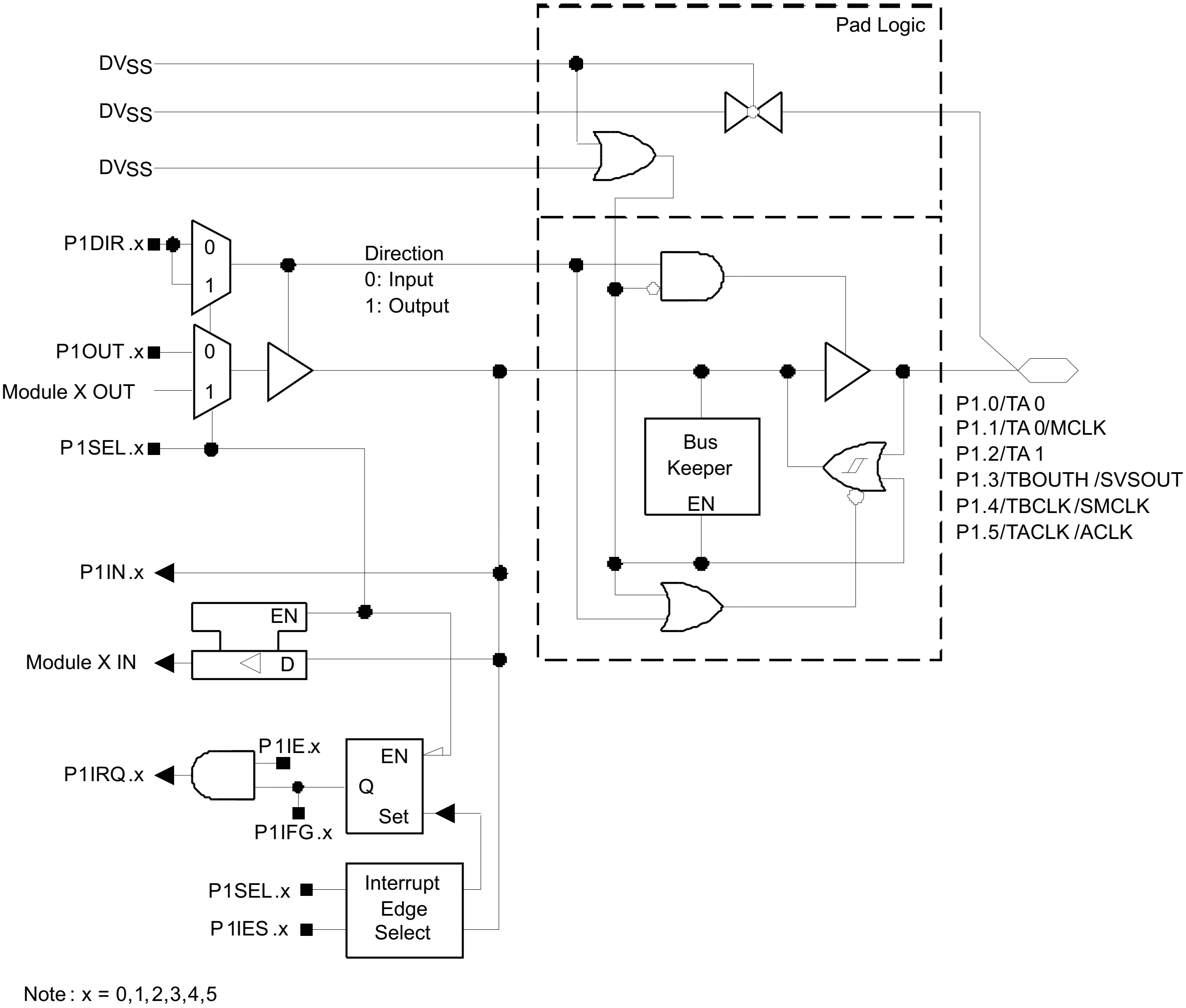
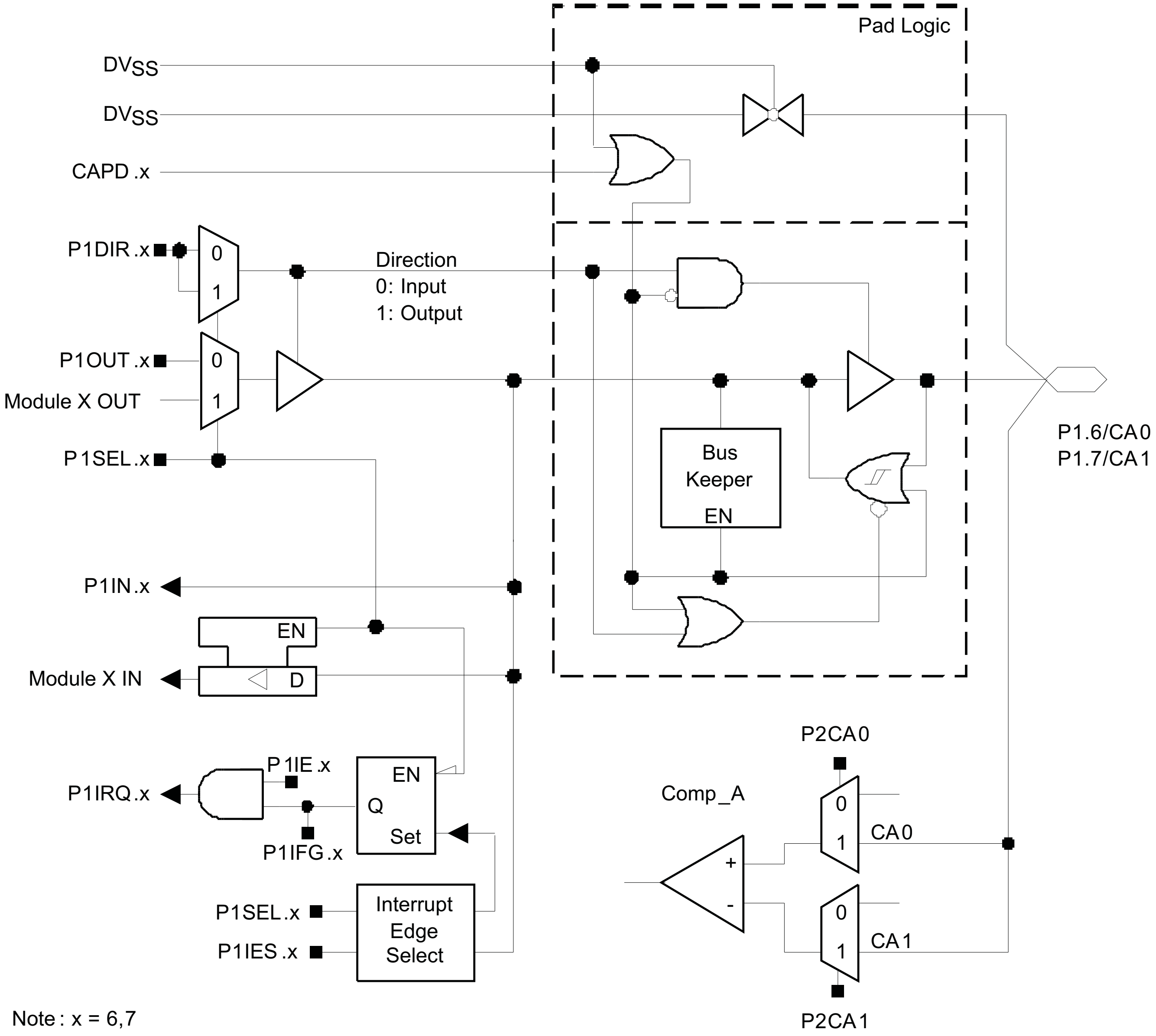


Table 6-11. Port P1 (P1.0 to P1.5) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TA0	0	P1.0 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.1/TA0/MCLK	1	P1.1 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0B	0	1
		MCLK	1	1
P1.2/TA1	2	P1.2 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI1A	0	1
		Timer_A3.TA1	1	1
P1.3/TBOUTH/SVSOUT	3	P1.3 (I/O)	I: 0; O: 1	0
		Timer_B7.TBOUTH	0	1
		SVSOUT	1	1
P1.4/TBCLK/SMCLK	4	P1.4 (I/O)	I: 0; O: 1	0
		Timer_B7.TBCLK	0	1
		SMCLK	1	1
P1.5/TACLK/ACLK	5	P1.5 (I/O)	I: 0; O: 1	0
		Timer_A3.TACLK	0	1
		ACLK	1	1

6.10.2 Port P1, P1.6, P1.7, Input/Output With Schmitt Trigger



Note: x = 6,7

Table 6-12. Port P1 (P1.6 and P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]		
			CAPD.x	P1DIR.x	P1SEL.x
P1.6/CA0	6	P1.6 (I/O)	0	I: 0; O: 1	0
		CA0	1	X	X
P1.7/CA1	7	P1.7 (I/O)	0	I: 0; O: 1	0
		CA1	1	X	X

(1) X = don't care

6.10.3 Port P2, P2.0 to P2.3, P2.6 to P2.7, Input/Output With Schmitt Trigger

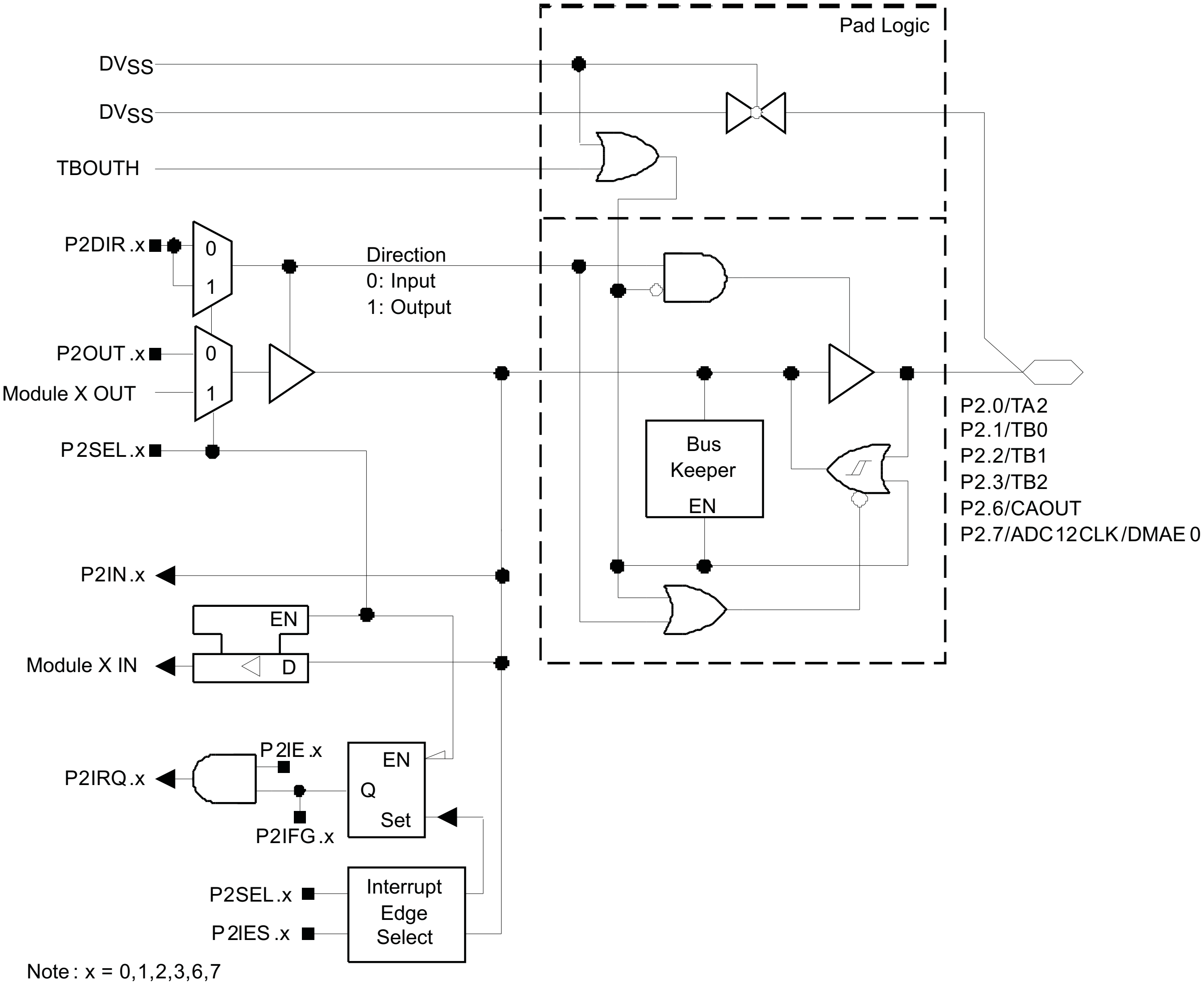
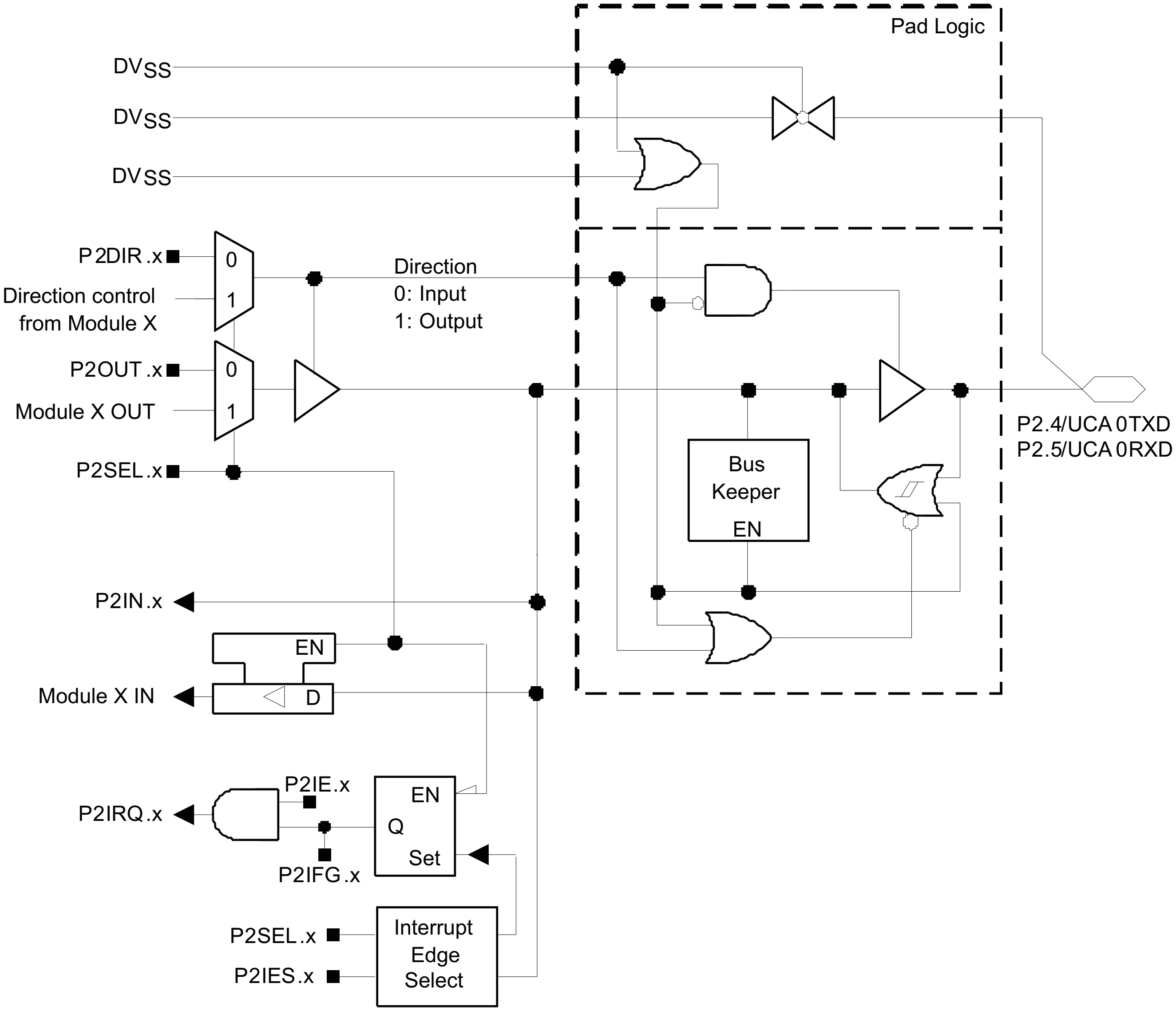


Table 6-13. Port P2 (P2.0, P2.1, P2.2, P2.3, P2.6 and P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P2DIR.x	P2SEL.x
P2.0/TA2	0	P2.0 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI2A	0	1
		Timer_A3.TA2	1	1
P2.1/TB0	1	P2.1 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI0A and Timer_B7.CCI0B	0	1
		Timer_B7.TB0 (1)	1	1
P2.2/TB1	2	P2.2 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI1A and Timer_B7.CCI1B	0	1
		Timer_B7.TB1 (1)	1	1
P2.3/TB3	3	P2.3 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI2A and Timer_B7.CCI2B	0	1
		Timer_B7.TB3 (1)	1	1
P2.6/CAOUT	6	P2.6 (I/O)	I: 0; O: 1	0
		CAOUT	1	1
P2.7/ADC12CLK/DMAE0	7	P2.7 (I/O)	I: 0; O: 1	0
		ADC12CLK	1	1
		DMAE0	0	1

(1) Setting TBOUTH causes all Timer_B outputs to be set to high impedance.

6.10.4 Port P2, P2.4 to P2.5, Input/Output With Schmitt Trigger



Note: x = 4,5

Table 6-14. Port P2 (P2.4 and P2.5) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]	
			P2DIR.x	P2SEL.x
P2.4/UCA0TXD	4	P2.4 (I/O)	I: 0; O: 1	0
		USCI_A0.UCA0TXD [2]	X	1
P2.5/UCA0RXD	5	P2.5 (I/O)	I: 0; O: 1	0
		USCI_A0.UCA0RXD [2]	X	1

(1) X = don't care
(2) When in USCI mode, P2.4 is set to output, P2.5 is set to input.

6.10.5 Port P3, P3.0 to P3.3, Input/Output With Schmitt Trigger

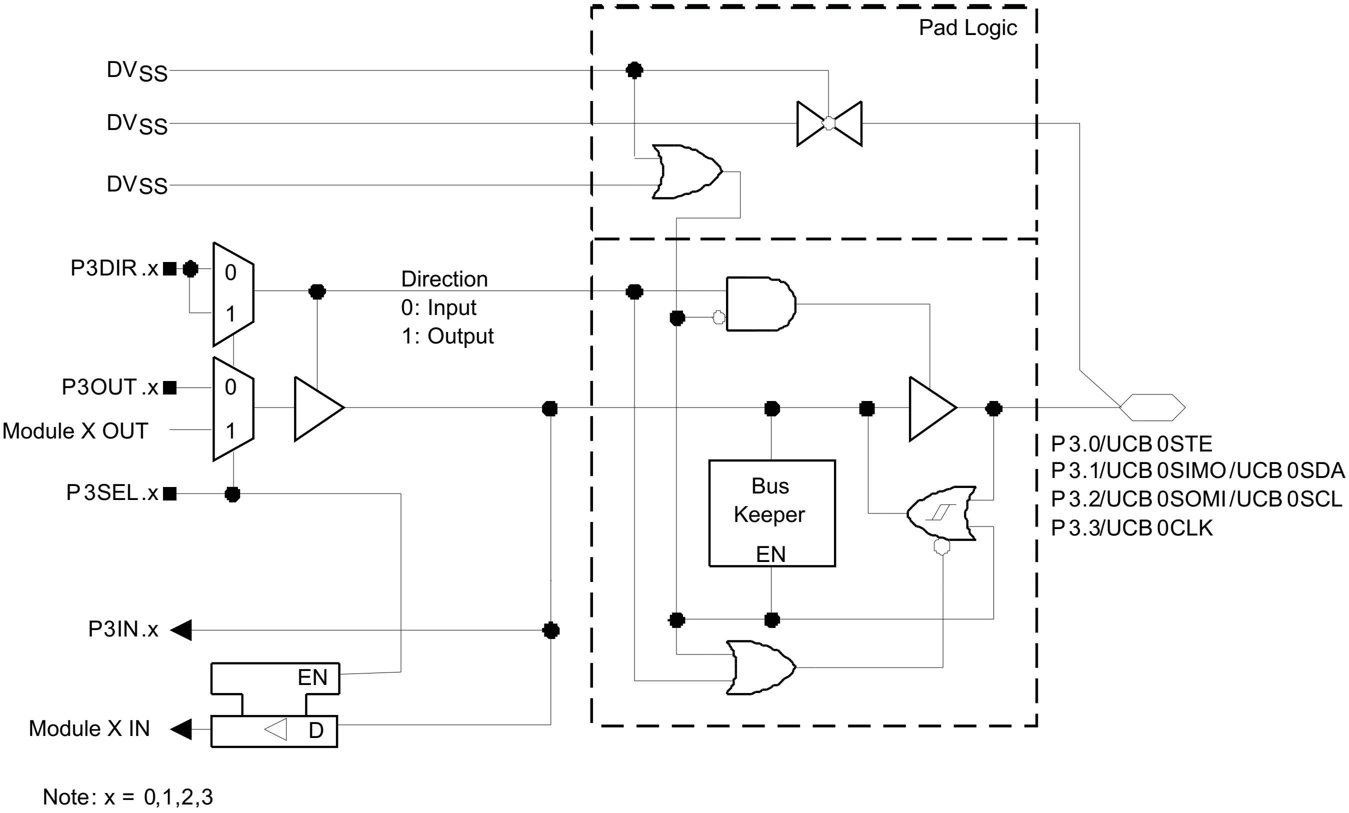
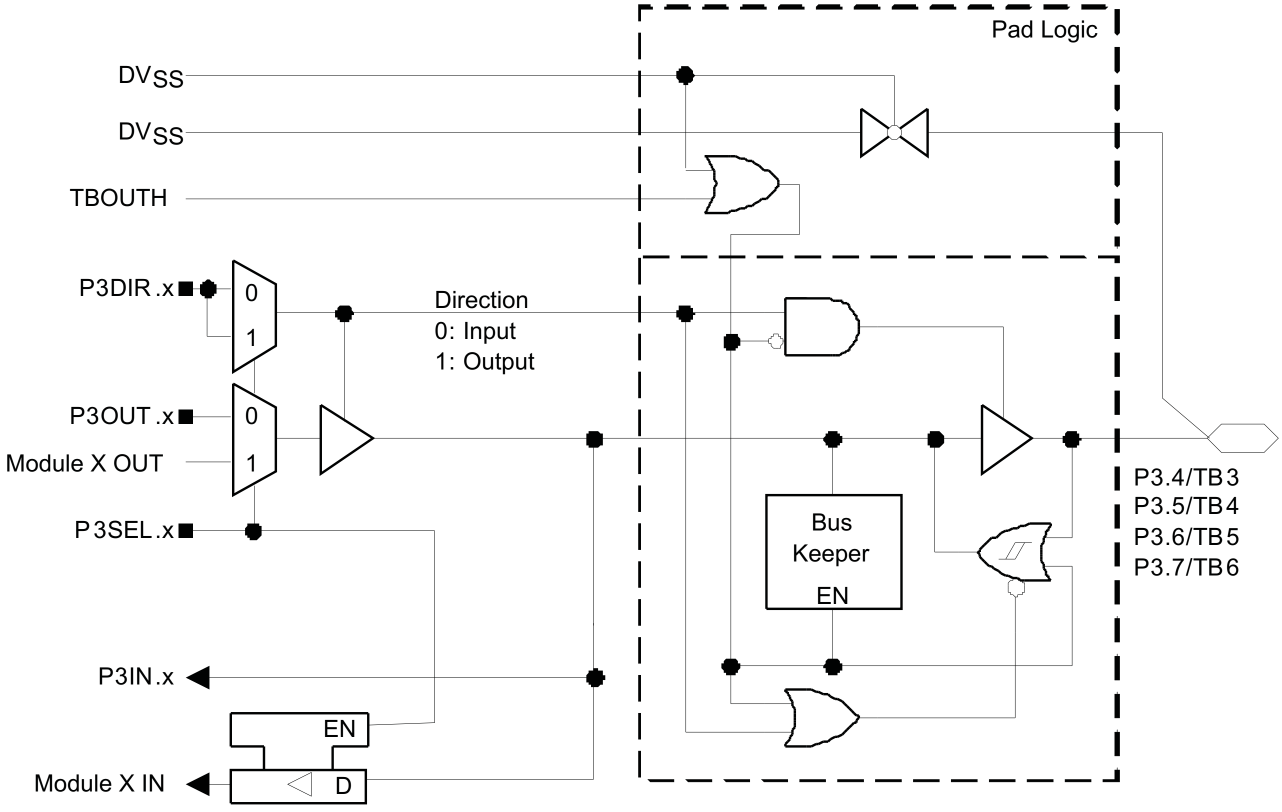


Table 6-15. Port P3 (P3.0 to P3.3) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[(1)]	
			P3DIR.x	P3SEL.x
P3.0/UCB0STE	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0STE (2)	X	1
P3.1/UCB0SIMO/UCB0SDA	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA (2) (3)	X	1
P3.2/UCB0SOMI/UCB0SCL	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL (2) (3)	X	1
P3.3/UCB0CLK	3	P3.3 (I/O)	I: 0; O: 1	0
		UCB0CLK (2)	X	1

(1) X = don't care
(2) The pin direction is controlled by the USCI module.
(3) If the I^2C functionality is selected the output drives only the logical 0 to V_{SS} level.

6.10.6 Port P3, P3.4 to P3.7, Input/Output With Schmitt Trigger



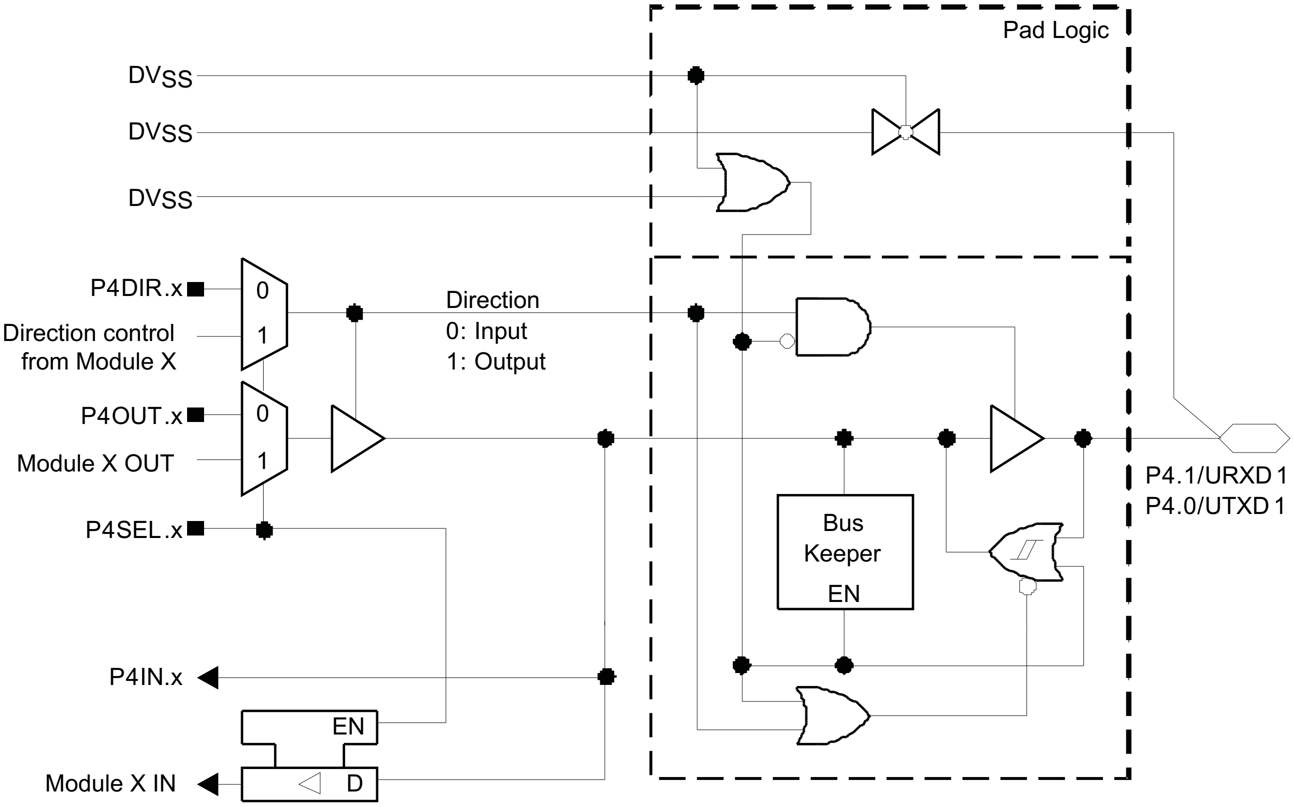
Note: x = 4,5,6,7

Table 6-16. Port P3 (P3.4 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P3DIR.x	P3SEL.x
P3.4/TB3	4	P3.4 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI3A and Timer_B7.CCI3B	0	1
		Timer_B7.TB3[1]	1	1
P3.5/TB4	5	P3.5 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI4A and Timer_B7.CCI4B	0	1
		Timer_B7.TB4 [1]	1	1
P3.6/TB5	6	P3.6 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI5A and Timer_B7.CCI5B	0	1
		Timer_B7.TB5[1]	1	1
P3.7/TB6	7	P3.7 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI6A and Timer_B7.CCI6B	0	1
		Timer_B7.TB6[1]	1	1

(1) Setting TBOUTH causes all Timer_B outputs to be set to high impedance.

6.10.7 Port P4, P4.0 to P4.1, Input/Output With Schmitt Trigger



Note: x = 0,1

Table 6-17. Port P4 (P4.0 to P4.1) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]	
			P4DIR.x	P4SEL.x
P4.0/UTXD1	0	P4.0 (I/O)	I: 0; O: 1	0
		USART1.UTXD1 [2]	X	1
P4.1/URXD1	1	P4.1 (I/O)	I: 0; O: 1	0
		USART1.URXD1 [2]	X	1

(1) X = don't care
(2) When in USART1 mode, P4.0 is set to output, P4.1 is set to input.

6.10.8 Port P4, P4.2 to P4.7, Input/Output With Schmitt Trigger

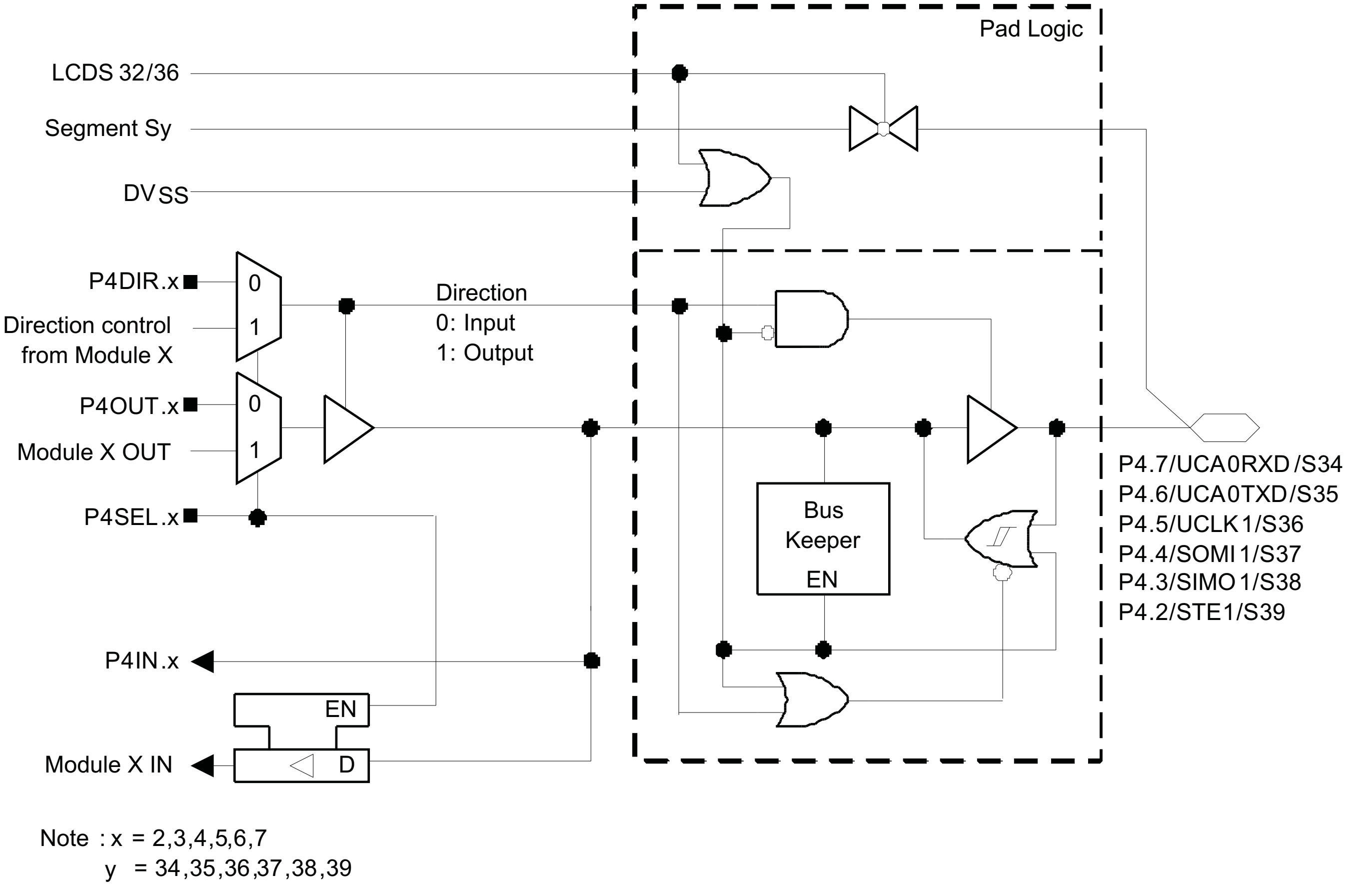


Table 6-18. Port P4 (P4.2 to P4.5) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]		
			P4DIR.x	P4SEL.x	LCDS36
P4.2/STE1/S39	2	P4.2 (I/O)	I: 0; O: 1	0	0
		USART1.STE1	X	1	0
		S39	X	X	1
P4.3/SIMO/S38	3	P4.3 (I/O)	I: 0; O: 1	0	0
		USART1.SIMO1 [2]	X	1	0
		S38	X	X	1
P4.4/SOMI/S37	4	P4.4 (I/O)	I: 0; O: 1	0	0
		USART1.SOMI1 [2]	X	1	0
		S37	X	X	1
P4.5/SOMI/S36	5	P4.5 (I/O)	I: 0; O: 1	0	0
		USART1.UCLK1 [2]	X	1	0
		S36	X	X	1

(1) X = don't care
(2) The pin direction is controlled by the USART1 module.

Table 6-19. Port P4 (P4.6 and P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P4DIR.x	P4SEL.x	LCDS32
P4.6/UCA0TXD/S35	6	P4.6 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0TXD (2)	X	1	0
		S35	X	X	1
P4.7/UCA0RXD/S34	7	P4.7 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0RXD (2)	X	1	0
		S34	X	X	1

(1) X = don't care
(2) When in USCI mode, P4.6 is set to output, P4.7 is set to input.

6.10.9 Port P5, P5.0, Input/Output With Schmitt Trigger

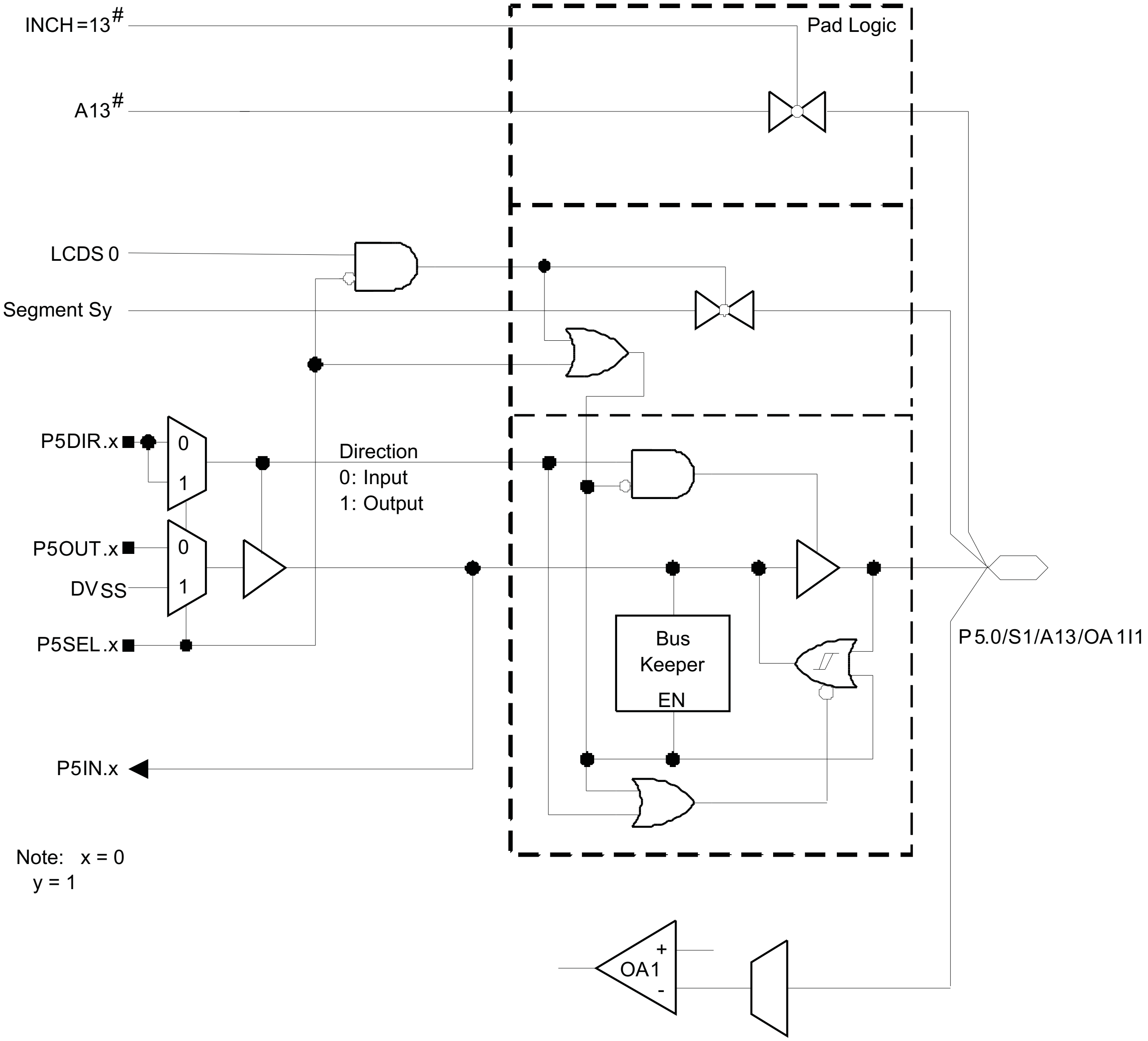


Table 6-20. Port P5 (P5.0) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)				
			P5DIR.x	P5SEL.x	INCHx	OAPx (OA1) OANx (OA1)	LCDS0
P5.0/S1/A13/OA1I1	0	P5.0 (I/O)	I: 0; O: 1	0	X	X	0
		OAI11	0	X	X	1	0
		A13 (2)	X	1	13	X	X
		S1 enabled	X	0	X	X	1
		S1 disabled	X	1	X	X	1

(1) X = don't care
(2) Setting the P5SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

6.10.10 Port P5, P5.1, Input/Output With Schmitt Trigger

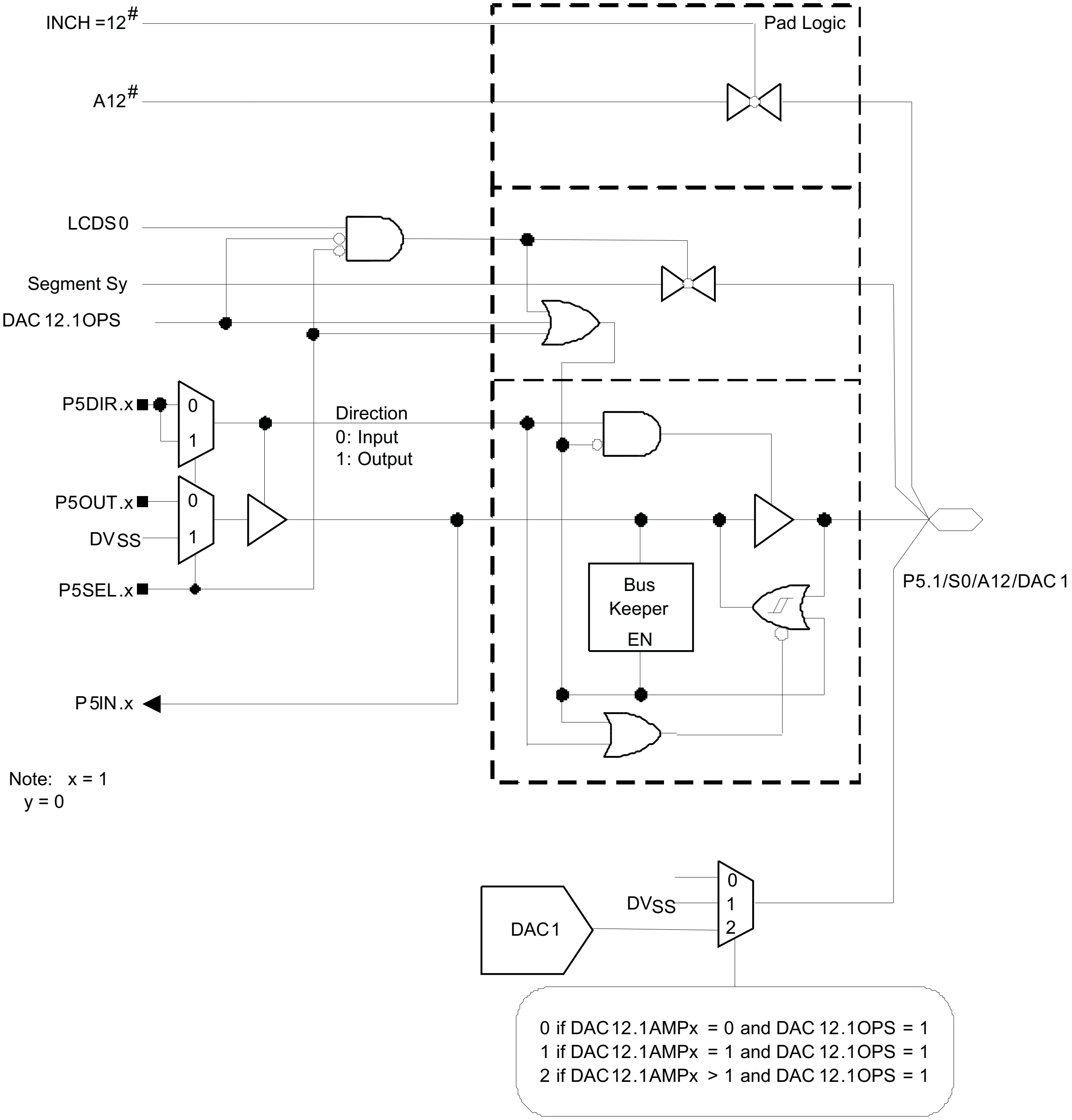


Table 6-21. Port P5 (P5.1) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]					
			P5DIR.x	P5SEL.x	INCHx	DAC12.1OPS	DAC12.1AMPx	LCDS0
P5.1/S0/A12/DAC1	1	P5.1 (I/O)	I: 0; O: 1	0	X	0	X	0
		DAC1 high impedance	X	X	X	1	0	X
		DVSS	X	X	X	1	1	X
		DAC1 output	X	X	X	1	>1	X
		A12 [2]	X	1	12	0	X	0
		S0 enabled	X	0	X	0	X	1
		S0 disabled	X	1	X	0	X	1

(1) X = don't care
(2) Setting the P5SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

6.10.11 Port P5, P5.2 to P5.4, Input/Output With Schmitt Trigger

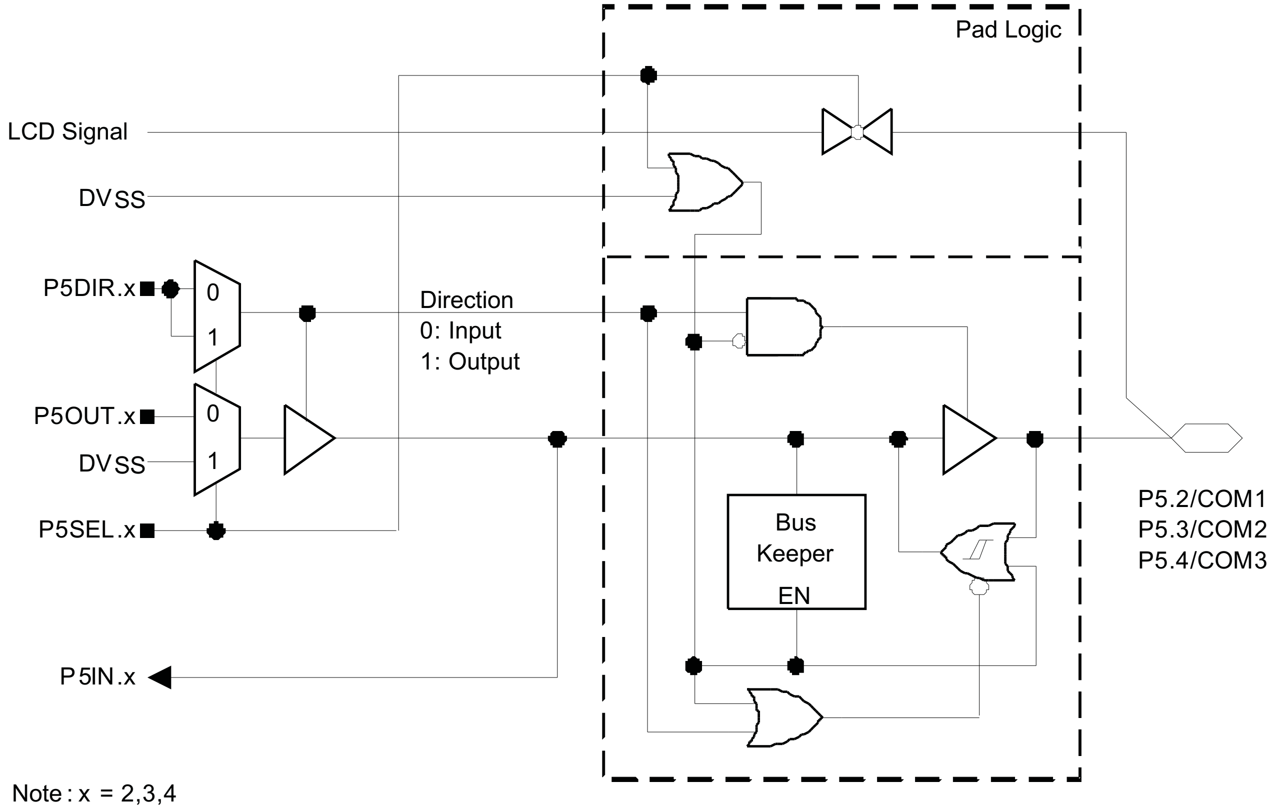


Table 6-22. Port P5 (P5.2 to P5.4) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]	
			P5DIR.x	P5SEL.x
P5.2/COM1	2	P5.2 (I/O)	I: 0; O: 1	0
		COM1	X	1
P5.3/COM2	3	P5.3 (I/O)	I: 0; O: 1	0
		COM2	X	1
P5.4/COM3	4	P5.4 (I/O)	I: 0; O: 1	0
		COM3	X	1

(1) X = don't care

6.10.12 Port P5, P5.5 to P5.7, Input/Output With Schmitt Trigger

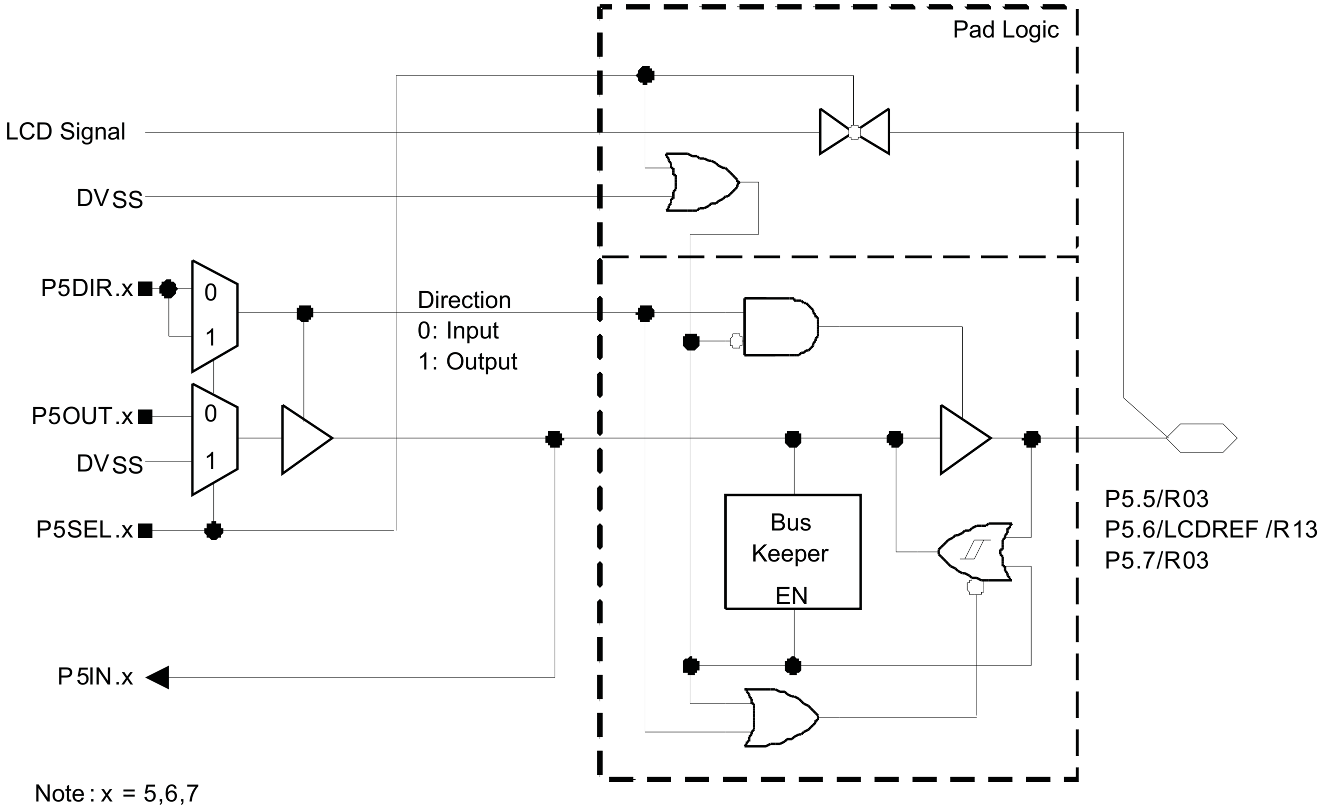


Table 6-23. Port P5 (P5.5 to P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]	
			P5DIR.x	P5SEL.x
P5.5/R03	5	P5.5 (I/O)	I: 0; O: 1	0
		R03	X	1
P5.6/LCDREF/R13	6	P5.6 (I/O)	I: 0; O: 1	0
		R13 or LCDREF [2]	X	1
P5.7/R03	7	P5.7 (I/O)	I: 0; O: 1	0
		R03	X	1

(1) X = don't care
(2) External reference for the LCD_A charge pump is applied when VLCDREFx = 01. Otherwise R13 is selected.

6.10.13 Port P6, P6.0, P6.2, and P6.4, Input/Output With Schmitt Trigger

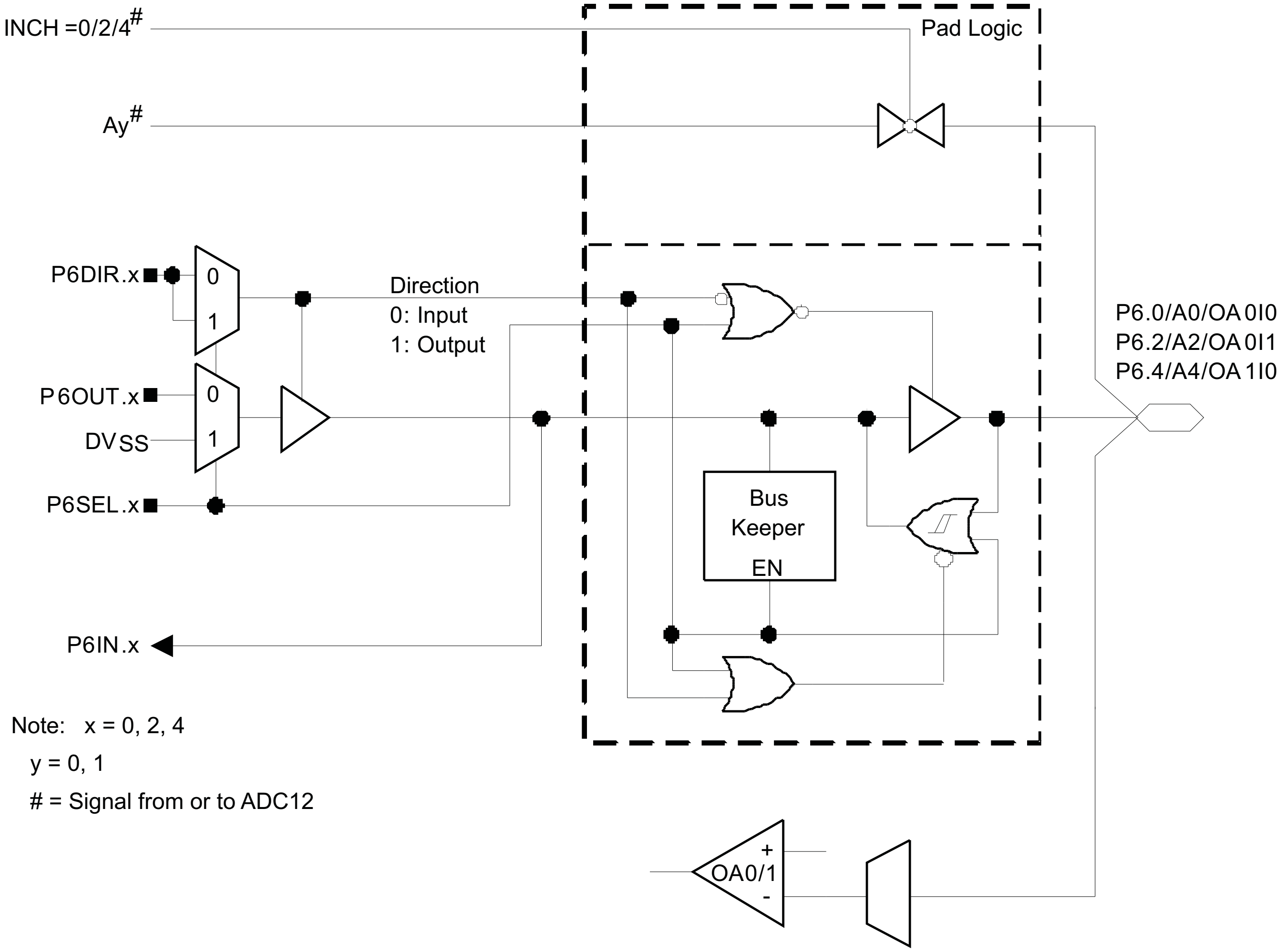
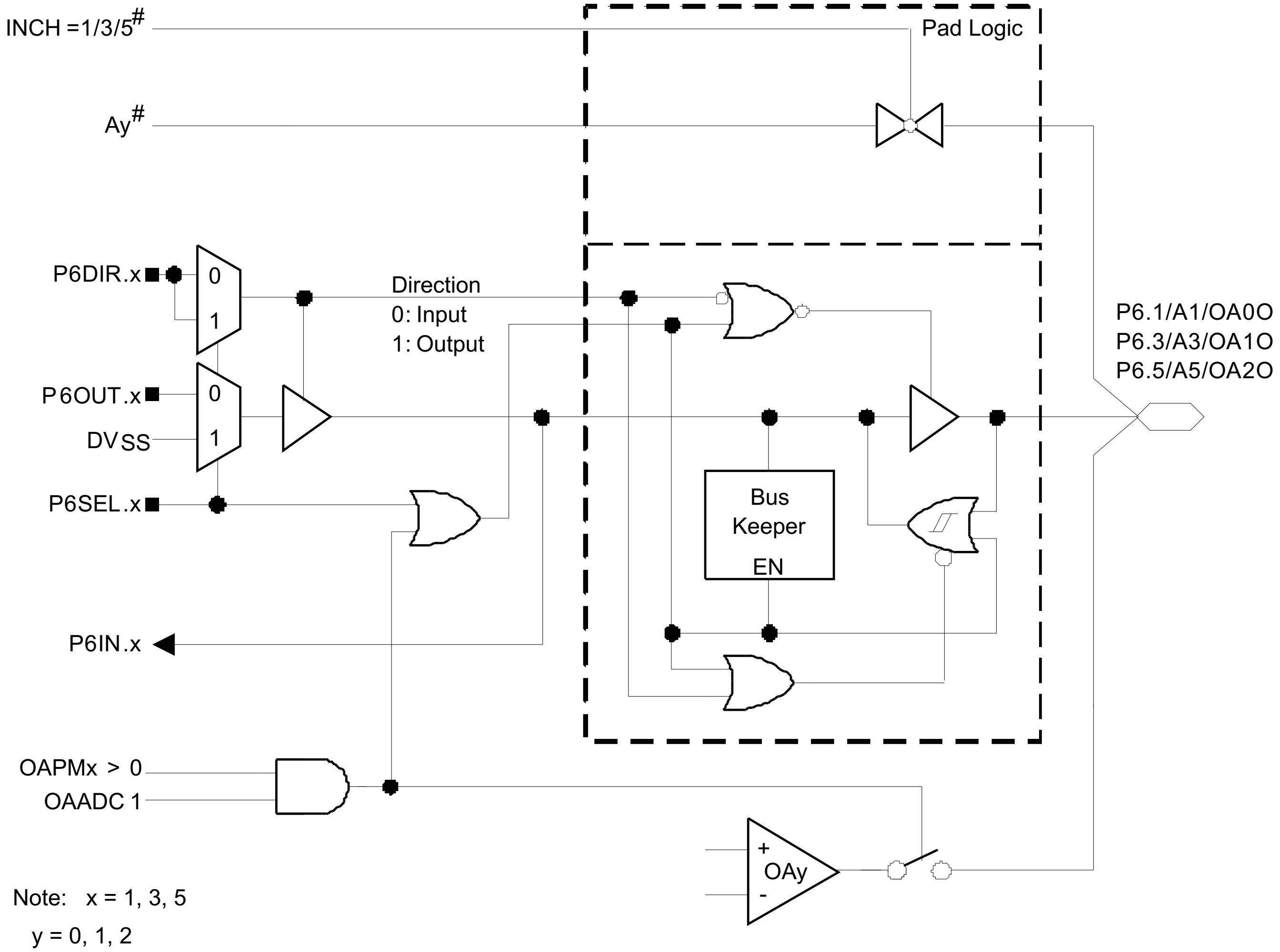


Table 6-24. Port P6 (P6.0, P6.2, and P6.4) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)				
			P6DIR.x	P6SEL.x	OAPx (OA0) OANx (OA0)	OAPx (OA1) OANx (OA1)	INCHx
P6.0/A0/OA0I0	0	P6.0 (I/O)	I: 0; O: 1	0	X	X	X
		OA0I0	0	X	0	X	X
		A0 (2)	X	1	X	X	0
P6.2/A2/OA0I1	2	P6.2 (I/O)	I: 0; O: 1	0	X	X	X
		OA0I1	0	X	1	X	X
		A2 (2)	X	1	X	X	2
P6.4/A4/OA1I0	4	P6.4 (I/O)	I: 0; O: 1	0	X	X	X
		OA1I0	0	X	X	0	X
		A4 (2)	X	1	X	X	4

(1) X = don't care
(2) Setting the P6SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

6.10.14 Port P6, P6.1, P6.3, and P6.5 Input/Output With Schmitt Trigger



Note: x = 1, 3, 5
y = 0, 1, 2
# = Signal from or to ADC12

Table 6-25. Port P6 (P6.1, P6.3, and P6.5) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)				
			P6DIR.x	P6SEL.x	OAADC1	OAPMx	INCHx
P6.1/A1/OA0O	1	P6.1 (I/O)	I: 0; O: 1	0	X	0	X
		OA0O (2)	X	X	1	>0	X
		A1 (3)	X	1	X	0	1
P6.3/A3/OA1O	3	P6.3 (I/O)	I: 0; O: 1	0	X	0	X
		OA1O (2)	X	X	1	>0	X
		A3 (3)	X	1	X	0	3
P6.5/A5/OA2O	5	P6.5 (I/O)	I: 0; O: 1	0	X	0	X
		OA2O (2)	X	X	1	>0	X
		A5 (3)	X	1	X	0	5

(1) X = don't care
(2) Setting the OAADC1 bit or setting OAFCx = 00 will cause the operational amplifier to be present at the pin as well as internally connected to the corresponding ADC12 input.
(3) Setting the P6SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

6.10.15 Port P6, P6.6, Input/Output With Schmitt Trigger

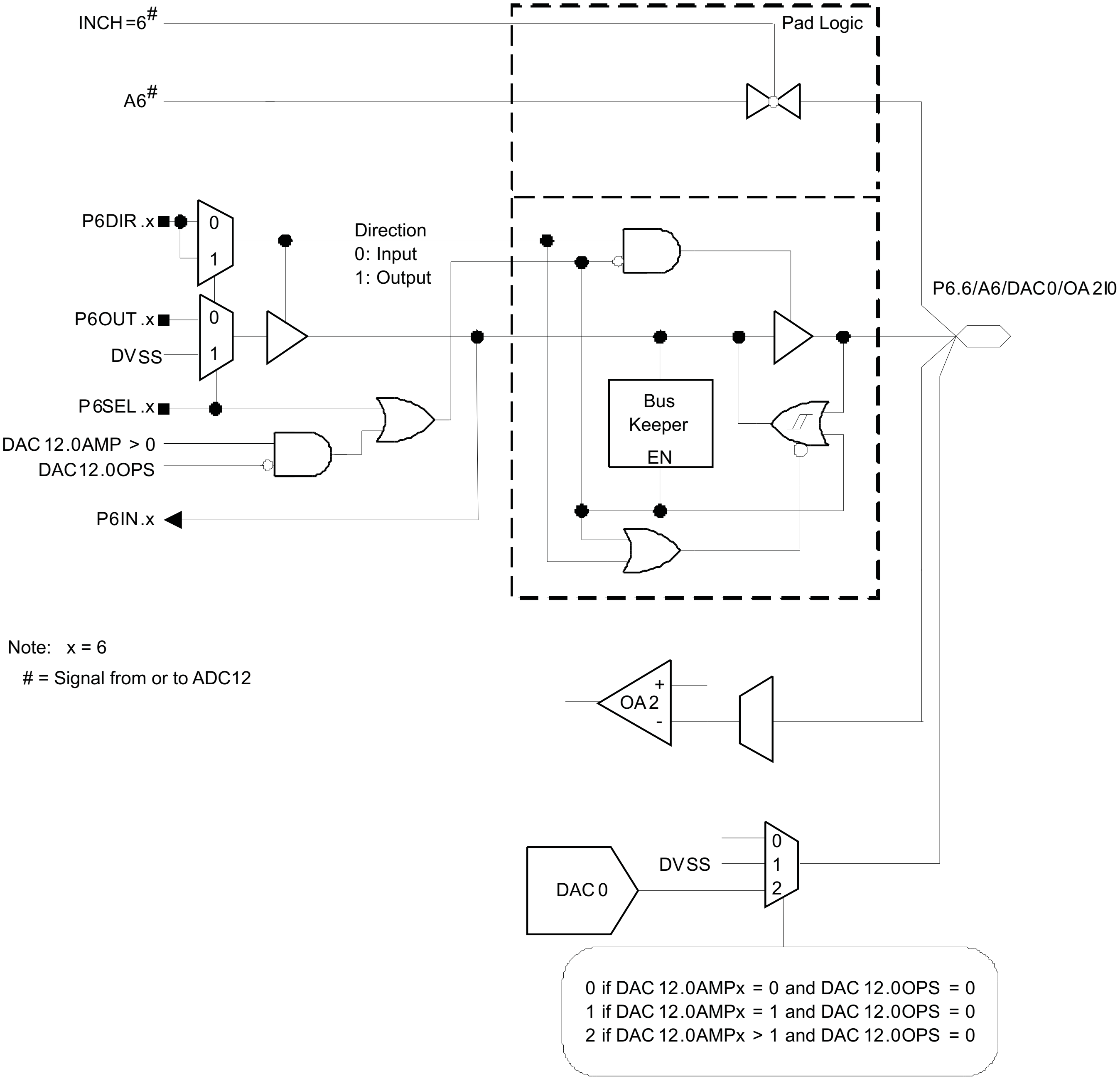
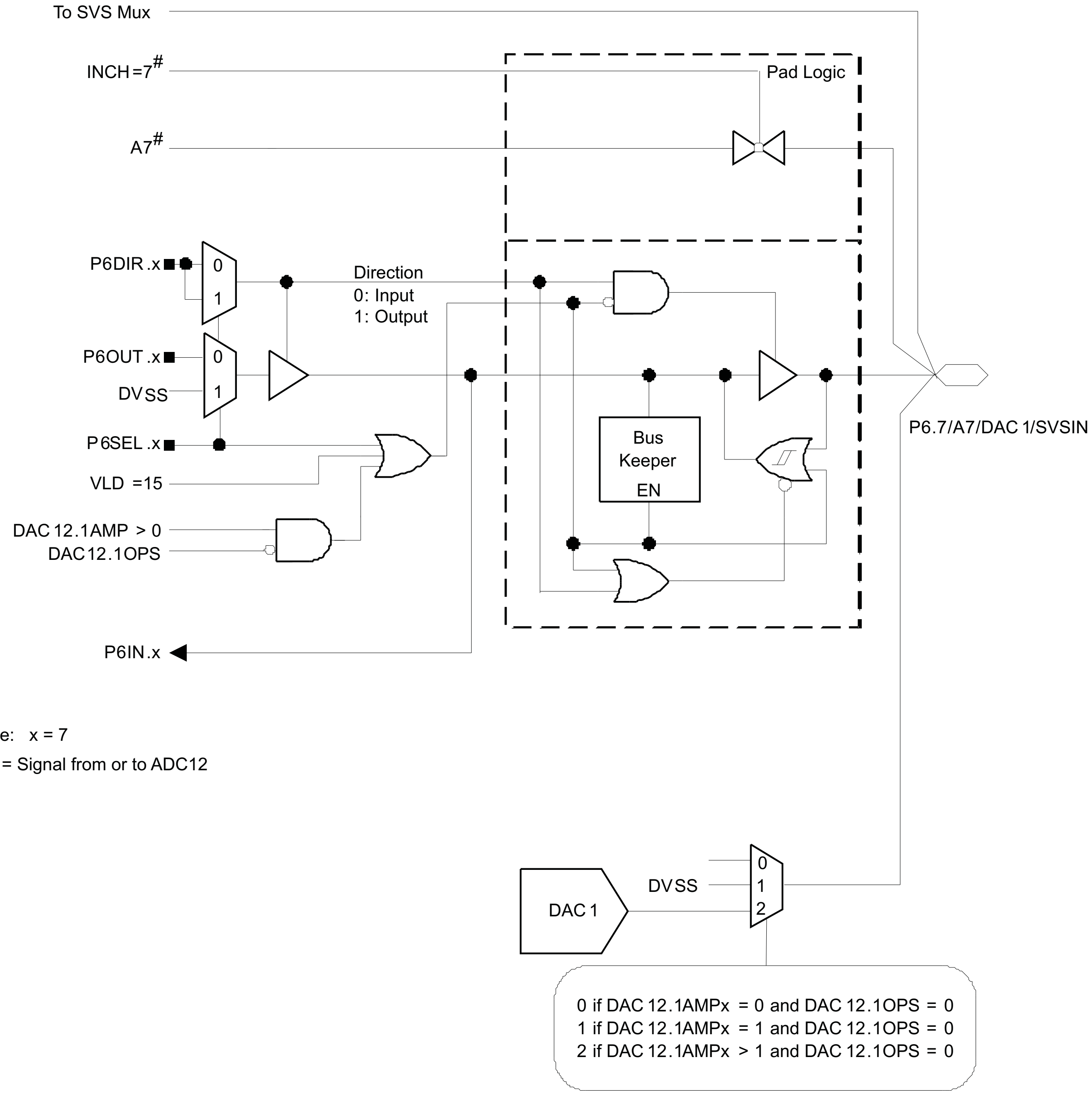


Table 6-26. Port P6 (P6.6) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)					
			P6DIR.x	P6SEL.x	INCHx	DAC12.0OPS	DAC12.0AMPx	OAPx (OA2) OANx (OA2)
P6.6/A6/DAC0/OA2I0	6	P6.6 (I/O)	I: 0; O: 1	0	X	1	X	X
		DAC0 high impedance	X	X	X	0	0	X
		DVSS	X	X	X	0	1	X
		DAC0 output	X	X	X	0	>1	X
		A6 (2)	X	1	6	X	X	X
		OA2I0	0	X	0	X	X	0

(1) X = don't care
(2) Setting the P6SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

6.10.16 Port P6, P6.7, Input/Output With Schmitt Trigger



Note: x = 7

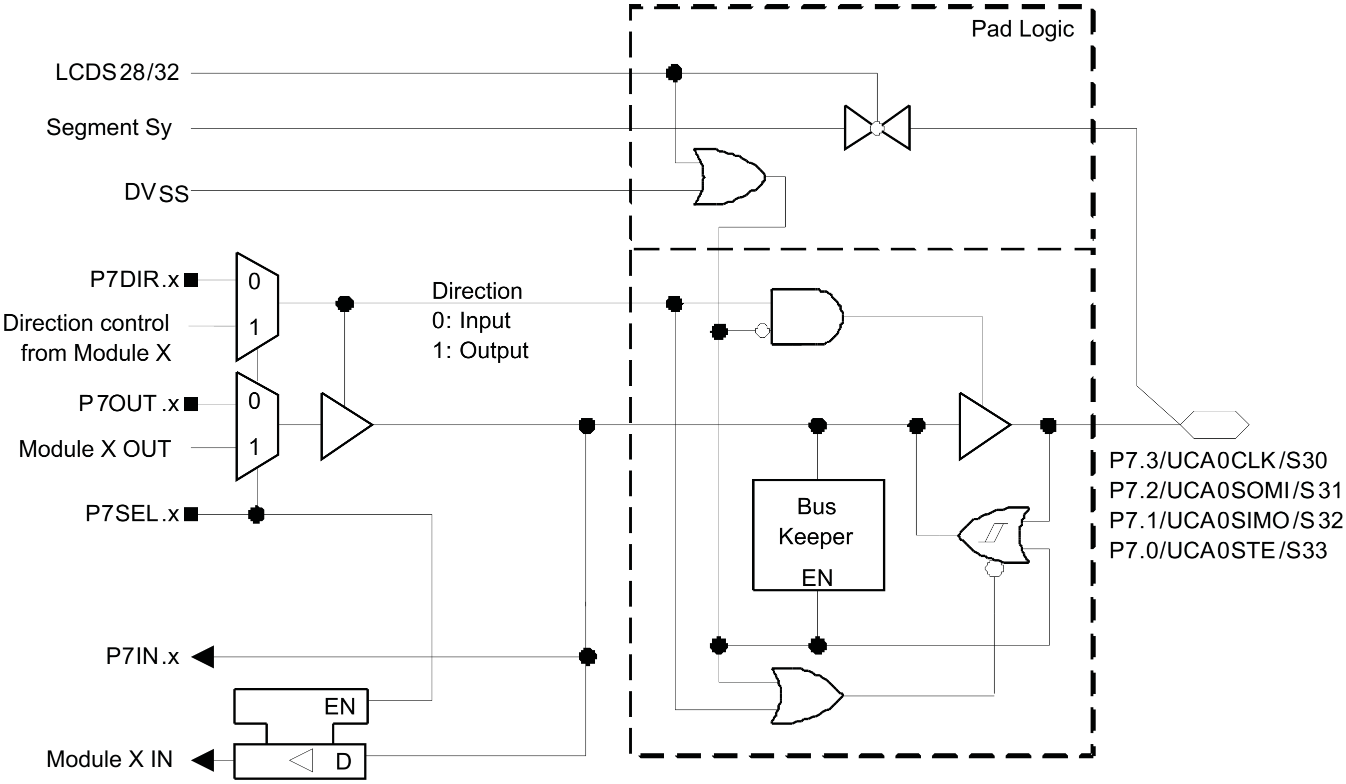
= Signal from or to ADC12

Table 6-27. Port P6 (P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]				
			P6DIR.x	P6SEL.x	INCHx	DAC12.1OPS	DAC12.1AMPx
P6.7/A7/DAC1/SVSIN	7	P6.7 (I/O)	I: 0; O: 1	0	X	1	X
		DAC1 high impedance	X	X	X	0	0
		DVSS	X	X	X	0	1
		DAC1 output	X	X	X	0	>1
		A7 [2]	X	1	7	X	X
		SVSIN [2]	0	1	0	1	X

(1) X = don't care
(2) Setting the P6SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

6.10.17 Port P7, P7.0 to P7.3, Input/Output With Schmitt Trigger



Note: x = 0, 1, 2, 3
y = 30, 31, 32, 33

Table 6-28. Port P7 (P7.0 and P7.1) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P7DIR.x	P7SEL.x	LCDS32
P7.0/UCA0STE/S33	0	P7.0 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0STE (2)	X	1	0
		S33(1)	X	X	1
P7.1/UCA0SIMO/S32	1	P7.1 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0SIMO (2)	X	1	0
		S32	X	X	1

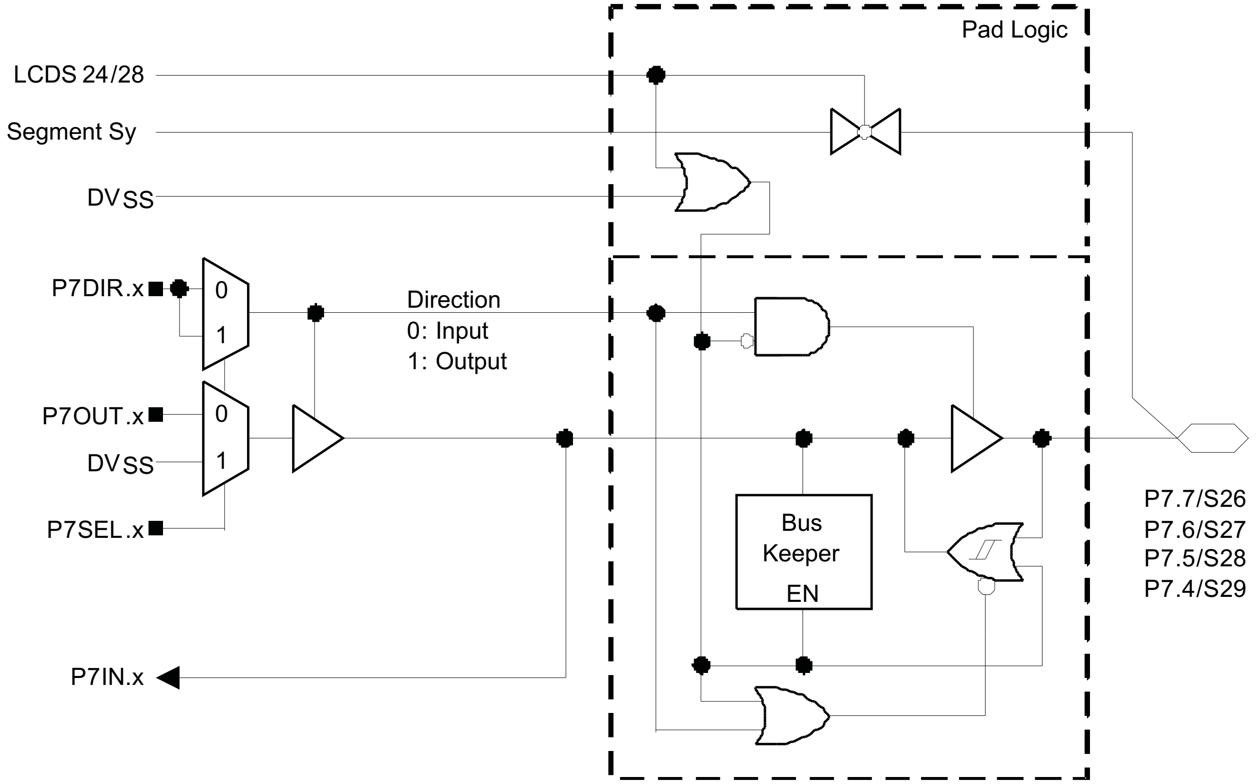
(1) X = don't care
(2) The pin direction is controlled by the USCI module.

Table 6-29. Port P7 (P7.2 and P7.3) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P7DIR.x	P7SEL.x	LCDS28
P7.2/UCA0SOMI/S31	2	P7.2 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0SOMI (2)	X	1	0
		S31	X	X	1
P7.3/UCA0CLK/S30	3	P7.3 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0CLK (2)	X	1	0
		S30	X	X	1

(1) X = don't care
(2) The pin direction is controlled by the USCI module.

6.10.18 Port P7, P7.4 to P7.7, Input/Output With Schmitt Trigger



Note: x = 4, 5, 6, 7
y = 26, 27, 28, 29

Table 6-30. Port P7 (P7.4 and P7.5) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P7DIR.x	P7SEL.x	LCDS28
P7.4/S29	4	P7.4 (I/O)	I: 0; O: 1	0	0
		S29	X	X	1
P7.5/S28	5	P7.5 (I/O)	I: 0; O: 1	0	0
		S28	X	X	1

(1) X = don't care

Table 6-31. Port P7 (P7.6 and P7.7) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P7DIR.x	P7SEL.x	LCDS24
P7.6/S27	6	P7.6 (I/O)	I: 0; O: 1	0	0
		S27	X	X	1
P7.7/S26	7	P7.7 (I/O)	I: 0; O: 1	0	0
		S26	X	X	1

(1) X = don't care

6.10.19 Port P8, P8.0 to P8.7, Input/Output With Schmitt Trigger

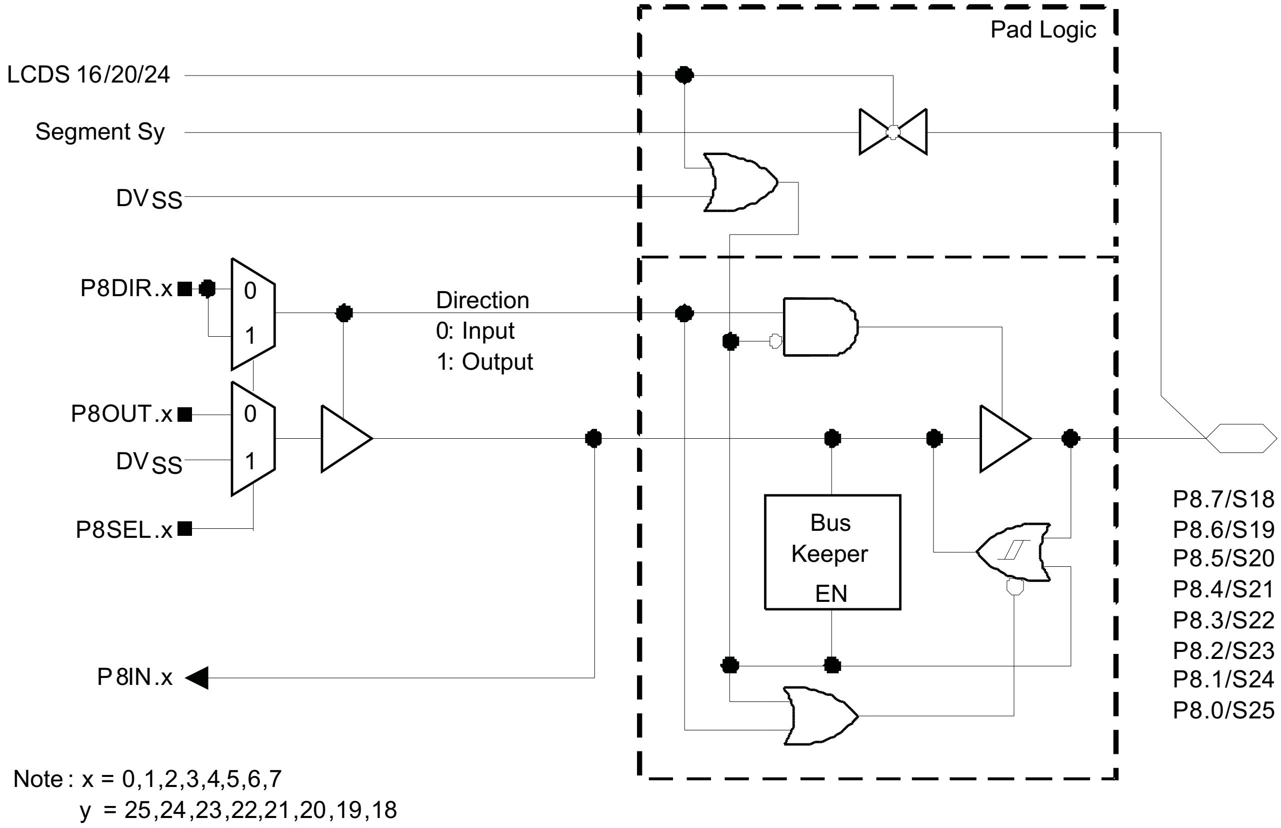


Table 6-32. Port P8 (P8.0 and P8.1) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]		
			P8DIR.x	P8SEL.x	LCDS16
P8.0/S18	0	P8.0 (I/O)	I: 0; O: 1	0	0
		S18	X	X	1
P8.1/S19	0	P8.0 (I/O)	I: 0; O: 1	0	0
		S19	X	X	1

(1) X = don't care

Table 6-33. Port P8 (P8.2 to P8.5) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]		
			P8DIR.x	P8SEL.x	LCDS20
P8.2/S20	2	P8.2 (I/O)	I: 0; O: 1	0	0
		S20	X	X	1
P8.3/S21	3	P8.3 (I/O)	I: 0; O: 1	0	0
		S21	X	X	1
P8.4/S22	4	P8.4 (I/O)	I: 0; O: 1	0	0
		S22	X	X	1
P8.5/S23	5	P8.5 (I/O)	I: 0; O: 1	0	0
		S23	X	X	1

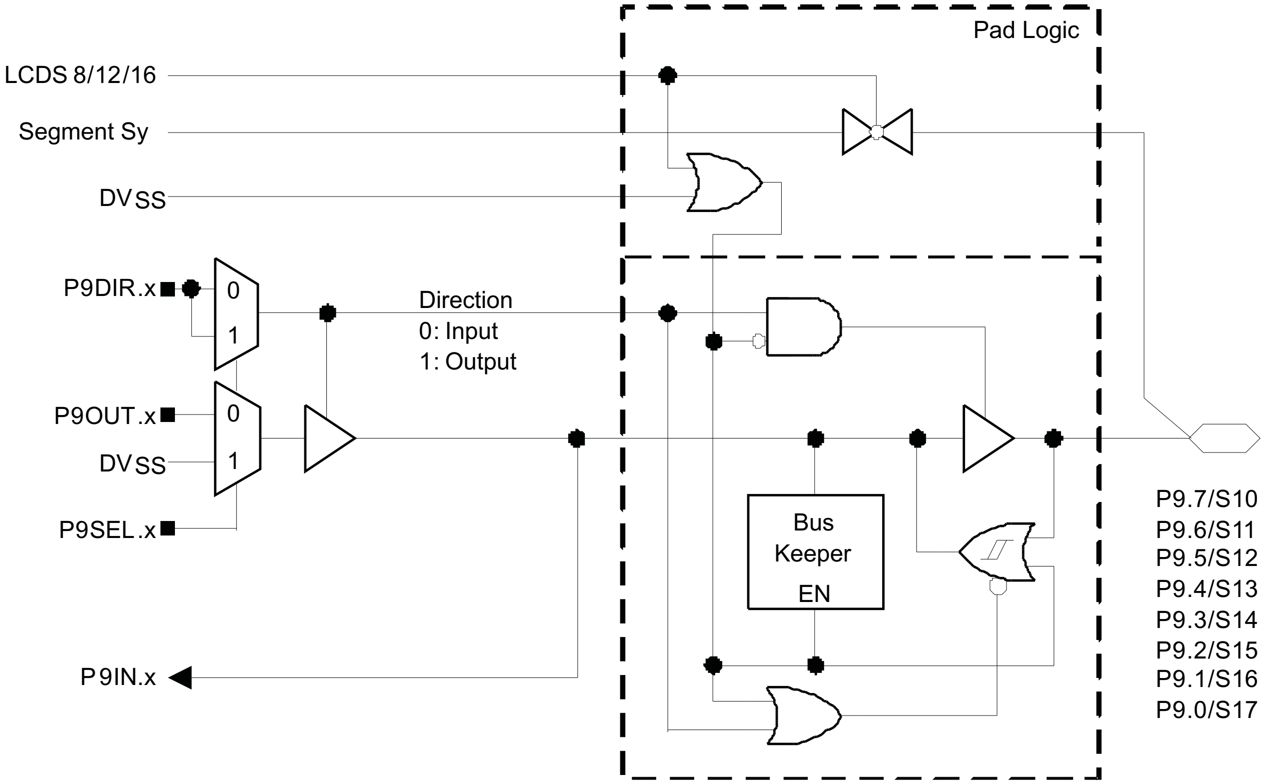
(1) X = don't care

Table 6-34. Port P8 (P8.6 and P8.7) Pin Functions

PIN NAME (P8.x)	X	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P8DIR.x	**P8SEL.x**	**LCDS24**
P8.6/S24	6	P8.6 (I/O)	I: 0; O: 1	0	0
		S24	X	X	1
P8.7/S25	7	P8.7 (I/O)	I: 0; O: 1	0	0
		S25	X	X	1

(1) X = don't care

6.10.20 Port P9, P9.0 to P9.7, Input/Output With Schmitt Trigger



Note : x = 0,1,2,3,4,5,6,7
y = 17,16,15,14,13,12,11,10

Table 6-35. Port P9 (P9.0 and P9.1) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P9DIR.x	P9SEL.x	LCDS16
P9.0/S17	0	P9.0 (I/O)	I: 0; O: 1	0	0
		S17	X	X	1
P9.1/S16	1	P9.1 (I/O)	I: 0; O: 1	0	0
		S16	X	X	1

(1) X = don't care

Table 6-36. Port P9 (P9.2 to P9.5) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P9DIR.x	P9SEL.x	LCDS12
P9.2/S15	2	P9.2 (I/O)	I: 0; O: 1	0	0
		S15	X	X	1
P9.3/S14	3	P9.3 (I/O)	I: 0; O: 1	0	0
		S14	X	X	1
P9.4/S13	4	P9.4 (I/O)	I: 0; O: 1	0	0
		S13	X	X	1
P9.5/S12	5	P9.5 (I/O)	I: 0; O: 1	0	0
		S12	X	X	1

(1) X = don't care

Table 6-37. Port P9 (P9.6 and P9.7) Pin Functions

PIN NAME (P9.x	x	FUNCTION	CONTROL BITS OR SIGNALS[1]		
			P9DIR.x	P9SEL.x	LCDS8
P9.6/S11	6	P9.6 (I/O)	I: 0; O: 1	0	0
		S11	X	X	1
P9.7/S10	7	P9.7 (I/O)	I: 0; O: 1	0	0
		S10	X	X	1

(1) X = don't care

6.10.21 Port P10, P10.0 to P10.5, Input/Output With Schmitt Trigger

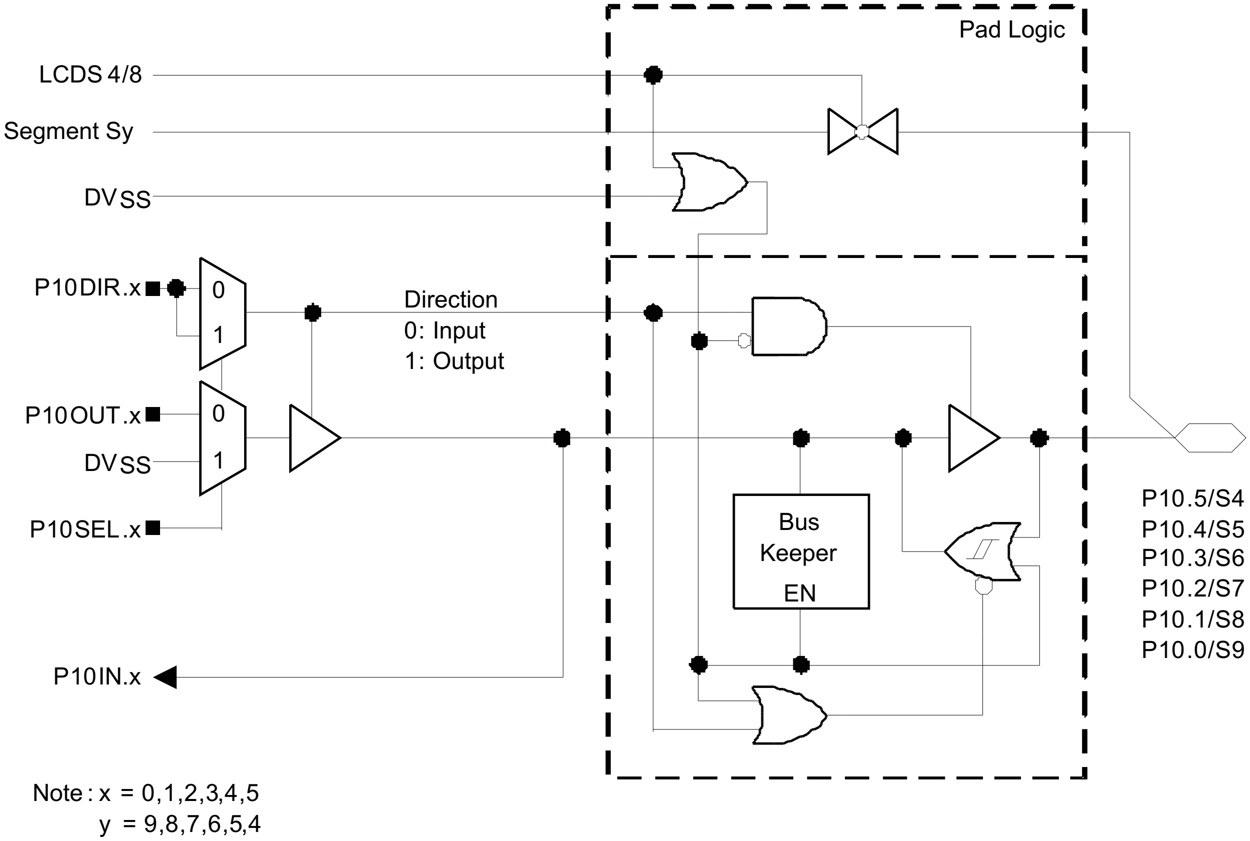


Table 6-38. Port P10 (P10.0 and P10.1) Pin Functions

PIN NAME (P10.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P10DIR.x	P10SEL.x	LCDS8
P10.0/S9	0	P10.0 (I/O)	I: 0; O: 1	0	0
		S9	X	X	1
P10.1/S8	1	P10.1 (I/O)	I: 0; O: 1	0	0
		S8	X	X	1

(1) X = don't care

Table 6-39. Port P10 (P10.2 to P10.5) Pin Functions

PIN NAME (P10.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P10DIR.x	P10SEL.x	LCDS4
P10.2/S7	2	P10.2 (I/O)	I: 0; O: 1	0	0
		S7	X	X	1
P10.3/S6	3	P10.3 (I/O)	I: 0; O: 1	0	0
		S6	X	X	1
P10.4/S5	4	P10.4 (I/O)	I: 0; O: 1	0	0
		S5	X	X	1
P10.5/S4	5	P10.5 (I/O)	I: 0; O: 1	0	0
		S4	X	X	1

(1) X = don't care

6.10.22 Port P10, P10.6, Input/Output With Schmitt Trigger

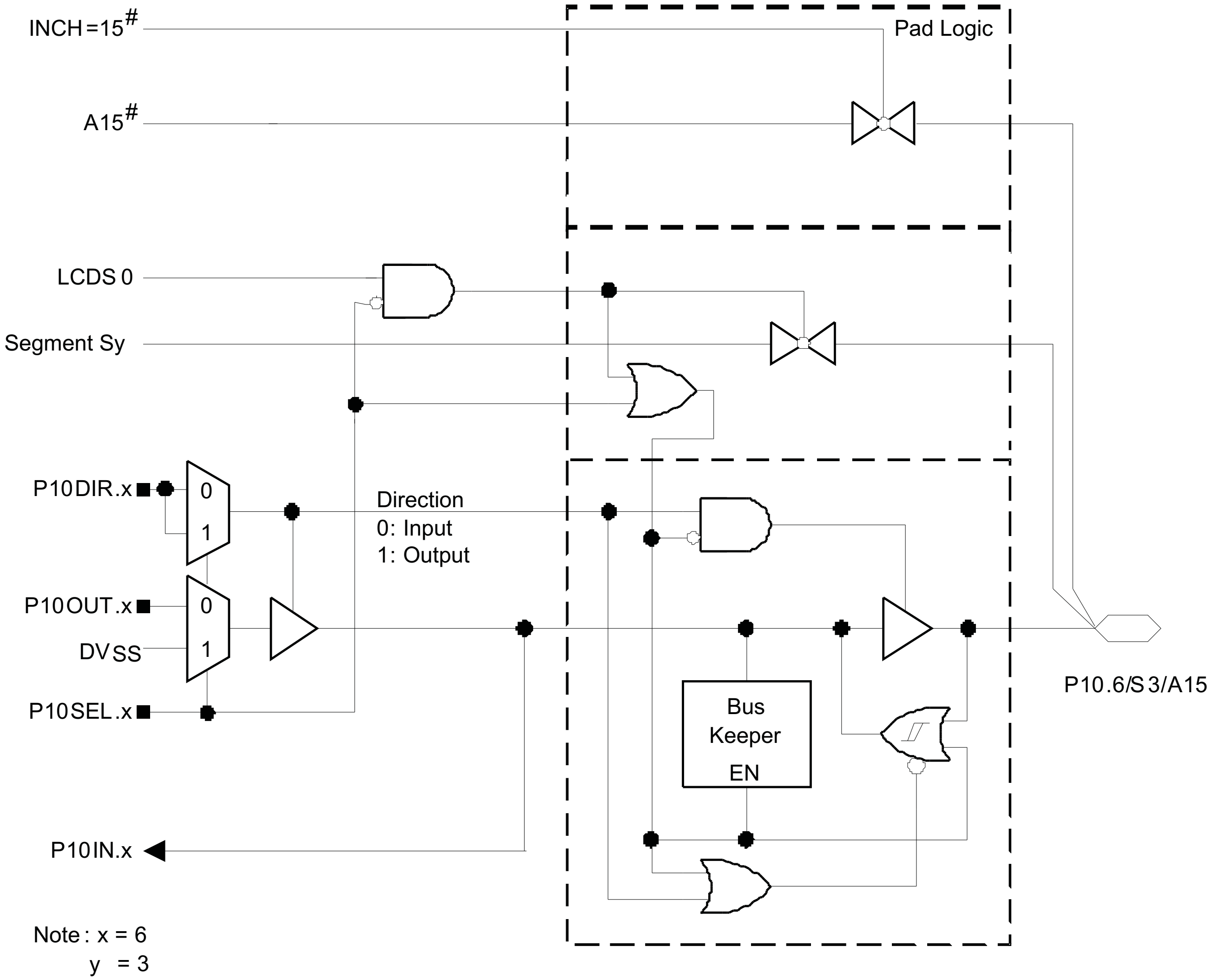


Table 6-40. Port P10 (P10.6) Pin Functions

PIN NAME (P10.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P10DIR.x	P10SEL.x	INCHx	LCDS0
P10.6/S3/A15	6	P5.0 (I/O)	I: 0; O: 1	0	X	0
		A15 (2)	X	1	15	0
		S3 enabled	X	0	X	1
		S3 disabled	X	1	X	1

(1) X = don't care
(2) Setting the P10SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

6.10.23 Port P10, P10.7, Input/Output With Schmitt Trigger

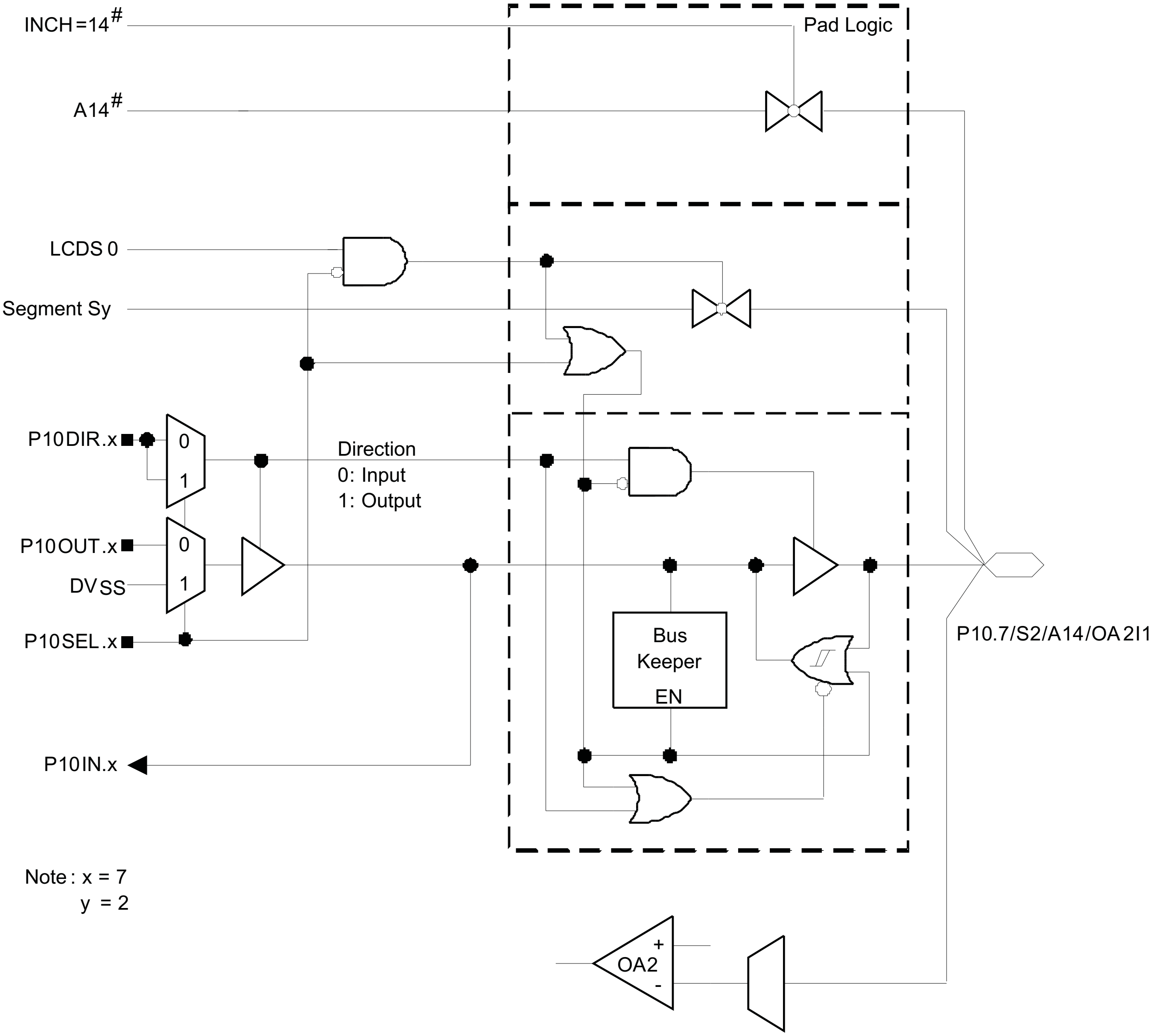
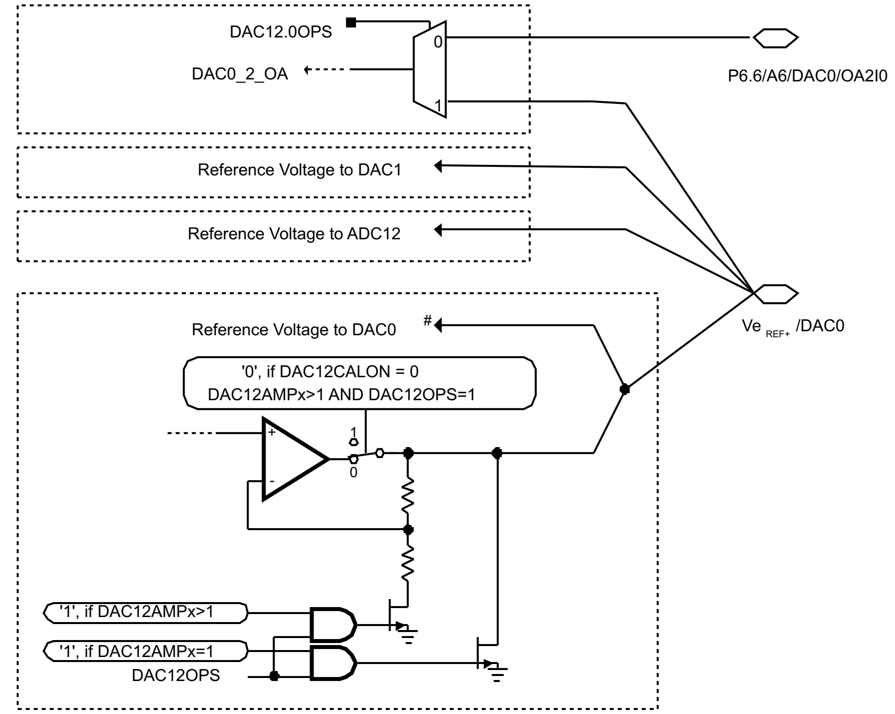


Table 6-41. Port P10 (P10.7) Pin Functions

PIN NAME (P10.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]				
			P10DIR.x	P10SEL.x	INCHx	OAPx (OA1) OANx (OA1)	LCDS0
P10.7/S2/A14/OA2I1	7	P10.7(I/O)	I: 0; O: 1	0	X	X	0
		A14 [2]	X	1	14	X	0
		OA2I1 [2]	0	X	X	1	0
		S2 enabled	X	0	X	X	1
		S2 disabled	X	1	X	X	1

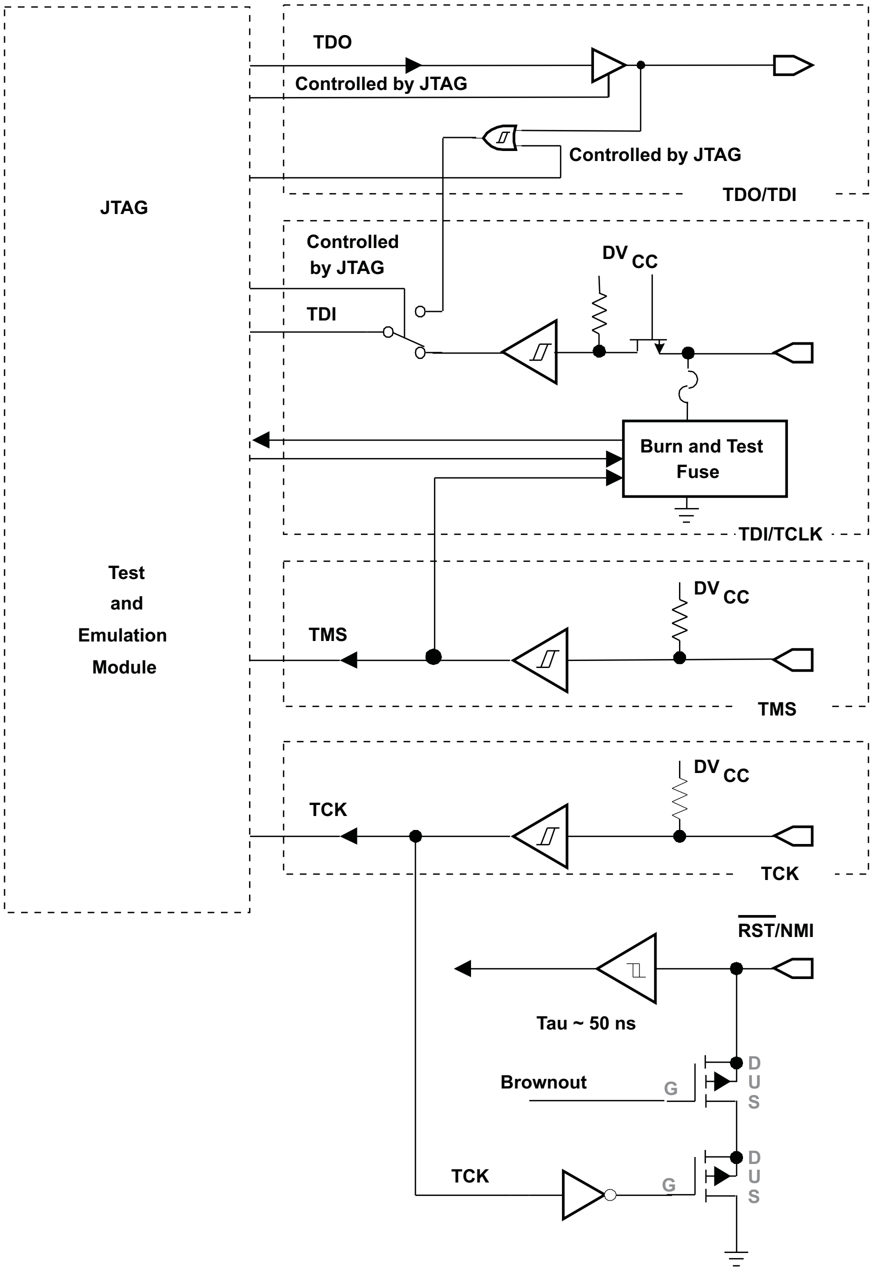
[1] X = don't care
[2] Setting the P10SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

6.10.24 Ve$_{REF+}$/DAC0



If the reference of DAC0 is taken from pin Ve$_{REF+}$/DAC0, unpredictable voltage levels will be on pin. In this situation, the DAC0 output is fed back to its own reference input.

6.10.25 JTAG Pins TMS, TCK, TDI/TCLK, TDO/TDI, Input/Output With Schmitt Trigger or Output



6.10.26 JTAG Fuse Check Mode

Devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current ($I_{(TF)}$) of 1 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 6-1). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition). The JTAG pins are terminated internally and therefore do not require external termination.

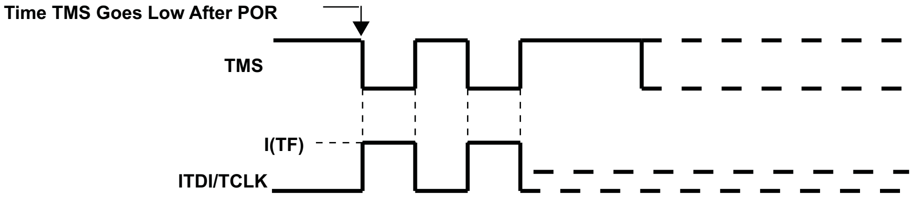


Figure 6-1. Fuse Check Mode Current

7 Device and Documentation Support

7.1 Device Support

7.1.1 Getting Started and Next Steps

For more information on the MSP430F4x family of devices and the tools and libraries that are available to help with your development, visit the Getting Started page.

7.1.2 Development Tools Support

All MSP430™ microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at www.ti.com/msp430tools.

7.1.2.1 Hardware Features

See the *Composer Studio for MSP430 User's Guide* (SLAU157) for details on the available features.

MSP430 Architecture	4-Wire JTAG	2-Wire JTAG	Break-points (N)	Range Break-points	Clock Control	State Sequencer	Trace Buffer	LPMx.5 Debugging Support
MSP430	Yes	No	2	No	Yes	No	No	No

7.1.2.2 Recommended Hardware Options

7.1.2.2.1 Target Socket Boards

The target socket boards allow easy programming and debugging of the device using JTAG. They also feature header pin outs for prototyping. Target socket boards are orderable individually or as a kit with the JTAG programmer and debugger included. The following table shows the compatible target boards and the supported packages.

Package	Target Board and Programmer Bundle	Target Board Only
100-pin LQFP (PZ)	MSP-FET430U100	MSP-TS430PZ100

7.1.2.2.2 Experimenter Boards

Experimenter Boards and Evaluation kits are available for some MSP430 devices. These kits feature additional hardware components and connectivity for full system evaluation and prototyping. See www.ti.com/msp430tools for details.

7.1.2.2.3 Debugging and Programming Tools

Hardware programming and debugging tools are available from TI and from its third party suppliers. See the full list of available tools at www.ti.com/msp430tools.

7.1.2.2.4 Production Programmers

The production programmers expedite loading firmware to devices by programming several devices simultaneously.

Part Number	PC Port	Features	Provider
MSP-GANG	Serial and USB	Program up to eight devices at a time. Works with PC or standalone.	Texas Instruments

7.1.2.3 Recommended Software Options

7.1.2.3.1 Integrated Development Environments

Software development tools are available from TI or from third parties. Open source solutions are also available.

This device is supported by Code Composer Studio™ IDE (CCS).

7.1.2.3.2 MSP430Ware

MSP430Ware is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware also includes a high-level API called MSP430 Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware is available as a component of CCS or as a standalone package.

7.1.2.3.3 Command-Line Programmer

MSP430 Flasher is an open-source shell-based interface for programming MSP430 microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP430 Flasher can be used to download binary files (.txt or .hex) files directly to the MSP430 microcontroller without the need for an IDE.

7.1.3 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

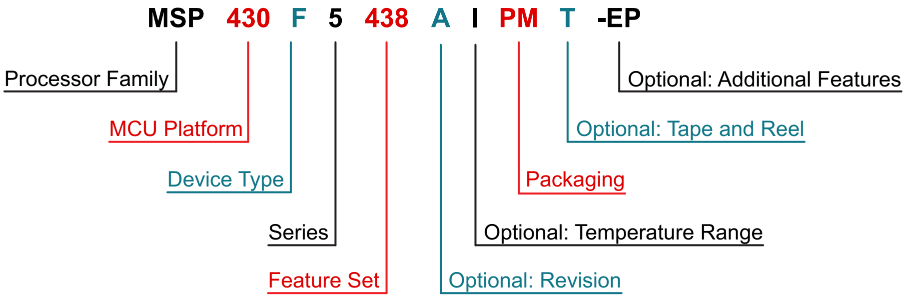
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 7-1 provides a legend for reading the complete device name.



Processor Family	CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device
MCU Platform	430 = MSP430 low-power microcontroller platform
Device Type	**Memory Type** C = ROM F = Flash FR = FRAM G = Flash L = No nonvolatile memory **Specialized Application** AFE = Analog front end BQ = Contactless power CG = ROM medical FE = Flash energy meter FG = Flash medical FW = Flash electronic flow meter
Series	1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD driver 5 = Up to 25 MHz 6 = Up to 25 MHz with LCD driver 0 = Low-voltage series
Feature Set	Various levels of integration within a series
Optional: Revision	Updated version of the base part number
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = –40°C to 85°C T = –40°C to 105°C
Packaging	http://www.ti.com/packaging
Optional: Tape and Reel	T = Small reel R = Large reel No markings = Tube or tray
Optional: Additional Features	-EP = Enhanced product (–40°C to 105°C) -HT = Extreme temperature parts (–55°C to 150°C) -Q1 = Automotive Q100 qualified

Figure 7-1. Device Nomenclature

7.2 Documentation Support

The following documents describe the MSP430FG461x and MSP430CG461x devices. Copies of these documents are available on the Internet at www.ti.com.

SLAU056	***MSP430F4xx Family User's Guide.*** Detailed information on the modules and peripherals available in this device family.
SLAZ369	***MSP430FG4619 Device Erratasheet.*** Describes the known exceptions to the functional specifications for all silicon revisions of the device.
SLAZ368	***MSP430FG4618 Device Erratasheet.*** Describes the known exceptions to the functional specifications for all silicon revisions of the device.
SLAZ367	***MSP430FG4617 Device Erratasheet.*** Describes the known exceptions to the functional specifications for all silicon revisions of the device.
SLAZ366	***MSP430FG4616 Device Erratasheet.*** Describes the known exceptions to the functional specifications for all silicon revisions of the device.
SLAZ123	***MSP430CG4619 Device Erratasheet.*** Describes the known exceptions to the functional specifications for all silicon revisions of the device.
SLAZ122	***MSP430CG4618 Device Erratasheet.*** Describes the known exceptions to the functional specifications for all silicon revisions of the device.
SLAZ121	***MSP430CG4617 Device Erratasheet.*** Describes the known exceptions to the functional specifications for all silicon revisions of the device.
SLAZ120	***MSP430CG4616 Device Erratasheet.*** Describes the known exceptions to the functional specifications for all silicon revisions of the device.

7.3 Related Links

Table 7-1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
MSP430FG4619	Click here	Click here	Click here	Click here	Click here
MSP430FG4618	Click here	Click here	Click here	Click here	Click here
MSP430FG4617	Click here	Click here	Click here	Click here	Click here
MSP430FG4616	Click here	Click here	Click here	Click here	Click here
MSP430CG4619	Click here	Click here	Click here	Click here	Click here
MSP430CG4618	Click here	Click here	Click here	Click here	Click here
MSP430CG4617	Click here	Click here	Click here	Click here	Click here
MSP430CG4616	Click here	Click here	Click here	Click here	Click here

7.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community
TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki
Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.5 Trademarks

MSP430, MicroStar Junior, Code Composer Studio, E2E are trademarks of Texas Instruments.

7.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.7 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

7.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430FG4616IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG4616	Samples
MSP430FG4616IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG4616	Samples
MSP430FG4616IZCA	ACTIVE	NFBGA	ZCA	113	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	FG4616	Samples
MSP430FG4616IZCAR	ACTIVE	NFBGA	ZCA	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	FG4616	Samples
MSP430FG4617IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG4617	Samples
MSP430FG4617IZCAR	ACTIVE	NFBGA	ZCA	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	FG4617	Samples
MSP430FG4617IZQWR	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	M430FG4617	
MSP430FG4618IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG4618	Samples
MSP430FG4618IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG4618	Samples
MSP430FG4618IZCA	ACTIVE	NFBGA	ZCA	113	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	FG4618	Samples
MSP430FG4618IZCAR	ACTIVE	NFBGA	ZCA	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	FG4618	Samples
MSP430FG4618IZCAT	ACTIVE	NFBGA	ZCA	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	FG4618	Samples
MSP430FG4619IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG4619 REV #	Samples
MSP430FG4619IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG4619	Samples
MSP430FG4619IZCAR	ACTIVE	NFBGA	ZCA	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	FG4619	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

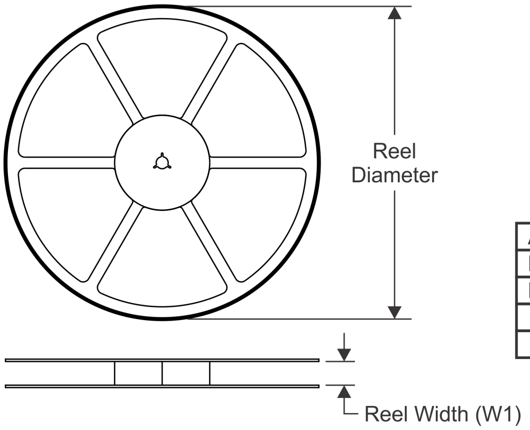
[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

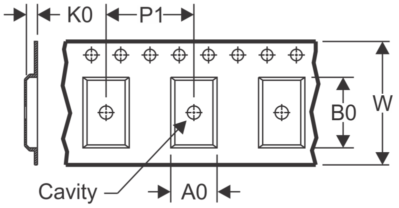
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

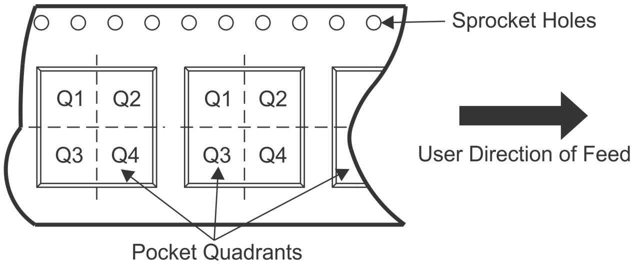


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

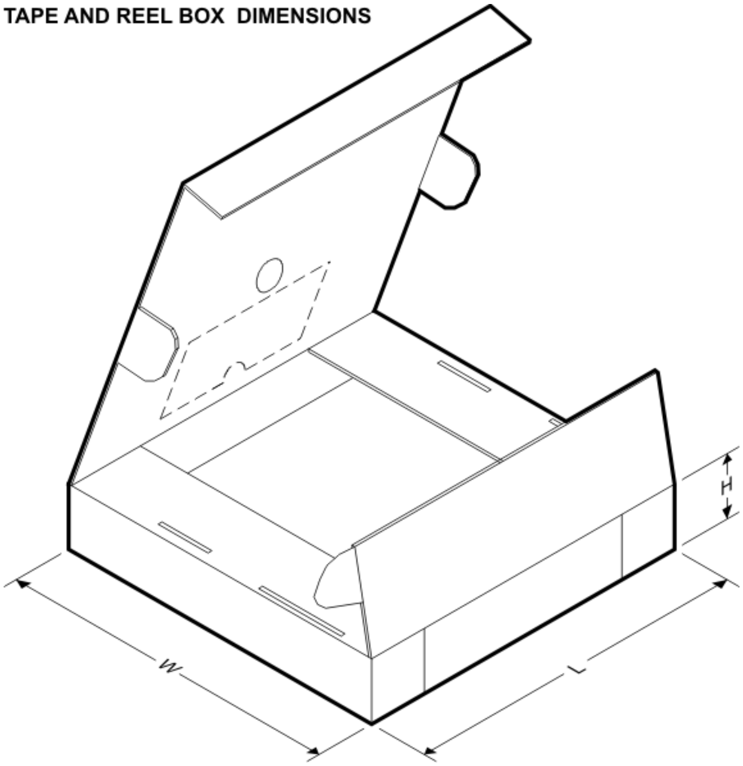
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FG4616IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430FG4616IZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG4617IZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG4617IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG4618IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430FG4618IZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG4619IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430FG4619IZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

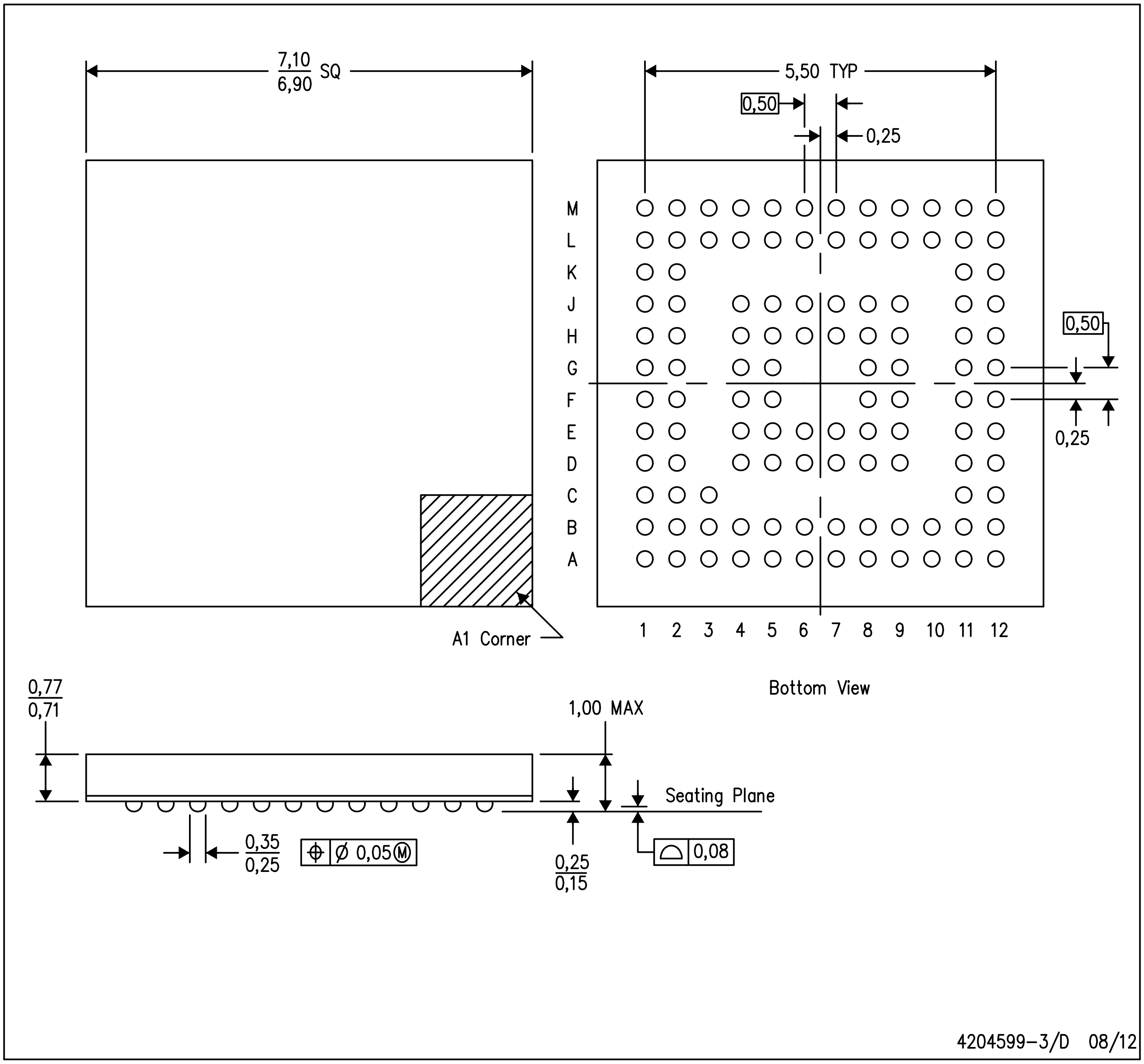
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

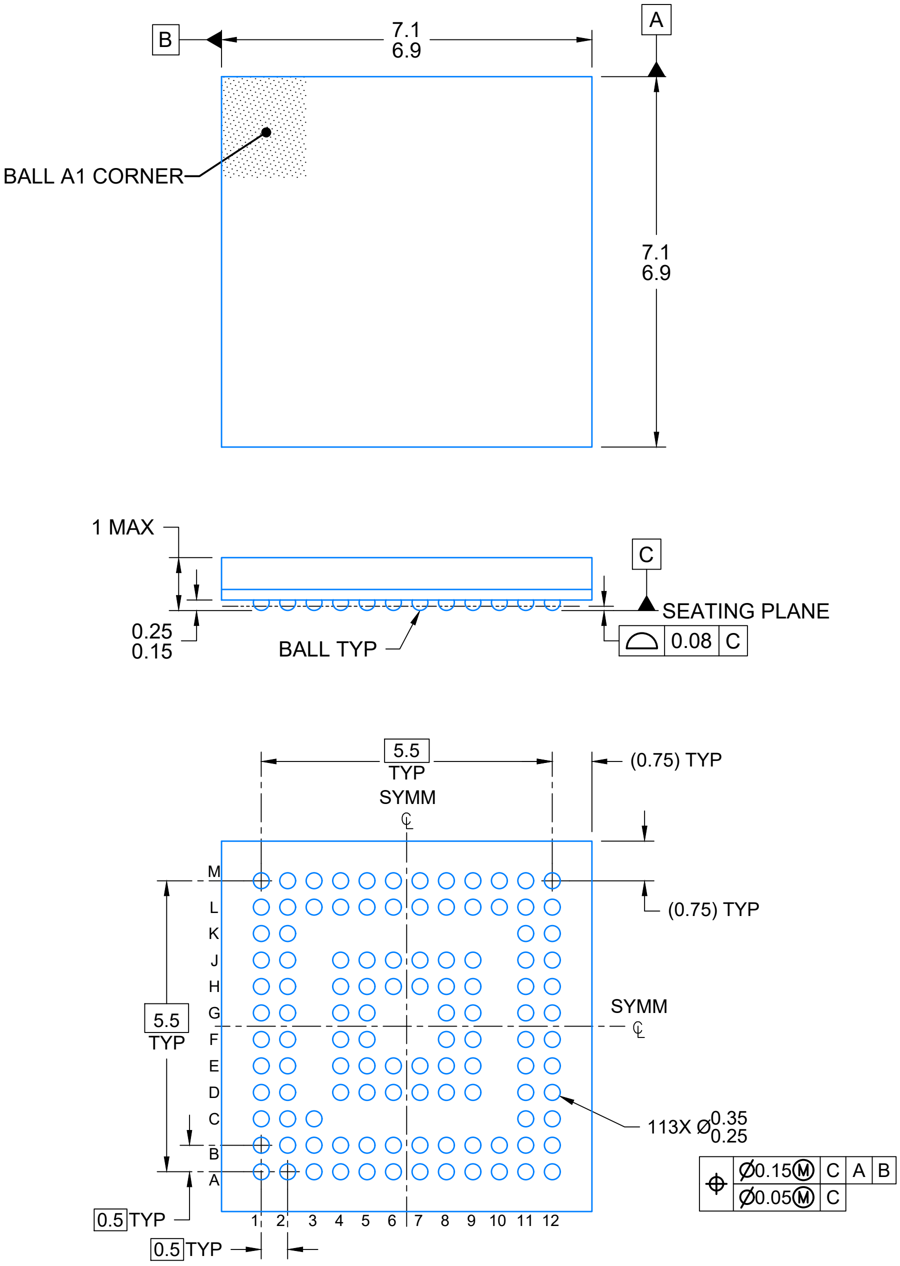
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FG4616IPZR	LQFP	PZ	100	1000	367.0	367.0	45.0
MSP430FG4616IZCAR	NFBGA	ZCA	113	2500	341.0	336.6	31.8
MSP430FG4617IZCAR	NFBGA	ZCA	113	2500	341.0	336.6	31.8
MSP430FG4617IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	350.0	350.0	43.0
MSP430FG4618IPZR	LQFP	PZ	100	1000	367.0	367.0	45.0
MSP430FG4618IZCAR	NFBGA	ZCA	113	2500	341.0	336.6	31.8
MSP430FG4619IPZR	LQFP	PZ	100	1000	367.0	367.0	45.0
MSP430FG4619IZCAR	NFBGA	ZCA	113	2500	341.0	336.6	31.8

ZQW (S-PBGA-N113) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-225
- D. This is a Pb-free solder ball design.

MicroStar Junior is a trademark of Texas Instruments.

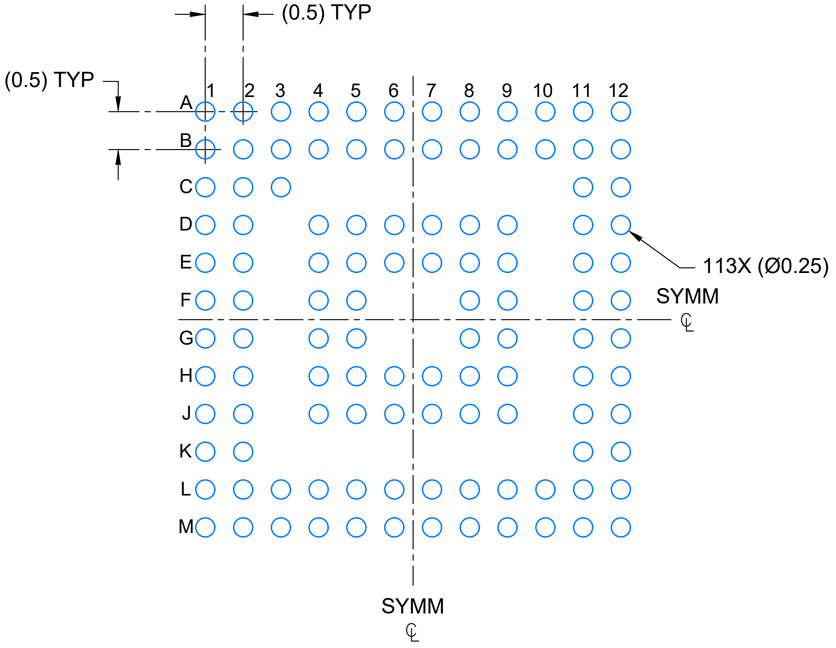


4225149/A 08/2019

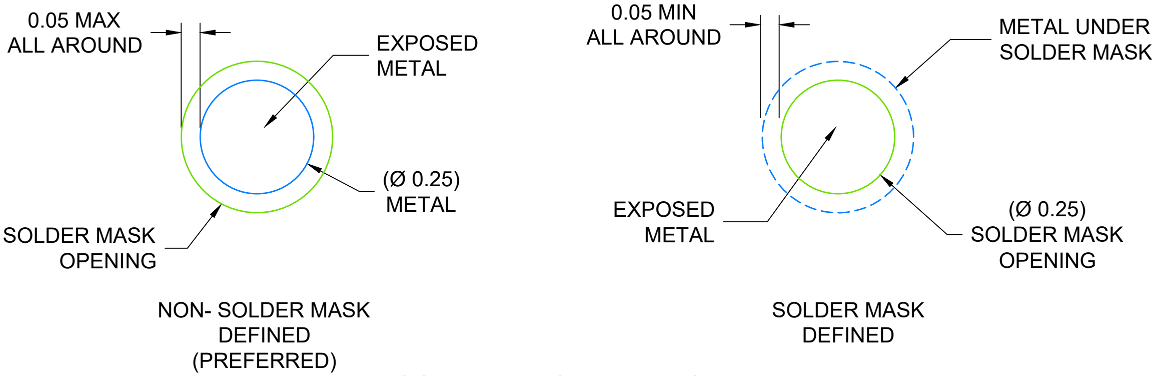
NOTES:

NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 10X

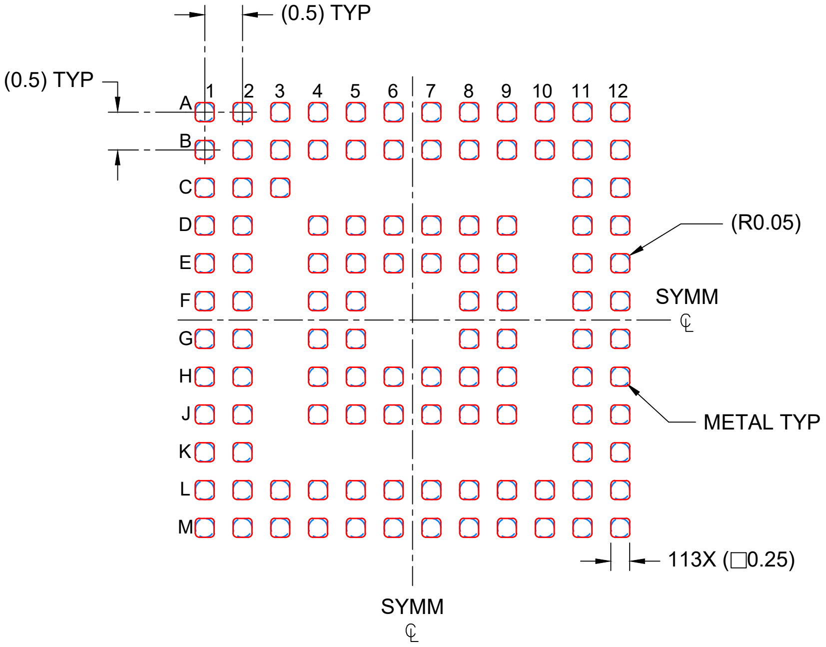


SOLDER MASK DETAILS
NOT TO SCALE

4225149/A 08/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



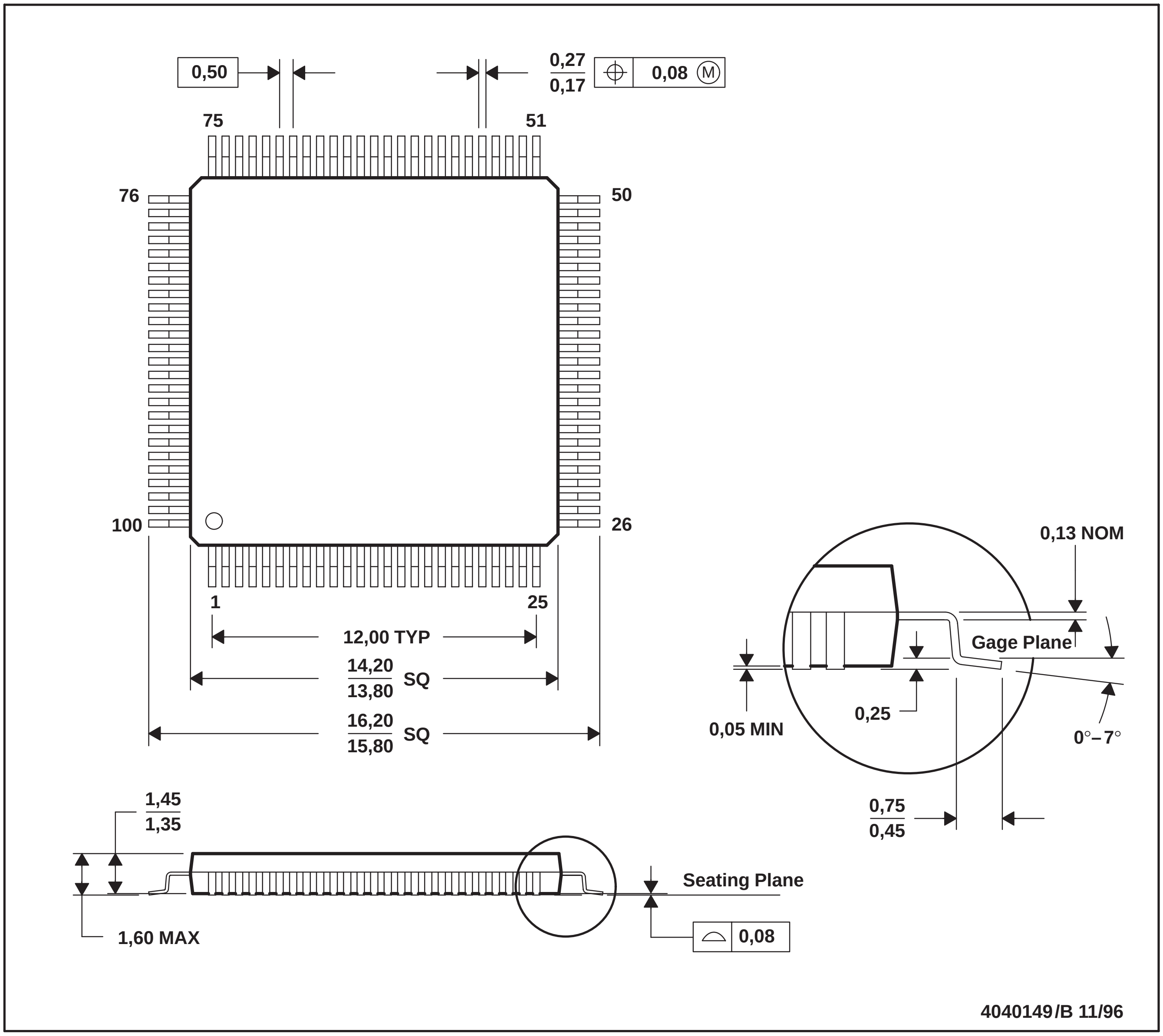
SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 10X

4225149/A 08/2019

NOTES: (continued)

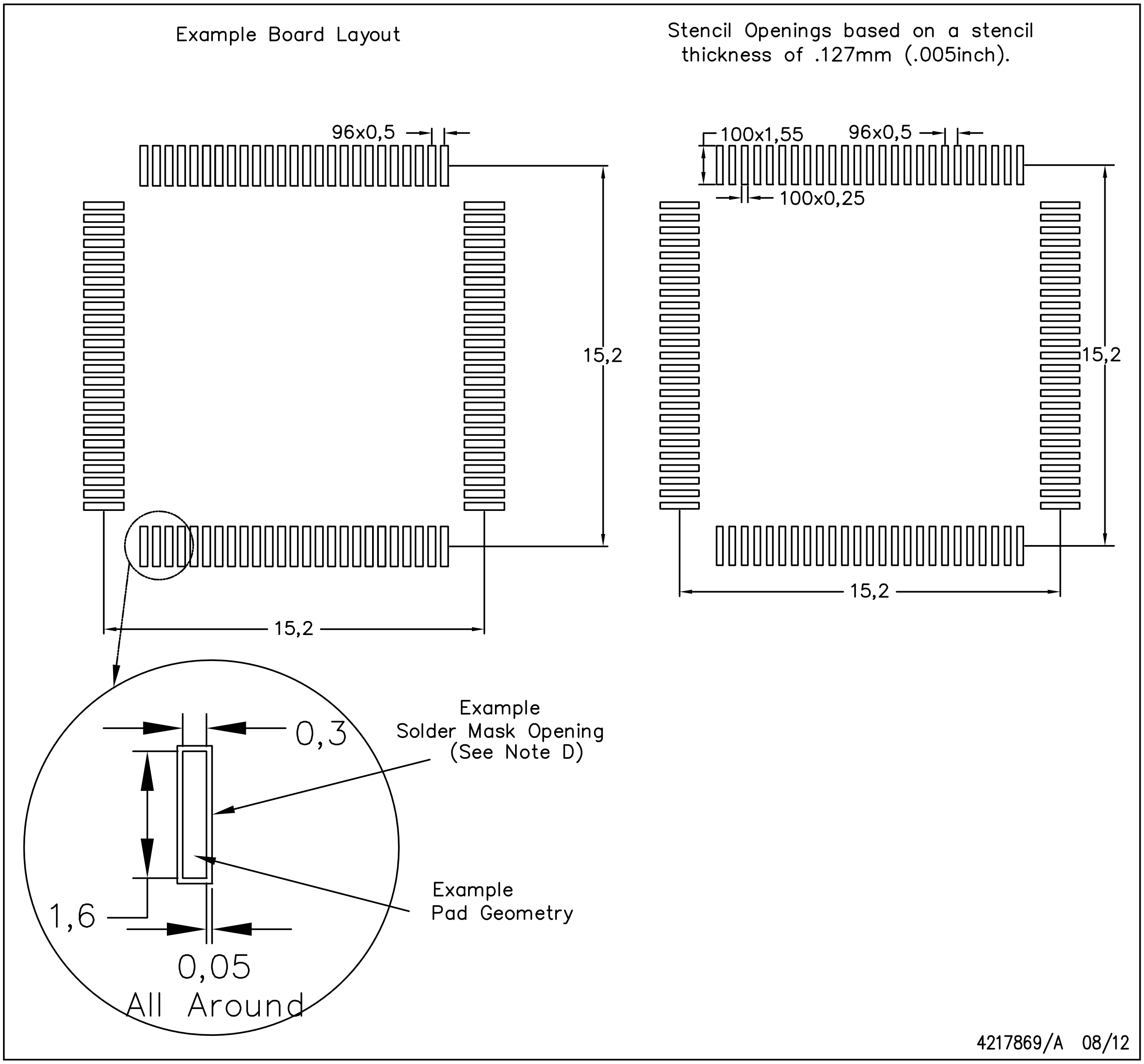
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PZ (S-PQFP-G100) PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-026

PZ (S–PQFP–G100) PLASTIC QUAD FLAT PACK



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated