HI-539

Precision, 4-Channel, Low-Level, Differential Multiplexer

FN3149
Rev 3.00
August 2003

The Intersil HI-539 is a monolithic, 4-Channel, differential multiplexer. Two digital inputs are provided for channel selection, plus an Enable input to disconnect all channels.

Performance is guaranteed for each channel over the voltage range ±10V, but is optimized for low level differential signals. Leakage current, for example, which varies slightly with input voltage, has its distribution centered at zero input volts.

In most monolithic multiplexers, the net differential offset due to thermal effects becomes significant for low level signals. This problem is minimized in the HI-539 by symmetrical placement of critical circuitry with respect to the few heat producing devices.

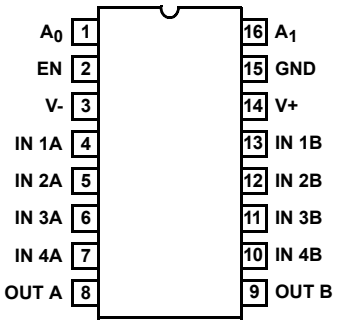
Supply voltages are ±15V and power consumption is only 2.5mW.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. DWG. #
HI1-0539-5	0 to 75	16 Ld CERDIP	F16.3

Pinouts

HI-539
(CERDIP)
TOP VIEW



Features

- Differential Performance, Typical:
  - Low Δr_{ON}, 125^{o}C 5.5Ω
  - Low $\Delta I_{D(ON)}$, 125^{o}C 0.6nA
  - Low Δ Charge Injection 0.1pC
  - Low Crosstalk . . . . . -124dB
- Settling Time, ±0.01% 900ns
- Wide Supply Range . . . . . ±5V to ±18V
- Break-Before-Make Switching
- No Latch-Up

Applications

- Low Level Data Acquisition
- Precision Instrumentation
- Test Systems

TRUTH TABLE

EN	A_1	A_0	ON CHANNEL TO	
			OUT A	OUT B
L	X	X	None	None
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

Absolute Maximum Ratings

V+ to V- 40V
V+ or V- to GND 20V
Analog Signal (V_{IN}, V_{OUT}) . . . . . V- to V+
Digital Input Voltage (V_{EN}, V_A) . . . . . V- to V+
Analog Current (IN or OUT) 20mA

Operating Conditions

Temperature Range
HI-539-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	75	20

Maximum Junction Temperature
Ceramic Package . . . . . 175^oC
Plastic Package . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = ±15V, V_{EN} = 4V, V_{AH} (Logic Level High) = 4V, V_{AL} (Logic Level Low) = 0.8V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Access Time, t_A		25	-	250	750	ns
		Full	-	-	1,000	ns
Break-Before-Make Delay, t_{OPEN}		25	30	85	-	ns
		Full	30	-	-	ns
Enable Delay (ON), $t_{ON(EN)}$		25	-	250	750	ns
		Full	-	-	1,000	ns
Enable Delay (OFF), $t_{OFF(EN)}$		25	-	160	650	ns
		Full	-	-	900	ns
Settling Time	To 0.01%	25	-	0.9	-	µs
Charge Injection (Output)		Full	-	3	-	pC
Δ Charge Injection (Output)		Full	-	0.1	-	pC
Charge Injection (Input)		Full	-	10	-	pC
Differential Crosstalk	Note 4	25	-	-124	-	dB
Single Ended Crosstalk	Note 4	25	-	-100	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		Full	-	5	-	pF
Channel Output Capacitance, $C_{D(OFF)}$		Full	-	7	-	pF
Channel On Output Capacitance, $C_{D(ON)}$		Full	-	17	-	pF
Input to Output Capacitance, $C_{DS(OFF)}$	Note 5	Full	-	0.08	-	pF
Digital Input Capacitance, C_A		Full	-	3	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Low Threshold, V_{AL}		Full	-	-	0.8	V
Input High Threshold, V_{AH}		Full	4.0	-	-	V
Input Leakage Current (High), I_{AH}		Full	-	-	1	µA
Input Leakage Current (Low), I_{AL}		Full	-	-	1	µA
ANALOG CHANNEL CHARACTERISTICS						
Analog Signal Range, V_{IN}		Full	-10	-	+10	V

Electrical Specifications Supplies = ±15V, V_{EN} = 4V, V_{AH} (Logic Level High) = 4V, V_{AL} (Logic Level Low) = 0.8V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^{o}C)	MIN	TYP	MAX	UNITS
On Resistance, r_{ON}	V_{IN} = 0V	25	-	650	850	Ω
		Full	-	800	1K	Ω
	V_{IN} = ±10V	25	-	700	900	Ω
		Full	-	900	1.1K	Ω
Δr_{ON}, (Side A-Side B)	V_{IN} = 0V	25	-	4.0	24	Ω
		Full	-	4.0	24	Ω
	V_{IN} = ±10V	25	-	4.5	27	Ω
		Full	-	4.5	27	Ω
Off Input Leakage Current, $I_{S(OFF)}$	Condition 0V (Note 2)	25	-	30	-	pA
		Full	-	0.2	1	nA
	Condition ±10V (Note 2)	25	-	100	-	pA
		Full	-	0.5	2.5	nA
$\Delta I_{S(OFF)}$, (Side A-Side B)	Condition 0V	25	-	3	-	pA
		Full	-	0.02	0.2	nA
	Condition ±10V	25	-	10	-	pA
		Full	-	0.05	0.5	nA
Off Output Leakage Current, $I_{D(OFF)}$	Condition 0V (Note 2)	25	-	30	-	pA
		Full	-	0.2	1	nA
	Condition ±10V (Note 2)	25	-	100	-	pA
		Full	-	0.5	2.5	nA
$\Delta I_{D(OFF)}$, (Side A-Side B)	Condition 0V	25	-	3	-	pA
		Full	-	0.02	0.2	nA
	Condition ±10V	25	-	10	-	pA
		Full	-	0.05	0.5	nA
On Channel Leakage Current, $I_{D(ON)}$	Condition 0V (Note 2)	25	-	50	-	pA
		Full	-	0.5	2.5	nA
	Condition ±10V (Note 2)	25	-	150	-	pA
		Full	-	0.8	4.0	nA
$\Delta I_{D(ON)}$, (Side A-Side B)	Condition 0V	25	-	10	-	pA
		Full	-	0.05	0.5	nA
	Condition ±10V	25	-	30	-	pA
		Full	-	0.08	0.8	nA
Differential Offset Voltage, ΔV_{OS}	Note 3	25	-	0.02	-	µV
		Full	-	0.08	-	µV
POWER SUPPLY CHARACTERISTICS						
Power Dissipation, P_D		25	-	2.3	-	mW
		Full	-	-	45	mW
Current, I+		25	-	0.150	-	mA
		Full	-	-	2.0	mA

Electrical Specifications Supplies = ±15V, V_{EN} = 4V, V_{AH} (Logic Level High) = 4V, V_{AL} (Logic Level Low) = 0.8V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^{o}C)	MIN	TYP	MAX	UNITS
Current, I-		25	-	0.001	-	mA
		Full	-	-	1.0	mA
Supply Voltage Range		Full	±5	±15	±18	V

NOTES:

2. See Figures 2B, 2C, 2D. The condition ±10V means:
   $I_{S(OFF)}$ and $I_{D(OFF)}$:
   (V_S = +10V, V_D = -10V), then
   (V_S = -10V, V_D = +10V)
   $I_{D(ON)}$: (+10V, then -10V)
3. ΔV_{OS} (Exclusive of thermocouple effects) = r_{ON} $\Delta I_{D(ON)}$ + $I_{D(ON)}$ Δr_{ON}. See Applications section for discussion of additional V_{OS} error.
4. V_{IN} = 1kHz, $15V_{P-P}$ on all but the selected channel. See Figure 7.
5. Calculated from typical Single-Ended Crosstalk performance.

Test Circuits and Waveforms Unless Otherwise Specified T_A = 25^{o}C, V+ = +15V, V- = -15V, V_{AH} = 4V and V_{AL} = 0.8V

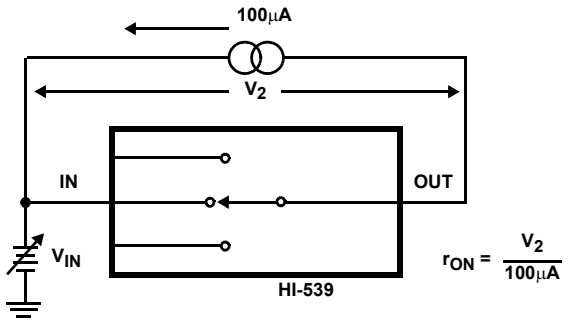


FIGURE 1A. TEST CIRCUIT

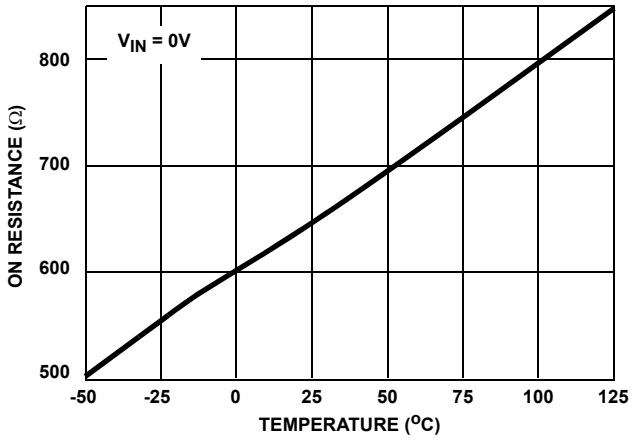


FIGURE 1B. ON RESISTANCE vs TEMPERATURE

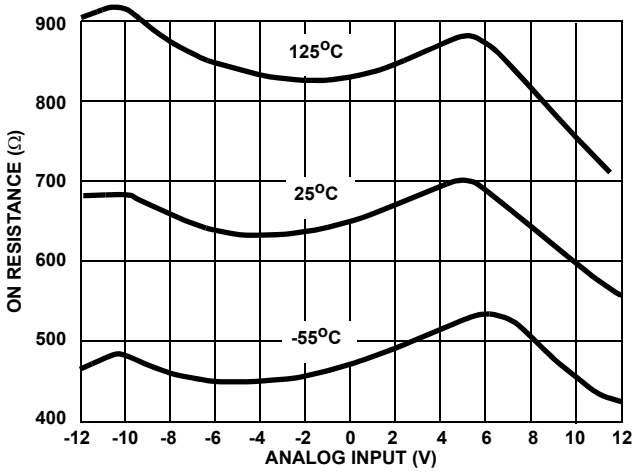


FIGURE 1C. ON RESISTANCE vs ANALOG INPUT VOLTAGE

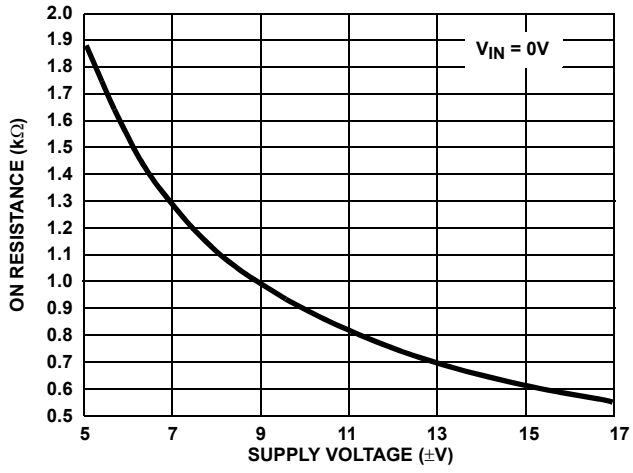


FIGURE 1D. ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

Test Circuits and Waveforms Unless Otherwise Specified $T_A = 25^oC$, V+ = +15V, V- = -15V, V_{AH} = 4V and V_{AL} = 0.8V **(Continued)**

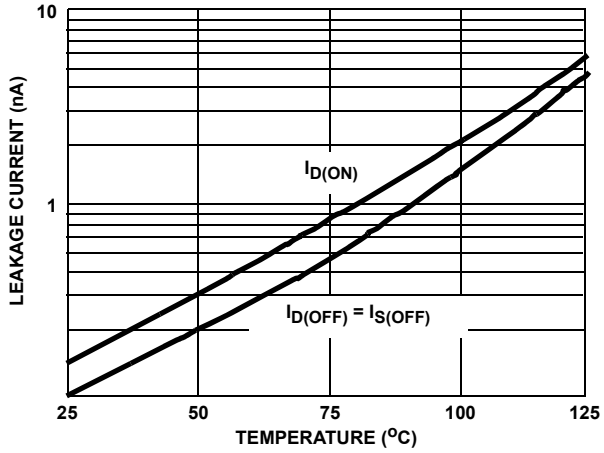


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

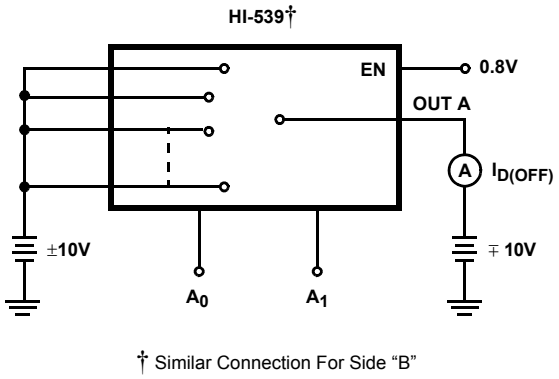


FIGURE 2B. $I_{D(OFF)}$ TEST CIRCUIT (NOTE 6)

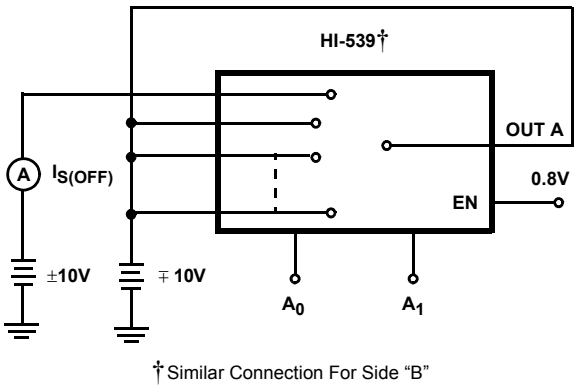


FIGURE 2C. $I_{S(OFF)}$ TEST CIRCUIT (NOTE 6)

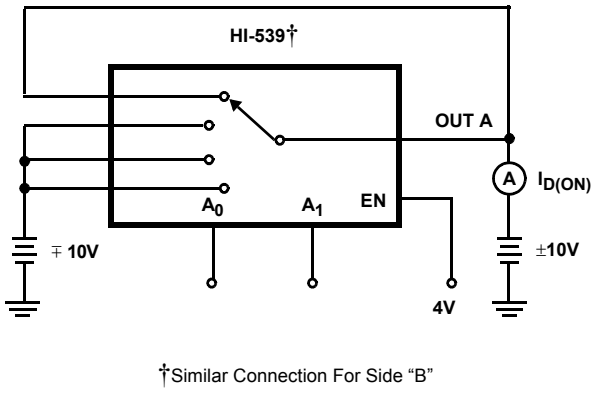


FIGURE 2D. $I_{D(ON)}$ TEST CIRCUIT (NOTE 6)

NOTE:
6. Three measurements = ±10V, ∓10V, and 0V.

FIGURE 2. LEAKAGE CURRENT

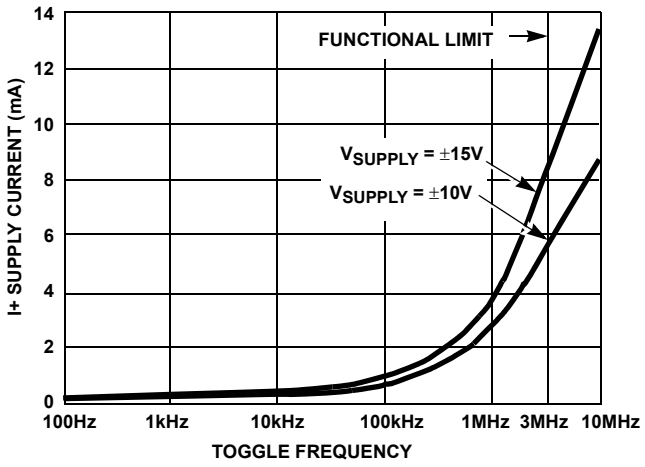


FIGURE 3A. SUPPLY CURRENT vs TOGGLE FREQUENCY

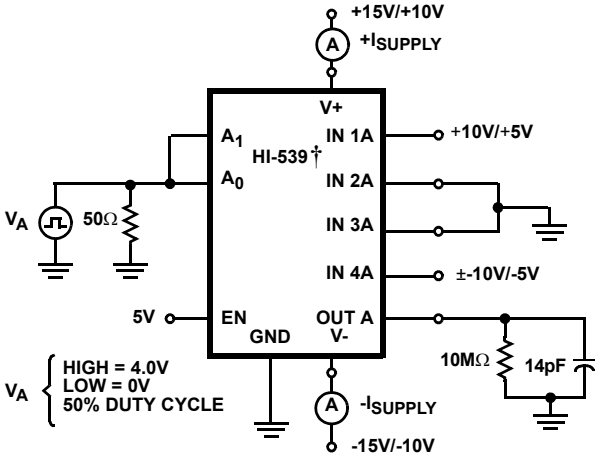


FIGURE 3B. TEST CIRCUIT

FIGURE 3. DYNAMIC SUPPLY CURRENT

Test Circuits and Waveforms Unless Otherwise Specified $T_A = 25^oC$, V+ = +15V, V- = -15V, V_{AH} = 4V and V_{AL} = 0.8V **(Continued)**

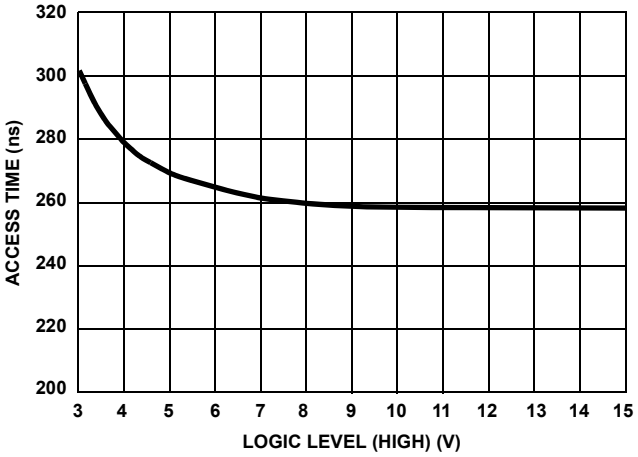


FIGURE 4A. ACCESS TIME vs LOGIC LEVEL (HIGH)

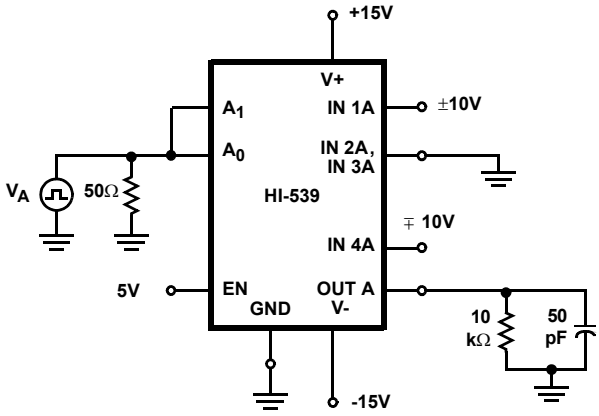


FIGURE 4B. TEST CIRCUIT

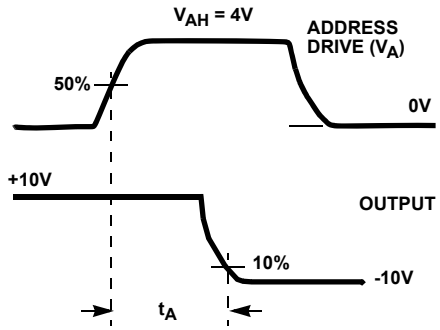


FIGURE 4C. MEASUREMENT POINTS

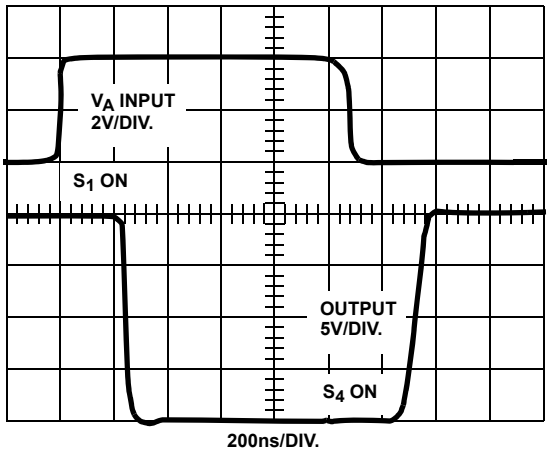


FIGURE 4D. WAVEFORMS

FIGURE 4. ACCESS TIME

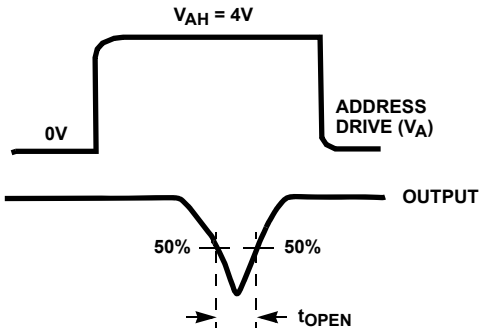


FIGURE 5A. MEASUREMENT POINTS

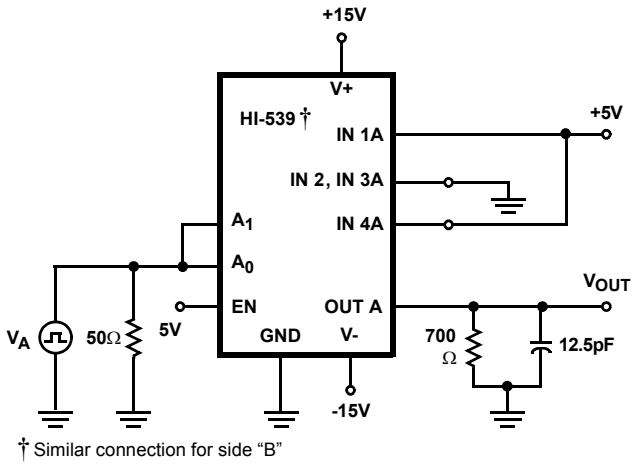


FIGURE 5B. TEST CIRCUIT

Test Circuits and Waveforms Unless Otherwise Specified $T_A = 25^oC$, V+ = +15V, V- = -15V, V_{AH} = 4V and V_{AL} = 0.8V **(Continued)**

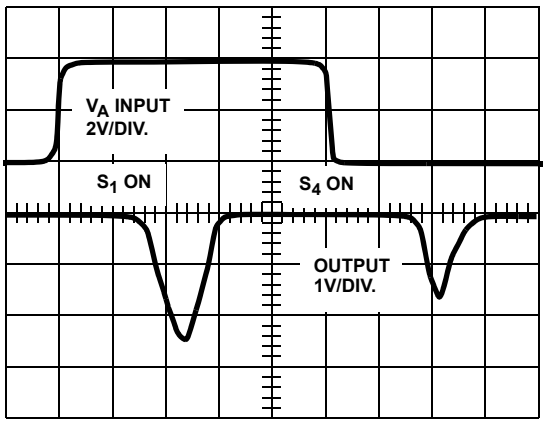


FIGURE 5C. WAVEFORMS

FIGURE 5. BREAK-BEFORE-MAKE DELAY

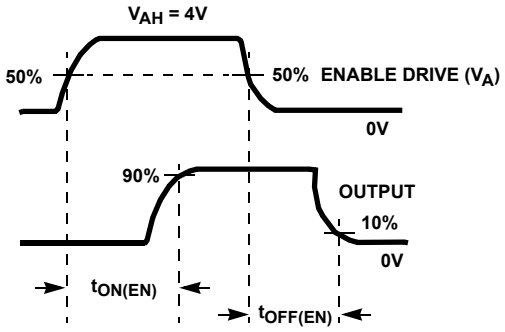


FIGURE 6A. MEASUREMENT POINTS

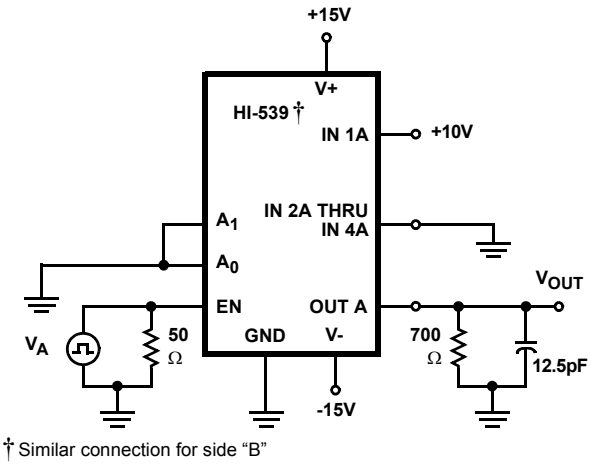


FIGURE 6B. TEST CIRCUIT

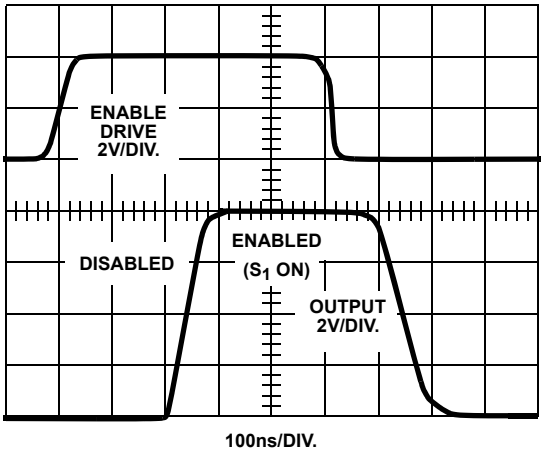


FIGURE 6C. WAVEFORMS

FIGURE 6. ENABLE DELAYS

Test Circuits and Waveforms Unless Otherwise Specified $T_A = 25^oC$, V+ = +15V, V- = -15V, V_{AH} = 4V and V_{AL} = 0.8V **(Continued)**

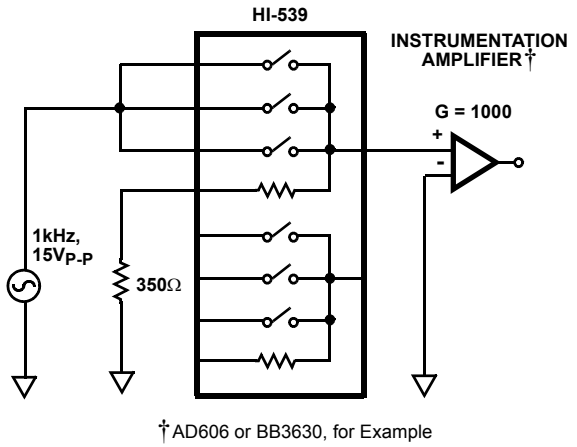


FIGURE 7A. SINGLE-ENDED CROSSTALK TEST CIRCUIT

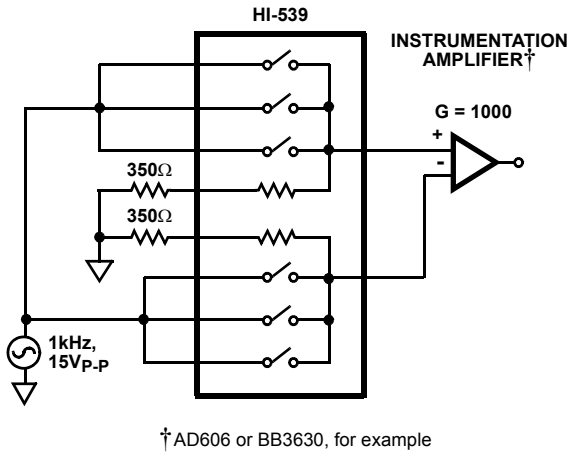


FIGURE 7B. DIFFERENTIAL CROSSTALK TEST CIRCUIT

FIGURE 7. CROSSTALK

Application Information

General

The HI-539 accepts inputs in the range -15V to +15V, with performance guaranteed over the ±10V range. At these higher levels of analog input voltage it is comparable to the HI-509, and is plug-in compatible with that device (as well as the HI-509A). However, as mentioned earlier, the HI-539 was designed to introduce minimum error when switching low level inputs.

Special care is required in working with these low level signals. The main concern with signals below 100mV is that noise, offset voltage, and other aberrations can represent a large percentage error. A shielded differential signal path is essential to maintain a noise level below $50\mu V_{RMS}$.

Low Level Signal Transmission

The transmission cable carrying the transducer signal is critical in a low level system. It should be as short as practical and rigidly supported. Signal conductors should be tightly twisted for minimum enclosed area to guard against pickup of electromagnetic interference, and the twisted pair should be shielded against capacitively coupled (electrostatic) interference. A braided wire shield may be satisfactory, but a lapped foil shield is better since it allows only $^1/_{10}$ as much leakage capacitance to ground per foot. A key requirement for the transmission cable is that it presents a balanced line to sources of noise interference. This means an equal series impedance in each conductor plus an equally distributed impedance from each conductor to ground. The result should be signals equal in magnitude but opposite in phase at any transverse plane. Noise will be coupled in phase to both conductors, and may be rejected as common-mode voltage by a differential amplifier connected to the multiplexer output.

Coaxial cable is not suitable for low level signals because the two conductors (center and shield) are unbalanced. Also, ground loops are produced if the shield is grounded at both ends by standard BNC connectors. If coax must be used, carry the signal on the center conductors of two equal-length cables whose shields are terminated only at the transducer end. As a general rule, terminate (ground) the shield at one end only, preferably at the end with greatest noise interference. This is usually the transducer end for both high and low level signals.

Watch Small ΔV Errors

Printed circuit traces and short lengths of wire can add substantial error to a signal even after it has traveled hundreds of feet and arrived on a circuit board. Here, the small voltage drops due to current flow through connections of a few milliohms must be considered, especially to meet an accuracy requirement of 12 bits or more.

Table 1 is a useful collection of data for calculating the effect of these short connections. (Proximity to a ground plane will lower the values of inductance.)

As an example, suppose the HI-539 is feeding a 12-bit converter system with an allowable error of $\pm^1/_2$ LSB (±1.22mV). If the interface logic draws 100mA from the 5V supply, this current will produce 1.28mV across 6 inches of #24 wire; more than the error budget. Obviously, this digital current must not be routed through any portion of the analog ground return network.

TABLE 1.

WIRE GAGE	EQUIVALENT WIDTH OF P.C. CONDUCTOR (2 oz. Cu)	DC RESISTANCE PER FOOT	INDUCTANCE PER FOOT	IMPEDANCE PER FOOT	
				60Hz	10kHz
18	0.47”	0.0064Ω	0.36µH	0.0064Ω	0.0235Ω
20	0.30”	0.0102Ω	0.37µH	0.0102Ω	0.0254Ω
22	0.19”	0.0161Ω	0.37µH	0.0161Ω	0.0288Ω
24	0.12”	0.0257Ω	0.40µH	0.0257Ω	0.0345Ω
26	0.075”	0.041Ω	0.42µH	0.041Ω	0.0488Ω
28	0.047”	0.066Ω	0.45µH	0.066Ω	0.0718Ω
30	0.029”	0.105Ω	0.49µH	0.105Ω	0.110Ω
32	0.018”	0.168Ω	0.53µH	0.168Ω	0.171Ω

Provide Path For I_{BIAS}

The input bias current for any DC-coupled amplifier must have an external path back to the amplifier’s power supply. No such path exists in Figure 8A, and consequently the amplifier output will remain in saturation.

A single large resistor (1MΩ to 10MΩ) from either signal line to power supply common will provide the required path, but a resistor on each line is necessary to preserve accuracy. A single pair of these bias current resistors on the HI-539 output may be used if their loading effect can be tolerated (each forms a voltage divider with r_{ON}). Otherwise, a resistor pair on each input channel of the multiplexer is required.

The use of bias current resistors is acceptable only if one is confident that the sum of signal plus common-mode voltage will remain within the input range of the multiplexer/amplifier combination.

Another solution is to simply run a third wire from the low side of the signal source, as in Figure 8B. This wire assures a low common-mode voltage as well as providing the path for bias currents. Making the connection near the multiplexer will save wire, but it will also unbalance the line and reduce the amplifier's common-mode rejection.

Differential Offset, ΔV_{OS}

There are two major sources of ΔV_{OS}. That part due to the expression ($r_{ON}\ \Delta I_{D(ON)} + I_{D(ON)}\ \Delta r_{ON}$) becomes significant with increasing temperature, as shown in the Electrical Specifications tables. The other source of offset is the thermocouple effects due to dissimilar materials in the signal path. These include silicon, aluminum, tin, nickel-iron and (often) gold, just to exit the package.

For the thermocouple effects in the package alone, the constraint on ΔV_{OS} may be stated in terms of a limit on the difference in temperature for package pins leading to any channel of the HI-539. For example, a difference of $0.13^{o}C$ produces a 5µV offset. Obviously, this ΔT effect can dominate the ΔV_{OS} parameter at any temperature unless care is taken in mounting the HI-539 package.

Temperature gradients across the HI-539 package should be held to a minimum in critical applications. Locate the HI-539 far from heat producing components, with any air currents flowing lengthwise across the package.

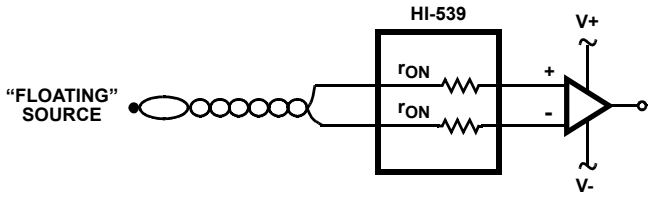
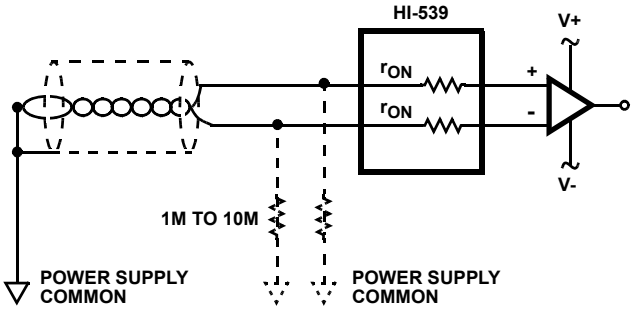


FIGURE 8A.



NOTE: The amplifier in Figure 8A is unusable because its bias currents cannot return to the power supply. Figure 8B shows two alternative paths for these bias currents: either a pair of resistors, or (better) a third wire from the low side of the signal source.

FIGURE 8B.

Die Characteristics

DIE DIMENSIONS:

92 mils x 100 mils

METALLIZATION:

Type: AlCu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2.0kÅ

WORST CASE CURRENT DENSITY:

2.54×10^5 A/cm^2 at 20mA

TRANSISTOR COUNT:

236

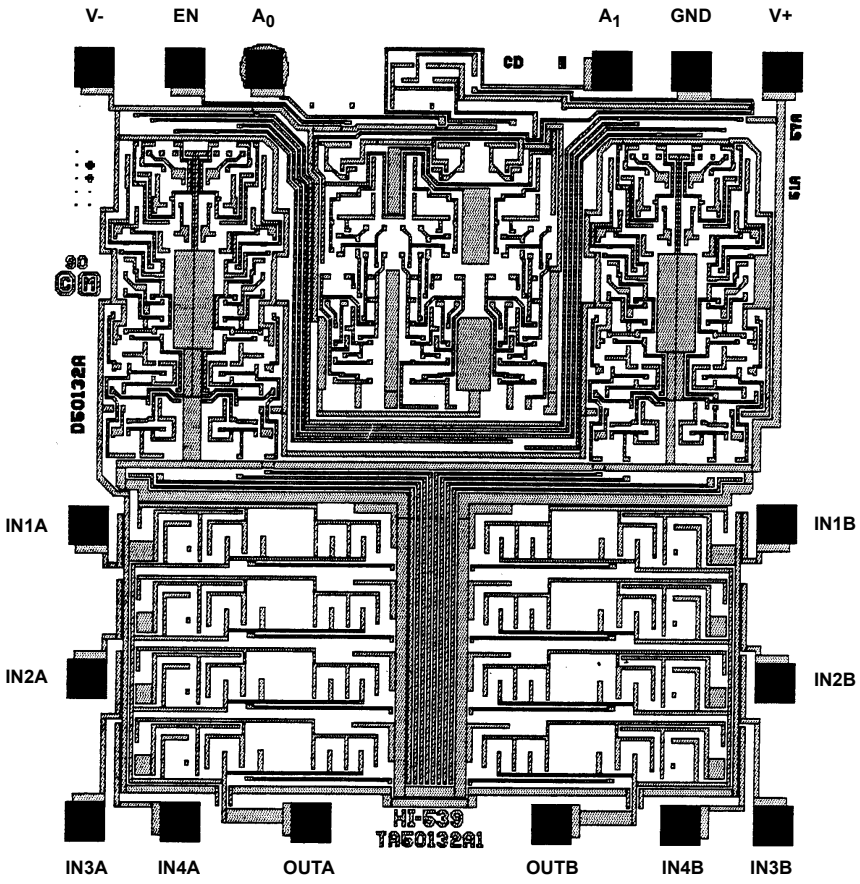
PROCESS:

CMOS-DI

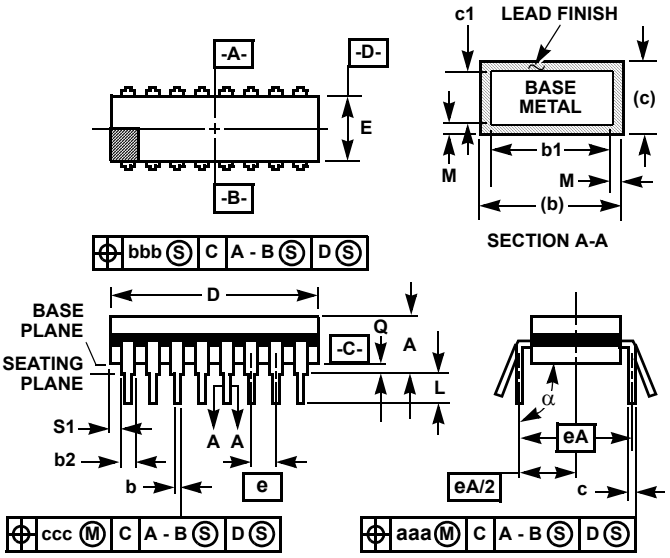
NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layout

HI-539



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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