SBAS100A – JANUARY 1998 – REVISED OCTOBER 2003

12-Bit, 8-Channel Serial Output Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- SINGLE SUPPLY: 2.7V to 5V
- 8-CHANNEL SINGLE-ENDED OR 4-CHANNEL DIFFERENTIAL INPUT
- UP TO 200kHz CONVERSION RATE
- ±1 LSB MAX INL AND DNL
- NO MISSING CODES
- 72dB SINAD
- SERIAL INTERFACE
- 20-LEAD QSOP AND 20-LEAD SSOP PACKAGES
- ALTERNATE SOURCE FOR MAX147

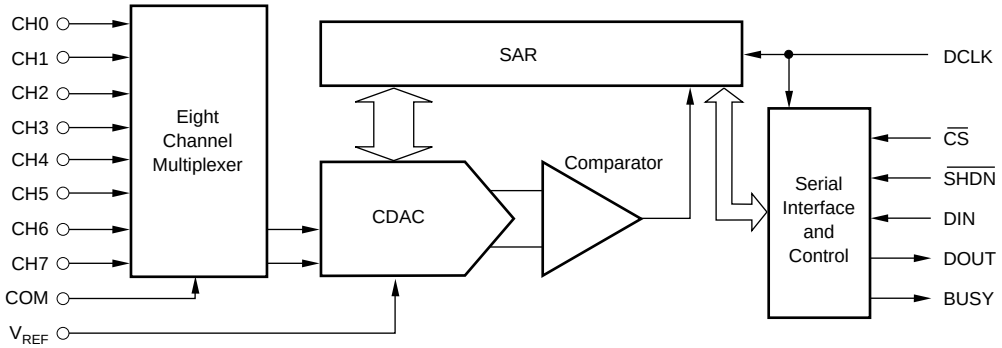
APPLICATIONS

- DATA ACQUISITION
- TEST AND MEASUREMENT
- INDUSTRIAL PROCESS CONTROL
- PERSONAL DIGITAL ASSISTANTS
- BATTERY-POWERED SYSTEMS

DESCRIPTION

The ADS7844 is an 8-channel, 12-bit sampling analog-to-digital converter (ADC) with a synchronous serial interface. Typical power dissipation is 3mW at a 200kHz throughput rate and a +5V supply. The reference voltage (V_{REF}) can be varied between 100mV and V_{CC}, providing a corresponding input voltage range of 0V to V_{REF}. The device includes a shutdown mode that reduces power dissipation to under 1µW. The ADS7844 is ensured down to 2.7V operation.

Low power, high speed, and onboard multiplexer make the ADS7844 ideal for battery-operated systems such as personal digital assistants, portable multichannel data loggers, and measurement equipment. The serial interface also provides low-cost isolation for remote data acquisition. The ADS7844 is available in a 20-lead QSOP package and the MAX147 equivalent 20-lead SSOP package and is ensured over the –40°C to +85°C temperature range.



SPECIFICATION: +5V

At T_A = –40°C to +85°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE} = 3.2MHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS7844E, N			ADS7844EB, NB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT								
Full-Scale Input Span	Positive Input - Negative Input	0		V_{REF}	*		*	V
Absolute Input Range	Positive Input	–0.2		$+V_{CC}$ +0.2	*		*	V
	Negative Input	–0.2		+1.25	*		*	V
Capacitance			25			*		pF
Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
Resolution			12			*		Bits
No Missing Codes		12			*			Bits
Integral Linearity Error				±2			±1	LSB(1)
Differential Linearity Error			±0.8			±0.5	±1	LSB
Offset Error				±3			*	LSB
Offset Error Match			0.15	1.0		*	*	LSB
Gain Error				±4			±3	LSB
Gain Error Match			0.1	1.0		*	*	LSB
Noise			30			*		µVrms
Power Supply Rejection			70			*		dB
SAMPLING DYNAMICS								
Conversion Time				12			*	Clk Cycles
Acquisition Time		3			*			Clk Cycles
Throughput Rate				200			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion(2)	V_{IN} = $5V_{PP}$ at 10kHz		–76			–78		dB
Signal-to-(Noise + Distortion)	V_{IN} = $5V_{PP}$ at 10kHz		71			72		dB
Spurious Free Dynamic Range	V_{IN} = $5V_{PP}$ at 10kHz		76			78		dB
Channel-to-Channel Isolation	V_{IN} = $5V_{PP}$ at 50kHz		120			*		dB
REFERENCE INPUT								
Range		0.1		$+V_{CC}$	*		*	V
Resistance	DCLK Static		5			*		GΩ
Input Current			45	100		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.5			*		µA
	DCLK Static		0.001	3		*	*	µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels								
V_{IH}	$\lvert I_{IH} \rvert \leq +5\mu A$	3.0		5.5	*		*	V
V_{IL}	$\lvert I_{IL} \rvert \leq +5\mu A$	–0.3		+0.8	*		*	V
V_{OH}	I_{OH} = –250µA	3.5			*			V
V_{OL}	I_{OL} = 250µA			0.4			*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENTS								
$+V_{CC}$	Specified Performance	4.75		5.25	*		*	V
Quiescent Current			550	900			*	µA
	f_{SAMPLE} = 12.5kHz		300			*		µA
	Power-Down Mode(3), $\overline{CS}$ = $+V_{CC}$			3			*	µA
Power Dissipation				4.5			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Same specifications as ADS7844E, ADS7844N.

NOTE: (1) LSB means Least Significant Bit. With V_{REF} equal to +5.0V, one LSB is 1.22mV. (2) First five harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{SHDN}$ = GND.

SPECIFICATION: +2.7V

At T_A = –40°C to +85°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS7844E, N			ADS7844EB, NB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT								
Full-Scale Input Span	Positive Input - Negative Input	0		V_{REF}	*		*	V
Absolute Input Range	Positive Input	–0.2		$+V_{CC}$ +0.2	*		*	V
	Negative Input	–0.2		+0.2	*		*	V
Capacitance			25			*		pF
Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
Resolution			12			*		Bits
No Missing Codes		12			*			Bits
Integral Linearity Error				±2			±1	LSB[1]
Differential Linearity Error			±0.8			±0.5	±1	LSB
Offset Error				±3			*	LSB
Offset Error Match			0.15	1.0		*	*	LSB
Gain Error				±4			±3	LSB
Gain Error Match			0.1	1.0		*	*	LSB
Noise			30			*		µVrms
Power Supply Rejection			70			*		dB
SAMPLING DYNAMICS								
Conversion Time				12			*	Clk Cycles
Acquisition Time		3			*			Clk Cycles
Throughput Rate				125			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion[2]	V_{IN} = $2.5V_{PP}$ at 10kHz		–75			–77		dB
Signal-to-(Noise + Distortion)	V_{IN} = $2.5V_{PP}$ at 10kHz		71			72		dB
Spurious Free Dynamic Range	V_{IN} = $2.5V_{PP}$ at 10kHz		78			80		dB
Channel-to-Channel Isolation	V_{IN} = $2.5V_{PP}$ at 50kHz		100			*		dB
REFERENCE INPUT								
Range		0.1		$+V_{CC}$	*		*	V
Resistance	DCLK Static		5			*		GΩ
Input Current			13	40		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.5			*		µA
	DCLK Static		0.001	3		*	*	µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels								
V_{IH}	$\lvert I_{IH} \rvert \leq +5\mu A$	$+V_{CC}$ • 0.7		5.5	*		*	V
V_{IL}	$\lvert I_{IL} \rvert \leq +5\mu A$	–0.3		+0.8	*		*	V
V_{OH}	I_{OH} = –250µA	$+V_{CC}$ • 0.8			*			V
V_{OL}	I_{OL} = 250µA			0.4			*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENTS								
$+V_{CC}$	Specified Performance	2.7		3.6	*		*	V
Quiescent Current			280	650		*	*	µA
	f_{SAMPLE} = 12.5kHz		220			*		µA
	Power-Down Mode[3], $\overline{CS}$ = $+V_{CC}$			3			*	µA
Power Dissipation				1.8			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Same specifications as ADS7844E, ADS7844N.

NOTE: (1) LSB means Least Significant Bit. With V_{REF} equal to +2.5V, one LSB is 610mV. (2) First five harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{SHDN}$ = GND.

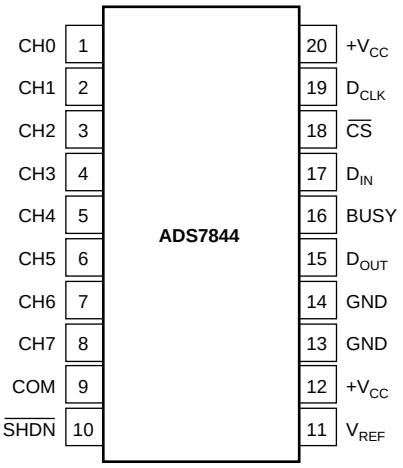
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	MAXIMUM GAIN ERROR (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE-LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7844E	±2	±4	–40°C to +85°C	QSOP-20	DBQ	ADS7844E	Rails, 56
"	"	"	"	"	"	ADS7844E/2K5	Tape and Reel, 2500
ADS7844N	"	"	"	SSOP-20	DB	ADS7844N	Rails, 68
"	"	"	"	"	"	ADS7844N/1K	Tape and Reel,1000
ADS7844EB	±1	±3	–40°C to +85°C	QSOP-20	DBQ	ADS7844EB	Rails, 56
"	"	"	"	"	"	ADS7844EB/2K5	Tape and Reel, 2500
ADS7844NB	"	"	"	SSOP-20	DB	ADS7844NB	Rails, 68
"	"	"	"	"	"	ADS7844NB/1K	Tape and Reel, 1000

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet.

PIN CONFIGURATION

Top View



ABSOLUTE MAXIMUM RATINGS(1)

$+V_{CC}$ to GND	–0.3V to +6V
Analog Inputs to GND	–0.3V to $+V_{CC}$ + 0.3V
Digital Inputs to GND	–0.3V to +6V
Power Dissipation	250mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	CH0	Analog Input Channel 0.
2	CH1	Analog Input Channel 1.
3	CH2	Analog Input Channel 2.
4	CH3	Analog Input Channel 3.
5	CH4	Analog Input Channel 4.
6	CH5	Analog Input Channel 5.
7	CH6	Analog Input Channel 6.
8	CH7	Analog Input Channel 7.
9	COM	Ground reference for analog inputs. Sets zero code voltage in single ended mode. Connect this pin to ground or ground reference point.
10	$\overline{SHDN}$	Shutdown. When LOW, the device enters a very low power shutdown mode.
11	V_{REF}	Voltage Reference Input. See Specification Table for ranges.
12	$+V_{CC}$	Power Supply, 2.7V to 5V.
13	GND	Ground
14	GND	Ground
15	D_{OUT}	Serial Data Output. Data is shifted on the falling edge of D_{CLK}. This output is high impedance when $\overline{CS}$ is high.
16	BUSY	Busy Output. Busy goes low when the DIN control bits are being read and also when the device is converting. The Output is high impedance when $\overline{CS}$ is High.
17	D_{IN}	Serial Data Input. If $\overline{CS}$ is LOW, data is latched on rising edge of D_{CLK}.
18	$\overline{CS}$	Chip Select Input. Active LOW. Data will not be clocked into D_{IN} unless $\overline{CS}$ is low. When $\overline{CS}$ is high D_{OUT} is high impedance.
19	CLK	External Clock Input. The clock speed determines the conversion rate by the equation $f_{CLK} = 16 \bullet f_{SAMPLE}$.
20	$+V_{CC}$	Power Supply

ELECTROSTATIC DISCHARGE SENSITIVITY

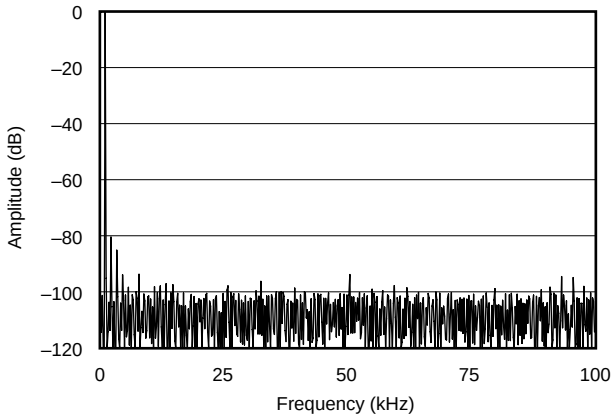
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

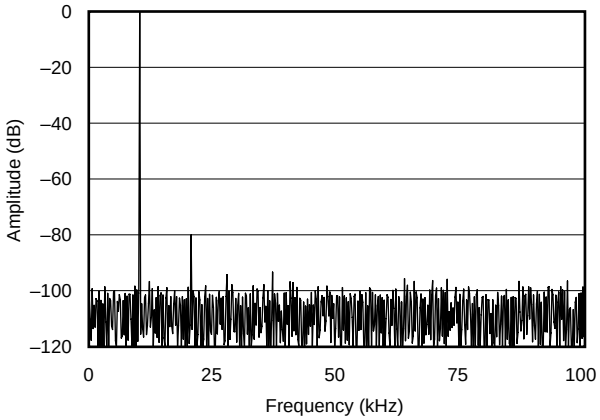
TYPICAL PERFORMANCE CURVES:+5V

At T_A = +25°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE} = 3.2MHz, unless otherwise noted.

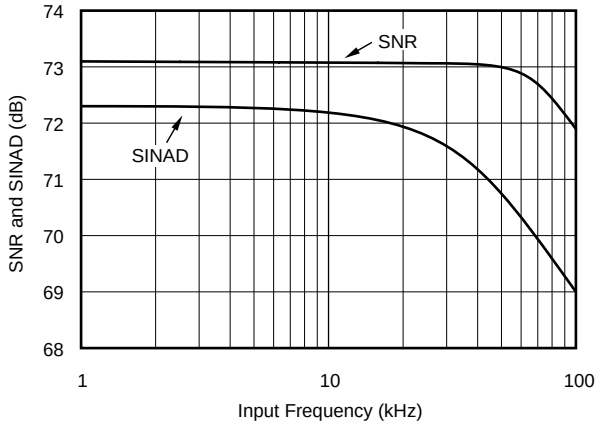
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1,123Hz, –0.2dB)



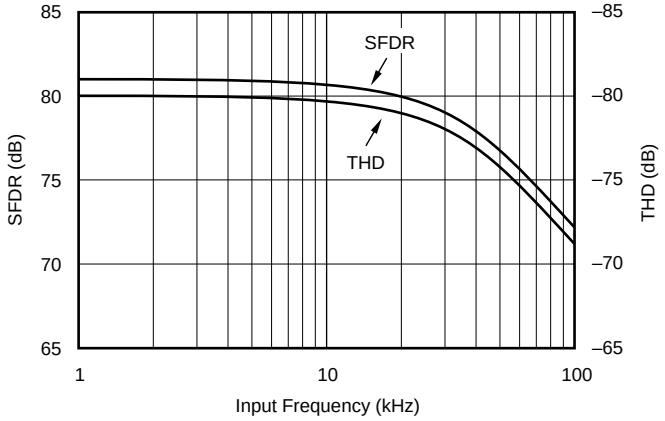
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 10.3kHz, –0.2dB)



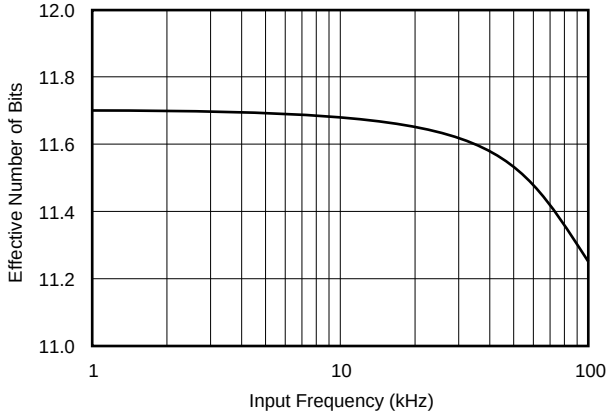
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-
(NOISE+DISTORTION) vs INPUT FREQUENCY



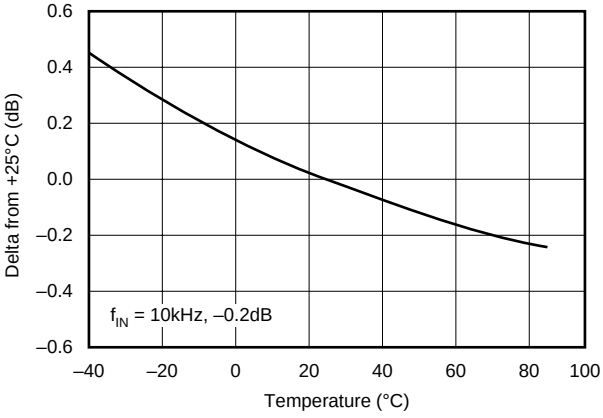
SPURIOUS FREE DYNAMIC RANGE AND TOTAL
HARMONIC DISTORTION vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY



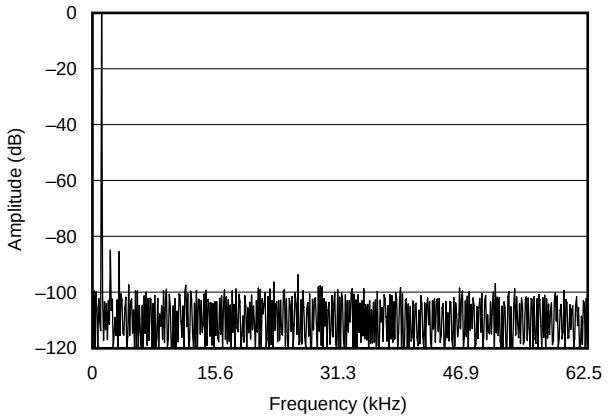
CHANGE IN SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE



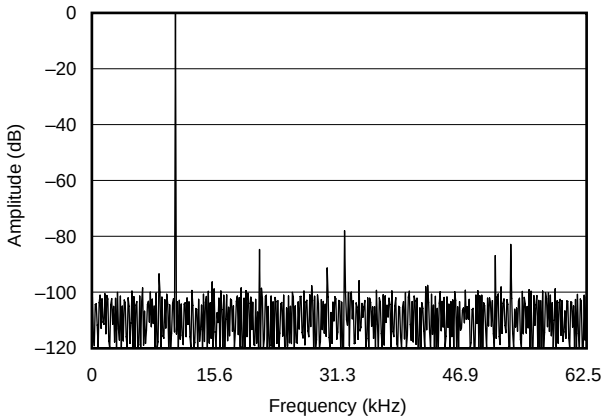
TYPICAL PERFORMANCE CURVES:+2.7V

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

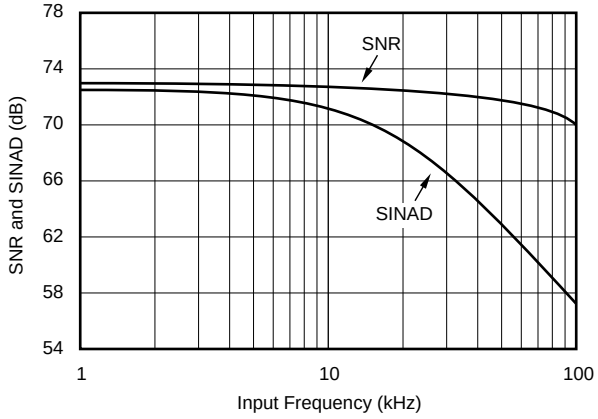
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1,129Hz, –0.2dB)



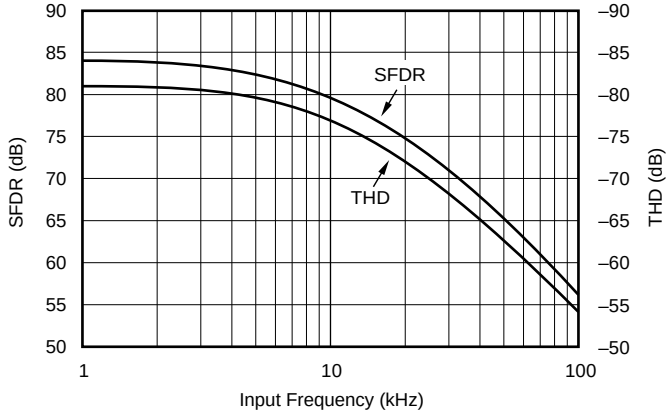
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 10.6kHz, –0.2dB)



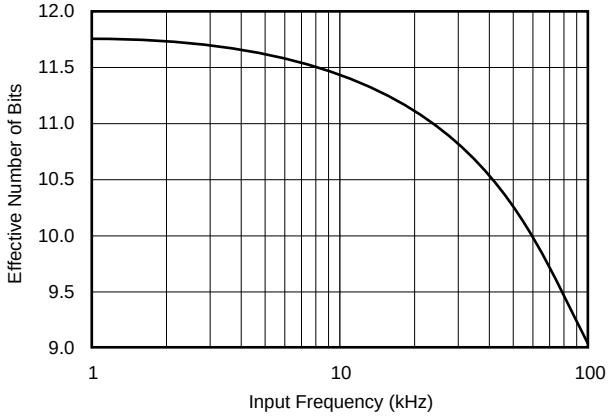
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-
(NOISE+DISTORTION) vs INPUT FREQUENCY



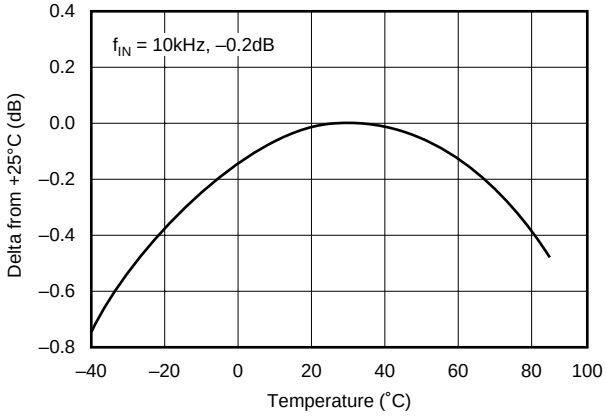
SPURIOUS FREE DYNAMIC RANGE AND TOTAL
HARMONIC DISTORTION vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY



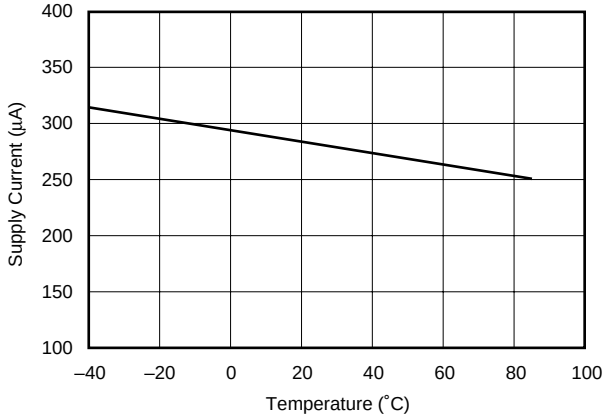
CHANGE IN SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE



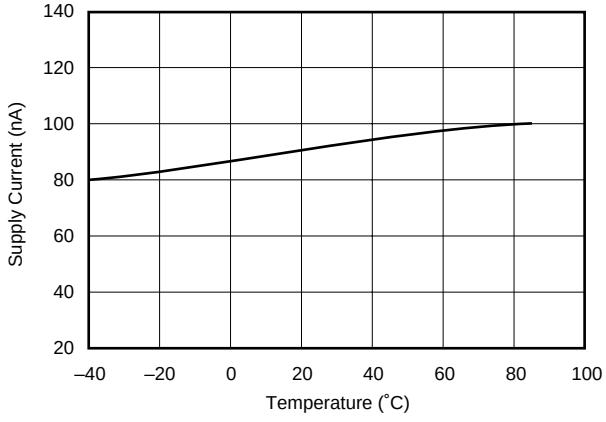
TYPICAL PERFORMANCE CURVES:+2.7V (CONT)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

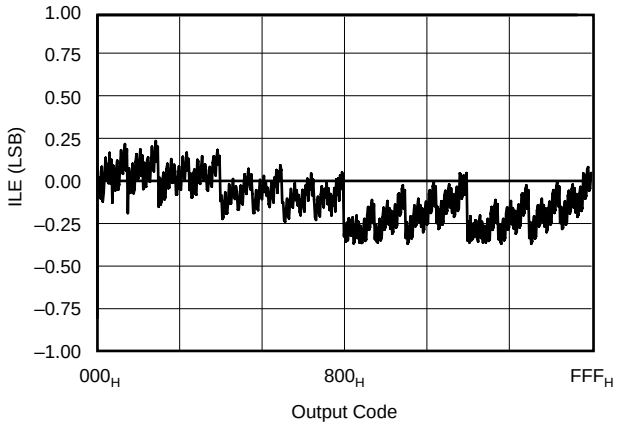
SUPPLY CURRENT vs TEMPERATURE



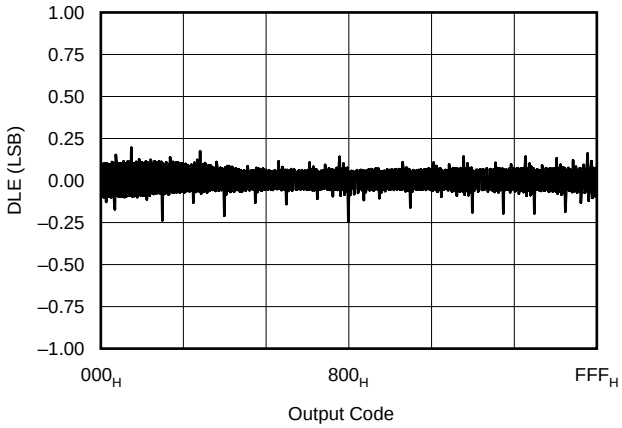
POWER DOWN SUPPLY CURRENT vs TEMPERATURE



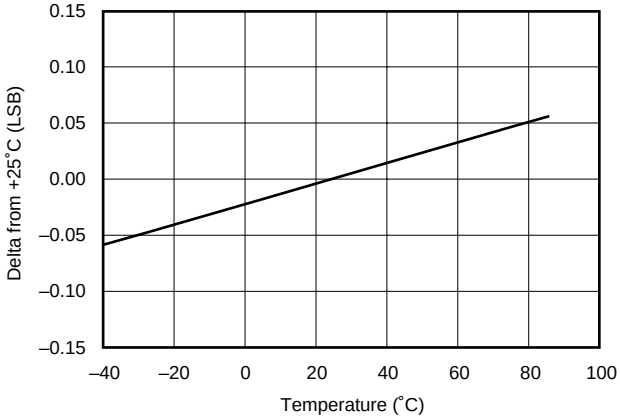
INTEGRAL LINEARITY ERROR vs CODE



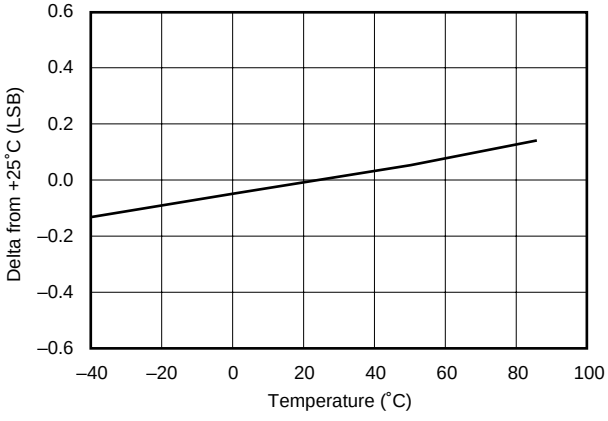
DIFFERENTIAL LINEARITY ERROR vs CODE



CHANGE IN GAIN vs TEMPERATURE



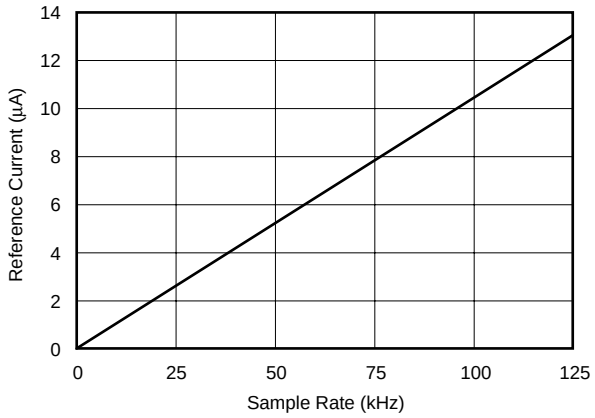
CHANGE IN OFFSET vs TEMPERATURE



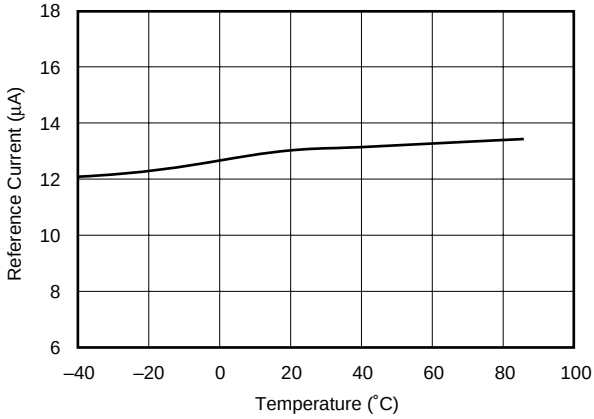
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

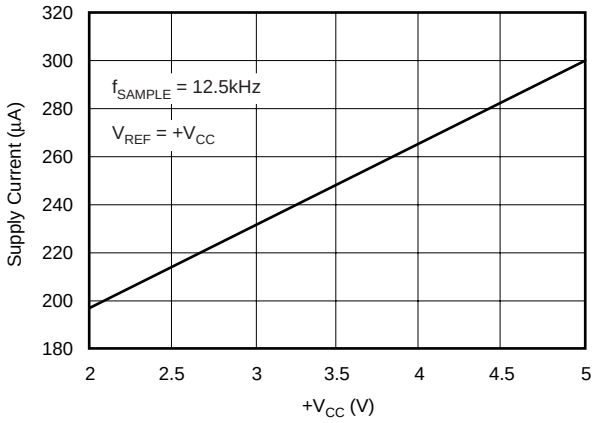
REFERENCE CURRENT vs SAMPLE RATE



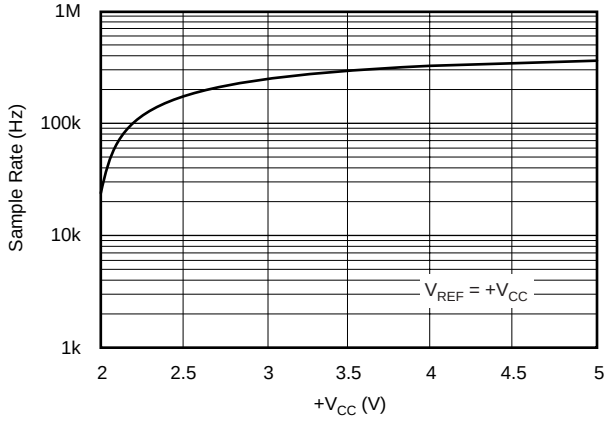
REFERENCE CURRENT vs TEMPERATURE



SUPPLY CURRENT vs $+V_{CC}$



MAXIMUM SAMPLE RATE vs $+V_{CC}$



THEORY OF OPERATION

The ADS7844 is a classic successive approximation register (SAR) analog-to-digital (A/D) converter. The architecture is based on capacitive redistribution which inherently includes a sample/hold function. The converter is fabricated on a 0.6µs CMOS process.

The basic operation of the ADS7844 is shown in Figure 1. The device requires an external reference and an external clock. It operates from a single supply of 2.7V to 5.25V. The external reference can be any voltage between 100mV and $+V_{CC}$. The value of the reference voltage directly sets the input range of the converter. The average reference input current depends on the conversion rate of the ADS7844.

The analog input to the converter is differential and is provided via an eight-channel multiplexer. The input can be provided in reference to a voltage on the COM pin (which is generally ground) or differentially by using four of the eight input channels (CH0 - CH7). The particular configuration is selectable via the digital interface.

ANALOG INPUT

Figure 2 shows a block diagram of the input multiplexer on the ADS7844. The differential input of the converter is derived from one of the eight inputs in reference to the COM pin or four of the eight inputs. Table I and Table II show the relationship between the A2, A1, A0, and SGL/$\overline{\text{DIF}}$ control bits and the configuration of the analog multiplexer. The control bits are provided serially via the DIN pin, see the Digital Interface section of this data sheet for more details.

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs (see Figure 2) is captured on the internal capacitor array. The voltage on the –IN input is limited between –0.2V and 1.25V, allowing the input to reject small signals which are common to both the +IN and –IN input. The +IN input has a range of –0.2V to $+V_{CC}$ + 0.2V.

The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typi-

A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	+IN								–IN
1	0	0		+IN							–IN
0	0	1			+IN						–IN
1	0	1				+IN					–IN
0	1	0					+IN				–IN
1	1	0						+IN			–IN
0	1	1							+IN		–IN
1	1	1								+IN	–IN

TABLE I. Single-Ended Channel Selection (SGL/$\overline{\text{DIF}}$ HIGH).

A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+IN	–IN						
0	0	1			+IN	–IN				
0	1	0					+IN	–IN		
0	1	1							+IN	–IN
1	0	0	–IN	+IN						
1	0	1			–IN	+IN				
1	1	0					–IN	+IN		
1	1	1							–IN	+IN

TABLE II. Differential Channel Control (SGL/$\overline{\text{DIF}}$ LOW).

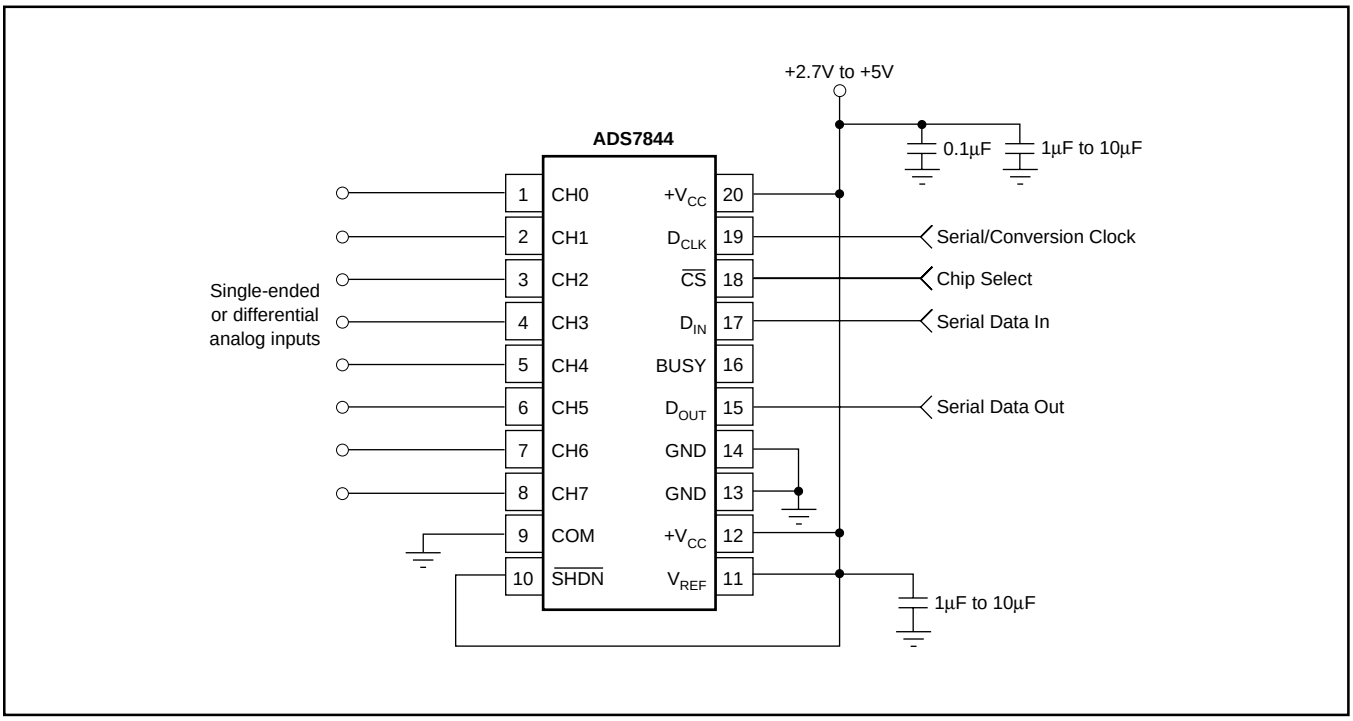


FIGURE 1. Basic Operation of the ADS7844.

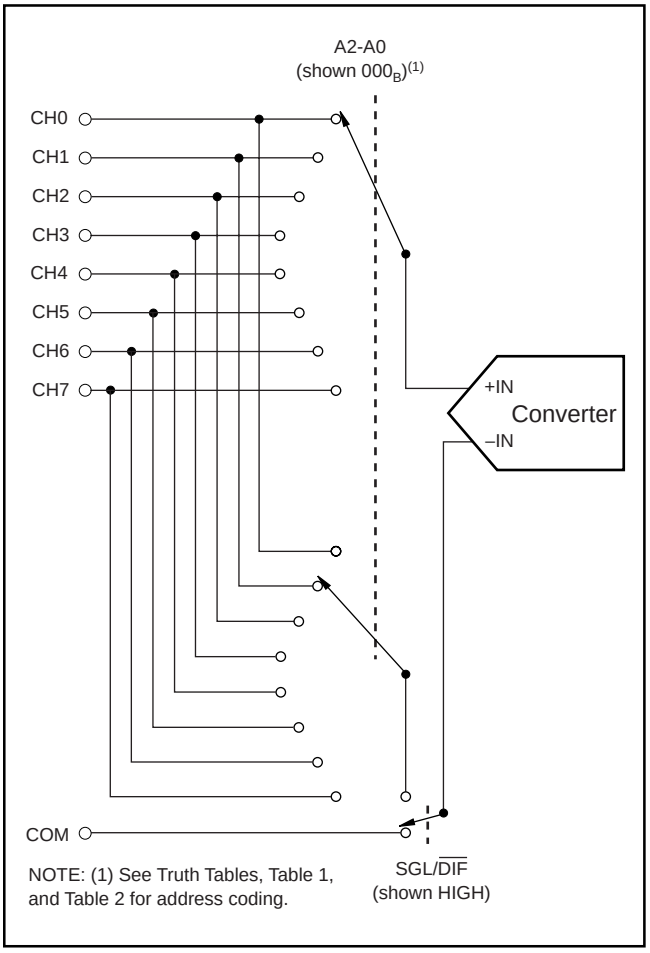


FIGURE 2. Simplified Diagram of the Analog Input.

cally 25pF). After the capacitor has been fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

REFERENCE INPUT

The external reference sets the analog input range. The ADS7844 will operate with a reference in the range of 100mV to $+V_{CC}$. Keep in mind that the analog input is the difference between the +IN input and the –IN input as shown in Figure 2. For example, in the single-ended mode, a 1.25V reference, and with the COM pin grounded, the selected input channel (CH0 - CH7) will properly digitize a signal in the range of 0V to 1.25V. If the COM pin is connected to 0.5V, the input range on the selected channel is 0.5V to 1.75V.

There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. Any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2 LSBs with a 2.5V reference, then it will typically be 10 LSBs with a 0.5V reference. In each case, the actual offset of the device is the same, 1.22mV.

Likewise, the noise or uncertainty of the digitized output will increase with lower LSB size. With a reference voltage of 100mV, the LSB size is 24μV. This level is below the internal noise of the device. As a result, the digital output code will not be stable and vary around a mean value by a number of LSBs. The distribution of output codes will be gaussian and the noise can be reduced by simply averaging consecutive conversion results or applying a digital filter.

With a lower reference voltage, care should be taken to provide a clean layout including adequate bypassing, a clean (low noise, low ripple) power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter will also be more sensitive to nearby digital signals and electromagnetic interference.

The voltage into the V_{REF} input is not buffered and directly drives the capacitor digital-to-analog converter (CDAC) portion of the ADS7844. Typically, the input current is 13μA with a 2.5V reference. This value will vary by microamps depending on the result of the conversion. The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period will not reduce overall current drain from the reference.

DIGITAL INTERFACE

Figure 3 shows the typical operation of the ADS7844's digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface (note that the digital inputs are over-voltage tolerant up to 5.5V, regardless of $+V_{CC}$). Each communication between the processor and the converter consists of eight clock cycles. One complete conversion can be accomplished with three serial communications, for a total of 24 clock cycles on the DCLK input.

The first eight clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer appropriately, it enters the acquisition (sample) mode. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample/hold goes into the hold mode. The next twelve clock cycles accomplish the actual analog-to-digital conversion. A thirteenth clock cycle is needed for the last bit of the conversion result. Three more clock cycles are needed to complete the last byte (DOUT will be LOW). These will be ignored by the converter.

Control Byte

Also shown in Figure 3 is the placement and order of the control bits within the control byte. Tables III and IV give detailed information about these bits. The first bit, the 'S' bit, must always be HIGH and indicates the start of the control byte. The ADS7844 will ignore inputs on the DIN pin until the start bit is detected. The next three bits (A2 - A0) select the active input channel or channels of the input multiplexer (see Tables I and II and Figure 2).

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
S	A2	A1	A0	—	SGL/$\overline{\text{DIF}}$	PD1	PD0

TABLE III. Order of the Control Bits in the Control Byte.

BIT	NAME	DESCRIPTION
7	S	Start Bit. Control byte starts with first HIGH bit on DIN. A new control byte starts with every 15th clock cycle.
6 - 4	A2 - A0	Channel Select Bits. Along with the SGL/DIF bit, these bits control the setting of the multiplexer input as detailed in Tables I and II.
3	—	Not Used.
2	SGL/$\overline{\text{DIF}}$	Single-Ended/Differential Select Bit. Along with bits A2 - A0, this bit controls the setting of the multiplexer input as detailed in Tables I and II.
1 - 0	PD1 - PD0	Power-Down Mode Select Bits. See Table V for details.

TABLE IV. Descriptions of the Control Bits within the Control Byte.

The SGL/$\overline{\text{DIF}}$ bit controls the multiplexer input mode: either single-ended (HIGH) or differential (LOW). In single-ended mode, the selected input channel is referenced to the COM pin. In differential mode, the two selected inputs provide a differential input. See Tables I and II and Figure 2 for more information. The last two bits (PD1 - PD0) select the power-down mode as shown in Table V. If both inputs are HIGH, the device is always powered up. If both inputs are LOW, the device enters a power-down mode between conversions. When a new conversion is initiated, the device will resume normal operation instantly—no delay is needed to allow the device to power up and the very first conversion will be valid.

16-Clocks per Conversion

The control bits for conversion n+1 can be overlapped with conversion 'n' to allow for a conversion every 16 clock cycles, as shown in Figure 4. This figure also shows possible serial communication occurring with other serial peripherals between each byte transfer between the processor and the converter. This is possible provided that each conversion completes within 1.6ms of starting. Otherwise, the signal that has been captured on the input sample/hold may droop enough to affect the conversion result. In addition, the ADS7844 is fully powered while other serial communications are taking place.

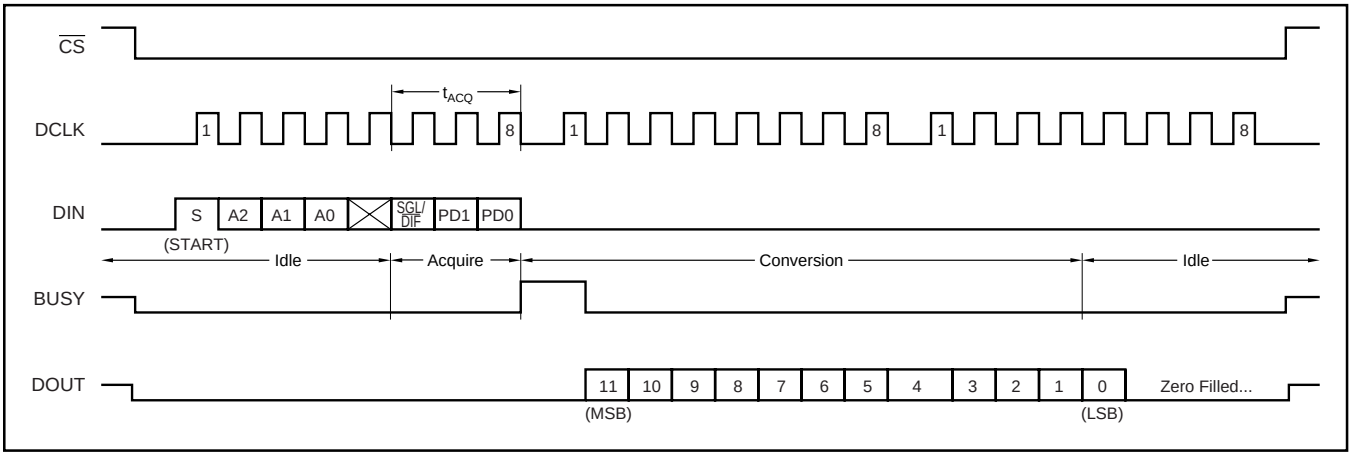


FIGURE 3. Conversion Timing, 24-Clocks per Conversion, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

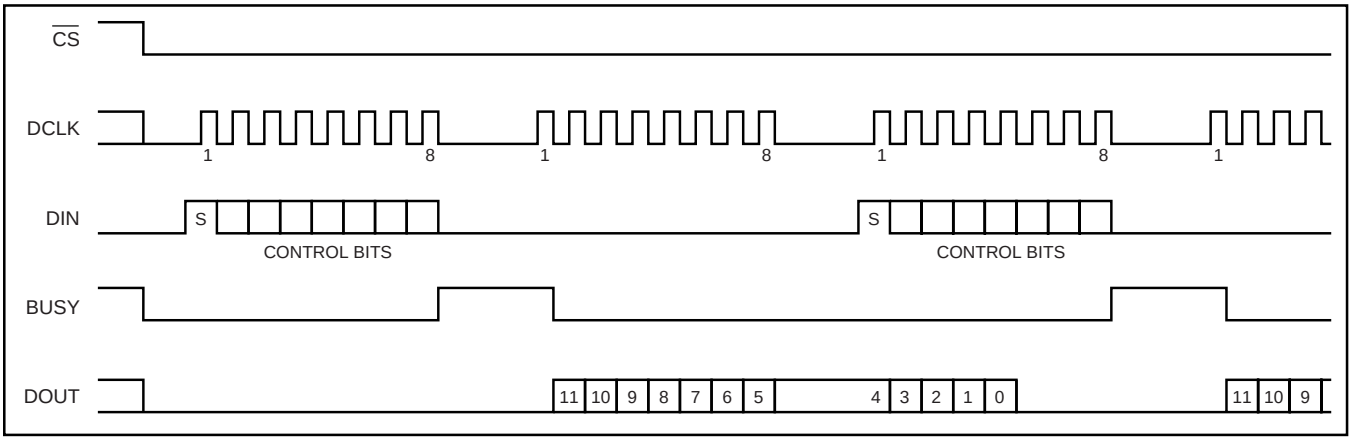


FIGURE 4. Conversion Timing, 16-Clocks per Conversion, 8-bit Bus Interface. No DCLK delay required with dedicated serial port.

PD1	PD0	Description
0	0	Power-down between conversions. When each conversion is finished, the converter enters a low power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to assure full operation and the very first conversion is valid.
0	1	Reserved for future use.
1	0	Reserved for future use.
1	1	No power-down between conversions, device always powered.

TABLE V. Power-Down Selection.

Digital Timing

Figure 5 and Tables VI and VII provide detailed timing for the digital interface of the ADS7844.

15-Clocks per Conversion

Figure 6 provides the fastest way to clock the ADS7844. This method will not work with the serial interface of most microcontrollers and digital signal processors as they are generally not capable of providing 15 clock cycles per serial transfer. However, this method could be used with field programmable gate arrays (FPGAs) or application specific integrated circuits (ASICs). Note that this effectively increases the maximum conversion rate of the converter beyond the values given in the specification tables, which assume 16 clock cycles per conversion.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	1.5			µs
t_{DS}	DIN Valid Prior to DCLK Rising	100			ns
t_{DH}	DIN Hold After DCLK HIGH	10			ns
t_{DO}	DCLK Falling to DOUT Valid			200	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			200	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			200	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	100			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	200			ns
t_{CL}	DCLK LOW	200			ns
t_{BD}	DCLK Falling to BUSY Rising			200	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			200	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			200	ns

TABLE VI. Timing Specifications ($+V_{CC}$ = +2.7V to 3.6V, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	900			ns
t_{DS}	DIN Valid Prior to DCLK Rising	50			ns
t_{DH}	DIN Hold After DCLK HIGH	10			ns
t_{DO}	DCLK Falling to DOUT Valid			100	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			70	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			70	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	50			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	150			ns
t_{CL}	DCLK LOW	150			ns
t_{BD}	DCLK Falling to BUSY Rising			100	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			70	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			70	ns

TABLE VII. Timing Specifications ($+V_{CC}$ = +4.75V to +5.25V, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

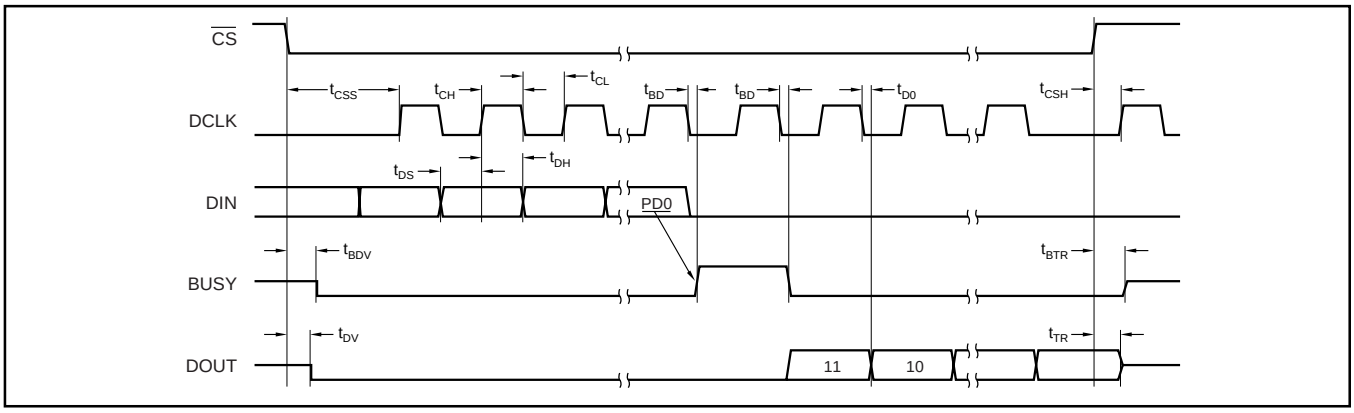


FIGURE 5. Detailed Timing Diagram.

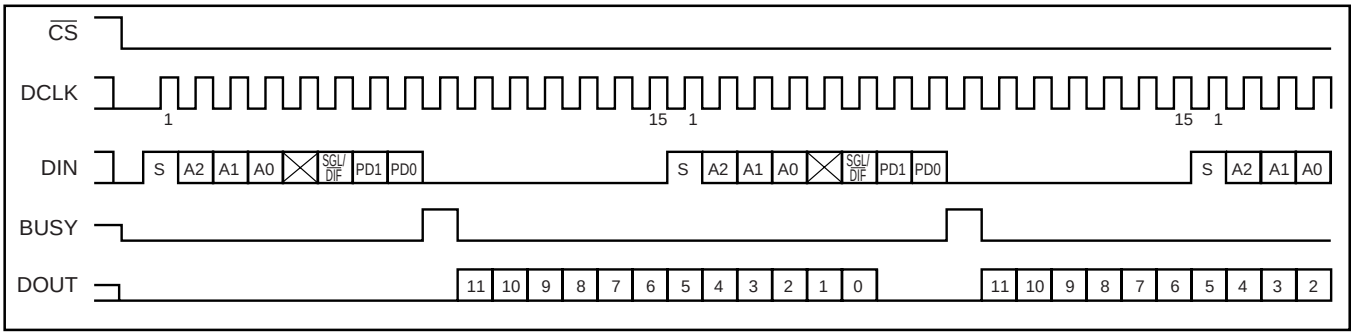


FIGURE 6. Maximum Conversion Rate, 15-Clocks per Conversion.

Data Format

The ADS7844 output data is in straight binary format as shown in Figure 7. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.

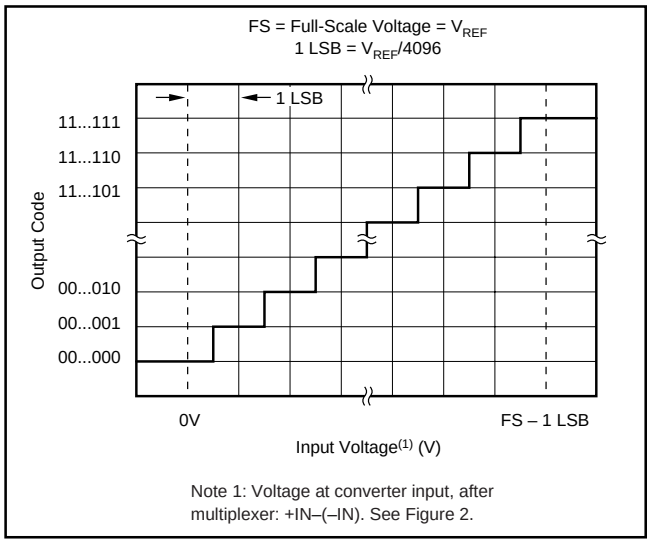


FIGURE 7. Ideal Input Voltages and Output Codes.

POWER DISSIPATION

There are three power modes for the ADS7844: full power (PD1 - PD0 = 11B), auto power-down (PD1 - PD0 = 00B), and shutdown ($\overline{SHDN}$ LOW). The affects of these modes varies depending on how the ADS7844 is being operated. For example, at full conversion rate and 16 clocks per conversion, there is very little difference between full power mode and auto power-down. Likewise, if the device has entered auto power-down, a shutdown ($\overline{SHDN}$ LOW) will not lower power dissipation.

When operating at full-speed and 16-clocks per conversion (as shown in Figure 4), the ADS7844 spends most of its time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Thus, the difference between full power mode and auto power-down is negligible. If the conversion rate is decreased by simply slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion, but conversion are simply done less often, then the difference between the two modes is dramatic. Figure 8 shows the difference between reducing the DCLK frequency ("scaling" DCLK to match the conversion rate) or maintaining DCLK at the highest frequency and reducing the number of conversion per second. In the later case, the converter spends an increasing percentage of its time in power-down mode (assuming the auto power-down mode is active).

If DCLK is active and $\overline{CS}$ is LOW while the ADS7844 is in auto power-down mode, the device will continue to dissipate some power in the digital logic. The power can be reduced to a minimum by keeping $\overline{CS}$ HIGH. The differences in supply current for these two cases are shown in Figure 9.

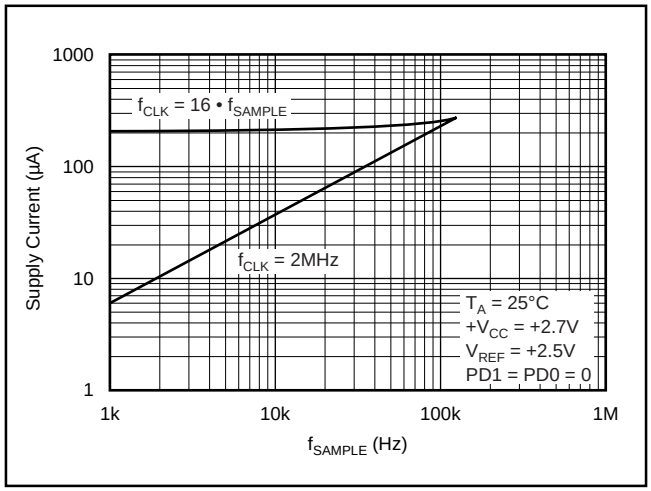


FIGURE 8. Supply Current vs Directly Scaling the Frequency of DCLK with Sample Rate or Keeping DCLK at the Maximum Possible Frequency.

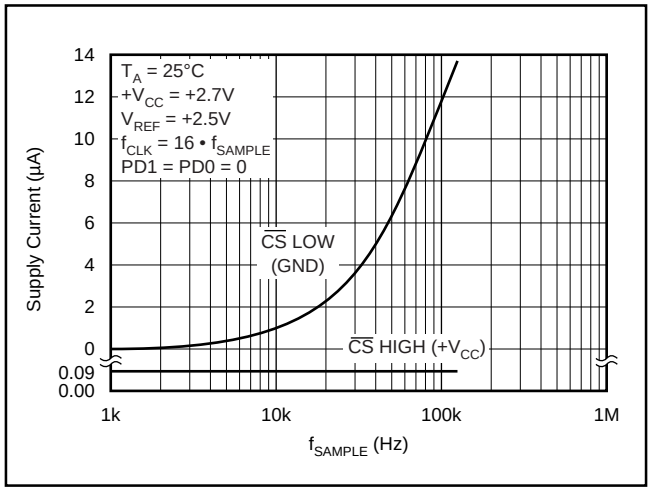


FIGURE 9. Supply Current vs State of $\overline{CS}$.

Operating the ADS7844 in auto power-down mode will result in the lowest power dissipation, and there is no conversion time "penalty" on power-up. The very first conversion will be valid. $\overline{SHDN}$ can be used to force an immediate power-down.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7844 circuitry. This is particularly true if the reference voltage is low and/or the conversion rate is high.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and

high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

With this in mind, power to the ADS7844 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor and a 5Ω or 10Ω series resistor may be used to lowpass filter a noisy supply.

The reference should be similarly bypassed with a 0.1µF capacitor. Again, a series resistor and large capacitor can be used to lowpass filter the reference voltage. If the reference voltage originates from an op amp, make sure that it can drive the bypass capacitor without oscillation (the series resistor can help in this case). The ADS7844 draws very little current from the reference on average, but it does place larger demands on the reference circuitry over short periods of time (on each rising edge of DCLK during a conversion).

The ADS7844 architecture offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high frequency noise can be filtered out as discussed in the previous paragraph, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the “analog” ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7844E	ACTIVE	SSOP	DBQ	20	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7844E	Samples
ADS7844E/2K5	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS7844E	Samples
ADS7844E/2K5G4	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS7844E	Samples
ADS7844EB	ACTIVE	SSOP	DBQ	20	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7844E B	Samples
ADS7844EB/2K5	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7844E B	Samples
ADS7844EBG4	ACTIVE	SSOP	DBQ	20	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7844E B	Samples
ADS7844EG4	ACTIVE	SSOP	DBQ	20	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7844E	Samples
ADS7844N	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7844N	Samples
ADS7844N/1K	ACTIVE	SSOP	DB	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS7844N	Samples
ADS7844N/1KG4	ACTIVE	SSOP	DB	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS7844N	Samples
ADS7844NB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7844N B	Samples
ADS7844NB/1K	ACTIVE	SSOP	DB	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7844N B	Samples
ADS7844NB/1KG4	ACTIVE	SSOP	DB	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7844N B	Samples
ADS7844NBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7844N B	Samples
ADS7844NG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ADS7844N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

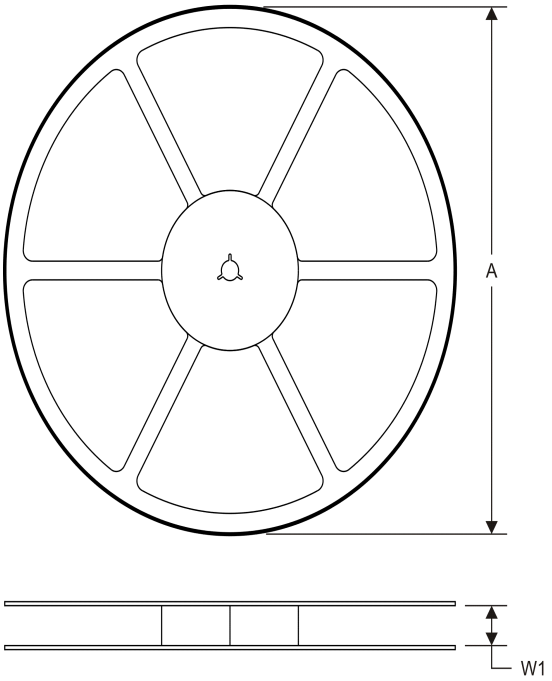
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

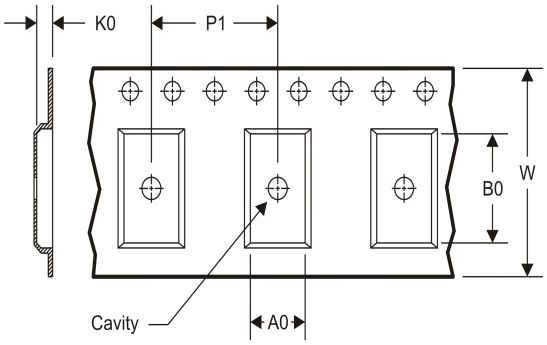
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



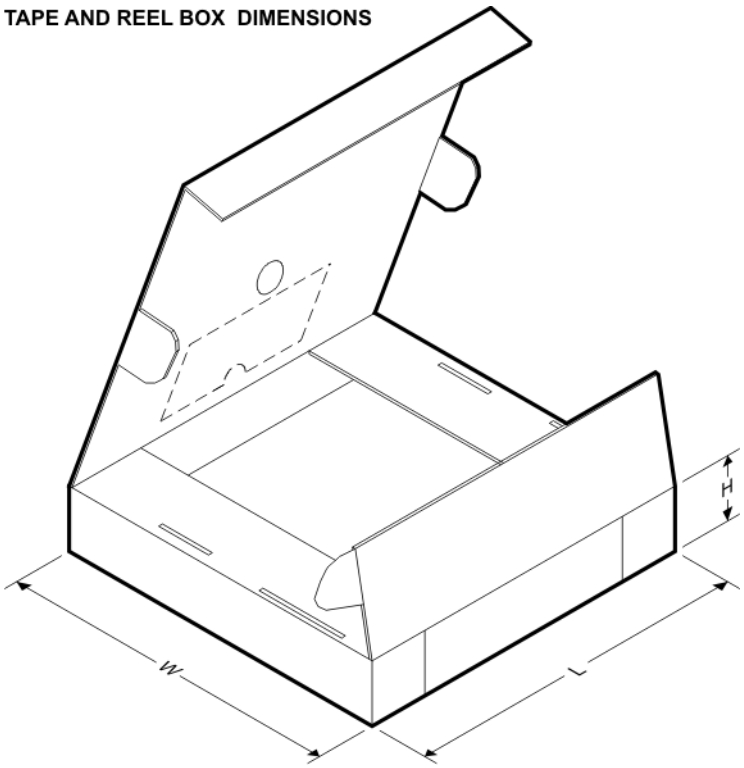
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7844E/2K5	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
ADS7844EB/2K5	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
ADS7844N/1K	SSOP	DB	20	1000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
ADS7844NB/1K	SSOP	DB	20	1000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

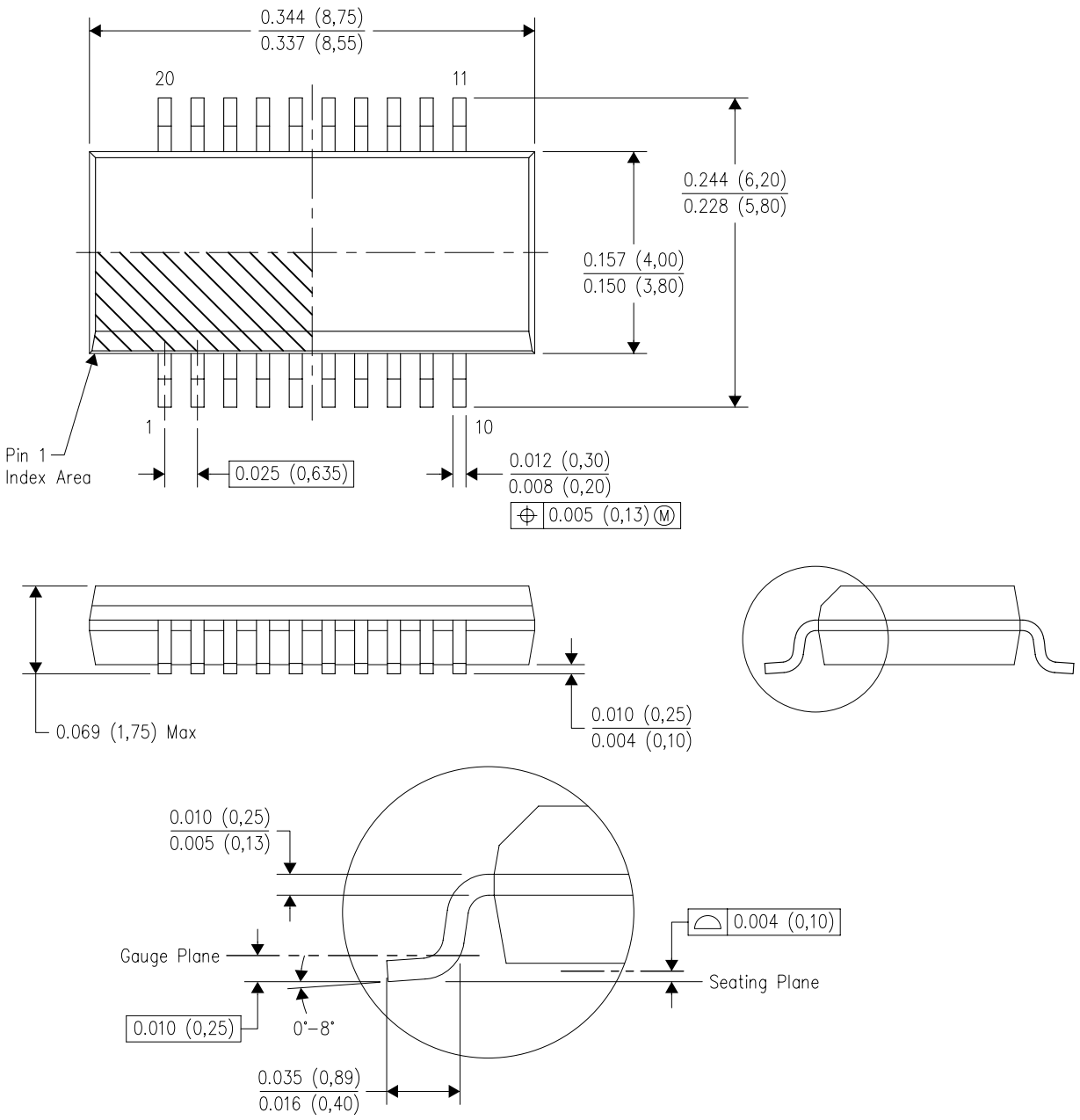
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

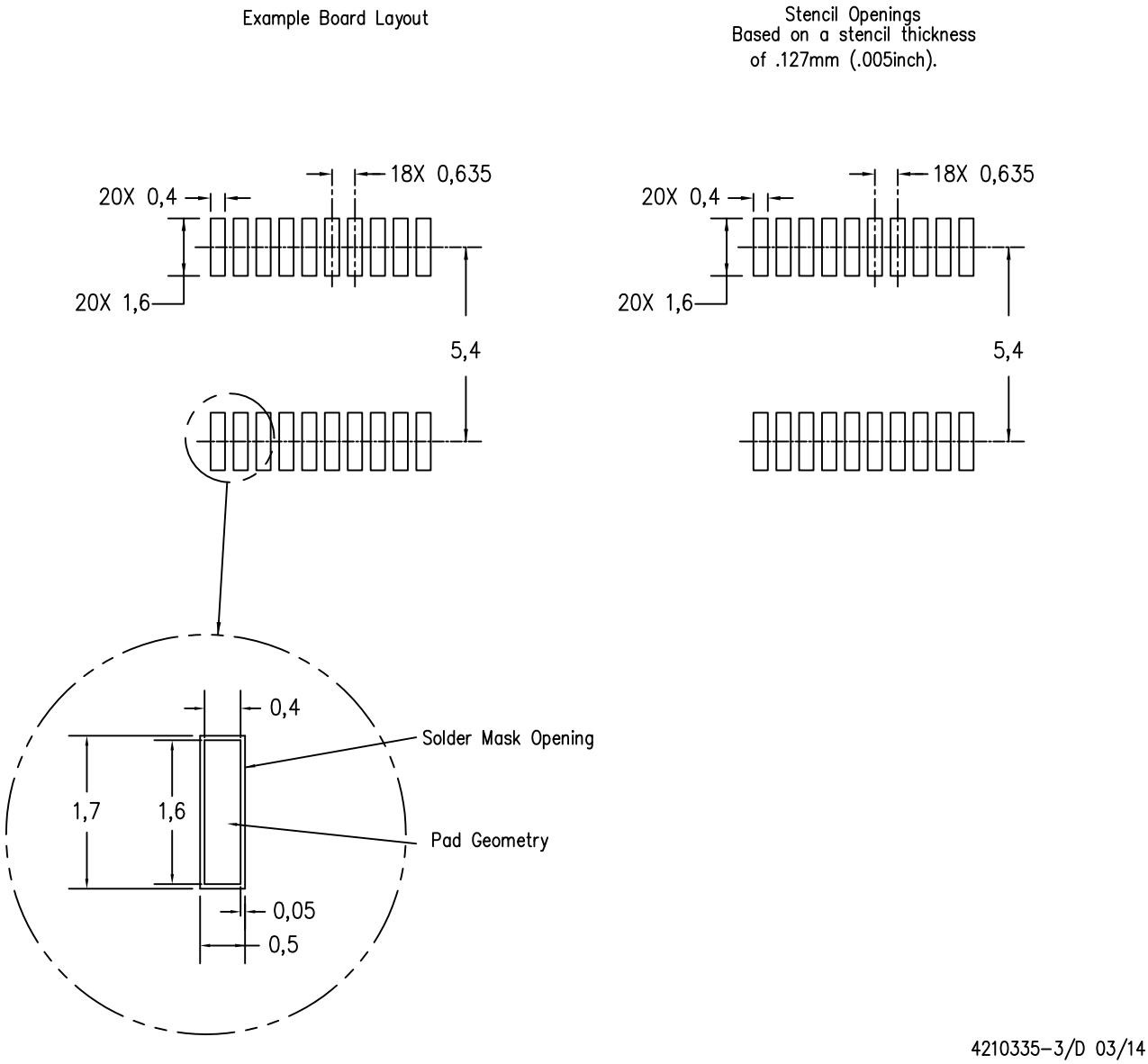
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7844E/2K5	SSOP	DBQ	20	2500	367.0	367.0	38.0
ADS7844EB/2K5	SSOP	DBQ	20	2500	367.0	367.0	38.0
ADS7844N/1K	SSOP	DB	20	1000	367.0	367.0	38.0
ADS7844NB/1K	SSOP	DB	20	1000	367.0	367.0	38.0

DBQ (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AD.

DBQ (R–PDSO–G20) PLASTIC SMALL OUTLINE PACKAGE



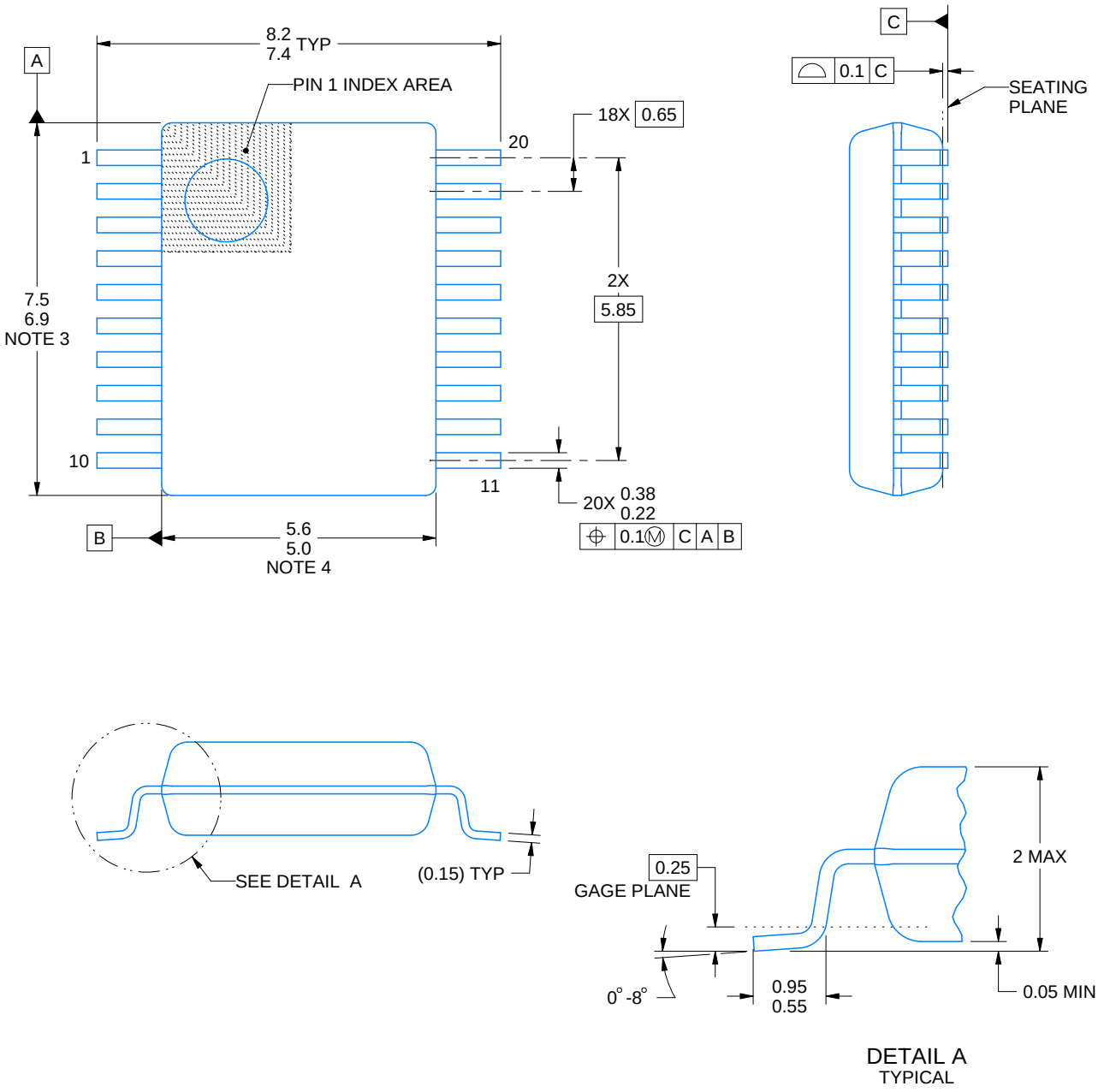
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

DB0020A

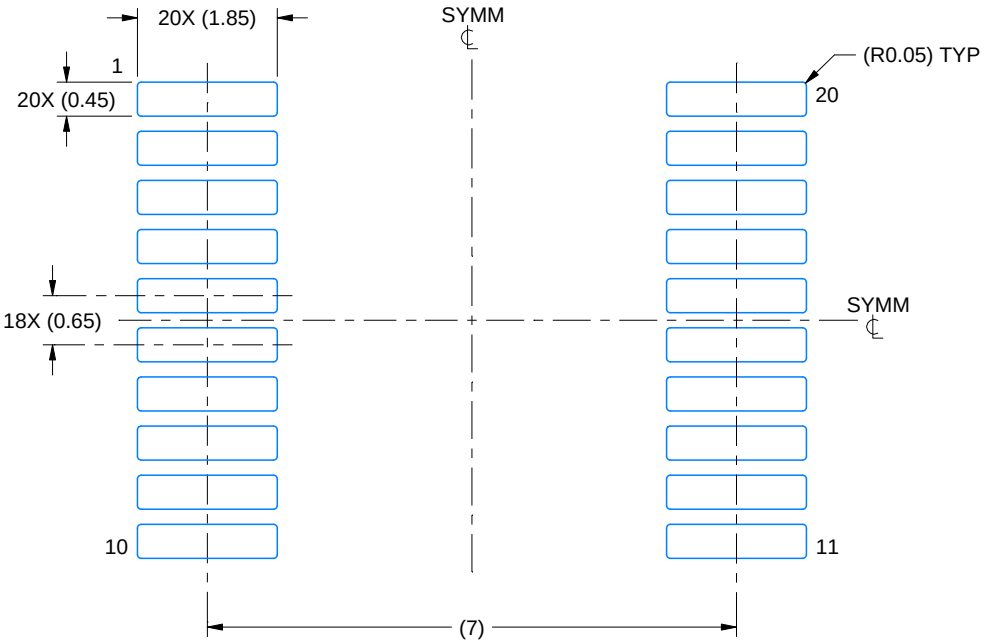
TSSOP - 2 mm max height

SMALL OUTLINE PACKAGE

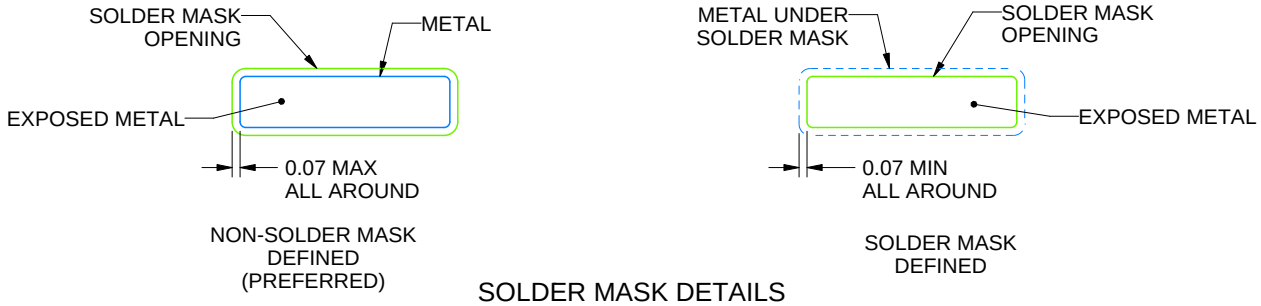


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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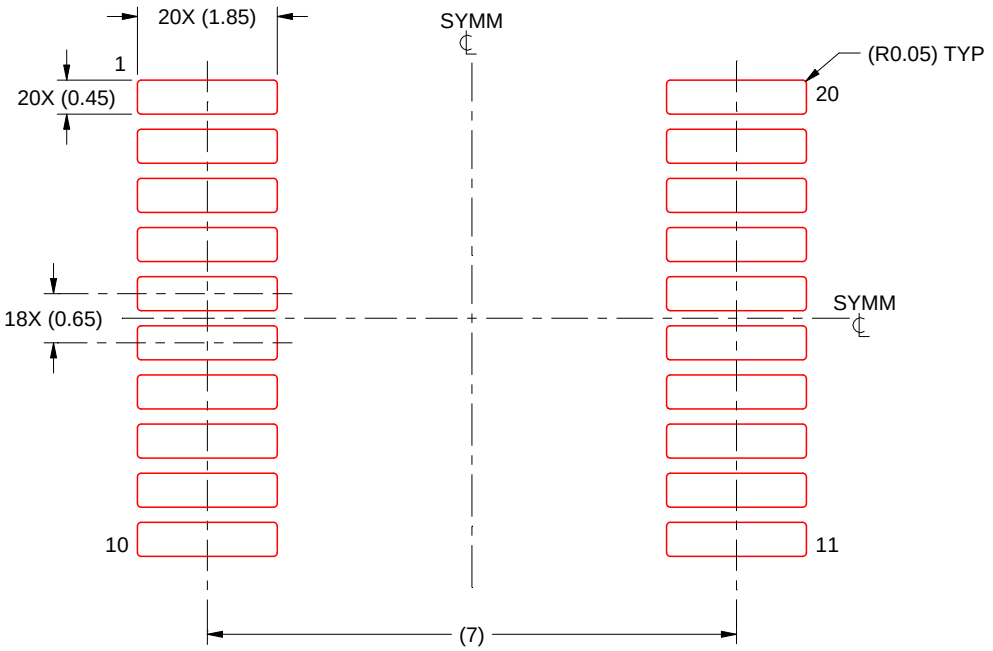
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265