HIGH-SPEED 32K x 16 DUAL-PORT STATIC RAM

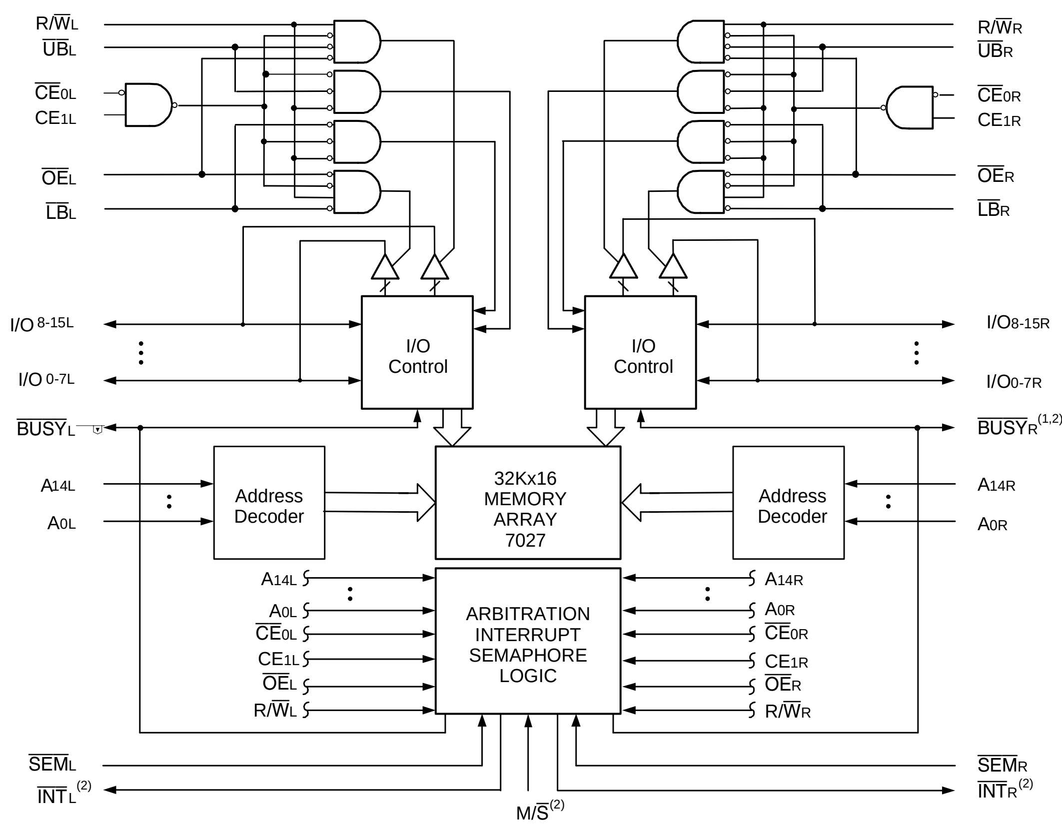
IDT7027S/L

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

Features

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed access
  - Commercial: 15/20/25/35/55ns (max.)
  - Industrial: 20/25ns (max.)
- Low-power operation
  - IDT7027S
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - IDT7027L
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- Separate upper-byte and lower-byte control for bus matching capability.
- Dual chip enables allow for depth expansion without external logic
- IDT7027 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = V_{IH} for $\overline{BUSY}$ output flag on Master, M/$\overline{S}$ = V_{IL} for $\overline{BUSY}$ input on Slave
- Busy and Interrupt Flags
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- TTL-compatible, single 5V (±10%) power supply
- Available in 100-pin Thin Quad Flatpack (TQFP) and 108-pin Ceramic Pin Grid Array (PGA)
- Industrial temperature range (–40°C to +85°C) is available for selected speeds
- Green parts available, see ordering information

Functional Block Diagram



NOTES:
1. $\overline{BUSY}$ is an input as a Slave (M/$\overline{S}$=V_{IL}) and an output as a Master (M/$\overline{S}$=V_{IH}).
2. $\overline{BUSY}$ and $\overline{INT}$ are non-tri-state totem-pole outputs (push-pull).

JUNE 2018

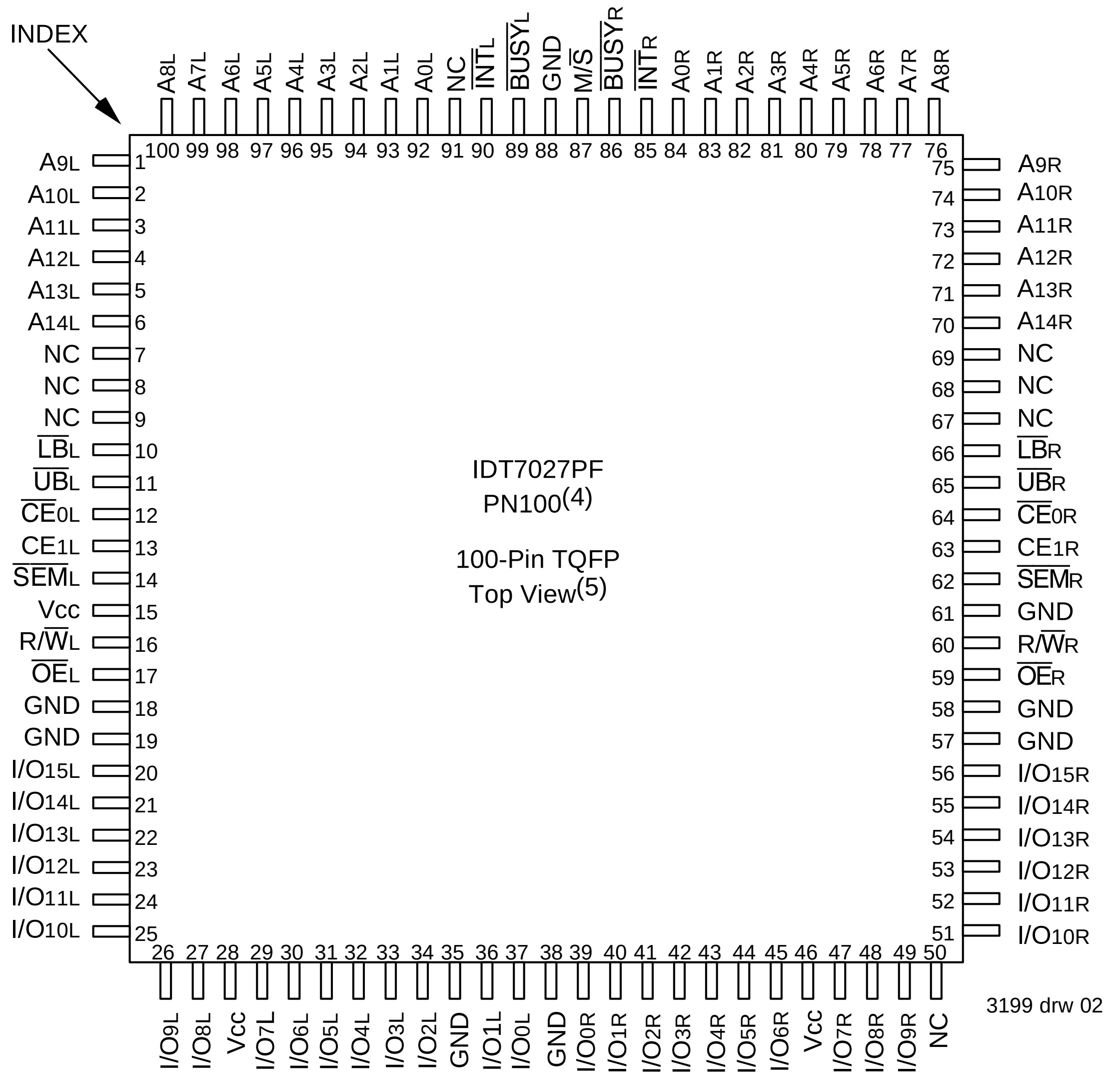
Description

The IDT7027 is a high-speed 32K x 16 Dual-Port Static RAM, designed to be used as a stand-alone 512K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

The device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by the chip enables ($\overline{CE}_0$ and CE_1) permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using CMOS high-performance technology, these devices typically operate on only 750mW of power. The IDT7027 is packaged in a 100-pin Thin Quad Flatpack (TQFP) and a 108-pin ceramic Pin Grid Array (PGA).

Pin Configurations(1,2,3)



NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configurations(1,2,3) (con't.)

	A	B	C	D	E	F	G	H	J	K	L	M
12	81 A_{10R}	80 A_{11R}	77 A_{14R}	74 NC	72 $\overline{UB}_R$	69 $\overline{SEM}_R$	68 GND	65 GND	63 NC	60 I/O_{13R}	57 I/O_{10R}	54 NC
11	84 A_{7R}	83 A_{8R}	78 A_{13R}	76 NC	73 $\overline{LB}_R$	70 CE_{1R}	67 $R/\overline{W}_R$	64 GND	61 I/O_{14R}	59 I/O_{12R}	56 I/O_{9R}	53 NC
10	87 A_{4R}	86 A_{5R}	82 A_{9R}	79 A_{12R}	75 NC	71 $\overline{CE}_{0R}$	66 $\overline{OE}_R$	62 I/O_{15R}	58 I/O_{11R}	55 NC	51 I/O_{8R}	50 I/O_{7R}
09	90 A_{1R}	88 A_{3R}	85 A_{6R}							52 NC	49 Vcc	47 I/O_{5R}
08	92 $\overline{INT}_R$	91 A_{0R}	89 A_{2R}							48 I/O_{6R}	46 I/O_{4R}	45 I/O_{3R}
07	95 GND	94 $M/\overline{S}$	93 $\overline{BUSY}_R$							44 I/O_{2R}	43 I/O_{1R}	42 I/O_{0R}
06	96 $\overline{BUSY}_L$	97 $\overline{INT}_L$	98 NC							39 I/O_{1L}	40 I/O_{0L}	41 GND
05	99 A_{0L}	100 A_{1L}	102 A_{3L}							35 I/O_{4L}	37 I/O_{2L}	38 GND
04	101 A_{2L}	103 A_{4L}	106 A_{7L}							31 Vcc	34 I/O_{5L}	36 I/O_{3L}
03	104 A_{5L}	105 A_{6L}	1 A_{10L}	4 A_{13L}	8 NC	12 CE_{1L}	17 GND	21 I/O_{14L}	25 I/O_{10L}	28 NC	32 I/O_{7L}	33 I/O_{6L}
02	107 A_{8L}	2 A_{11L}	5 A_{14L}	7 NC	10 $\overline{UB}_L$	13 $\overline{SEM}_L$	16 $\overline{OE}_L$	19 GND	22 I/O_{13L}	24 I/O_{11L}	29 NC	30 I/O_{8L}
01	108 A_{9L}	3 A_{12L}	6 NC	9 $\overline{LB}_L$	11 $\overline{CE}_{0L}$	14 Vcc	15 $R/\overline{W}_L$	18 NC	20 I/O_{15L}	23 I/O_{12L}	26 I/O_{9L}	27 NC

IDT7027G
G108(4)

108-Pin PGA
Top View(5)

INDEX

3199 drw 03

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately 1.21 in x 1.21 in x .16 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{14L}	A_{0R} - A_{14R}	Address
I/O_{0L} - I/O_{15L}	I/O_{0R} - I/O_{15R}	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

3199 tbl 01

Truth Table I – Chip Enable

$\overline{CE}$	$\overline{CE}_0$	CE_1	Mode
L	V_{IL}	V_{IH}	Port Selected (TTL Active)
	$\leq$ 0.2V	$\geq V_{CC}$ - 0.2V	Port Selected (CMOS Active)
H	V_{IH}	X	Port Deselected (TTL Inactive)
	X	V_{IL}	Port Deselected (TTL Inactive)
	$\geq V_{CC}$ - 0.2V	X	Port Deselected (CMOS Inactive)
	X	$\leq$0.2V	Port Deselected (CMOS Inactive)

3199 tbl 02

NOTES:
1. Chip Enable references are shown above with the actual $\overline{CE}_0$ and CE_1 levels, $\overline{CE}$ is a reference only.
2. Port "A" and "B" references are located where $\overline{CE}$ is used.
3. "H" = V_{IH} and "L" = V_{IL}.

Truth Table II – Non-Contention Read/Write Control

Inputs(1)						Outputs		
$\overline{CE}$(2)	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	X	X	X	X	H	High-Z	High-Z	Deselected: Power-Down
X	X	X	H	H	H	High-Z	High-Z	Both Bytes Deselected
L	L	X	L	H	H	DATAIN	High-Z	Write to Upper Byte Only
L	L	X	H	L	H	High-Z	DATAIN	Write to Lower Byte Only
L	L	X	L	L	H	DATAIN	DATAIN	Write to Both Bytes
L	H	L	L	H	H	DATAOUT	High-Z	Read Upper Byte Only
L	H	L	H	L	H	High-Z	DATAOUT	Read Lower Byte Only
L	H	L	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
X	X	H	X	X	X	High-Z	High-Z	Outputs Disabled

3199 tbl 03

NOTES:
1. A_{0L} — $A_{14L} \neq A_{0R}$ — A_{14R}.
2. Refer to Chip Enable Truth Table.

Truth Table III – Semaphore Read/Write Control

Inputs(1)						Outputs		
$\overline{CE}$(2)	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	H	L	X	X	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
X	H	L	H	H	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
H	↑	X	X	X	L	DATAIN	DATAIN	Write I/O0 into Semaphore Flag
X	↑	X	H	H	L	DATAIN	DATAIN	Write I/O0 into Semaphore Flag
L	X	X	L	X	L	——	——	Not Allowed
L	X	X	X	L	L	——	——	Not Allowed

3199 tbl 04

NOTES:
1. There are eight semaphore flags written to via I/O_0 and read from all the I/Os (I/O_0 –I/O_{15}). These eight semaphore flags are addressed by A_0-A_2.
2. Refer to Chip Enable Truth Table.

Absolute Maximum Ratings(1,3)

Symbol	Rating	Commercial & Industrial	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	50	mA

3199 tbl 05

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq$ 20mA for the period of $V_{TERM} \geq$ Vcc + 10%.

Maximum Operating Temperature and Supply Voltage(1)

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V $\pm$ 10%
Industrial	-40°C to +85°C	0V	5.0V $\pm$ 10%

3199 tbl 06

NOTE:
1. This is the parameter T_A. This is the "instant on" case temperature.

Capacitance(1)

(T_A = +25°C, f = 1.0mhz) TQFP ONLY

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	9	pF
$C_{OUT}^{(2)}$	Output Capacitance	V_{OUT} = 0V	10	pF

3199 tbl 08

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. C_{OUT} also references $C_{I/O}$.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	$6.0^{(2)}$	V
V_{IL}	Input Low Voltage	$-0.5^{(1)}$	—	0.8	V

3199 tbl 07

NOTES:
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7027S		7027L		Unit
			Min.	Max.	Min.	Max.	
$\lvert I_{LI}\rvert$	Input Leakage Current(1)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

3199 tbl 09

NOTE:
1. At Vcc $\leq$ 2.0V, input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1,6) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7027X15 Com'l Only Typ.(2)	7027X15 Com'l Only Max.	7027X20 Com'l & Ind Typ.(2)	7027X20 Com'l & Ind Max.	7027X25 Com'l & Ind Typ.(2)	7027X25 Com'l & Ind Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Disabled $\overline{SEM}$ = V_{IH} f = f_{MAX}(3)	COM'L	S	205	365	190	325	180	305	mA
				L	200	325	180	285	170	265	
			IND	S	—	—	—	—	170	345	
				L	—	—	180	335	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}(3)	COM'L	S	65	110	50	90	40	85	mA
				L	65	90	50	70	40	60	
			IND	S	—	—	—	—	40	100	
				L	—	—	50	85	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}(5) Active Port Outputs Disabled, f=f_{MAX}(3) $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L	S	130	245	115	215	105	200	mA
				L	130	215	115	185	105	170	
			IND	S	—	—	—	—	105	230	
				L	—	—	115	220	—	—	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0(4) $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$ - 0.2V	COM'L	S	1.0	15	1.0	15	1.0	15	mA
				L	0.2	5	0.2	5	0.2	5	
			IND	S	—	—	—	—	1.0	30	
				L	—	—	0.2	10	—	—	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{"A"} \leq$ 0.2V and $\overline{CE}_{"B"} \geq V_{CC}$ - 0.2V(5) $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Disabled f = f_{MAX}(3)	COM'L	S	120	220	110	190	100	170	mA
				L	120	190	110	160	100	145	
			IND	S	—	—	—	—	100	200	
				L	—	—	110	195	—	—	

3199 tbl 10a

Symbol	Parameter	Test Condition	Version		7027X35 Com'l Only Typ.(2)	7027X35 Com'l Only Max.	7027X55 Com'l Only Typ.(2)	7027X55 Com'l Only Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Disabled $\overline{SEM}$ = V_{IH} f = f_{MAX}(3)	COM'L	S	160	295	150	270	mA
				L	160	255	150	230	
			IND	S	—	—	—	—	
				L	—	—	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L	S	30	85	20	85	mA
				L	30	60	20	60	
			IND	S	—	—	—	—	
				L	—	—	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}(5) Active Port Outputs Disabled, f=f_{MAX}(3) $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L	S	95	185	85	165	mA
				L	95	155	85	135	
			IND	S	—	—	—	—	
				L	—	—	—	—	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0(4) $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$ - 0.2V	COM'L	S	1.0	15	1.0	15	mA
				L	0.2	5	0.2	5	
			IND	S	—	—	—	—	
				L	—	—	—	—	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{"A"} \leq$ 0.2V and $\overline{CE}_{"B"} \geq V_{CC}$ - 0.2V(5) $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Disabled f = f_{MAX}(3)	COM'L	S	90	160	80	135	mA
				L	90	135	80	110	
			IND	S	—	—	—	—	
				L	—	—	—	—	

3199 tbl 10b

NOTES:
1. 'X' in part numbers indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. I_{CCDC} = 120mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/ t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
6. Refer to Chip Enable Truth Table.

AC Test Conditions

dInput Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

3199 tbl 11

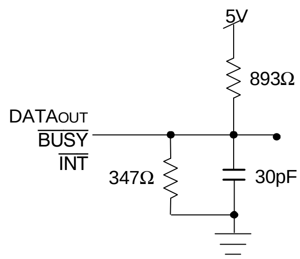


Figure 1. AC Output Test Load

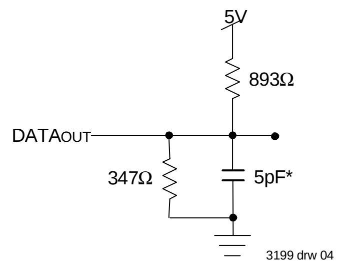


Figure 2. Output Test Load
(for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
***Including scope and jig.**

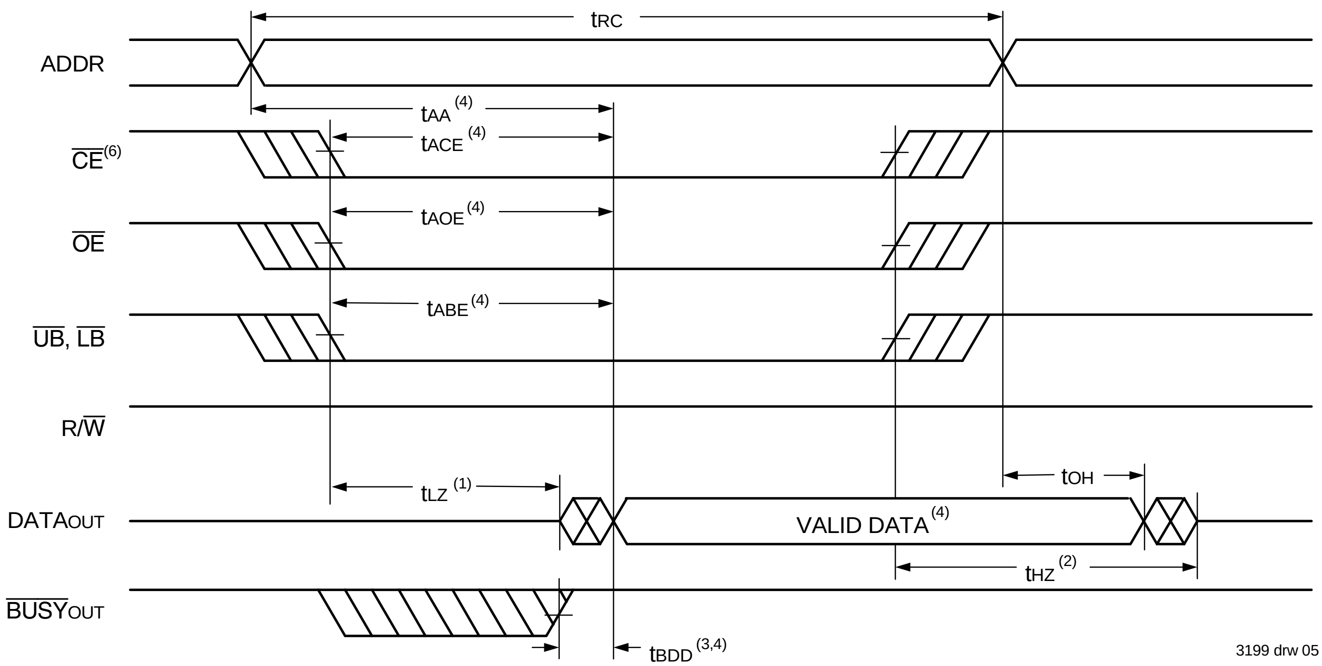
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Ranges(4)

Symbol	Parameter	7027X15 Com'l Only		7027X20 Com'l & Ind		7027X25 Com'l & Ind		7027X35 Com'l Only		7027X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	55	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	—	35	—	55	ns
t_{ACE}	Chip Enable Access Time(4)	—	15	—	20	—	25	—	35	—	55	ns
t_{AOE}	Output Enable Access Time	—	10	—	12	—	13	—	20	—	30	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time(1,2)	3	—	3	—	3	—	3	—	3	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	10	—	12	—	15	—	15	—	25	ns
t_{PU}	Chip Enable to Power Up Time(2,5)	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(2,5)	—	15	—	20	—	25	—	35	—	50	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	12	—	15	—	15	—	ns
t_{SAA}	Semaphore Address Access Time	—	15	—	20	—	25	—	35	—	55	ns

3199 tbl 12

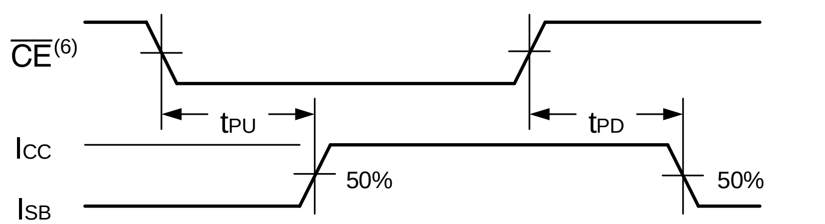
NOTES:.
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$= V_{IH} and $\overline{SEM}$ = V_{IL}.
4. 'X' in part numbers indicates power rating (S or L).
5. Refer to Chip Enable Truth Table.

Waveform of Read Cycles[5]



3199 drw 05

Timing of Power-Up Power-Down



3199 drw 06

NOTES:
1. Timing depends on which signal is asserted last, $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.
3. t_{BDD} delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last t_{AOE}, t_{ACE}, t_{AA} or t_{BDD}.
5. $\overline{SEM}$ = V_{IH}.
6. Refer to Chip Enable Truth Table.

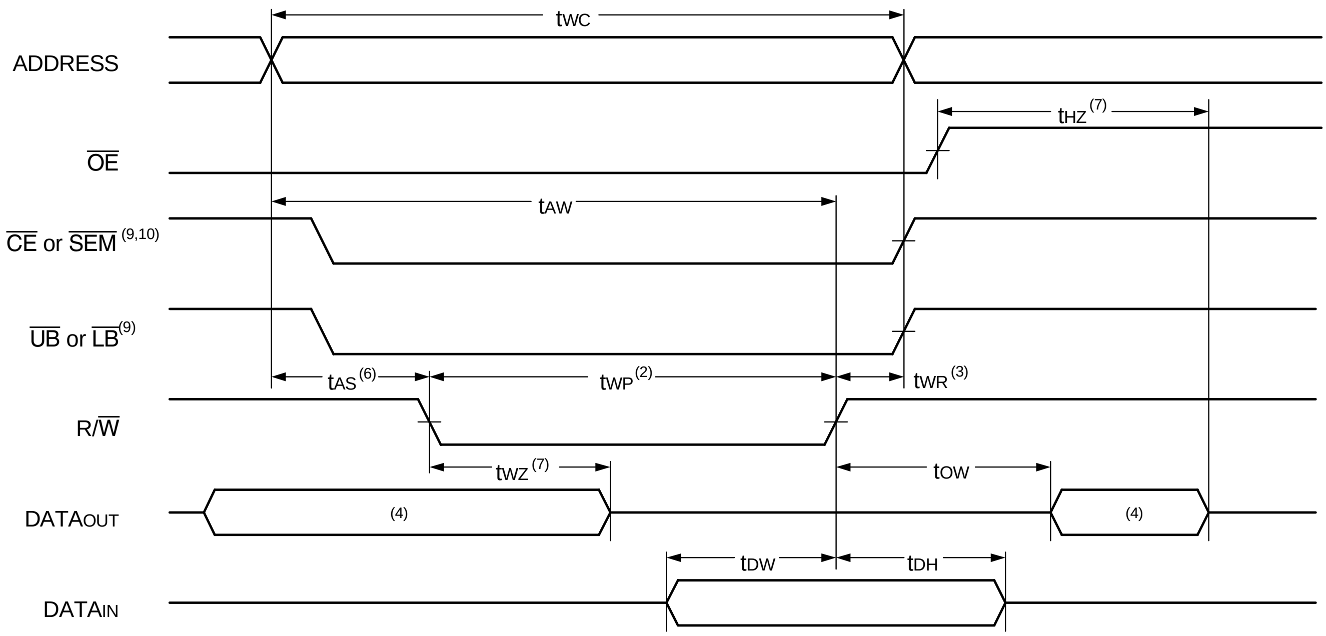
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage(5)

Symbol	Parameter	7027X15 Com'l Only		7027X20 Com'l & Ind		7027X25 Com'l & Ind		7027X35 Com'l Only		7027X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE												
t_{WC}	Write Cycle Time	15	—	20	—	25	—	35	—	55	—	ns
t_{EW}	Chip Enable to End-of-Write(3)	12	—	15	—	20	—	30	—	45	—	ns
t_{AW}	Address Valid to End-of-Write	12	—	15	—	20	—	30	—	45	—	ns
t_{AS}	Address Set-up Time(3)	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	20	—	25	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	10	—	15	—	15	—	15	—	30	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	10	—	12	—	15	—	15	—	25	ns
t_{DH}	Data Hold Time(5)	0	—	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z(1,2)	—	10	—	12	—	15	—	15	—	25	ns
t_{OW}	Output Active from End-of-Write(1,2,5)	0	—	0	—	0	—	0	—	0	—	ns
t_{SWRD}	SEM Flag Write to Read Time	5	—	5	—	5	—	5	—	5	—	ns
t_{SPS}	SEM Flag Contention Window	5	—	5	—	5	—	5	—	5	—	ns

3199 tbl 13

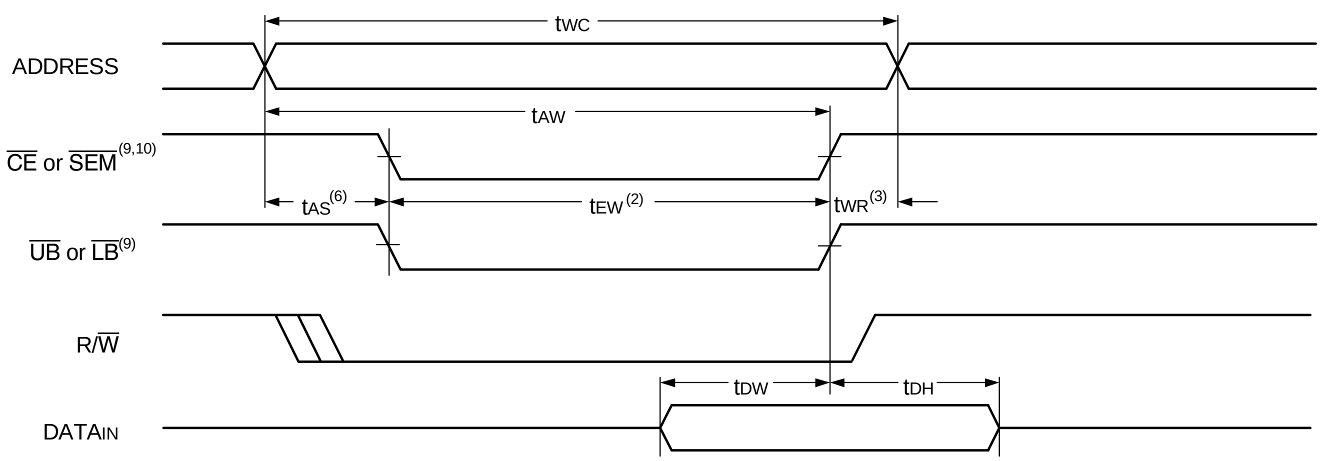
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM $\overline{CE}$= V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time. Refer to Chip Enable Truth Table.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. 'X' in part numbers indicates power rating (S or L).

Timing Waveform of Write Cycle No. 1, R/$\overline{W}$ Controlled Timing(1,5,8)



3199 drw 07

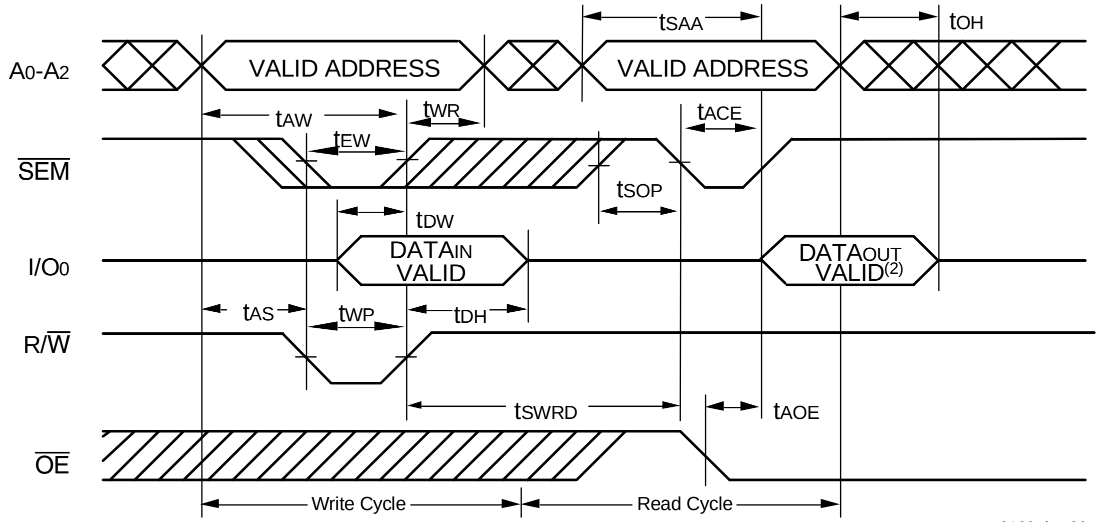
Timing Waveform of Write Cycle No. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ Controlled Timing(1,5)



3199 drw 08

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ and $\overline{LB}$ = V_{IH} during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE}$ = V_{IL} and a R/$\overline{W}$ = V_{IL} for memory array writing cycle.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ = V_{IL} transition occurs simultaneously with or after the R/$\overline{W}$ = V_{IL} transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ = V_{IL} during R/W controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ = V_{IH} during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
9. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. t_{EW} must be met for either condition.
10. Refer to Chip Enable Truth Table.

Timing Waveform of Semaphore Read after Write Timing, Either Side[1]

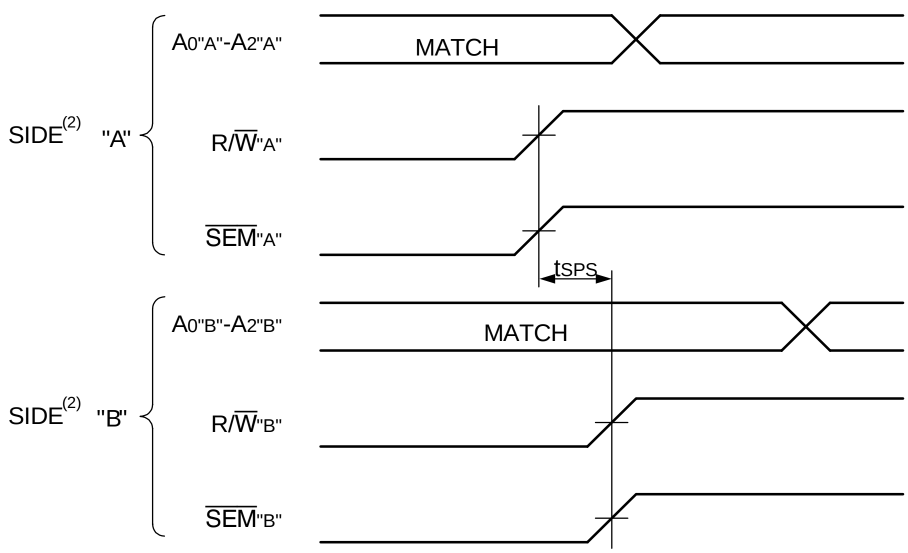


3199 drw 09

NOTES:

1. $\overline{CE}$ = VIH or $\overline{UB}$ and $\overline{LB}$ = VIH for the duration of the above timing (both write and read cycle), refer to Chip Enable Truth Table.
2. "DATAOUT VALID" represents all I/O's (I/O0-I/O15) equal to the semaphore value.

Timing Waveform of Semaphore Write Contention[1,3,4]



3199 drw 10

NOTES:

1. DOR = DOL = VIL, $\overline{CE}$R = $\overline{CE}$L = VIH, or both $\overline{UB}$ & $\overline{LB}$ = VIH (refer to Chip Enable Truth Table).
2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from R/$\overline{W}$"A" or $\overline{SEM}$"A" going HIGH to R/$\overline{W}$"B" or $\overline{SEM}$"B" going HIGH.
4. If tSPS is not satisfied, there is no guarantee which side will be granted the semaphore flag.

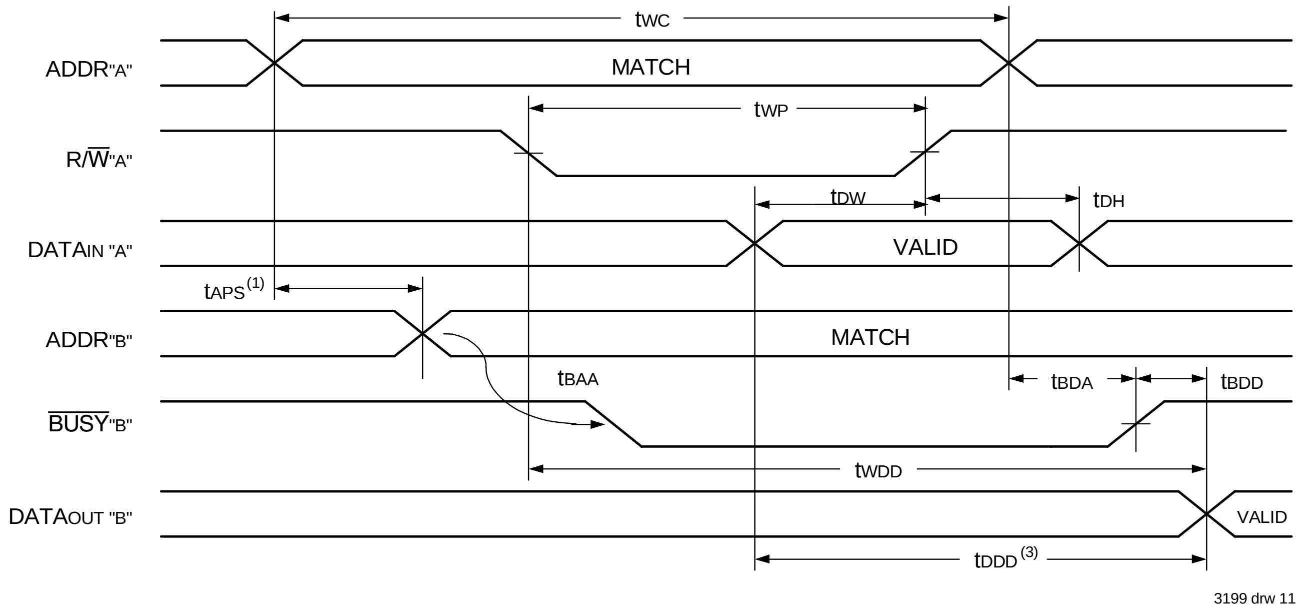
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(6)

Symbol	Parameter	7027X15 Com'l Only		7027X20 Com'l & Ind		7027X25 Com'l & Ind		7027X35 Com'l Only		7027X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{BUSY}$ TIMING (M/$\overline{S}$=V_{IH})												
t_{BAA}	$\overline{BUSY}$ Access Time from Address Match	—	15	—	20	—	20	—	20	—	45	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address Not Matched	—	15	—	20	—	20	—	20	—	40	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable Low	—	15	—	20	—	20	—	20	—	40	ns
t_{BDC}	$\overline{BUSY}$ Access Time from Chip Enable High	—	15	—	17	—	17	—	20	—	35	ns
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	5	—	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data(3)	—	15	—	20	—	25	—	35	—	55	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	12	—	15	—	17	—	25	—	25	—	ns
$\overline{BUSY}$ TIMING (M/$\overline{S}$=V_{IL})												
t_{WB}	$\overline{BUSY}$ Input to Write(4)	0	—	0	—	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	12	—	15	—	17	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING												
t_{WDD}	Write Pulse to Data Delay(1)	—	30	—	45	—	50	—	60	—	80	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	25	—	30	—	35	—	45	—	65	ns

3199 tbl 14

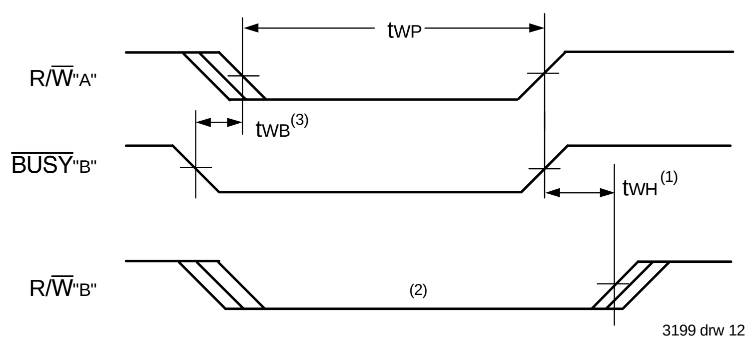
NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$ (M/$\overline{S}$ = V_{IH})".
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual), or $t_{DDD} - t_{DW}$ (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. 'X' in part numbers indicates power rating (S or L).

Timing Waveform of Write with Port-to-Port Read and $\overline{\text{BUSY}}$ (M/$\overline{\text{S}}$ = VIH)(2,4,5)



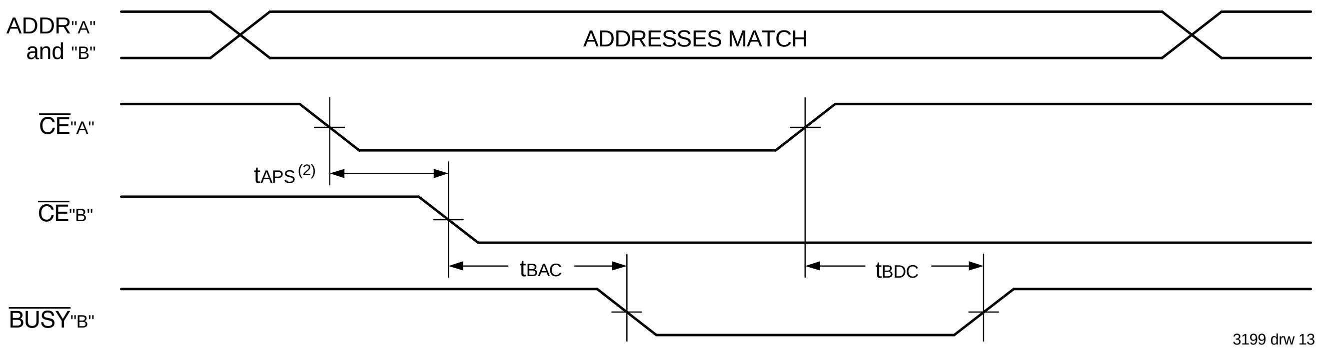
NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for M/$\overline{\text{S}}$ = VIL (slave).
2. $\overline{\text{CE}}$L = $\overline{\text{CE}}$R = VIL (refer to Chip Enable Truth Table).
3. $\overline{\text{OE}}$ = VIL for the reading port.
4. If M/$\overline{\text{S}}$ = VIL (slave), $\overline{\text{BUSY}}$ is an input. Then for this example $\overline{\text{BUSY}}$"A" = VIH and $\overline{\text{BUSY}}$"B" input is shown above.
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

Timing Waveform of Write with $\overline{\text{BUSY}}$ (M/$\overline{\text{S}}$ = VIL)

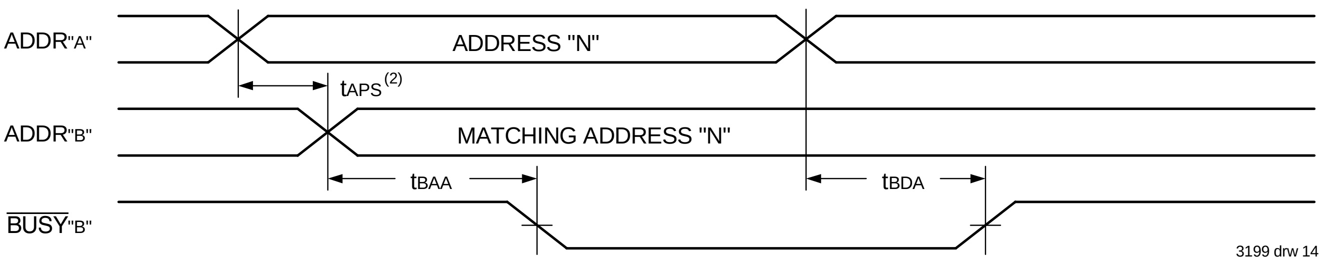


NOTES:
1. tWH must be met for both $\overline{\text{BUSY}}$ input (SLAVE) and output (MASTER).
2. $\overline{\text{BUSY}}$ is asserted on port "B" blocking R/$\overline{\text{W}}$"B", until $\overline{\text{BUSY}}$"B" goes HIGH.
3. tWB is only for the "Slave" version.

Waveform of $\overline{BUSY}$ Arbitration Controlled by $\overline{CE}$ Timing (M/$\overline{S}$ = VIH)(1,3)



Waveform of $\overline{BUSY}$ Arbitration Cycle Controlled by Address Match Timing (M/$\overline{S}$ = VIH)(1)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the $\overline{BUSY}$ signal will be asserted on one side or another but there is no guarantee on which side $\overline{BUSY}$ will be asserted.
3. Refer to Chip Enable Truth Table.

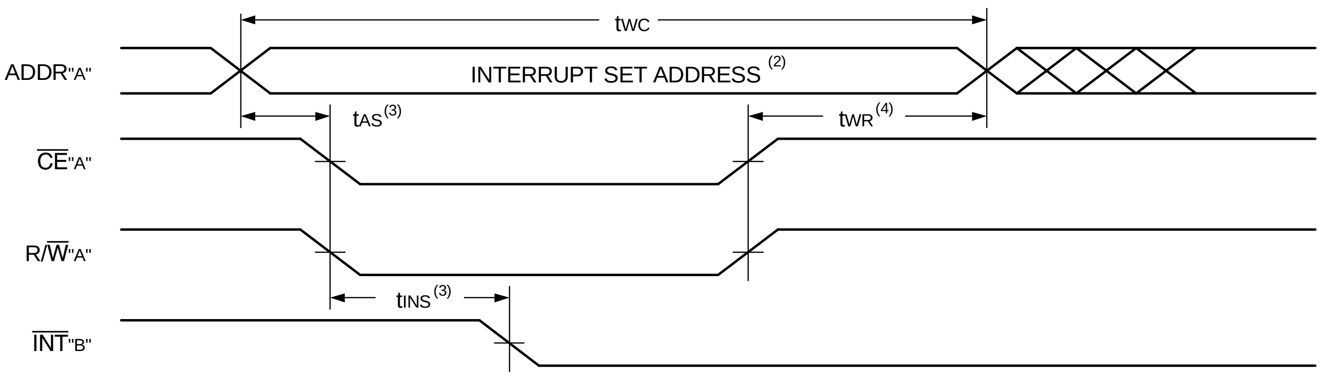
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1)

Symbol	Parameter	7027X15 Com'l Only		7027X20 Com'l & Ind		7027X25 Com'l & Ind		7027X35 Com'l Only		7027X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
INTERRUPT TIMING												
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	15	—	20	—	20	—	25	—	40	ns
tINR	Interrupt Reset Time	—	15	—	20	—	20	—	25	—	40	ns

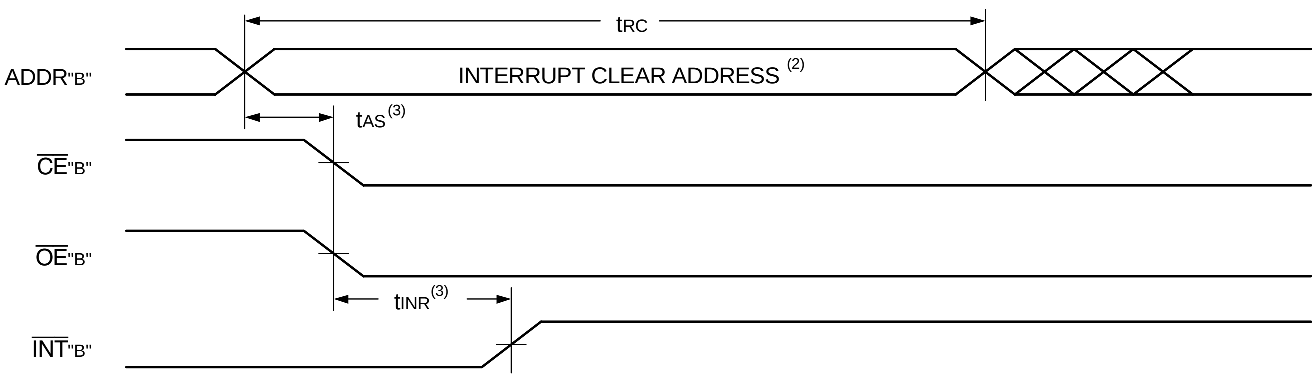
3199 tbl 15

NOTES:
1. 'X' in part numbers indicates power rating (S or L).

Waveform of Interrupt Timing(1,5)



3199 drw 15



3199 drw 16

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. See the Interrupt Truth Table IV.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.
5. Refer to Chip Enable Truth Table.

Truth Table IV — Interrupt Flag(1,4)

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{14L}-A_{0L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{14R}-A_{0R}	$\overline{INT}_R$	Function
L	L	X	7FFF	X	X	X	X	X	L(2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FFF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L(3)	L	L	X	7FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FFE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

3199 tbl 16

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = V_{IH}.
2. If $\overline{BUSY}_L$ = V_{IL}, then no change.
3. If $\overline{BUSY}_R$ = V_{IL}, then no change.
4. Refer to Chip Enable Truth Table.

Truth Table V — Address Bus Arbitration(4)

Inputs			Outputs		Function
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{14L} A_{0R}-A_{14R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

3199 tbl 17

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$ outputs on the IDT7027 are push-pull, not open drain outputs. On slaves the $\overline{BUSY}$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of the actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of the actual logic level on the pin.
4. Refer to Chip Enable Truth Table.

Truth Table VI — Example of Semaphore Procurement Sequence(1,2,3)

Functions	D_0 - D_{15} Left	D_0 - D_{15} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

3199 tbl 18

NOTES:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7027.
2. There are eight semaphore flags written to via I/O_0 and read from all the I/O's (I/O_0-I/O_{15}). These eight semaphores are addressed by A_0-A_2.
3. $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL}, to access the semaphores. Refer to the Semaphore Read/Write Control Truth Table.

Functional Description

The IDT7027 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7027 has an automatic power down feature controlled by $\overline{CE}_0$ and CE_1. The $\overline{CE}_0$ and CE_1 control the on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ = V_{IH}). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FFE (HEX), where a write is defined as $\overline{CE}_R$ = R/$\overline{W}_R$ = V_{IL} per Truth Table IV. The left port clears the interrupt through access of address location 7FFE when $\overline{CE}_L$ = $\overline{OE}_L$ = V_{IL}, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 7FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 7FFF. The message (16 bits) at 7FFE or 7FFF is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FFE and 7FFF are not used as mail-boxes by ignoring the interrupt, but as part of the random access memory. Refer to Truth Table IV for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The $\overline{\text{BUSY}}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a $\overline{\text{BUSY}}$ indication, the write signal is gated internally to prevent the write from proceeding.

The use of $\overline{\text{BUSY}}$ logic is not required or desirable for all applications. In some cases it may be useful to logically OR the $\overline{\text{BUSY}}$ outputs together and use any $\overline{\text{BUSY}}$ indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the $\overline{\text{BUSY}}$ logic can be disabled by placing the part in slave mode with the M/$\overline{\text{S}}$ pin. Once in slave mode the $\overline{\text{BUSY}}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{\text{BUSY}}$ pins HIGH. If desired, unintended write operations can be prevented to a port by tying the BUSY pin for that port LOW.

The $\overline{\text{BUSY}}$ outputs on the IDT7027 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the $\overline{\text{BUSY}}$ indication for the resulting array requires the use of an external AND gate.

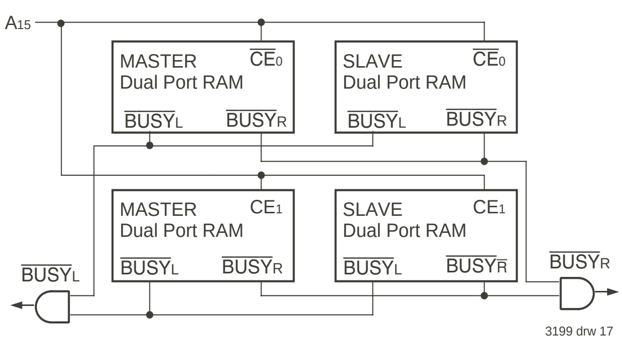


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7027 RAMs.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT7027 RAM array in width while using $\overline{\text{BUSY}}$ logic, one master part is used to decide which side of the RAM array will receive a $\overline{\text{BUSY}}$ indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the $\overline{\text{BUSY}}$ signal as a write inhibit signal. Thus on the IDT7027 RAM the $\overline{\text{BUSY}}$ pin is an output if the part is used as a Master (M/$\overline{\text{S}}$ pin = V_{IH}), and the $\overline{\text{BUSY}}$ pin is an input if the part used as a Slave (M/$\overline{\text{S}}$ pin = V_{IL}) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating $\overline{\text{BUSY}}$ on one side of the array and another master indicating $\overline{\text{BUSY}}$ on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The $\overline{\text{BUSY}}$ arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a $\overline{\text{BUSY}}$ flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{\text{W}}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

Semaphores

The IDT7027 is a fast Dual-Port 32K x 16 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port SRAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port SRAM or any other shared resource.

The Dual-Port SRAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port SRAM. These devices have an automatic power-down feature controlled by $\overline{\text{CE}}$ the Dual-Port SRAM enable, and $\overline{\text{SEM}}$, the semaphore enable. The $\overline{\text{CE}}$ and $\overline{\text{SEM}}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table II where $\overline{\text{CE}}$ and $\overline{\text{SEM}}$ = V_{IH}.

Systems which can best use the IDT7027 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7027's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7027 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port SRAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7027 in a separate memory space from the Dual-Port SRAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A_0 – A_2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a LOW level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Truth Table VI). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Truth Table VI). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the

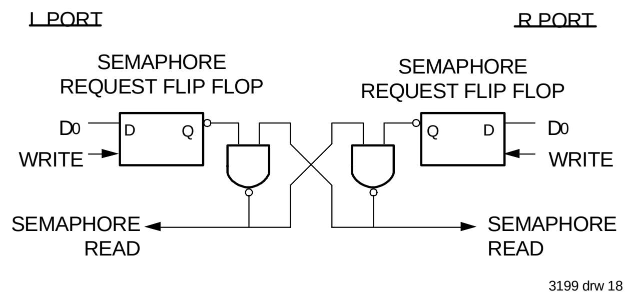


Figure 4. IDT7027 Semaphore Logic

semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Ordering Information

XXXXX A 999 A A A A

Device Type, Power, Speed, Package, Process/ Temperature Range

	Blank	Tube or Tray
	8	Tape and Reel
Process/ Temperature Range	Blank	Commercial (0°C to +70°C)
	I[(1)]	Industrial (-40°C to + 85°C)
	G[(2)]	Green
Package	PF	100-pin TQFP (PN100)
	G	108-pin PGA (G108)
Speed	15	Commercial Only
	20	Commercial & Industrial
	25	Commercial & Industrial
	35	Commercial Only
	55	Commercial Only
Power	S	Standard Power
	L	Low Power
Device Type	7027	512K (32K x 16) Dual-Port RAM

Speed in nanoseconds

3199 drw 19

NOTES:
1. Contact your local sales office for industrial temp range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office
   LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

Datasheet Document History

01/15/99:		Initiated datasheet document history
		Converted to new format
		Cosmetic and typographical corrections
		Pages 2 and 3 Added additional notes to pin configurations
05/19/99:		Pages 4 and 16 Fixed typographical errors
06/03/99:		Changed drawing format
	Page 1	Corrected DSC number
11/10/99:		Replaced IDT logo
05/22/00:	Page 5	Increased storage temperature parameter
		Clarified TA parameter
	Page 6	DC Electrical parameters–changed wording from "open" to "disabled"
		Changed ±200mV to 0mV in notes
07/23/04:	Page 2 & 3	Added date revision for pin configurations
	Page 5	Updated Capacitance table
	Page 6	Added 15ns commercial speed grade to the DC Electrical Characteristics
		Added 20ns Industrial temp for low power to DC Electrical Characteristics
		Removed military temp range for 25/35/55ns from DC Electrical Characteristics
	Page 7, 9, 12 & 14	Added 15ns commercial speed grade to AC Electrical Characteristics
		Added 20ns Industrial temp for low power to AC Electrical Characteristics for Read, Write, Busy and Interrupt
		Removed military temp range for 25/35/55ns from AC Electrical Characteristics
	Page 19	Added Commercial speed grade for 15ns and Industrial temp to 20ns in ordering information
	Page 1 & 19	Replaced old TM logo with new TM logo
01/29/09:	Page 19	Removed "IDT" from orderable part number

Datasheet Document History (con't)

08/04/15: Page 1 In Features: Added text: "Green parts available, see ordering information"
Page 2 Removed IDT in reference to fabrication
Page 2 & 5 Removed all of the military information
Page 2 & 3 Removed date from all of the pin configurations 100-pin TQFP & 108-pin PGA configurations
Page 2, 3 & 17 The package code PN100-1 and G108-1 changed to PN100 and G108 respectively to match standard package codes
Page 7 Added annotation for footnote 5 to Chip Enable & Chip Disable Parameters in the AC Elec Chars table
Page 17 Removed overbar for CE_1 in figure 3
Page 19 Added T&R and Green, removed military temp range and updated footnotes for ordering information

06/08/18: Product Discontinuation Notice - PDN# SP-17-02
Last time buy expires June 15, 2018

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
408-284-2794
DualPortHelp@idt.com