

## ISL43120, ISL43121, ISL43122

Low-Voltage, Single Supply, Dual SPST Analog Switches

FN6033  
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The Intersil [ISL43120](#), [ISL43121](#) and [ISL43122](#) devices are precision, bidirectional, dual analog SPST switches designed to operate from a single +2.7V to +12V supply. Targeted applications include battery powered equipment that benefit from the devices' low power consumption (5μW), low leakage currents (100pA max) and fast switching speeds ( $t_{ON} = 28ns$ ,  $t_{OFF} = 20ns$ ). Cell phones, for example, often face ASIC functionality limitations. The number of analog input or GPIO pins may be limited and digital geometries are not well suited to analog switch performance. This family of parts may be used to "mux-in" additional functionality while reducing ASIC design risk. Some of the smallest packages are available, alleviating board space limitations and making Intersil's newest line of low-voltage switches an ideal solution.

The ISL43120, ISL43121, ISL43122 are dual single-pole/single-throw (SPST) devices. The ISL43120 has two normally open (NO) switches; the ISL43121 has two normally closed (NC) switches; the ISL43122 has one NO and one NC switch and can be used as an SPDT.

**TABLE 1. FEATURES AT A GLANCE**

	ISL43120	ISL43121	ISL43122
SW 1/SW 2	NO/NO	NC/NC	NO/NC
3.3V $r_{ON}$	32Ω	32Ω	32Ω
3.3V $t_{ON}/t_{OFF}$	40ns/20ns	40ns/20ns	40ns/20ns
5V $r_{ON}$	19Ω	19Ω	19Ω
5V $t_{ON}/t_{OFF}$	28ns/20ns	28ns/20ns	28ns/20ns
12V $r_{ON}$	11Ω	11Ω	11Ω
12V $t_{ON}/t_{OFF}$	25ns/17ns	25ns/17ns	25ns/17ns
Packages	8 Ld SOT-23		

## Related Literature

- [TB363](#) "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- [AN557](#) "Recommended Test Procedures for Analog Switches"
- [TB401](#) "Using the ISL43120 SPST Switch in a Multi-Phase PWM Power Application"

## Features

- Fully specified at 1.2V, 5V, and 3.3V supplies for 10% tolerances
- ON-resistance ( $r_{ON}$ ) ..... 19Ω
- $r_{ON}$  matching between channels ..... <1Ω
- Low charge injection ..... 5pC (Max)
- Single supply operation ..... +2.7V to +12V
- Low power consumption ( $P_D$ ) ..... <5μW
- Low leakage current ..... 10nA
- Fast switching action
  - $t_{ON}$  ..... 28ns
  - $t_{OFF}$  ..... 20ns
- Guaranteed break-before-make (ISL43122 only)
- Minimum 2000V ESD protection per method 3015.7
- TTL, CMOS compatible
- Available in SOT-23 packaging
- Pb-free (RoHS Compliant)

## Applications

- Battery-powered, handheld and portable equipment
  - Cellular/mobile phones
  - Pagers
  - Laptops, notebooks, palmtops
- Communications systems
  - Radios, ADSL Modems
  - PBX, PABX
- Test and measurement equipment
  - Ultrasound
  - Computerized Tomography (CT) Scanner
  - Magnetic Resonance Image (MRI)
  - Position Emission Tomography (PET) Scanner
  - Electrocardiograph
- Heads-up displays
- Audio and video switching
- Various circuits
  - +3V/+5V DACs and ADCs
  - Sample and hold circuits
  - Digital filters
  - Operational amplifier gain switching networks
  - High frequency analog switching
  - High speed multiplexing
  - Integrator reset circuits

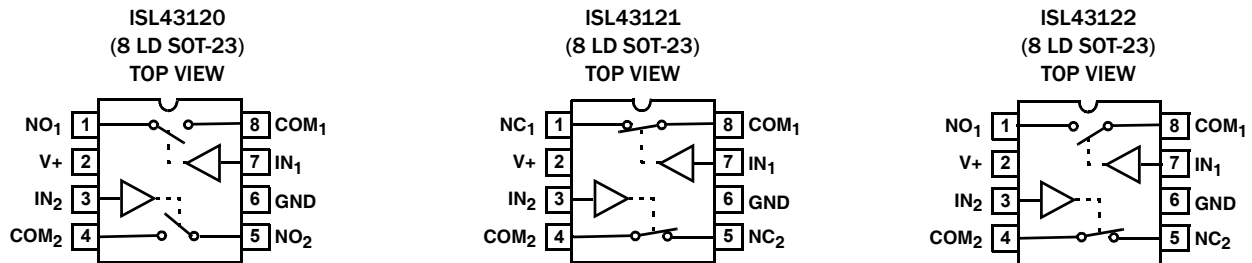
## Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL43120IHZ-T	120Z (Note 4)	-40 to +85	8 Ld SOT-23	P8.064
ISL43121IHZ-T (No longer available, recommended replacement: ISL43120IHZ-T)	121Z (Note 4)	-40 to +85	8 Ld SOT-23	P8.064
ISL43122IHZ-T (No longer available, recommended replacement: ISL43120IHZ-T)	122Z (Note 4)	-40 to +85	8 Ld SOT-23	P8.064

**NOTES:**

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for [ISL43120](#), [ISL43121](#), [ISL43122](#). For more information on MSL, please see tech brief [TB363](#).
4. The part marking is located on the bottom of the part.

## Pin Configurations (Note 5)



**NOTE:**

5. Switches Shown for Logic "0" Input.

## Truth Table

IN1	IN2	ISL43120		ISL43121		ISL43122	
		NO1	NO2	NC1	NC2	NO1	NC2
0	0	OFF	OFF	ON	ON	OFF	ON
0	1	OFF	ON	ON	OFF	OFF	OFF
1	0	ON	OFF	OFF	ON	ON	ON
1	1	ON	ON	OFF	OFF	ON	OFF

NOTE: Logic "0" ≤0.8V. Logic "1" ≥2.4V.

## Pin Descriptions

ISL43120 PIN NUMBER	ISL43121 PIN NUMBER	ISL43122 PIN NUMBER	PIN NAME	FUNCTION
2	2	2	V+	System Power Supply Input (+2.7V to +12V)
6	6	6	GND	Ground Connection
3, 7	3, 7	3, 7	INx	Digital Control Input
4, 8	4, 8	4, 8	COMx	Analog Switch Common Pin
1, 5		1	NOx	Analog Switch Normally Open Pin
	1, 6	5	NCx	Analog Switch Normally Closed Pin

### Absolute Maximum Ratings

V+ to GND .....	-0.3V to 15V
Input Voltages	
IN (Note 6) .....	-0.3V to ((V+) + 0.3V)
NO, NC (Note 6) .....	-0.3V to ((V+) + 0.3V)
Output Voltages	
COM (Note 6) .....	-0.3V to ((V+) + 0.3V)
Continuous Current (Any Terminal) .....	30mA
Peak Current NO, NC, or COM (Pulsed 1ms, 10% Duty Cycle, Max) .....	40mA
ESD Rating	
Human Body Model (Per MIL-STD-883 Method 3015) .....	>2kV

### Thermal Information

Thermal Resistance (Typical, Note 7)	$\theta_{JA}$ (°C/W)
8 Ld SOT-23 Package .....	215
Maximum Junction Temperature (Plastic Package) .....	+150°C
Maximum Storage Temperature Range .....	-65°C to +150°C
Pb-free Reflow Profile .....	see <a href="#">TB493</a>

### Recommended Operating Conditions

Temperature Range .....	-40°C to +85°C
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CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Signals on NC, NO, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
7.  $\theta_{JA}$  is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.

**Electrical Specifications - 5V Supply** V+ = +4.5V to +5.5V, GND = 0V, V<sub>INH</sub> = 2.4V, V<sub>INL</sub> = 0.8V (Note 8), unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 9, 10)	TYP	MAX (Notes 9, 10)	UNIT
<b>ANALOG SWITCH CHARACTERISTICS</b>						
Analog Signal Range, V <sub>ANALOG</sub>		Full	<b>0</b>	-	<b>V+</b>	V
ON-resistance, r <sub>ON</sub>	V+ = 4.5V, I <sub>COM</sub> = 1.0mA, V <sub>NO</sub> or V <sub>NC</sub> = 3.5V (see Figure 5)	25	-	19	30	Ω
		Full	-	23	<b>40</b>	Ω
r <sub>ON</sub> Matching Between Channels, Δr <sub>ON</sub>	V+ = 5V, I <sub>COM</sub> = 1.0mA, V <sub>NO</sub> or V <sub>NC</sub> = 3.5V	25	-	0.8	2	Ω
		Full	-	1	<b>4</b>	Ω
r <sub>ON</sub> Flatness, r <sub>FLAT(ON)</sub>	V+ = 5V, I <sub>COM</sub> = 1.0mA, V <sub>NO</sub> or V <sub>NC</sub> = 1V, 2V, 3V	Full	-	7	<b>8</b>	Ω
NO or NC OFF Leakage Current, I <sub>NO(OFF)</sub> or I <sub>NC(OFF)</sub>	V+ = 5.5V, V <sub>COM</sub> = 1V, 4.5V, V <sub>NO</sub> or V <sub>NC</sub> = 4.5V, 1V	25	-0.1	0.01	0.1	nA
		Full	<b>-5</b>	-	<b>5</b>	nA
COM OFF Leakage Current, I <sub>COM(OFF)</sub>	V+ = 5.5V, V <sub>COM</sub> = 4.5V, 1V, V <sub>NO</sub> or V <sub>NC</sub> = 1V, 4.5V	25	-0.1	-	0.1	nA
		Full	<b>-5</b>	-	<b>5</b>	nA
COM ON Leakage Current, I <sub>COM(ON)</sub>	V+ = 5.5V, V <sub>COM</sub> = 1V, 4.5V, or V <sub>NO</sub> or V <sub>NC</sub> = 1V, 4.5V, or Floating	25	-0.2	-	0.2	nA
		Full	<b>-10</b>	-	<b>10</b>	nA
<b>DYNAMIC CHARACTERISTICS</b>						
Turn-ON Time, t <sub>ON</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 3V, R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 35pF, V <sub>IN</sub> = 0V to 3V (see Figure 1, Note 11)	25	-	28	75	ns
		Full	-	40	<b>150</b>	ns
Turn-OFF Time, t <sub>OFF</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 3V, R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 35pF, V <sub>IN</sub> = 0V to 3V (see Figure 1, Note 11)	25	-	20	50	ns
		Full	-	30	<b>100</b>	ns
Break-Before-Make Time Delay (ISL43122 only), t <sub>D</sub>	R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, V <sub>NO</sub> = V <sub>NC</sub> = 3V, V <sub>IN</sub> = 0V to 3V (see Figure 3, Note 11)	Full	<b>3</b>	10	-	ns
Charge Injection, Q	C <sub>L</sub> = 1.0nF, V <sub>G</sub> = 0V, R <sub>G</sub> = 0Ω (see Figure 2, Note 11)	25	-	3	5	pC
OFF Isolation	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, f = 1MHz (see Figure 4)	25	-	76	-	dB
Crosstalk (Channel-to-Channel)	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, f = 1MHz (see Figure 6)	25	-	-105	-	dB
Power Supply Rejection Ratio	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, f = 1MHz	25	-	60	-	dB
NO or NC OFF Capacitance, C <sub>OFF</sub>	f = 1MHz, V <sub>NO</sub> or V <sub>NC</sub> = V <sub>COM</sub> = 0V (see Figure 7)	25	-	8	-	pF
COM OFF Capacitance, C <sub>COM(OFF)</sub>	f = 1MHz, V <sub>NO</sub> or V <sub>NC</sub> = V <sub>COM</sub> = 0V (see Figure 7)	25	-	8	-	pF
COM ON Capacitance, C <sub>COM(ON)</sub>	f = 1MHz, V <sub>NO</sub> or V <sub>NC</sub> = V <sub>COM</sub> = 0V (see Figure 7)	25	-	21	-	pF

**Electrical Specifications - 5V Supply**  $V_+ = +4.5V$  to  $+5.5V$ ,  $GND = 0V$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 8), unless otherwise specified. **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ .** (Continued)

PARAMETER	TEST CONDITIONS	TEMP ( $^\circ C$ )	MIN (Notes 9, 10)	TYP	MAX (Notes 9, 10)	UNIT
<b>POWER SUPPLY CHARACTERISTICS</b>						
Power Supply Range		Full	<b>2.7</b>	-	<b>12</b>	V
Positive Supply Current, $I_+$	$V_+ = 5.5V$ , $V_{IN} = 0V$ or $V_+$ , all channels on or off	Full	<b>-1</b>	0.0001	<b>1</b>	$\mu A$
<b>DIGITAL INPUT CHARACTERISTICS</b>						
Input Voltage Low, $V_{INL}$		Full	-	-	<b>0.8</b>	V
Input Voltage High, $V_{INH}$		Full	<b>2.4</b>	-	-	V
Input Current, $I_{INH}$ , $I_{INL}$	$V_+ = 5.5V$ , $V_{IN} = 0V$ or $V_+$	Full	<b>-1</b>	-	<b>1</b>	$\mu A$

**Electrical Specifications - 3.3V Supply**  $V_+ = +3.0V$  to  $+3.6V$ ,  $GND = 0V$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 8), unless otherwise specified. **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ .**

PARAMETER	TEST CONDITIONS	TEMP ( $^\circ C$ )	MIN (Notes 9, 10)	TYP	MAX (Notes 9, 10)	UNIT
<b>ANALOG SWITCH CHARACTERISTICS</b>						
Analog Signal Range, $V_{ANALOG}$		Full	<b>0</b>	-	<b><math>V_+</math></b>	V
ON-resistance, $r_{ON}$	$V_+ = 3V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = 1.5V$	25	-	32	<b>50</b>	$\Omega$
		Full	-	40	<b>60</b>	$\Omega$
$r_{ON}$ Matching Between Channels, $\Delta r_{ON}$	$V_+ = 3.3V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = 1.5V$	25	-	0.8	<b>2</b>	$\Omega$
		Full	-	1	<b>4</b>	$\Omega$
$r_{ON}$ Flatness, $r_{FLAT(ON)}$	$V_+ = 3.3V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = 0.5V, 1V, 1.5V$	25	-	6	<b>8</b>	$\Omega$
		Full	-	7	<b>12</b>	$\Omega$
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	$V_+ = 3.6V$ , $V_{COM} = 1V, 3V$ , $V_{NO}$ or $V_{NC} = 3V, 1V$	25	-0.1	0.01	<b>0.1</b>	nA
		Full	<b>-5</b>	-	<b>5</b>	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	$V_+ = 3.6V$ , $V_{COM} = 3V, 1V$ , $V_{NO}$ or $V_{NC} = 1V, 3V$	25	-0.1	0.01	<b>0.1</b>	nA
		Full	<b>-5</b>	-	<b>5</b>	nA
COM ON Leakage Current, $I_{COM(ON)}$	$V_+ = 3.6V$ , $V_{COM} = 1V, 3V$ , or $V_{NO}$ or $V_{NC} = 1V, 3V$ , or floating	25	-0.2	-	<b>0.2</b>	nA
		Full	<b>-10</b>	-	<b>10</b>	nA
<b>DYNAMIC CHARACTERISTICS</b>						
Turn-ON Time, $t_{ON}$	$V_{NO}$ or $V_{NC} = 1.5V$ , $R_L = 1k\Omega$ , $C_L = 35pF$ , $V_{IN} = 0V$ to $3V$ (Note 11)	25	-	40	<b>120</b>	ns
		Full	-	60	<b>200</b>	ns
Turn-OFF Time, $t_{OFF}$	$V_{NO}$ or $V_{NC} = 1.5V$ , $R_L = 1k\Omega$ , $C_L = 35pF$ , $V_{IN} = 0V$ to $3V$ (Note 11)	25	-	20	<b>50</b>	ns
		Full	-	30	<b>120</b>	ns
Break-before-make Time Delay (ISL43122 only), $t_D$	$R_L = 300\Omega$ , $C_L = 35pF$ , $V_{NO}$ or $V_{NC} = 1.5V$ , $V_{IN} = 0V$ to $3V$ (Note 11)	Full	<b>3</b>	20	-	ns
Charge Injection, $Q$	$C_L = 1.0nF$ , $V_G = 0V$ , $R_G = 0\Omega$ (Note 11)	25	-	1	<b>5</b>	pC
OFF-isolation	$R_L = 50\Omega$ , $C_L = 5pF$ , $f = 1MHz$	25	-	76	-	dB
Crosstalk (Channel-to-channel)	$R_L = 50\Omega$ , $C_L = 5pF$ , $f = 1MHz$	25	-	-105	-	dB
Power Supply Rejection Ratio	$R_L = 50\Omega$ , $C_L = 5pF$ , $f = 1MHz$	25	-	56	-	dB
NO or NC OFF Capacitance, $C_{OFF}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$	25	-	8	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$	25	-	8	-	pF
COM ON Capacitance, $C_{COM(ON)}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$ (See Figure 7)	25	-	21	-	pF
<b>POWER SUPPLY CHARACTERISTICS</b>						
Positive Supply Current, $I_+$	$V_+ = 3.6V$ , $V_{IN} = 0V$ or $V_+$ , all channels on or off	Full	<b>-1</b>	-	<b>1</b>	$\mu A$

**Electrical Specifications - 3.3V Supply**  $V_+ = +3.0V$  to  $+3.6V$ ,  $GND = 0V$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 8), unless otherwise specified. **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ .** (Continued)

PARAMETER	TEST CONDITIONS	TEMP ( $^\circ C$ )	MIN (Notes 9, 10)	TYP	MAX (Notes 9, 10)	UNIT
<b>DIGITAL INPUT CHARACTERISTICS</b>						
Input Voltage Low, $V_{INL}$		Full	-	-	<b>0.8</b>	V
Input Voltage High, $V_{INH}$		Full	<b>2.4</b>	-	-	V
Input Current, $I_{INH}$ , $I_{INL}$	$V_+ = 3.6V$ , $V_{IN} = 0V$ or $V_+$	Full	<b>-1</b>	-	<b>1</b>	$\mu A$

**Electrical Specifications - 12V Supply**  $V_+ = +10.8V$  to  $+13V$ ,  $GND = 0V$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 8), unless otherwise specified. **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ .**

PARAMETER	TEST CONDITIONS	TEMP ( $^\circ C$ )	MIN (Notes 9, 10)	TYP	MAX (Notes 9, 10)	UNIT
<b>ANALOG SWITCH CHARACTERISTICS</b>						
Analog Signal Range, $V_{ANALOG}$		Full	<b>0</b>	-	<b>V+</b>	V
ON-resistance, $r_{ON}$	$V_+ = 10.8V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = 10V$	25	-	<b>11</b>	<b>20</b>	$\Omega$
		Full	-	<b>15</b>	<b>25</b>	$\Omega$
$r_{ON}$ Matching Between Channels, $\Delta r_{ON}$	$V_+ = 12V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = 10V$	25	-	<b>0.8</b>	<b>2</b>	$\Omega$
		Full	-	<b>1</b>	<b>4</b>	$\Omega$
$r_{ON}$ Flatness, $r_{FLAT}(ON)$	$V_+ = 12V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = 3V, 6V, 9V$	25	-	<b>1</b>	<b>4</b>	$\Omega$
		Full	-	-	<b>6</b>	$\Omega$
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	$V_+ = 13V$ , $V_{COM} = 1V, 12V$ , $V_{NO}$ or $V_{NC} = 12V, 1V$	25	<b>-0.1</b>	<b>0.01</b>	<b>0.1</b>	nA
		Full	<b>-5</b>	-	<b>5</b>	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	$V_+ = 13V$ , $V_{COM} = 12V, 1V$ , $V_{NO}$ or $V_{NC} = 1V, 12V$	25	<b>-0.1</b>	<b>0.01</b>	<b>0.1</b>	nA
		Full	<b>-5</b>	-	<b>5</b>	nA
COM ON Leakage Current, $I_{COM(ON)}$	$V_+ = 13V$ , $V_{COM} = 1V, 12V$ , or $V_{NO}$ or $V_{NC} = 1V, 12V$ , or floating	25	<b>-0.2</b>	-	<b>0.2</b>	nA
		Full	<b>-10</b>	-	<b>10</b>	nA
<b>DYNAMIC CHARACTERISTICS</b>						
Turn-ON Time, $t_{ON}$	$V_{NO}$ or $V_{NC} = 10V$ , $R_L = 1k\Omega$ , $C_L = 35pF$ , $V_{IN} = 0V$ to $4V$ (Note 11)	25	-	<b>25</b>	<b>35</b>	ns
		Full	-	<b>35</b>	<b>55</b>	ns
Turn-OFF Time, $t_{OFF}$	$V_{NO}$ or $V_{NC} = 10V$ , $R_L = 1k\Omega$ , $C_L = 35pF$ , $V_{IN} = 0V$ to $4V$ (Note 11)	25	-	<b>17</b>	<b>30</b>	ns
		Full	-	<b>26</b>	<b>50</b>	ns
Break-before-make Time Delay (ISL43122 only), $t_D$	$R_L = 300\Omega$ , $C_L = 35pF$ , $V_{NO}$ or $V_{NC} = 10V$ , $V_{IN} = 0$ to $4V$	Full	<b>0</b>	<b>2</b>		ns
Charge Injection, $Q$	$C_L = 1.0nF$ , $V_G = 0V$ , $R_G = 0\Omega$ (Note 11)	25	-	<b>5</b>	<b>15</b>	pC
OFF-isolation	$R_L = 50\Omega$ , $C_L = 5pF$ , $f = 1MHz$	25	-	<b>76</b>	-	dB
Crosstalk (Channel-to-channel)	$R_L = 50\Omega$ , $C_L = 5pF$ , $f = 1MHz$	25	-	<b>-105</b>	-	dB
Power Supply Rejection Ratio	$R_L = 50\Omega$ , $C_L = 5pF$ , $f = 1MHz$	25	-	<b>63</b>	-	dB
NO or NC OFF Capacitance, $C_{OFF}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$	25	-	<b>8</b>	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$	25	-	<b>8</b>	-	pF
COM ON Capacitance, $C_{COM(ON)}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$ (see Figure 7)	25	-	<b>21</b>	-	pF
<b>POWER SUPPLY CHARACTERISTICS</b>						
Positive Supply Current, $I_+$	$V_+ = 13V$ , $V_{IN} = 0V$ or $V_+$ , all channels on or off	Full	<b>-1</b>	-	<b>1</b>	$\mu A$

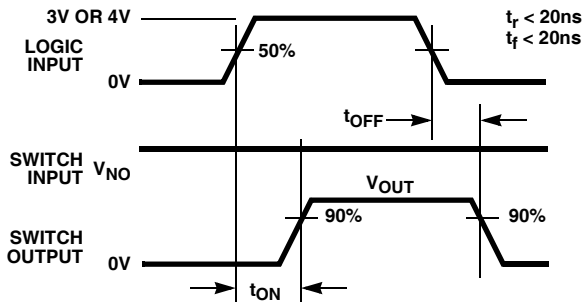
**Electrical Specifications - 12V Supply**  $V_+ = +10.8V$  to  $+13V$ ,  $GND = 0V$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 8), unless otherwise specified. **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ .** (Continued)

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 9, 10)	TYP	MAX (Notes 9, 10)	UNIT
<b>DIGITAL INPUT CHARACTERISTICS</b>						
Input Voltage Low, $V_{INL}$		Full	-	-	<b>0.8</b>	V
Input Voltage High, $V_{INH}$		Full	<b>4</b>	-	-	V
Input Current, $I_{INH}$ , $I_{INL}$	$V_+ = 13V$ , $V_{IN} = 0V$ or $V_+$	Full	<b>-1</b>	-	<b>1</b>	$\mu A$

NOTES:

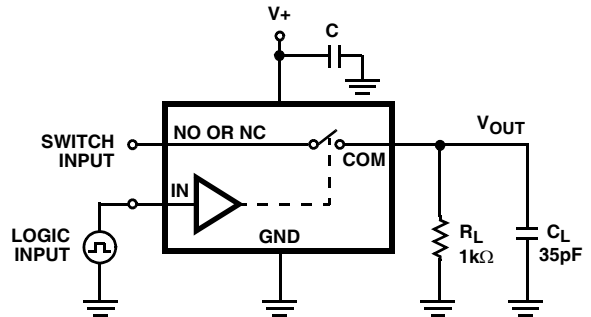
- 8.  $V_{IN}$  = input voltage to perform proper function.
- 9. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- 10. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
- 11. Limits established by characterization and are not production tested.

**Test Circuits and Waveforms**



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches.  $C_L$  includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO \text{ OR } NC)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

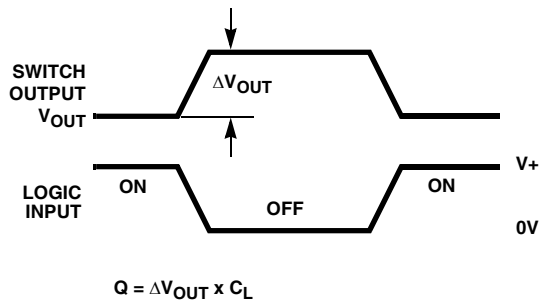


FIGURE 2A. MEASUREMENT POINTS

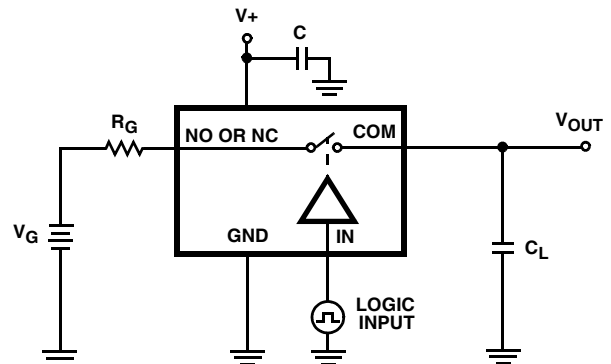


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

## Test Circuits and Waveforms (Continued)

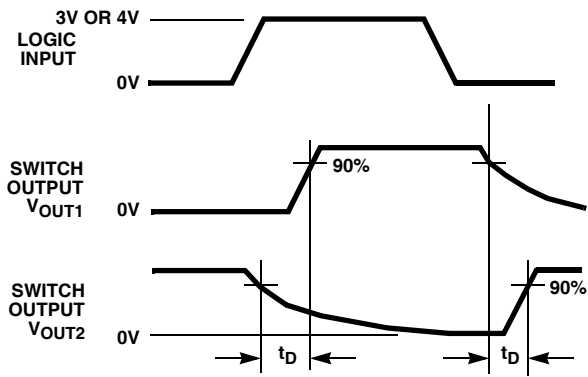
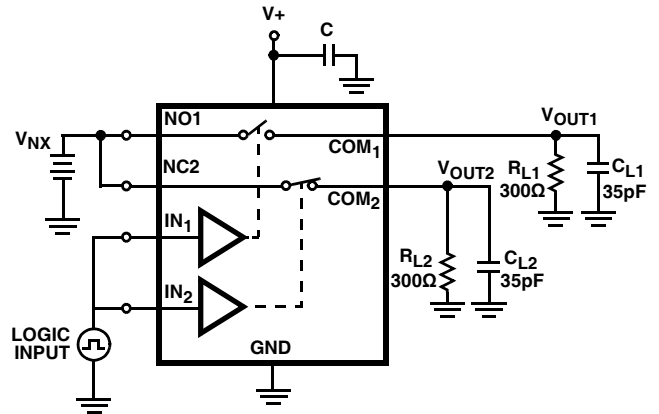


FIGURE 3A. MEASUREMENT POINTS (ISL43122 ONLY)



$C_L$  includes fixture and stray capacitance.

FIGURE 3B. TEST CIRCUIT (ISL43122 ONLY)

FIGURE 3. BREAK-BEFORE-MAKE TIME

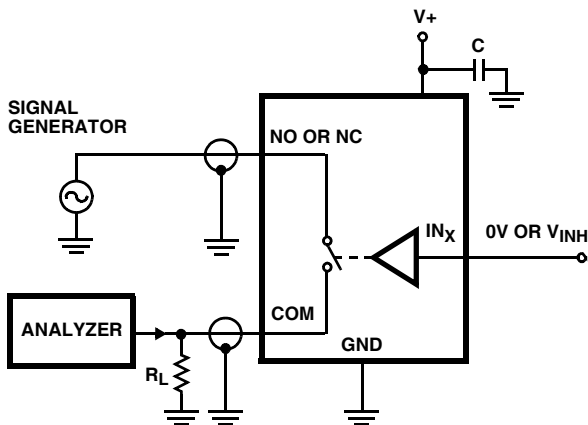


FIGURE 4. OFF-ISOLATION TEST CIRCUIT

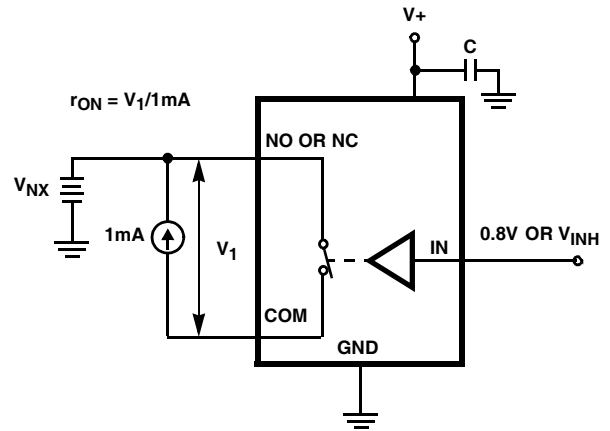


FIGURE 5.  $r_{ON}$  TEST CIRCUIT

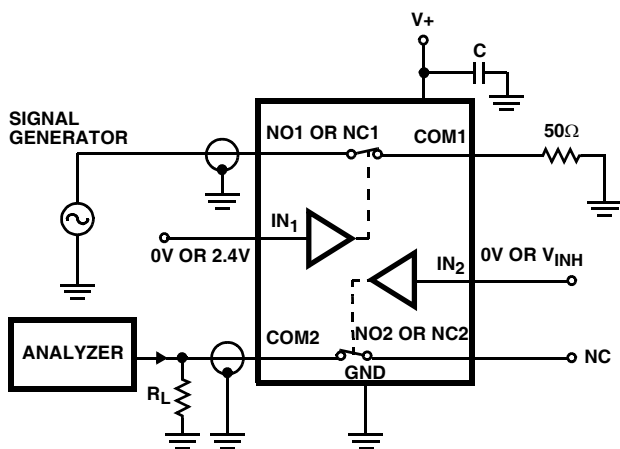


FIGURE 6. CROSSTALK TEST CIRCUIT

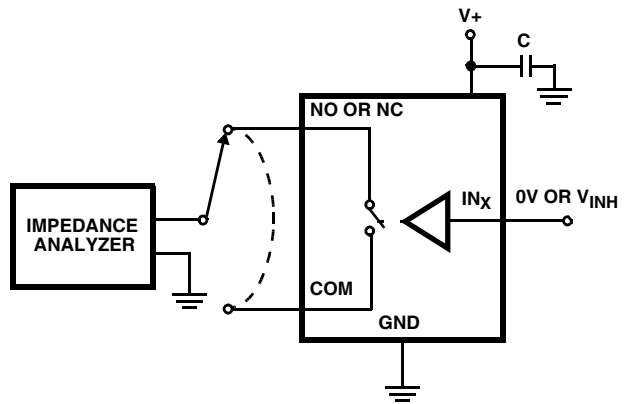


FIGURE 7. CAPACITANCE TEST CIRCUIT

## Detailed Description

The ISL43120, ISL43121, ISL43122 bidirectional dual SPST analog switches offer precise switching capability from a single 2.7V to 12V supply with low ON-resistance (19 $\Omega$ ) and high speed operation ( $t_{ON} = 28\text{ns}$ ,  $t_{OFF} = 20\text{ns}$ ). The devices are especially well suited to portable battery-powered equipment thanks to the low operating supply voltage (2.7V), low power consumption (5 $\mu\text{W}$ ), low leakage currents (100pA max), and the tiny SOT-23 packaging. High frequency applications also benefit from the wide bandwidth, and the very high off-isolation and crosstalk rejection.

### Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents, which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and GND (see [Figure 8](#)). To prevent forward biasing these diodes, V+ must be applied before any input signals, and input signal voltages must remain between V+ and GND. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1k $\Omega$  resistor in series with the input (see [Figure 8](#)). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

Adding a series resistor to the switch input defeats the purpose of using a low  $r_{ON}$  switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see [Figure 8](#)). These additional diodes limit the analog signal from 1V below V+ to 1V above GND. The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

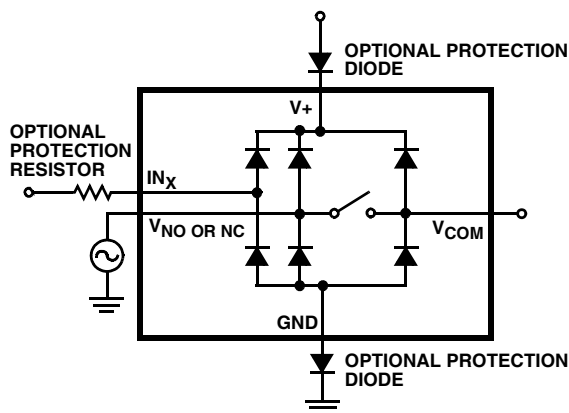


FIGURE 8. OVERVOLTAGE PROTECTION

### Power-Supply Considerations

The ISL43120, ISL43121, ISL43122 construction is typical of most CMOS analog switches, except that they have only two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 13V maximum supply voltage, the ISL43120, ISL43121, ISL43122 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 2.7V. It is important to note that the input signal range, switching times, and ON-resistance degrade at lower supply voltages. Refer to the “Electrical Specifications” tables starting on [page 3](#) and “Typical Performance Curves” (starting on [page 9](#)) for details.

V+ and GND also power the internal logic and level shifter. The level shifter convert the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

### Logic-level Thresholds

This switch family is TTL compatible (0.8V and 2.4V) over a supply range of 3V to 11V (see [Figure 15](#)). At 12V the  $V_{IH}$  level is about 2.5V. This is still below the TTL guaranteed high output minimum level of 2.8V, but noise margin is reduced. For best results with a 12V supply, use a logic family the provides a  $V_{OH}$  greater than 3V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

### High-frequency Performance

In 50 $\Omega$  systems, signal response is reasonably flat even past 300MHz (see [Figure 16](#)). Figure 16 also illustrates that the frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch’s input to its output. Off-isolation is the resistance to this feedthrough, while crosstalk indicates the amount of feedthrough from one switch to another. [Figure 17](#) details the high off-isolation and crosstalk rejection provided by this family. At 10MHz, off isolation is about 50dB in 50 $\Omega$  systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease off isolation and crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.



## Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the

signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

## Typical Performance Curves $T_A = +25^\circ\text{C}$ , unless otherwise specified.

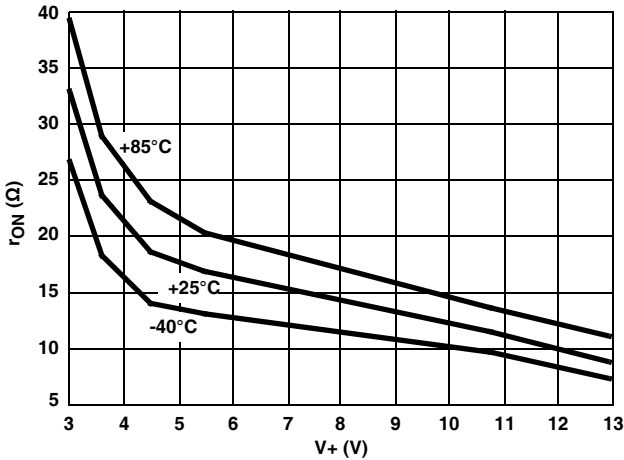


FIGURE 9. ON-RESISTANCE vs SUPPLY VOLTAGE

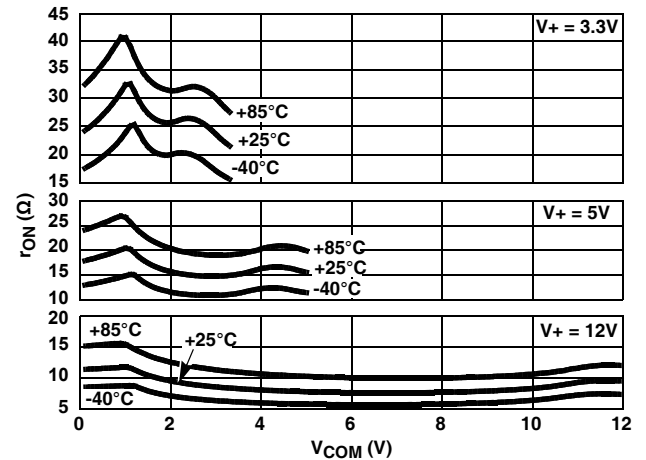


FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE

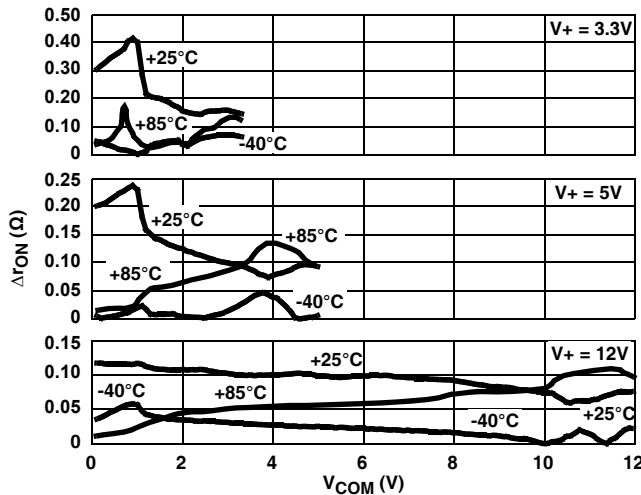


FIGURE 11.  $r_{ON}$  MATCH vs SWITCH VOLTAGE

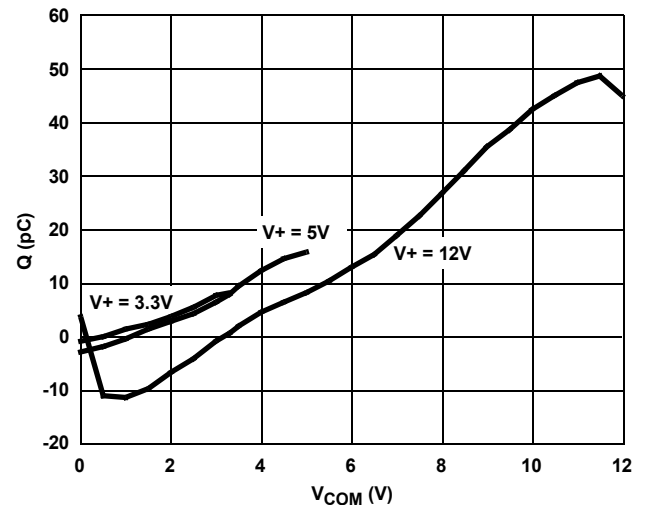


FIGURE 12. CHARGE INJECTION vs SWITCH VOLTAGE

**Typical Performance Curves**  $T_A = +25^\circ\text{C}$ , unless otherwise specified. (Continued)

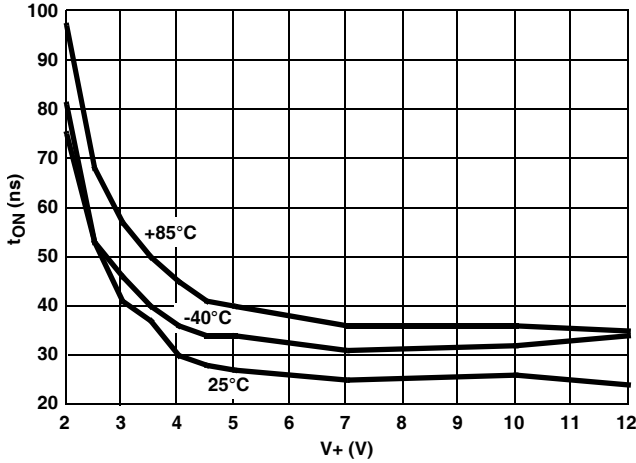


FIGURE 13. TURN-ON TIME vs SUPPLY VOLTAGE

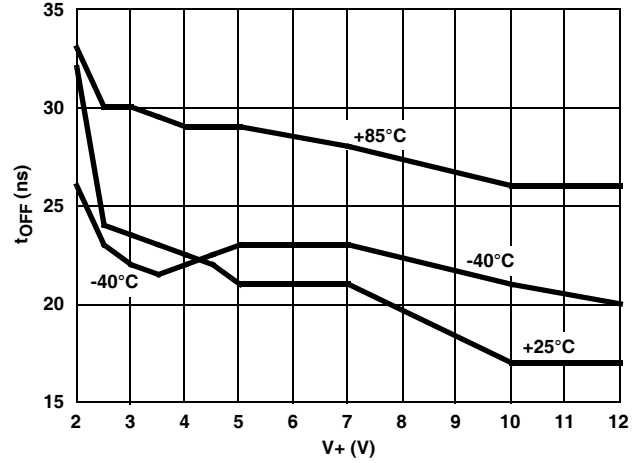


FIGURE 14. TURN-OFF TIME vs SUPPLY VOLTAGE

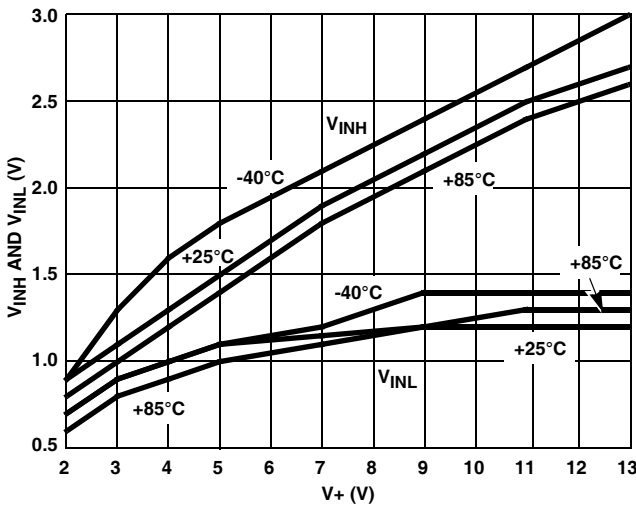


FIGURE 15. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

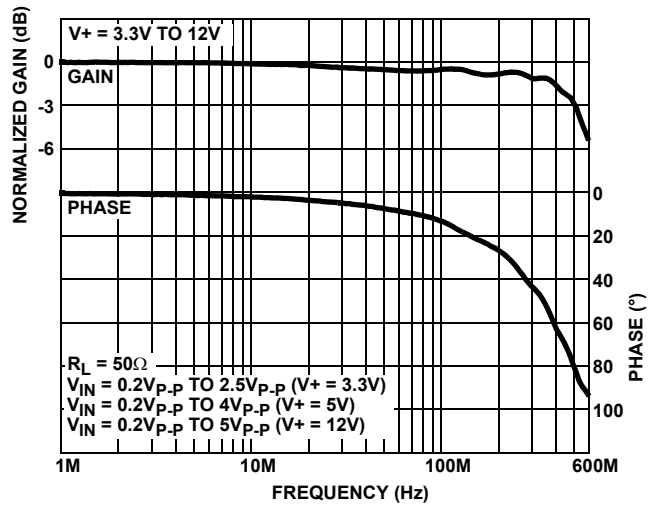


FIGURE 16. FREQUENCY RESPONSE

**Typical Performance Curves**  $T_A = +25^\circ\text{C}$ , unless otherwise specified. **(Continued)**

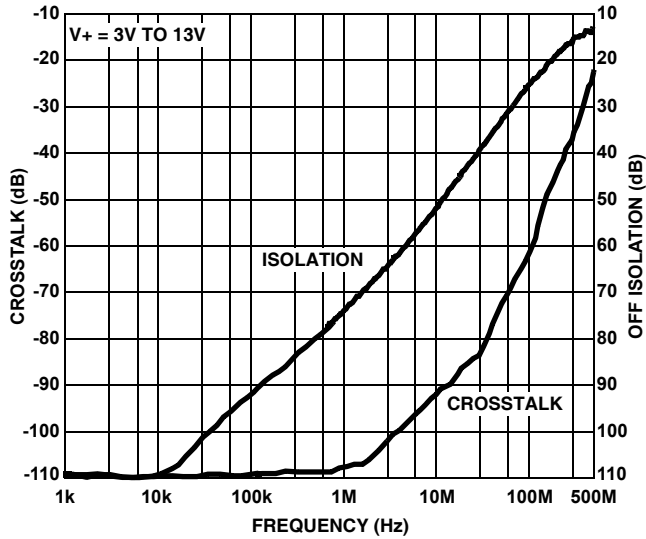


FIGURE 17. CROSSTALK AND OFF-ISOLATION

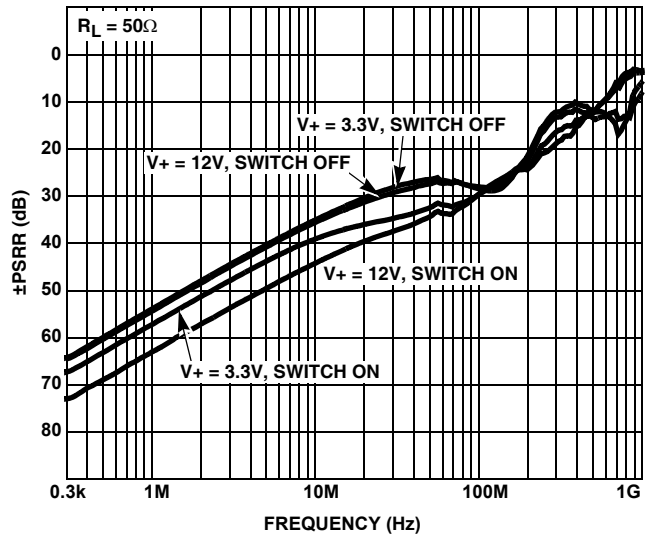


FIGURE 18.  $\pm$ PSRR vs FREQUENCY

**Die Characteristics**

**SUBSTRATE POTENTIAL (POWERED UP):**

GND

**TRANSISTOR COUNT:**

- ISL43120: 66
- ISL43121: 66
- ISL43122: 66

**PROCESS:**

Si Gate CMOS

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 17, 2015	FN6033.7	Updated Ordering Information table on page 2.
May 28, 2015	FN6033.6	Added Rev History beginning with Rev 6. Updated entire datasheet applying Intersil's new standards. Updated Ordering information by removing obsolete parts, adding MSL and part marking notes.

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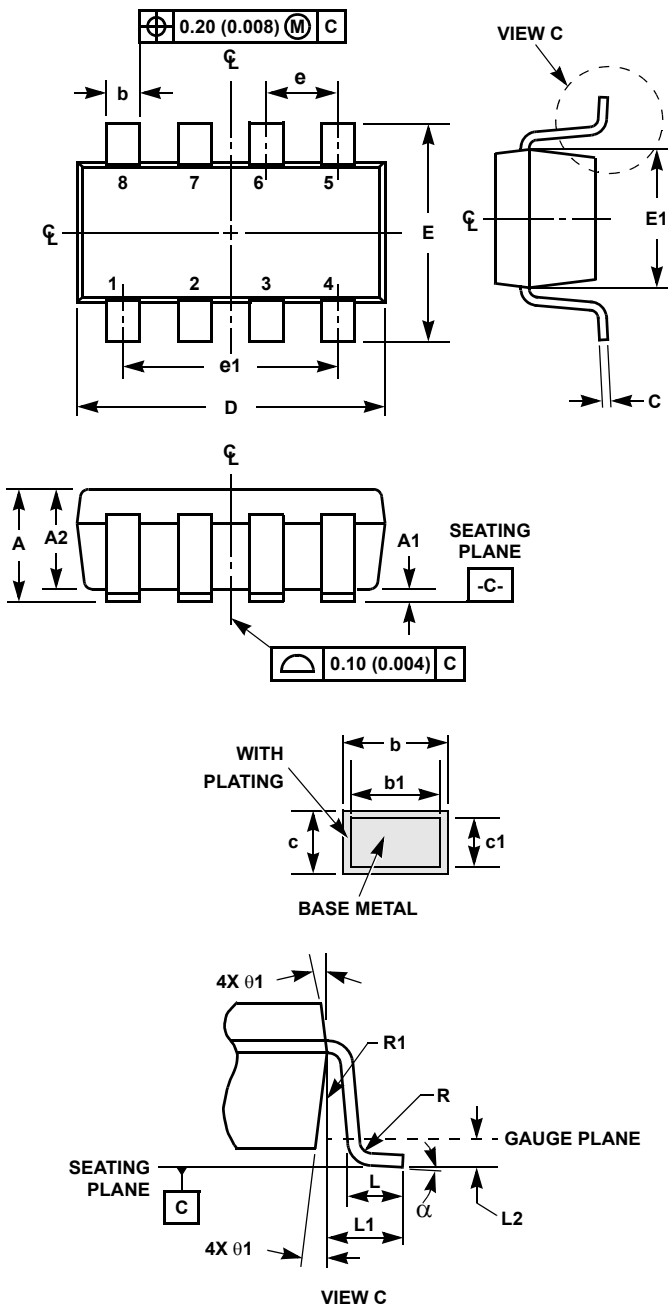
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**Small Outline Transistor Plastic Packages (SOT23-8)**



**P8.064**

**8 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.036	0.057	0.90	1.45	-
A1	0.000	0.0059	0.00	0.15	-
A2	0.036	0.051	0.90	1.30	-
b	0.009	0.015	0.22	0.38	-
b1	0.009	0.013	0.22	0.33	-
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.008	0.08	0.20	6
D	0.111	0.118	2.80	3.00	3
E	0.103	0.118	2.60	3.00	-
E1	0.060	0.067	1.50	1.70	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0768 Ref		1.95 Ref		-
L	0.014	0.022	0.35	0.55	4
L1	0.024 Ref.		0.60 Ref.		-
L2	0.010 Ref.		0.25 Ref.		-
N	8		8		5
R	0.004	-	0.10	-	-
R1	0.004	0.010	0.10	0.25	-
$\alpha$	0°	8°	0°	8°	-

Rev. 2 9/03

**NOTES:**

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178BA.
3. Dimensions  $D$  and  $E_1$  are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength  $L$  measured at reference to gauge plane.
5. "N" is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only