- **Member of the Texas Instruments Widebus+™ Family**
- **Pinout Optimizes DDR-II DIMM PCB Layout**
- **Configurable as 25-Bit 1:1 or 14-Bit 1:2 Registered Buffer**
- **Chip-Select Inputs Gate the Data Outputs from Changing State and Minimizes System Power Consumption**
- **Output Edge-Control Circuitry Minimizes Switching Noise in an Unterminated Line**
- **Supports SSTL_18 Data Inputs**
- **Differential Clock (CLK and $\overline{\text{CLK}}$) Inputs**
- **Supports LVCMOS Switching Levels on the Control and $\overline{\text{RESET}}$ Inputs**
- **$\overline{\text{RESET}}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **5000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

description/ordering information

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V V_{CC} operation. In the 1:1 pinout configuration, only one device per DIMM is required to drive nine SDRAM loads. In the 1:2 pinout configuration, two devices per DIMM are required to drive 18 SDRAM loads.

All inputs are SSTL_18, except the LVCMOS reset ($\overline{\text{RESET}}$) and LVCMOS control (Cn) inputs. All outputs are edge-controlled circuits optimized for unterminated DIMM loads and meet SSTL_18 specifications.

The SN74SSTU32864 operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and $\overline{\text{CLK}}$ going low.

The C0 input controls the pinout configuration of the 1:2 pinout from register-A configuration (when low) to register-B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high). C0 and C1 should not be switched during normal operation. They should be hard-wired to a valid low or high level to configure the register in the desired mode. In the 25-bit 1:1 pinout configuration, the A6, D6, and H6 terminals are driven low and should not be used.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ and Cn inputs always must be held at a valid logic high or low level.

The two V_{REF} pins (A3 and T3), are connected together internally by approximately 150 Ω. However, it is necessary to connect only one of the two V_{REF} pins to the external V_{REF} power supply. An unused V_{REF} pin should be terminated with a V_{REF} coupling capacitor.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	LFBGA – GKE	Tape and reel	SN74SSTU32864GKER	SU864

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

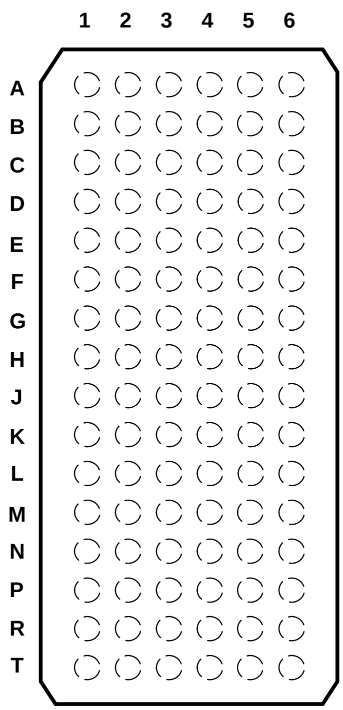
Widebus+ is a trademark of Texas Instruments.

description/ordering information (continued)

The device also supports low-power active operation by monitoring both system chip select ($\overline{\text{DCS}}$ and $\overline{\text{CSR}}$) inputs and will gate the Qn outputs from changing states when both $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs are high. If either $\overline{\text{DCS}}$ or $\overline{\text{CSR}}$ input is low, the Qn outputs function normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control and forces the output low. If the $\overline{\text{DCS}}$ control functionality is not desired, the $\overline{\text{CSR}}$ input can be hard-wired to ground, in which case, the setup-time requirement for $\overline{\text{DCS}}$ is the same as for the other D data inputs.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

GKE PACKAGE
(TOP VIEW)

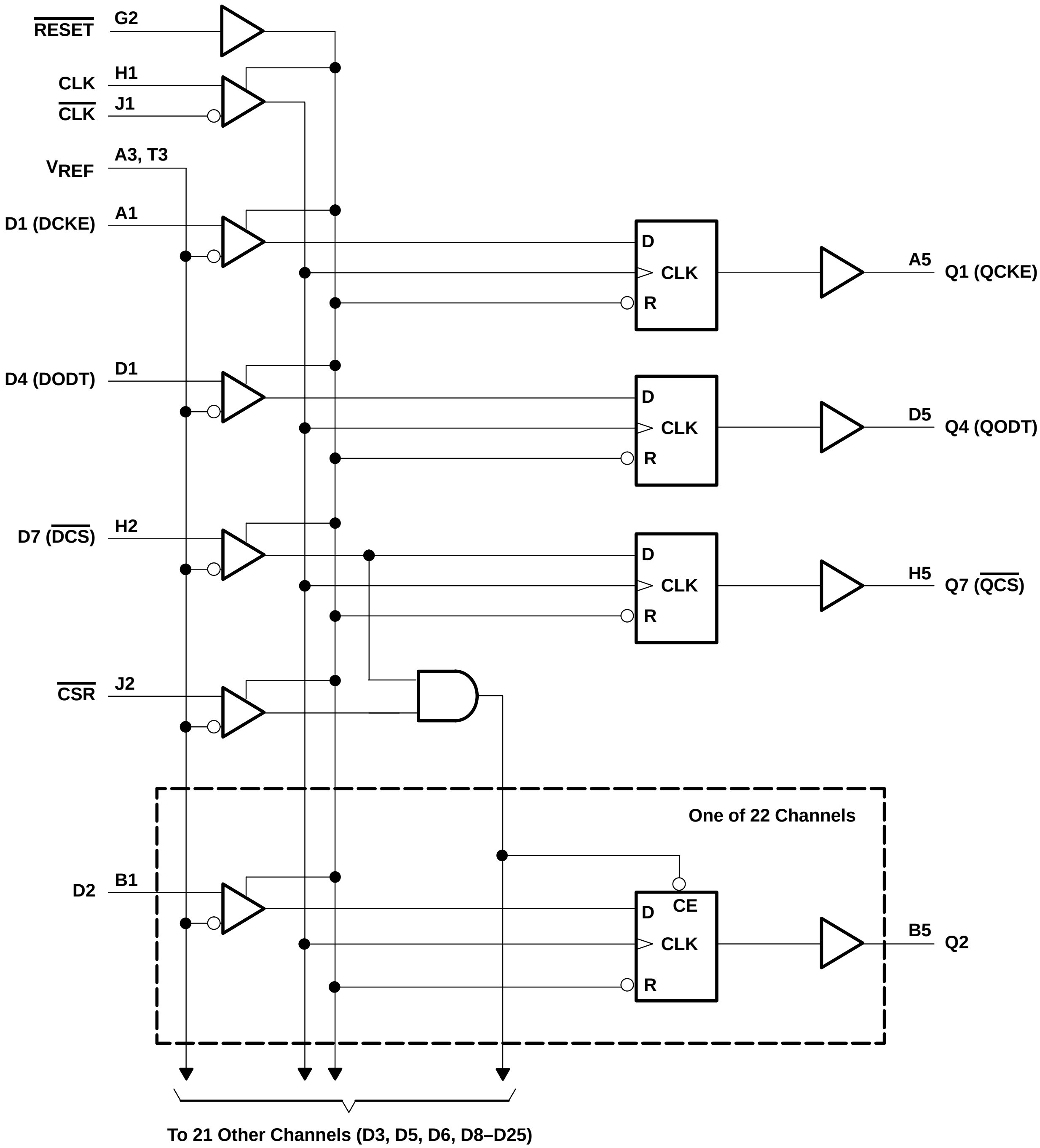


terminal assignments for 1:1 register (C0 = 0, C1 = 0)

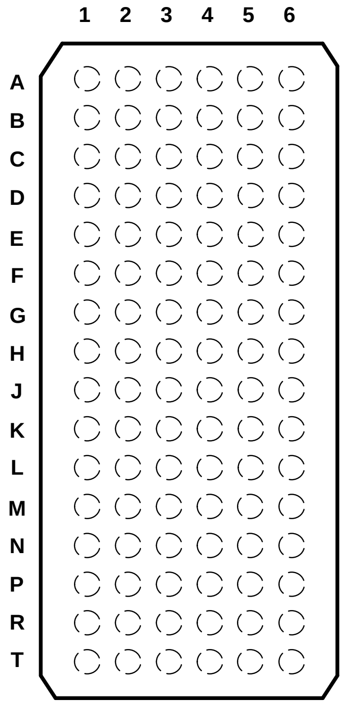
	1	2	3	4	5	6
A	D1 (DCKE)	NC	V_{REF}	V_{CC}	Q1 (QCKE)	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	V_{CC}	V_{CC}	Q3	Q16
D	D4 (DODT)	NC	GND	GND	Q4 (QODT)	DNU
E	D5	D17	V_{CC}	V_{CC}	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	NC	$\overline{\text{RESET}}$	V_{CC}	V_{CC}	C1	C0
H	CLK	D7 ($\overline{\text{DCS}}$)	GND	GND	Q7 ($\overline{\text{QCS}}$)	DNU
J	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	V_{CC}	V_{CC}	NC	NC
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V_{CC}	V_{CC}	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	V_{CC}	V_{CC}	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V_{CC}	V_{CC}	Q13	Q24
T	D14	D25	V_{REF}	V_{CC}	Q14	Q25

Each pin name in parentheses indicates the DDR-II DIMM signal name.
NC – No internal connection
DNU – Do not use

logic diagram for 1:1 register configuration (positive logic)



GKE PACKAGE
(TOP VIEW)

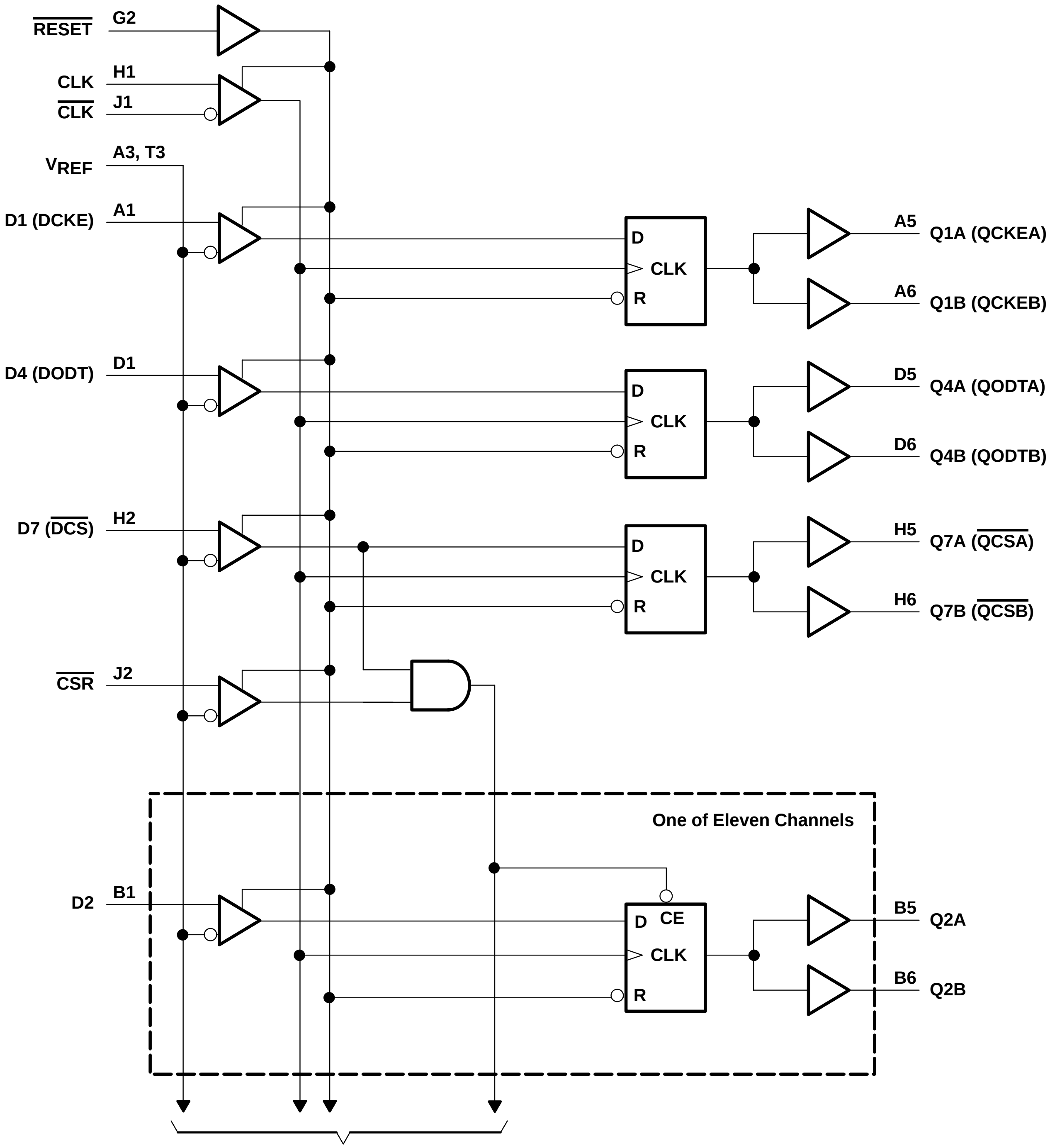


terminal assignments for 1:2 register A (C0 = 0, C1 = 1)

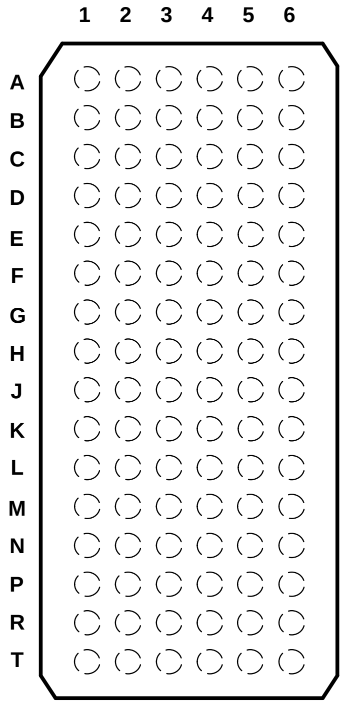
	1	2	3	4	5	6
A	D1 (DCKE)	NC	V_{REF}	V_{CC}	Q1A (QCKEA)	Q1B (QCKEB)
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V_{CC}	V_{CC}	Q3A	Q3B
D	D4 (DODT)	NC	GND	GND	Q4A (QODTA)	Q4B (QODTB)
E	D5	DNU	V_{CC}	V_{CC}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	$\overline{\text{RESET}}$	V_{CC}	V_{CC}	C1	C0
H	CLK	D7 ($\overline{\text{DCS}}$)	GND	GND	Q7A ($\overline{\text{QCSA}}$)	Q7B ($\overline{\text{QCSB}}$)
J	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	V_{CC}	V_{CC}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V_{CC}	V_{CC}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	V_{CC}	V_{CC}	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V_{CC}	V_{CC}	Q13A	Q13B
T	D14	DNU	V_{REF}	V_{CC}	Q14A	Q14B

Each pin name in parentheses indicates the DDR-II DIMM signal name.
NC – No internal connection
DNU – Do not use

logic diagram 1:2 register-A configuration (positive logic)



**GKE PACKAGE
(TOP VIEW)**

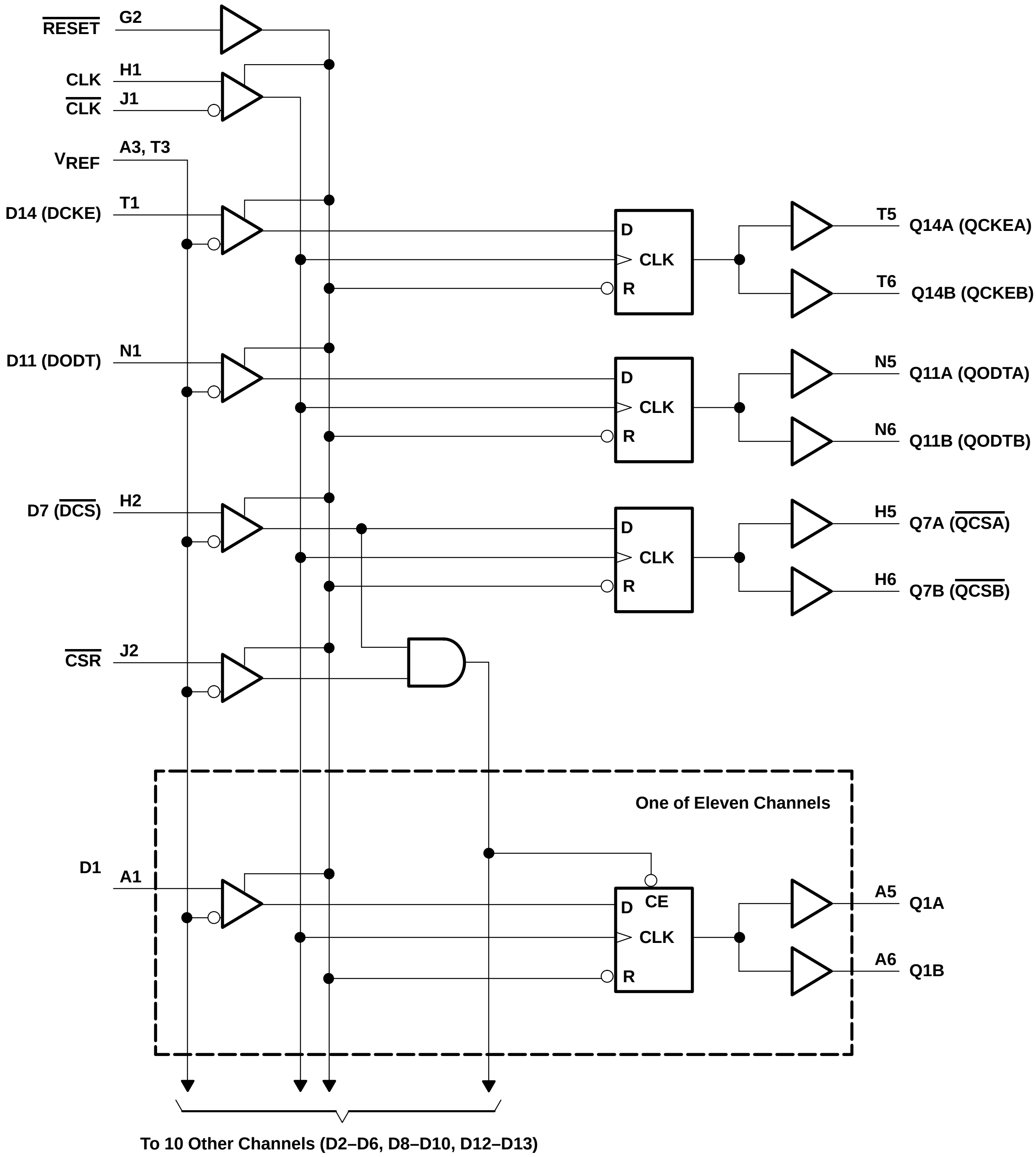


terminal assignments for 1:2 register B (C0 = 1, C1 = 1)

	1	2	3	4	5	6
A	D1	NC	V_{REF}	V_{CC}	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V_{CC}	V_{CC}	Q3A	Q3B
D	D4	NC	GND	GND	Q4A	Q4B
E	D5	DNU	V_{CC}	V_{CC}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	$\overline{\text{RESET}}$	V_{CC}	V_{CC}	C1	C0
H	CLK	D7 ($\overline{\text{DCS}}$)	GND	GND	Q7A ($\overline{\text{QCSA}}$)	Q7B ($\overline{\text{QCSB}}$)
J	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	V_{CC}	V_{CC}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V_{CC}	V_{CC}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11 (DODT)	DNU	V_{CC}	V_{CC}	Q11A (QODTA)	Q11B (QODTB)
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V_{CC}	V_{CC}	Q13A	Q13B
T	D14 (DCKE)	DNU	V_{REF}	V_{CC}	Q14A (QCKEA)	Q14B (QCKEB)

Each pin name in parentheses indicates the DDR-II DIMM signal name.
NC – No internal connection
DNU – Do not use

logic diagram 1:2 register-B configuration (positive logic)



TERMINAL FUNCTIONS

TERMINAL NAME	DESCRIPTION	ELECTRICAL CHARACTERISTICS
GND	Ground	Ground input
V_{CC}	Power-supply voltage	1.8 V nominal
V_{REF}	Input reference voltage	0.9 V nominal
CLK	Positive master clock input	Differential input
$\overline{CLK}$	Negative master clock input	Differential input
C0, C1	Configuration control inputs – Register A, Register B, 1:1, 1:2 select	LVCMOS inputs
$\overline{RESET}$	Asynchronous reset input – resets registers and disables V_{REF} data and clock differential-input receivers	LVCMOS input
D1–D25	Data inputs – clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{CLK}$	SSTL_18 inputs
$\overline{CSR}$, $\overline{DCS}$	Chip select inputs – disables D1-D25† outputs switching when both inputs are high	SSTL_18 inputs
DODT	The outputs of this register bit will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control.	SSTL_18 input
DCKE	The outputs of this register bit will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control.	SSTL_18 input
Q1–Q25‡	Data outputs that are suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8 V CMOS outputs
$\overline{QCS}$	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8 V CMOS output
QODT	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8 V CMOS output
QCKE	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8 V CMOS output
NC	No internal connection	
DNU	Do not use – inputs are in standby-equivalent mode, and outputs are driven low.	

† Data inputs = D2, D3, D5, D6, D8–D25 when C0 = 0 and C1 = 0
Data inputs = D2, D3 D5, D6, D8–D14 when C0 = 0 and C1 = 1
Data inputs = D1–D6, D8–D10, D12, D13 when C0 = 1 and C1 = 1.
‡ Data outputs = Q2, Q3, Q5, Q6, Q8–Q25 when C0 = 0 and C1 = 0
Data outputs = Q2, Q3 Q5, Q6, Q8–Q14 when C0 = 0 and C1 = 1
Data outputs = Q1–Q6, Q8–Q10, Q12, Q13 when C0 = 1 and C1 = 1.

FUNCTION TABLES

INPUTS						OUTPUT
$\overline{\text{RESET}}$	$\overline{\text{DCS}}$	$\overline{\text{CSR}}$	CLK	$\overline{\text{CLK}}$	Dn	Qn
H	L	X	↑	↓	L	L
H	L	X	↑	↓	H	H
H	X	L	↑	↓	L	L
H	X	L	↑	↓	H	H
H	H	H	↑	↓	X	Q_0
H	X	X	L or H	L or H	X	Q_0
L	X or floating	X or floating	X or floating	X or floating	X or floating	L

INPUTS				OUTPUTS
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	DCKE, $\overline{\text{DCS}}$, DODT	QCKE, $\overline{\text{QCS}}$, QODT
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0
L	X or floating	X or floating	X or floating	L

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 2.5 V
Input voltage range, V_I (see Notes 1 and 2) . . . . –0.5 V to 2.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . ±50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . ±50 mA
Continuous current through each V_{CC} or GND . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . 36°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 2.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		1.7		1.9	V
V_{REF}	Reference voltage		$0.49 \times V_{CC}$	$0.5 \times V_{CC}$	$0.51 \times V_{CC}$	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	AC high-level input voltage	Data inputs, $\overline{CSR}$	V_{REF}+250 mV			V
V_{IL}	AC low-level input voltage	Data inputs, $\overline{CSR}$			V_{REF}–250 mV	V
V_{IH}	DC high-level input voltage	Data inputs, $\overline{CSR}$	V_{REF}+125 mV			V
V_{IL}	DC low-level input voltage	Data inputs, $\overline{CSR}$			V_{REF}–125 mV	V
V_{IH}	High-level input voltage	$\overline{RESET}$, Cn	$0.65 \times V_{CC}$			V
V_{IL}	Low-level input voltage	$\overline{RESET}$, Cn			$0.35 \times V_{CC}$	V
V_{ICR}	Common-mode input voltage range	CLK, $\overline{CLK}$	0.675		1.125	V
$V_{I(PP)}$	Peak-to-peak input voltage	CLK, $\overline{CLK}$	600			mV
I_{OH}	High-level output current				–8	mA
I_{OL}	Low-level output current				8	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 4: The $\overline{RESET}$ and Cn inputs of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{RESET}$ is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		1.7 V to 1.9 V	V_{CC}–0.2			V
		I_{OH} = –6 mA		1.7 V	1.2			
V_{OL}		I_{OL} = 100 µA		1.7 V to 1.9 V			0.2	V
		I_{OL} = 6 mA		1.7 V			0.5	
I_I	All inputs‡	V_I = V_{CC} or GND		1.9 V			±5	µA
I_{CC}	Static standby	$\overline{RESET}$ = GND	I_O = 0	1.9 V			100	µA
	Static operating	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$					40	mA
I_{CCD}	Dynamic operating – clock only	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle	I_O = 0	1.8 V		28		µA/ MHz
	Dynamic operating – per each data input, 1:1 configuration	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle				18		µA/ clock MHz/ D input
	Dynamic operating – per each data input, 1:2 configuration					36		
I_{CCDLP}	Chip-select-enabled low-power active mode – clock only	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle	I_O = 0	1.8 V		27		µA/ MHz
	Chip-select-enabled low-power active mode – 1:1 configuration	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle				2		µA/ clock MHz/ D input
	Chip-select-enabled low-power active mode – 1:2 configuration					2		
C_i	Data inputs, $\overline{CSR}$	V_I = V_{REF} ± 250 mV		1.8 V	2.5	3	3.5	pF
	CLK, $\overline{CLK}$	V_{ICR} = 0.9 V, $V_{I(PP)}$ = 600 mV			2		3	
	$\overline{RESET}$	V_I = V_{CC} or GND				2.5		

† All typical values are at V_{CC} = 1.8 V, T_A = 25°C.
‡ Each V_{REF} pin (A3 or T3) should be tested independently, with the other (untested) pin open.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 and Note 5)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			500	MHz
t_w	Pulse duration, CLK, $\overline{CLK}$ high or low		1		ns
t_{act}	Differential inputs active time (see Note 6)			10	ns
t_{inact}	Differential inputs inactive time (see Note 7)			15	ns
t_{su}	Setup time	$\overline{DCS}$ before CLK↑, $\overline{CLK}$↓, $\overline{CSR}$ high; $\overline{CSR}$ before CLK↑, $\overline{CLK}$↓, $\overline{DCS}$ high	0.7		ns
		$\overline{DCS}$ before CLK↑, $\overline{CLK}$↓, $\overline{CSR}$ low	0.5		
		DODT, DCKE, and Data before CLK↑, $\overline{CLK}$↓	0.5		
t_h	Hold time	$\overline{DCS}$, DODT, DCKE, and Data after CLK↑, $\overline{CLK}$↓	0.5		ns

NOTES: 5. All input slew rates are 1 V/ns ±20%.
6. V_{REF} must be held at a valid input level and data inputs must be held low for a minimum time of t_{act} max, after $\overline{RESET}$ is taken high.
7. V_{REF}, data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t_{inact} max, after $\overline{RESET}$ is taken low.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.1 V		UNIT
			MIN	MAX	
f_{max}			500		MHz
t_{pdm}†	CLK and $\overline{CLK}$	Q	1.4	2.5	ns
t_{pdmss}†	CLK and $\overline{CLK}$	Q		2.7	ns
t_{RPHL}†	$\overline{RESET}$	Q		3	ns

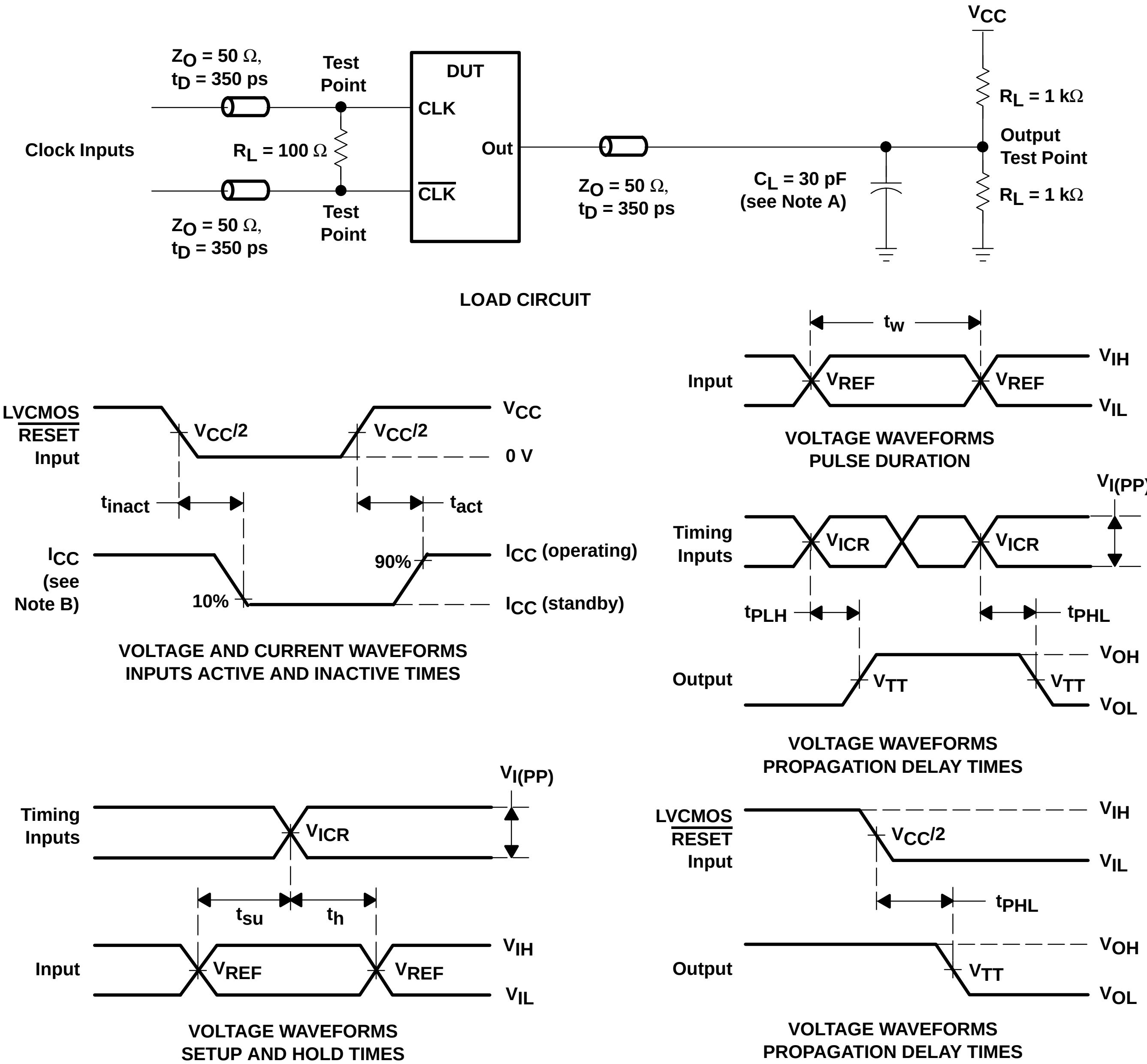
† Includes 350-ps test-load transmission-line delay

output slew rates over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM	TO	V_{CC} = 1.8 V ± 0.1 V		UNIT
			MIN	MAX	
dV/dt_r	20%	80%	1.9	4.9	V/ns
dV/dt_f	80%	20%	1.9	4.9	V/ns
dV/dt_Δ§	20% or 80%	80% or 20%		1	V/ns

§ Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

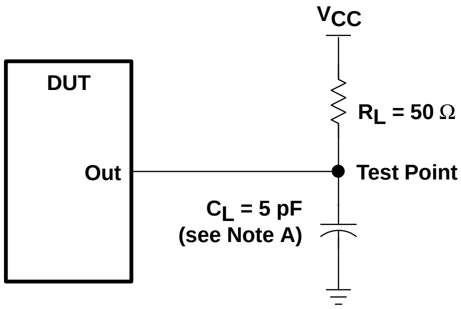
PARAMETER MEASUREMENT INFORMATION



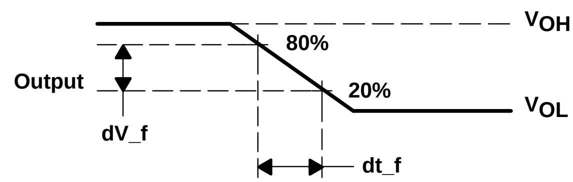
NOTES:
A. C_L includes probe and jig capacitance.
B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
D. The outputs are measured one at a time with one transition per measurement.
E. $V_{REF} = V_{CC}/2$
F. $V_{IH} = V_{REF}$ + 250 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
G. $V_{IL} = V_{REF}$ – 250 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
H. $V_{I(PP)}$ = 600 mV
I. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

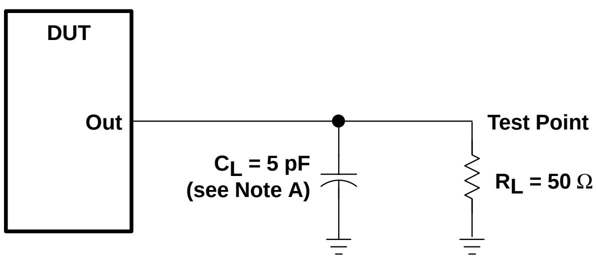
PARAMETER MEASUREMENT INFORMATION



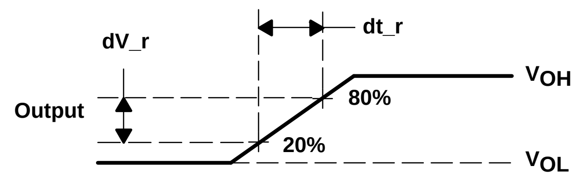
LOAD CIRCUIT
HIGH-TO-LOW SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS
HIGH-TO-LOW SLEW-RATE MEASUREMENT



LOAD CIRCUIT
LOW-TO-HIGH SLEW-RATE MEASUREMENT

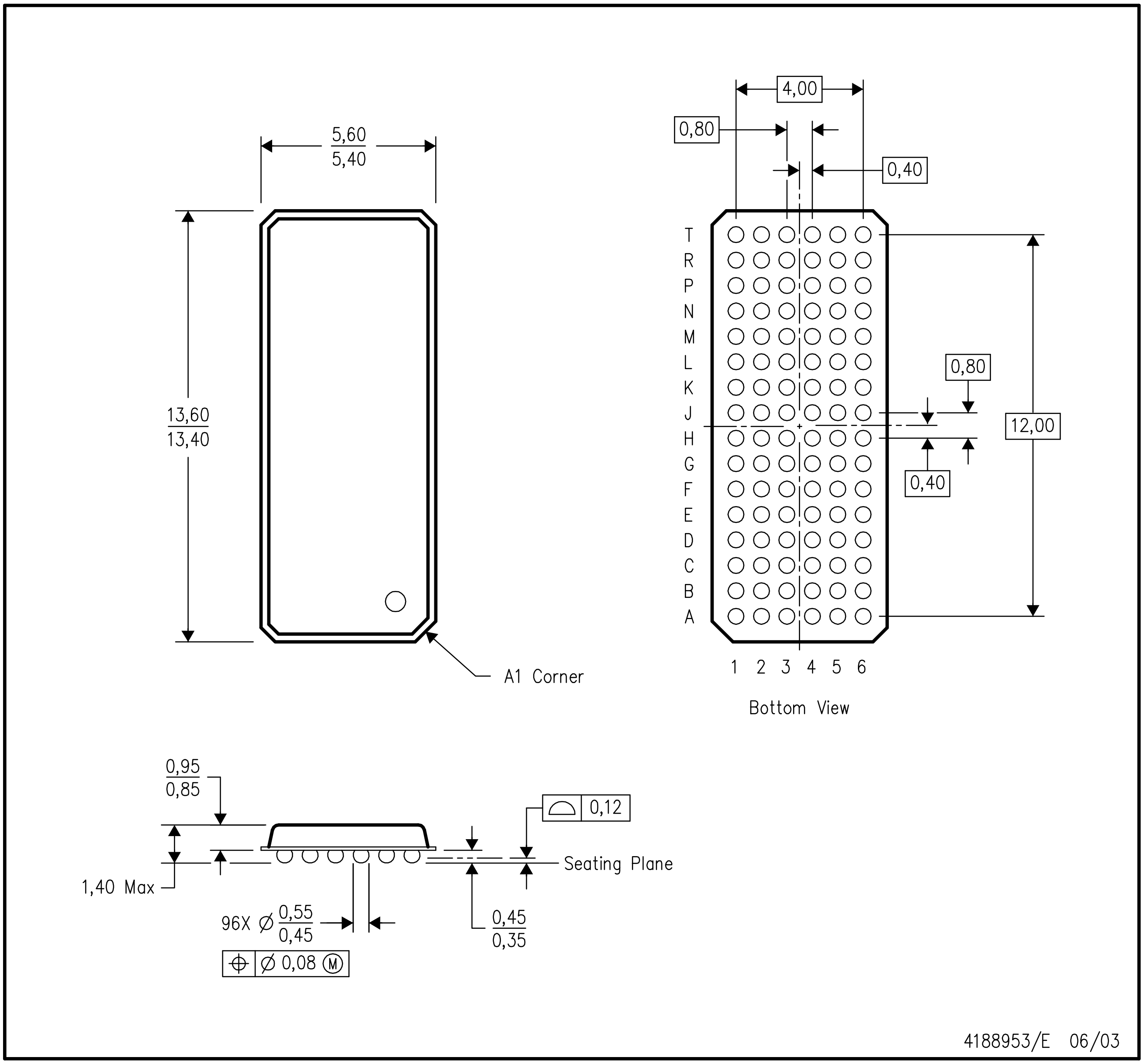


VOLTAGE WAVEFORMS
LOW-TO-HIGH SLEW-RATE MEASUREMENT

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ± 20% (unless otherwise specified).

Figure 2. Output Slew-Rate Measurement Information

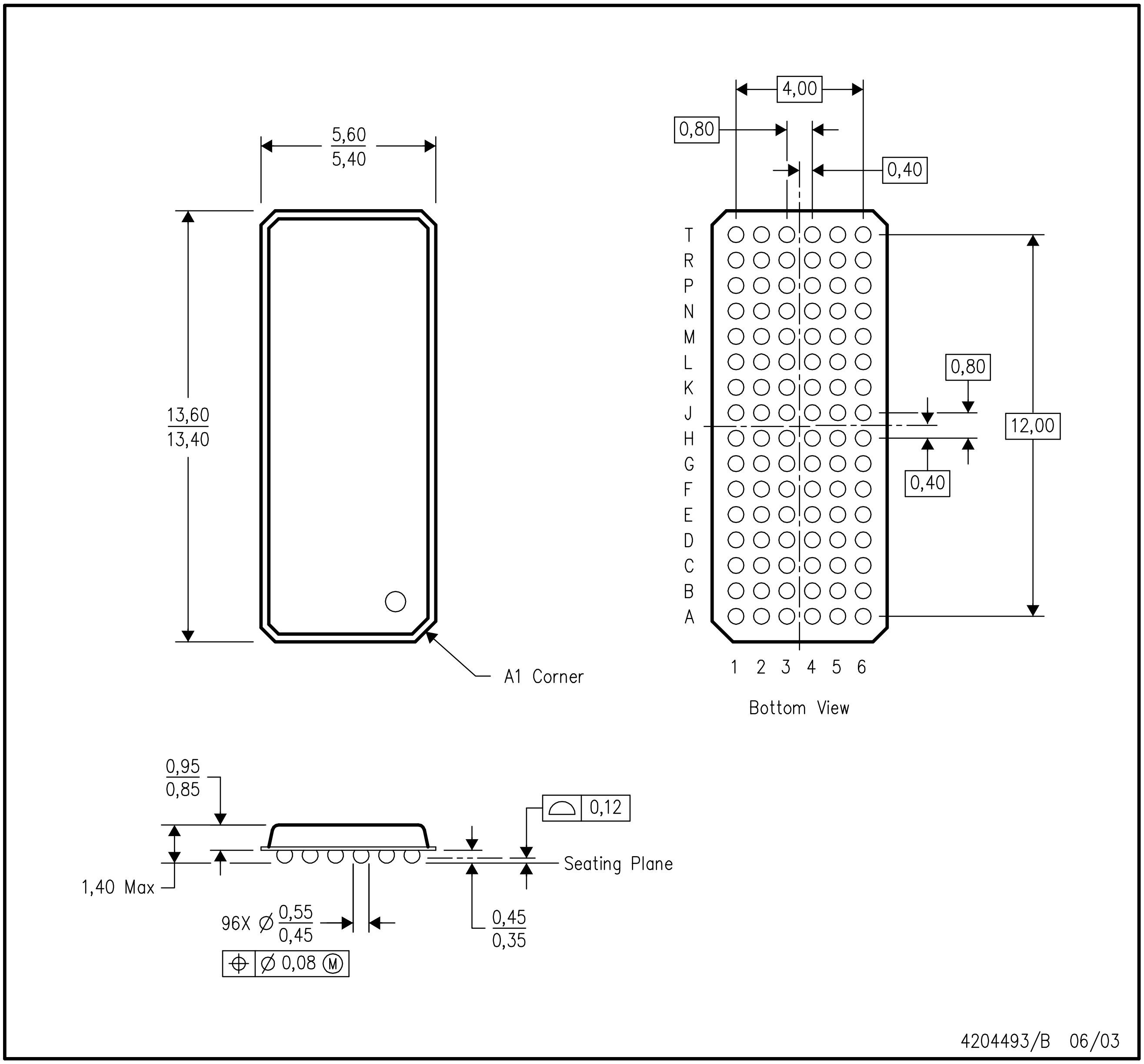
GKE (R–PBGA–N96) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration
D. Falls within JEDEC MO–205 variation CC.
E. This package is tin–lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead–free.

MicroStar BGA is a trademark of Texas Instruments.

ZKE (R–PBGA–N96) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration
D. Falls within JEDEC MO–205 variation CC.
E. This package is lead–free. Refer to the 96 GKE package (drawing 4188953) for tin–lead (SnPb).

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

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Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
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Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
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Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
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