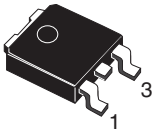
STD65N55LF3

N-channel 55 V, 7.0 mΩ, 80 A DPAK STripFET™ III Power MOSFET

Features

Order code	V_{DSS}	$R_{DS(on)}$ max.	I_D	Pw
STD65N55LF3	55 V	< 8.5 mΩ	80 A	110 W

- Low threshold drive
- 100% avalanche tested



DPAK

Application

- Switching applications
- Automotive

Description

This product is a N-channel enhancement mode Power MOSFET built with STripFET™ III technology which is especially tailored to minimized on-state resistance and gate charge, providing superior switching performance.

Figure 1. Internal schematic diagram

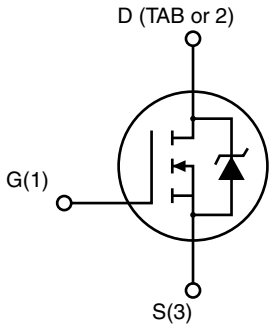


Table 1. Device summary

Order code	Marking	Package	Packaging
STD65N55LF3	65N55LF3	DPAK	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS}=0)	55	V
V_{GS}	Gate-Source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25 °C	80	A
I_D	Drain current (continuous) at T_C = 100 °C	56	A
I_{DM} (1)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25 °C	110	W
	Derating factor	0.73	W/°C
dv/dt (2)	Peak diode recovery voltage slope	11	V/ns
E_{AS} (3)	Single pulse avalanche energy	300	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤ 65 A, di/dt ≤300 A/µs, V_{DD} ≤ $V_{(BR)DSS}$, Tj ≤ Tjmax
3. Starting Tj = 25 °C, I_D = 10 A, V_{DD} = 25 V

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	1.36	°C/W
Rthj-pcb (1)	Thermal resistance junction-pcb max	50	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	I_D = 250 µA, V_{GS}= 0	55			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating,Tc = 125 °C			10 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±200	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D= 32 A		7.0	8.5	mΩ
		V_{GS} = 5 V, I_D= 32 A		8.5	12	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f=1 MHz, V_{GS} =0	-	2200 470 35	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}= 27.5 V, I_D = 65 A V_{GS} = 5 V *(see Figure 16)*	-	20 8 8	-	nC nC nC

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}= 27 V, I_D= 32 A, R_G= 4.7 Ω, V_{GS}=10 V *(see Figure 15)*	-	10 25	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time		-	50 10	-	ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)(1)		-		80 320	A A
V_{SD}	Forward on voltage	I_{SD}=65 A, V_{GS}=0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=65 A, di/dt =100 A/µs, V_{DD}=30 V, Tj=150 °C *(see Figure 17)*	-	40 60 3		ns nC A

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

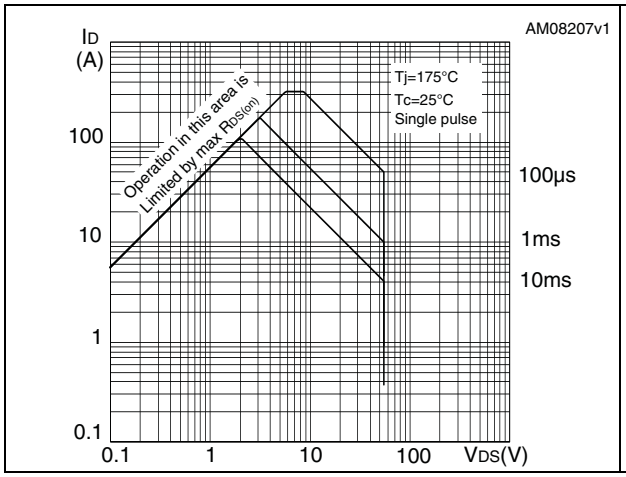


Figure 3. Thermal impedance

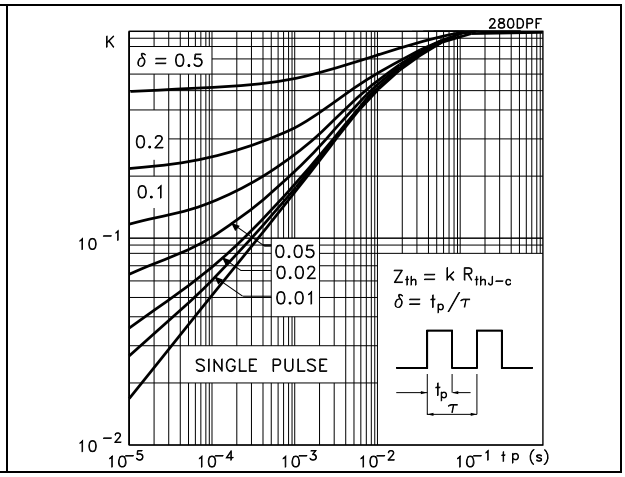


Figure 4. Output characteristics

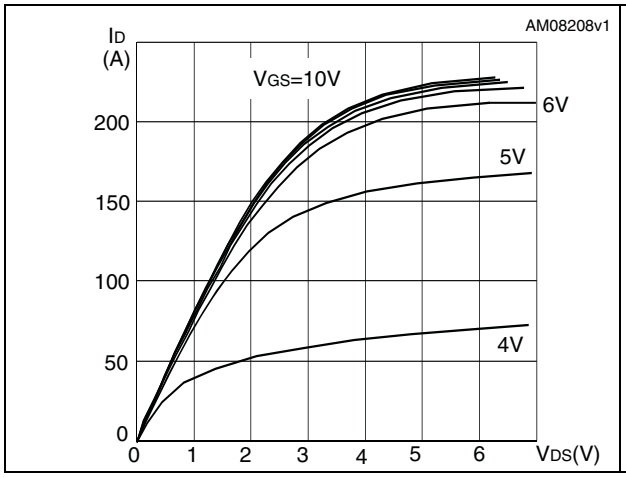


Figure 5. Transfer characteristics

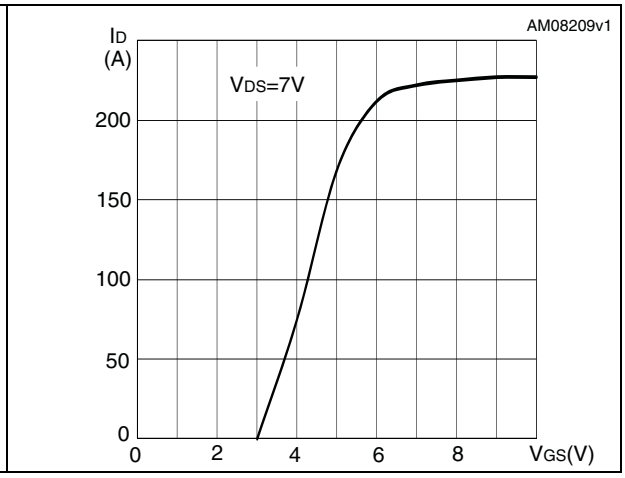


Figure 6. Normalized B_{VDSS} vs temperature

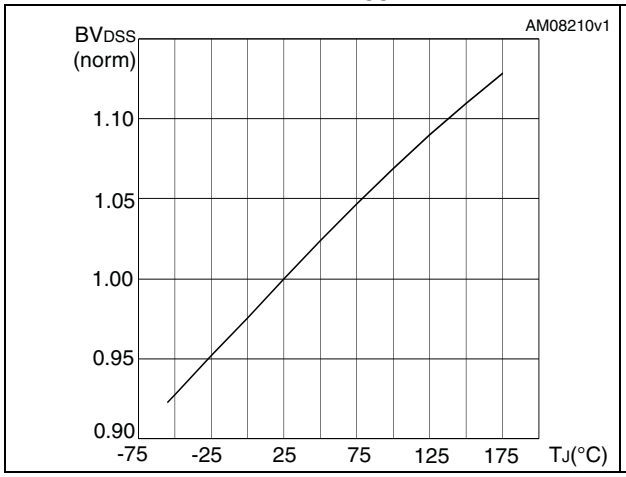


Figure 7. Static drain-source on resistance

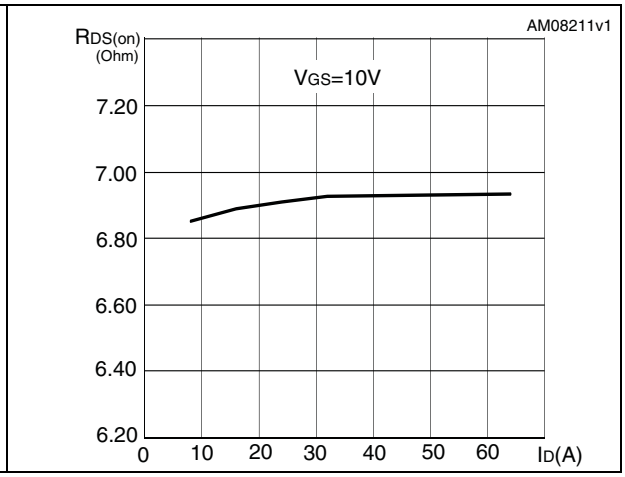


Figure 8. Gate charge vs gate-source voltage

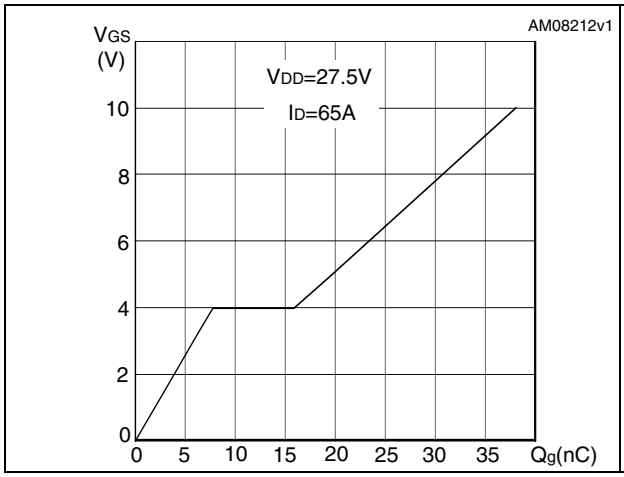


Figure 9. Capacitance variations

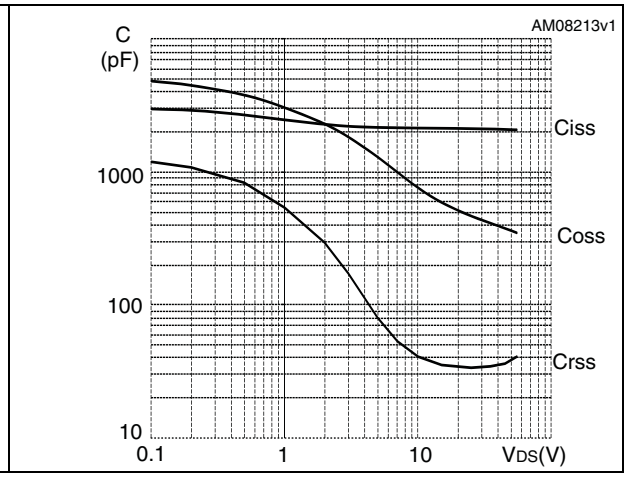


Figure 10. Normalized gate threshold voltage vs temperature

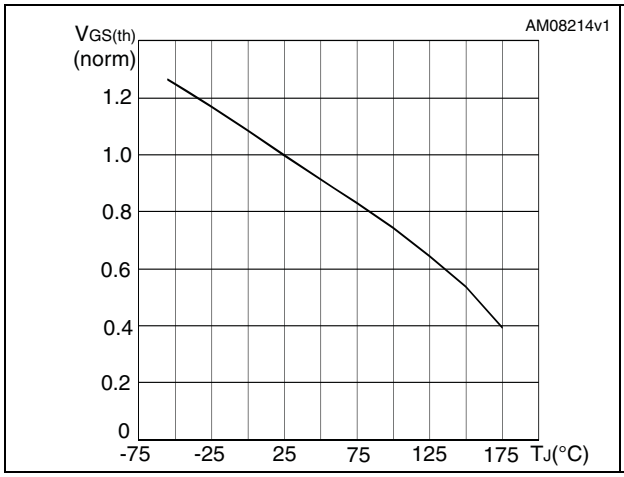


Figure 11. Normalized on resistance vs temperature

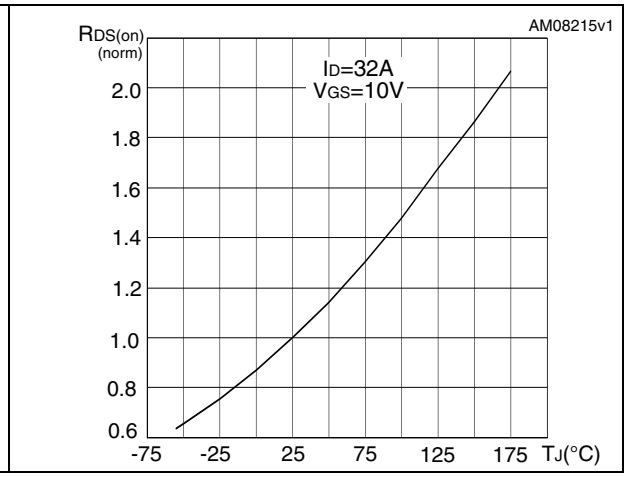
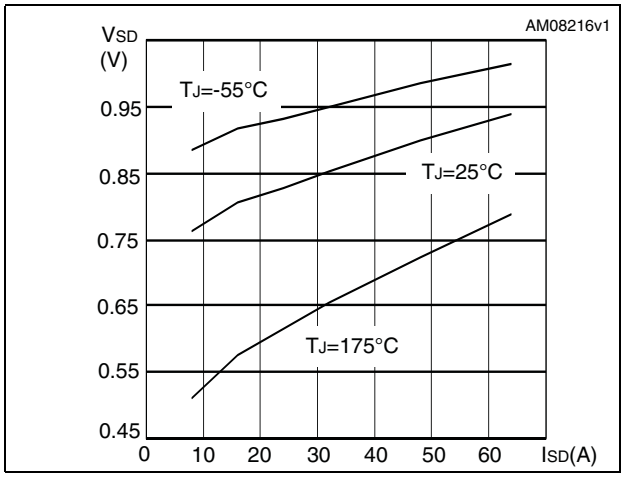


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

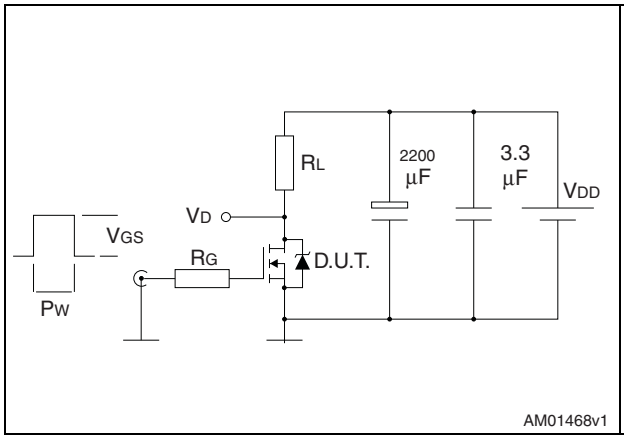


Figure 14. Gate charge test circuit

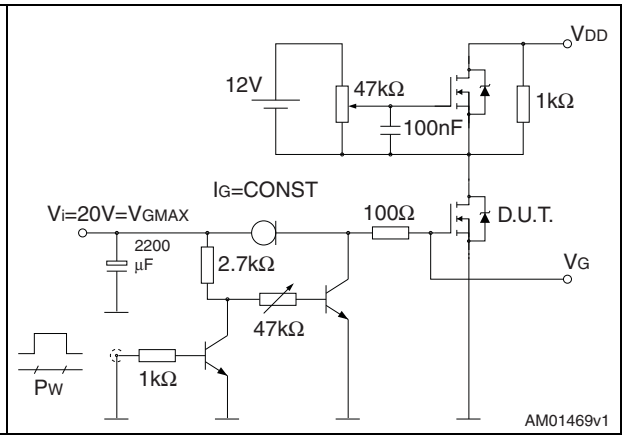


Figure 15. Test circuit for inductive load switching and diode recovery times

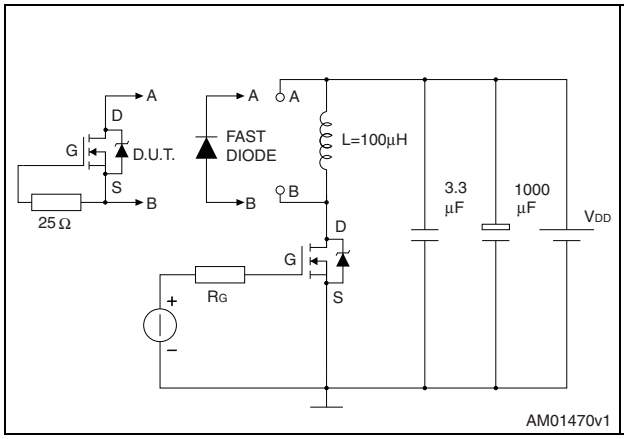


Figure 16. Unclamped inductive load test circuit

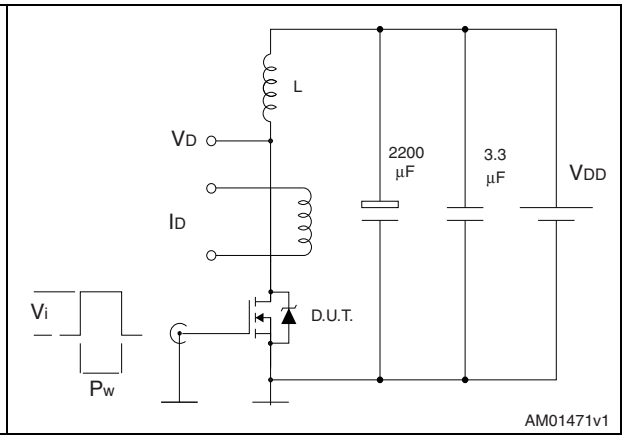


Figure 17. Unclamped inductive waveform

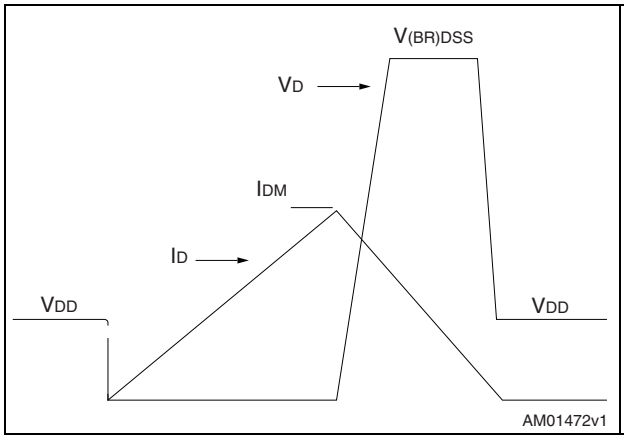
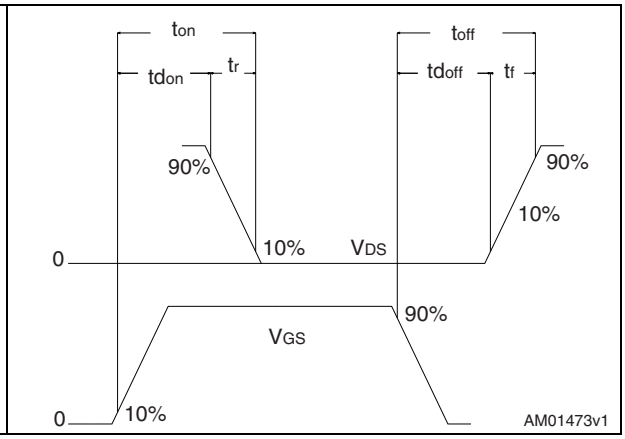


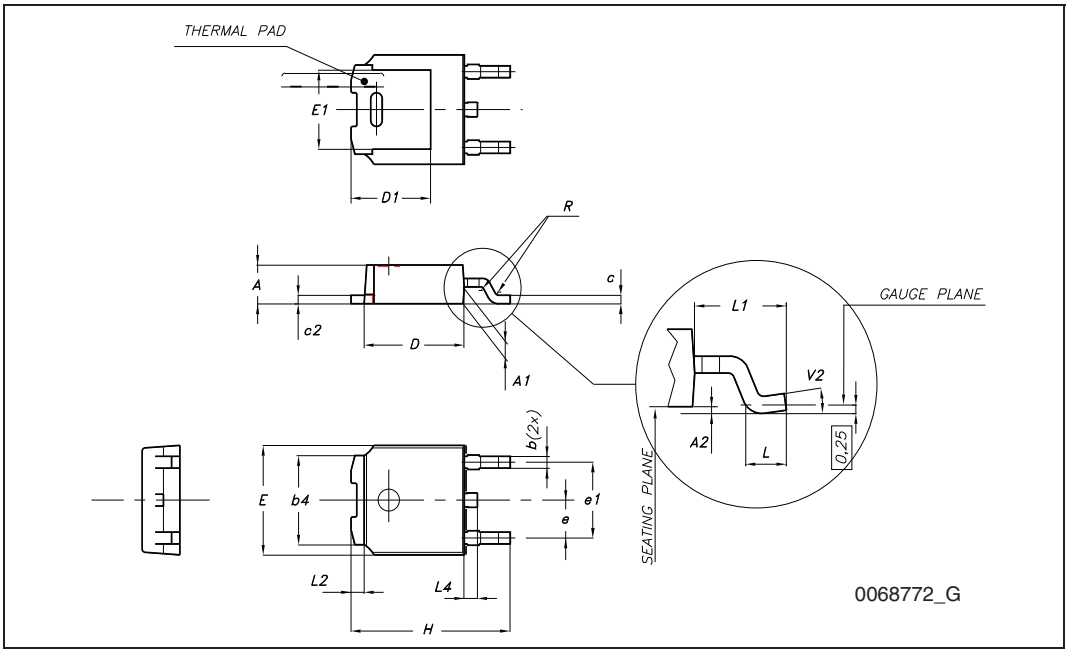
Figure 18. Switching time waveform



4 Package mechanical data

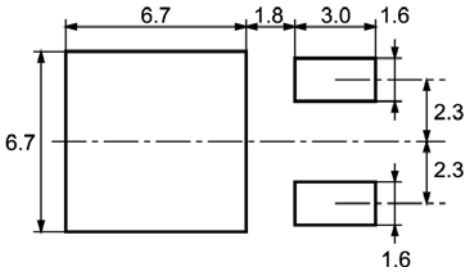
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

TO-252 (DPAK) mechanical data			
DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °



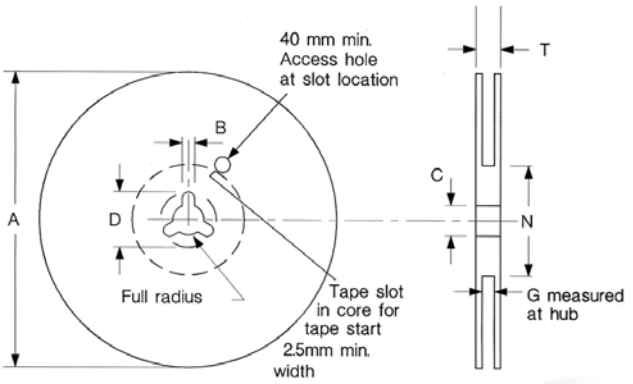
5 Packaging mechanical data

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



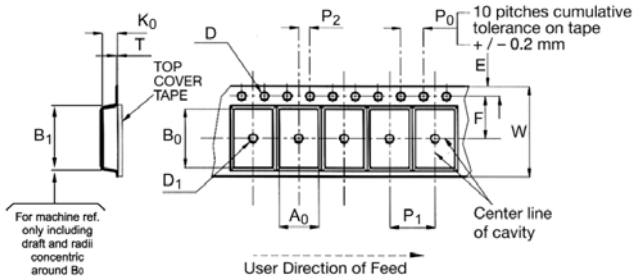
REEL MECHANICAL DATA

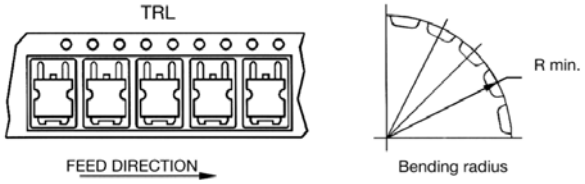
DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641





6 Revision history

Table 8. Revision history

Date	Revision	Changes
20-Oct-2009	1	First release.
12-Oct-2010	2	Document status promoted from preliminary data to datasheet.

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