MCP4021/2/3/4

Low-Cost NV Digital POT with WiperLock™ Technology

Features

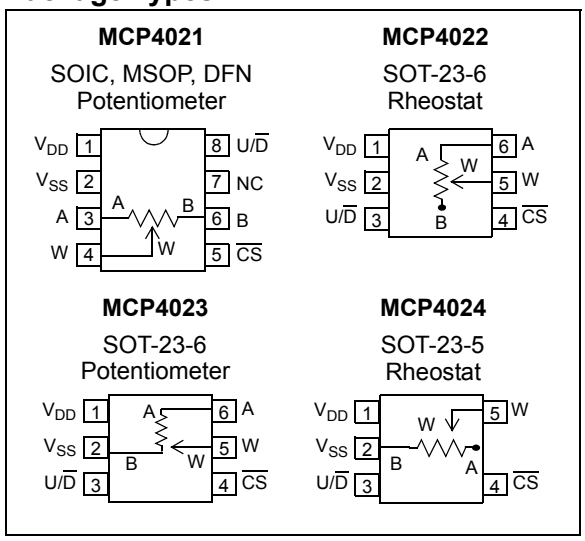
- Non-volatile Digital Potentiometer in SOT-23, SOIC, MSOP and DFN packages
- 64 Taps: 63 Resistors with Taps to terminal A and terminal B
- Simple Up/$\overline{\text{Down}}$ (U/$\overline{\text{D}}$) Protocol
- Power-on Recall of Saved Wiper Setting
- Resistance Values: 2.1 kΩ, 5 kΩ, 10 kΩ or 50 kΩ
- Low Tempco:
  - Absolute (Rheostat): 50 ppm (0°C to 70°C typ.)
  - Ratiometric (Potentiometer): 10 ppm (typ.)
- Low Wiper Resistance: 75Ω (typ.)
- WiperLock™ Technology to Secure the wiper setting in non-volatile memory (EEPROM)
- High-Voltage Tolerant Digital Inputs: Up to 12.5V
- Low-Power Operation: 1 µA Max Static Current
- Wide Operating Voltage: 2.7V to 5.5V
- Extended Temperature Range: -40°C to +125°C
- Wide Bandwidth (-3 dB) Operation:
  - 4 MHz (typ.) for 2.1 kΩ device

Description

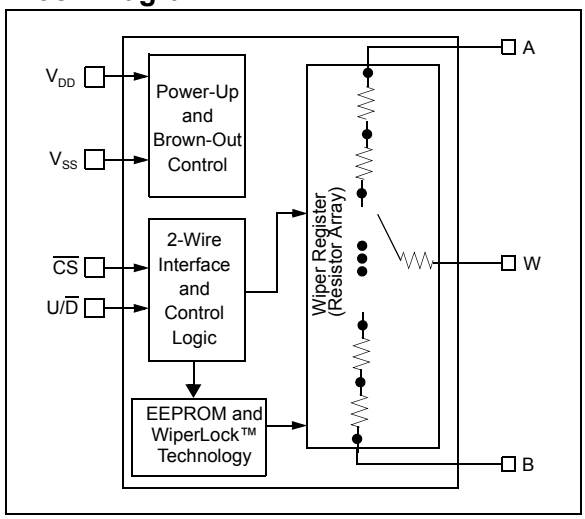
The MCP4021/2/3/4 devices are non-volatile, 6-bit digital potentiometers that can be configured as either a potentiometer or rheostat. The wiper setting is controlled through a simple Up/$\overline{\text{Down}}$ (U/$\overline{\text{D}}$) serial interface.

These device's implement Microchip's WiperLock technology, which allows application-specific calibration settings to be secured in the EEPROM without requiring the use of an additional write-protect pin.

Package Types



Block Diagram



Device Features

Device	Wiper Configuration	Memory Type	Resistance (typical)		# of Steps	V_{DD} Operating Range	Control Interface	WiperLock™ Technology
			Options (kΩ)	Wiper (Ω)				
MCP4021	Potentiometer (1)	EE	2.1, 5.0, 10.0, 50.0	75	64	2.7V - 5.5V	U/$\overline{\text{D}}$	Yes
MCP4022	Rheostat	EE	2.1, 5.0, 10.0, 50.0	75	64	2.7V- 5.5V	U/$\overline{\text{D}}$	Yes
MCP4023	Potentiometer	EE	2.1, 5.0, 10.0, 50.0	75	64	2.7V - 5.5V	U/$\overline{\text{D}}$	Yes
MCP4024	Rheostat	EE	2.1, 5.0, 10.0, 50.0	75	64	2.7V - 5.5V	U/$\overline{\text{D}}$	Yes

Note 1: Floating either terminal (A or B) allows the device to be used in Rheostat mode.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} 6.5V

$\overline{CS}$ and U/$\overline{D}$ inputs w.r.t V_{SS} ..... -0.3V to 12.5V

A, B and W terminals w.r.t V_{SS} ..... -0.3V to V_{DD} + 0.3V

Current at Input Pins .....±10 mA

Current at Supply Pins .....±10 mA

Current at Potentiometer Pins .....±2.5 mA

Storage temperature .....-65°C to +150°C

Ambient temp. with power applied .....-55°C to +125°C

ESD protection on all pins .....≥ 4 kV (HBM), ≥ 400V (MM)

Maximum Junction Temperature (T_J) .....+150°C

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply across the specified operating ranges. T_A = -40°C to +125°C, 2.1 kΩ, 5 kΩ, 10 kΩ and 50 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, V_{SS} = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Operating Voltage Range	V_{DD}	2.7	—	5.5	V	
$\overline{CS}$ Input Voltage	V_{CS}	V_{SS}	—	12.5	V	The $\overline{CS}$ pin will be at one of three input levels (V_{IL}, V_{IH} or V_{IHH}). (**Note 6**)
Supply Current	I_{DD}	—	45	—	µA	5.5V, $\overline{CS}$ = V_{SS}, $f_{U/\overline{D}}$ = 1 MHz
		—	15	—	µA	2.7V, $\overline{CS}$ = V_{SS}, $f_{U/\overline{D}}$ = 1 MHz
		—	0.3	1	µA	Serial Interface Inactive ($\overline{CS}$ = V_{IH}, U/$\overline{D}$ = V_{IH})
		—	0.6	3	mA	EE Write cycle, T_A = +25°C
Resistance (± 20%)	R_{AB}	1.68	2.1	2.52	kΩ	-202 devices **(Note 1)**
		4.0	5	6.0	kΩ	-502 devices **(Note 1)**
		8.0	10	12.0	kΩ	-103 devices **(Note 1)**
		40.0	50	60.0	kΩ	-503 devices **(Note 1)**
Resolution	N		64		Taps	No Missing Codes
Step Resistance	R_S	—	R_{AB} / 63	—	Ω	**Note 6**

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}. (-202 devices V_A = 4V).

3: **MCP4021/23** only, test conditions are: I_W = 1.9 mA, code = 00h.

4: **MCP4022/24** only, test conditions are:

Device Resistance	Current at Voltage		Comments
	5.5V	2.7V	
2.1 kΩ	2.25 mA	1.1 mA	**MCP4022** includes V_{WZSE} **MCP4024** includes V_{WFSE}
5 kΩ	1.4 mA	450 µA	
10 kΩ	450 µA	210 µA	
50 kΩ	90 µA	40 µA	

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature. See **Section 6.0 "Resistor"** for additional information.

8: The **MCP4021** is externally connected to match the configurations of the **MCP4022** and **MCP4024**, and then tested.

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply across the specified operating ranges. T_A = -40°C to +125°C, 2.1 kΩ, 5 kΩ, 10 kΩ and 50 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, V_{SS} = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions	
Wiper Resistance (**Note 3, Note 4)**	R_W	—	70	125	Ω	5.5V	
		—	70	325	Ω	2.7V	
Nominal Resistance Tempco	ΔR/ΔT	—	50	—	ppm/°C	T_A = -20°C to +70°C	
		—	100	—	ppm/°C	T_A = -40°C to +85°C	
		—	150	—	ppm/°C	T_A = -40°C to +125°C	
Ratiometeric Tempco	$\Delta V_{WA}/\Delta T$	—	10	—	ppm/°C	**MCP4021** and **MCP4023** only, code = 1Fh	
Full-Scale Error	V_{WFSE}	-0.5	-0.1	+0.5	LSb	Code 3Fh (**MCP4021/23** only)	
Zero-Scale Error	V_{WZSE}	-0.5	+0.1	+0.5	LSb	Code 00h (**MCP4021/23** only)	
Monotonicity	N		Yes		Bits		
Potentiometer Integral Non-linearity	INL	-0.5	±0.25	+0.5	LSb	**MCP4021/23** only **(Note 2)**	
Potentiometer Differential Non-linearity	DNL	-0.5	±0.25	+0.5	LSb	**MCP4021/23** only **(Note 2)**	
Resistor Terminal Input Voltage Range (Terminals A, B and W)	V_A, V_W, V_B	Vss	—	V_{DD}	V	**Note 5, Note 6**	
Maximum current through A, W or B	I_W	—	—	2.5	mA	**Note 6**	
Leakage current into A, W or B	I_{WL}	—	100	—	nA	**MCP4021** A = W = B = V_{SS}	
		—	100	—	nA	**MCP4022/23** A = W = V_{SS}	
		—	100	—	nA	**MCP4024** W = V_{SS}	
Capacitance (P_A)	C_{AW}	—	75	—	pF	f =1 MHz, code = 1Fh	
Capacitance (P_w)	C_W	—	120	—	pF	f =1 MHz, code = 1Fh	
Capacitance (P_B)	C_{BW}	—	75	—	pF	f =1 MHz, code = 1Fh	
Bandwidth -3 dB	BW	—	4	—	MHz	-202 devices	Code = 1F, output load = 30 pF
		—	2	—	MHz	-502 devices	
		—	1	—	MHz	-103 devices	
		—	200	—	kHz	-503 devices	

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$. (-202 devices V_A = 4V).

3: **MCP4021/23** only, test conditions are: I_W = 1.9 mA, code = 00h.

4: **MCP4022/24** only, test conditions are:

Device Resistance	Current at Voltage		Comments
	5.5V	2.7V	
2.1 kΩ	2.25 mA	1.1 mA	**MCP4022** includes V_{WZSE} **MCP4024** includes V_{WFSE}
5 kΩ	1.4 mA	450 µA	
10 kΩ	450 µA	210 µA	
50 kΩ	90 µA	40 µA	

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature. See **Section 6.0 "Resistor"** for additional information.

8: The **MCP4021** is externally connected to match the configurations of the **MCP4022** and **MCP4024**, and then tested.

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply across the specified operating ranges. T_A = -40°C to +125°C, 2.1 kΩ, 5 kΩ, 10 kΩ and 50 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, V_{SS} = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions	
Rheostat Integral Non-linearity **MCP4021** (**Note 4, Note 8**) **MCP4022** and **MCP4024 (Note 4)**	R-INL	-0.5	±0.25	+0.5	LSb	-202 devices (2.1 kΩ)	5.5V
		-8.5	+4.5	+8.5	LSb		2.7V **(Note 7)**
		-0.5	±0.25	+0.5	LSb	-502 devices (5 kΩ)	5.5V
		-5.5	+2.5	+5.5	LSb		2.7V **(Note 7)**
		-0.5	±0.25	+0.5	LSb	-103 devices (10 kΩ)	5.5V
		-3	+1	+3	LSb		2.7V **(Note 7)**
		-0.5	±0.25	+0.5	LSb	-503 devices (50 kΩ)	5.5V
		-1	+0.25	+1	LSb		2.7V **(Note 7)**
Rheostat Differential Non-linearity **MCP4021** (**Note 4, Note 8**) **MCP4022** and **MCP4024 (Note 4)**	R-DNL	-0.5	±0.25	+0.5	LSb	-202 devices (2.1 kΩ)	5.5V
		-1	+0.5	+2	LSb		2.7V **(Note 7)**
		-0.5	±0.25	+0.5	LSb	-502 devices (5 kΩ)	5.5V
		-1	+0.25	+1.25	LSb		2.7V **(Note 7)**
		-0.5	±0.25	+0.5	LSb	-103 devices (10 kΩ)	5.5V
		-1	0	+1	LSb		2.7V **(Note 7)**
		-0.5	±0.25	+0.5	LSb	-503 devices (50 kΩ)	5.5V
		-0.5	0	+0.5	LSb		2.7V **(Note 7)**

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$. (-202 devices V_A = 4V).

3: **MCP4021/23** only, test conditions are: I_W = 1.9 mA, code = 00h.

4: **MCP4022/24** only, test conditions are:

Device Resistance	Current at Voltage		Comments
	5.5V	**2.7V**	
2.1 kΩ	2.25 mA	1.1 mA	**MCP4022** includes V_{WZSE} **MCP4024** includes V_{WFSE}
5 kΩ	1.4 mA	450 µA	
10 kΩ	450 µA	210 µA	
50 kΩ	90 µA	40 µA	

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature. See **Section 6.0 "Resistor"** for additional information.

8: The **MCP4021** is externally connected to match the configurations of the **MCP4022** and **MCP4024**, and then tested.

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply across the specified operating ranges. T_A = -40°C to +125°C, 2.1 kΩ, 5 kΩ, 10 kΩ and 50 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, V_{SS} = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Digital Inputs/Outputs ($\overline{CS}$, U/$\overline{D}$)						
Input High Voltage	V_{IH}	0.7 V_{DD}	—	—	V	
Input Low Voltage	V_{IL}	—	—	0.3 V_{DD}	V	
High-Voltage Input Entry Voltage	V_{IHH}	8.5	—	12.5**(6)**	V	Threshold for WiperLock™ Technology
High-Voltage Input Exit Voltage	V_{IHH}	—	—	V_{DD}+0.8**(6)**	V	
$\overline{CS}$ Pull-up/Pull-down Resistance	R_{CS}	—	16	—	kΩ	V_{DD} = 5.5V, V_{CS} = 3V
$\overline{CS}$ Weak Pull-up/Pull-down Current	I_{PU}	—	170	—	µA	V_{DD} = 5.5V, V_{CS} = 3V
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{IN} = V_{DD}
$\overline{CS}$ and U/$\overline{D}$ Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 1 MHz
RAM (Wiper) Value						
Value Range	N	0h	—	3Fh	hex	
EEPROM						
Endurance	$E_{ndurance}$	—	1M	—	Cycles	
EEPROM Range	N	0h	—	3Fh	hex	
Initial Factory Setting	N		1Fh		hex	WiperLock Technology = Off
Power Requirements						
Power Supply Sensitivity (**MCP4021** and **MCP4023** only)	PSS	—	0.0015	0.0035	%/%	V_{DD} = 4.5V to 5.5V, V_A = 4.5V, Code = 1Fh
		—	0.0015	0.0035	%/%	V_{DD} = 2.7V to 4.5V, V_A = 2.7V, Code = 1Fh

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}. (-202 devices V_A = 4V).

3: **MCP4021/23** only, test conditions are: I_W = 1.9 mA, code = 00h.

4: **MCP4022/24** only, test conditions are:

Device Resistance	Current at Voltage		Comments
	5.5V	**2.7V**	
2.1 kΩ	2.25 mA	1.1 mA	**MCP4022** includes V_{WZSE} **MCP4024** includes V_{WFSE}
5 kΩ	1.4 mA	450 µA	
10 kΩ	450 µA	210 µA	
50 kΩ	90 µA	40 µA	

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly over voltage and temperature. See **Section 6.0 "Resistor"** for additional information.

8: The **MCP4021** is externally connected to match the configurations of the **MCP4022** and **MCP4024**, and then tested.

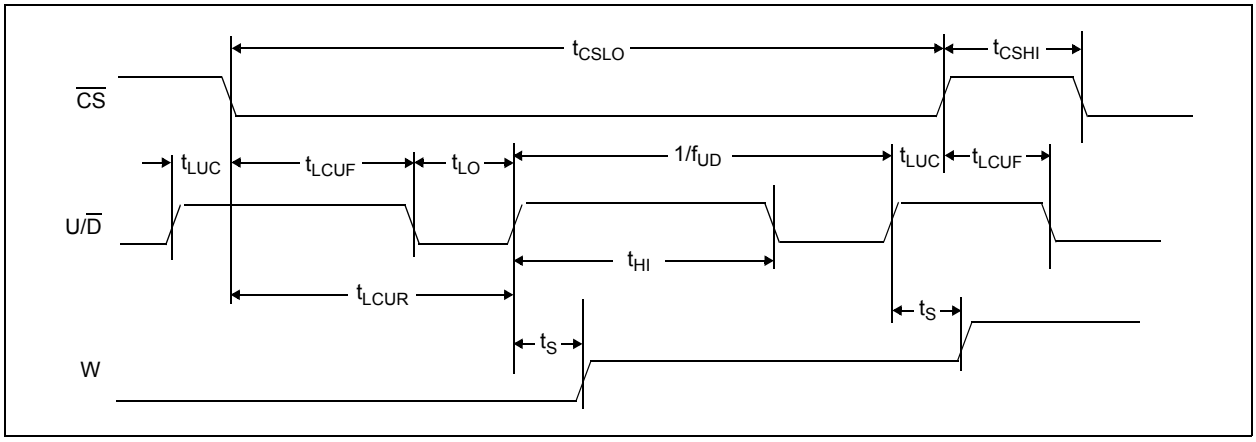

FIGURE 1-1: *Increment Timing Waveform.*

SERIAL TIMING CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply across the specified operating ranges. Extended (E): V_{DD} = +2.7V to 5.5V, T_A = -40°C to +125°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Time	t_{CSLO}	5	—	—	µs	
$\overline{CS}$ High Time	t_{CSHI}	500	—	—	ns	
U/$\overline{D}$ to $\overline{CS}$ Hold Time	t_{LUC}	500	—	—	ns	
$\overline{CS}$ to U/$\overline{D}$ Low Setup Time	t_{LCUF}	500	—	—	ns	
$\overline{CS}$ to U/$\overline{D}$ High Setup Time	t_{LCUR}	3	—	—	µs	
U/$\overline{D}$ High Time	t_{HI}	500	—	—	ns	
U/$\overline{D}$ Low Time	t_{LO}	500	—	—	ns	
Up/$\overline{Down}$ Toggle Frequency	f_{UD}	—	—	1	MHz	
Wiper Settling Time	t_S	0.5	—	—	µs	2.1 kΩ, C_L = 100 pF
		1	—	—	µs	5 kΩ, C_L = 100 pF
		2	—	—	µs	10 kΩ, C_L = 100 pF
		10	5	—	µs	50 kΩ, C_L = 100 pF
Wiper Response on Power-up	t_{PU}	—	200	—	ns	
Internal EEPROM Write Time	twc	—	—	5	ms	@25°C
		—	—	10	ms	-40°C to +125°C

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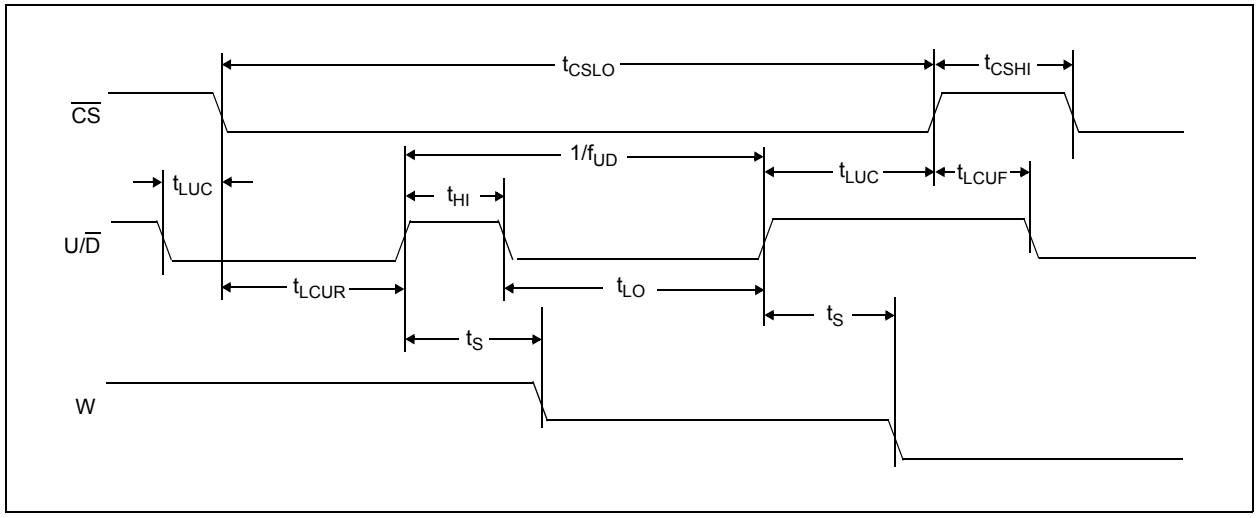

FIGURE 1-2: *Decrement Timing Waveform.*

SERIAL TIMING CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply across the specified operating ranges. Extended (E): V_{DD} = +2.7V to 5.5V, T_A = -40°C to +125°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Time	t_{CSLO}	5	—	—	µs	
$\overline{CS}$ High Time	t_{CSHI}	500	—	—	ns	
U/$\overline{D}$ to $\overline{CS}$ Hold Time	t_{LUC}	500	—	—	ns	
$\overline{CS}$ to U/$\overline{D}$ Low Setup Time	t_{LCUF}	500	—	—	ns	
$\overline{CS}$ to U/$\overline{D}$ High Setup Time	t_{LCUR}	3	—	—	µs	
U/$\overline{D}$ High Time	t_{HI}	500	—	—	ns	
U/$\overline{D}$ Low Time	t_{LO}	500	—	—	ns	
Up/$\overline{Down}$ Toggle Frequency	f_{UD}	—	—	1	MHz	
Wiper Settling Time	t_S	0.5	—	—	µs	2.1 kΩ, C_L = 100 pF
		1	—	—	µs	5 kΩ, C_L = 100 pF
		2	—	—	µs	10 kΩ, C_L = 100 pF
		10	5	—	µs	50 kΩ, C_L = 100 pF
Wiper Response on Power-up	t_{PU}	—	200	—	ns	
Internal EEPROM Write Time	twc	—	—	5	ms	@25°C
		—	—	10	ms	-40°C to +125°C

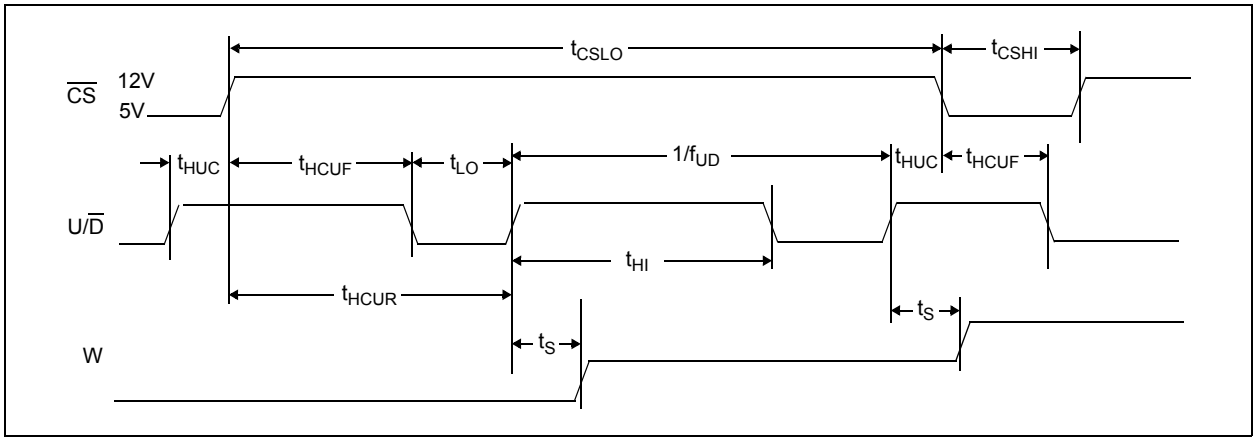

FIGURE 1-3: *High-Voltage Increment Timing Waveform.*

SERIAL TIMING CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply across the specified operating ranges. Extended (E): V_{DD} = +2.7V to 5.5V, T_A = -40°C to +125°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Time	t_{CSLO}	5	—	—	µs	
$\overline{CS}$ High Time	t_{CSHI}	500	—	—	ns	
U/$\overline{D}$ High Time	t_{HI}	500	—	—	ns	
U/$\overline{D}$ Low Time	t_{LO}	500	—	—	ns	
Up/$\overline{Down}$ Toggle Frequency	f_{UD}	—	—	1	MHz	
HV U/$\overline{D}$ to $\overline{CS}$ Hold Time	t_{HUC}	1.5	—	—	µs	
HV $\overline{CS}$ to U/$\overline{D}$ Low Setup Time	t_{HCUF}	8	—	—	µs	
HV $\overline{CS}$ to U/$\overline{D}$ High Setup Time	t_{HCUR}	4.5	—	—	µs	
Wiper Settling Time	t_S	0.5	—	—	µs	2.1 kΩ, C_L = 100 pF
		1	—	—	µs	5 kΩ, C_L = 100 pF
		2	—	—	µs	10 kΩ, C_L = 100 pF
		10	5	—	µs	50 kΩ, C_L = 100 pF
Wiper Response on Power-up	t_{PU}	—	200	—	ns	
Internal EEPROM Write Time	twc	—	—	5	ms	@25°C
		—	—	10	ms	-40°C to +125°C

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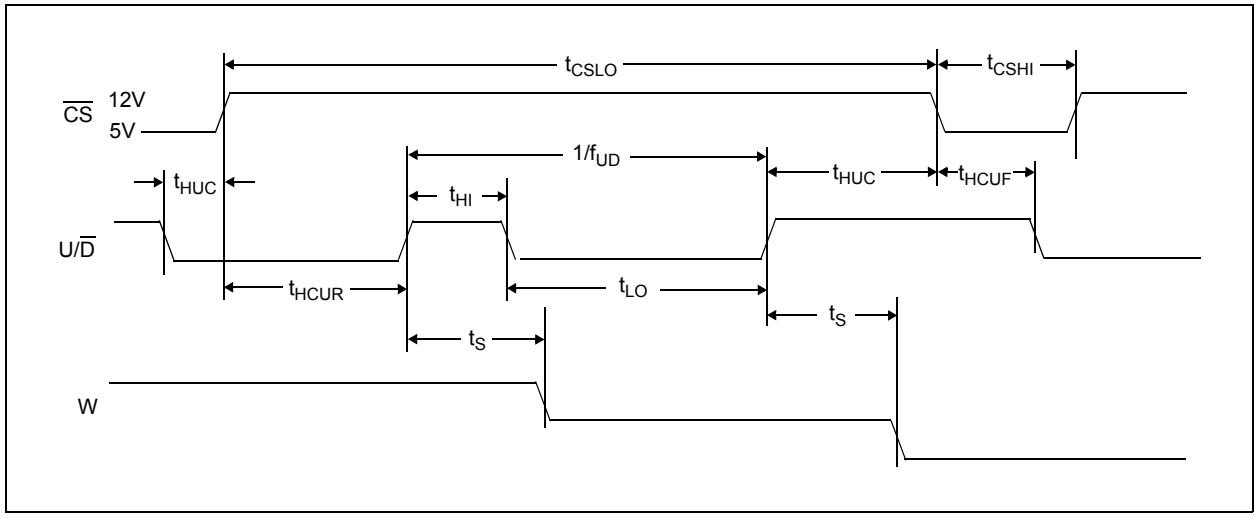

FIGURE 1-4: *High-Voltage Decrement Timing Waveform.*

SERIAL TIMING CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply across the specified operating ranges. Extended (E): V_{DD} = +2.7V to 5.5V, T_A = -40°C to +125°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Time	t_{CSLO}	5	—	—	µs	
$\overline{CS}$ High Time	t_{CSHI}	500	—	—	ns	
U/$\overline{D}$ High Time	t_{HI}	500	—	—	ns	
U/$\overline{D}$ Low Time	t_{LO}	500	—	—	ns	
Up/$\overline{Down}$ Toggle Frequency	f_{UD}	—	—	1	MHz	
HV U/$\overline{D}$ to $\overline{CS}$ Hold Time	t_{HUC}	1.5	—	—	µs	
HV $\overline{CS}$ to U/$\overline{D}$ Low Setup Time	t_{HCUF}	8	—	—	µs	
HV $\overline{CS}$ to U/$\overline{D}$ High Setup Time	t_{HCUR}	4.5	—	—	µs	
Wiper Settling Time	t_S	0.5	—	—	µs	2.1 kΩ, C_L = 100 pF
		1	—	—	µs	5 kΩ, C_L = 100 pF
		2	—	—	µs	10 kΩ, C_L = 100 pF
		10	5	—	µs	50 kΩ, C_L = 100 pF
Wiper Response on Power-up	t_{PU}	—	200	—	ns	
Internal EEPROM Write Time	twc	—	—	5	ms	@25°C
		—	—	10	ms	-40°C to +125°C

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	255	—	°C/W	
Thermal Resistance, 6L-SOT-23	θ_{JA}	—	230	—	°C/W	
Thermal Resistance, 8L-DFN (2x3)	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	117	—	°C/W	

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

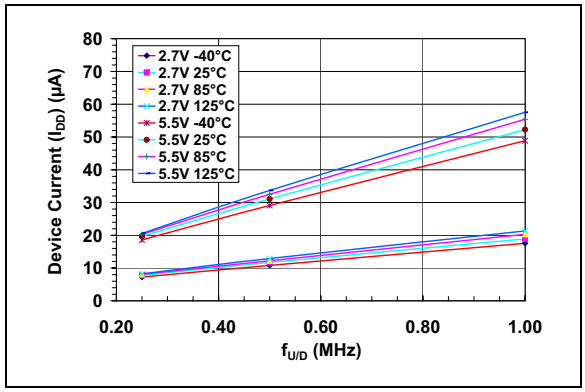

FIGURE 2-1: *Device Current (I_{DD}) vs. U/$\overline{D}$ Frequency ($f_{U/D}$) and Ambient Temperature (V_{DD} = 2.7V and 5.5V).*

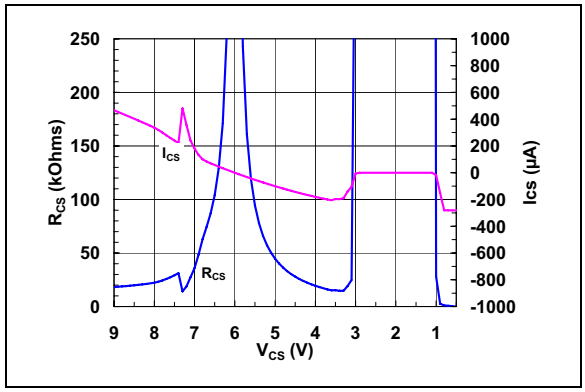

FIGURE 2-4: *$\overline{CS}$ Pull-up/Pull-down Resistance (R_{CS}) and Current (I_{CS}) vs. $\overline{CS}$ Input Voltage (V_{CS}) (V_{DD} = 5.5V).*

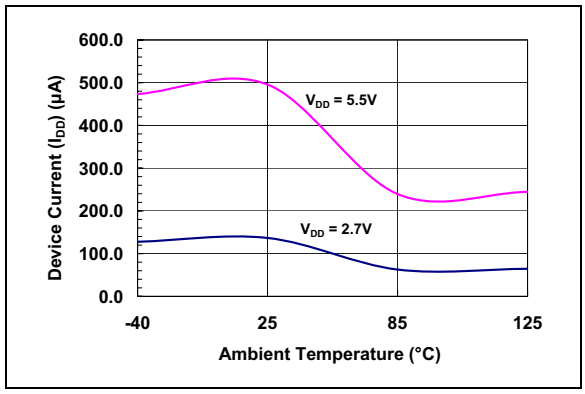

FIGURE 2-2: *Write Current (I_{WRITE}) vs. Ambient Temperature and V_{DD}.*

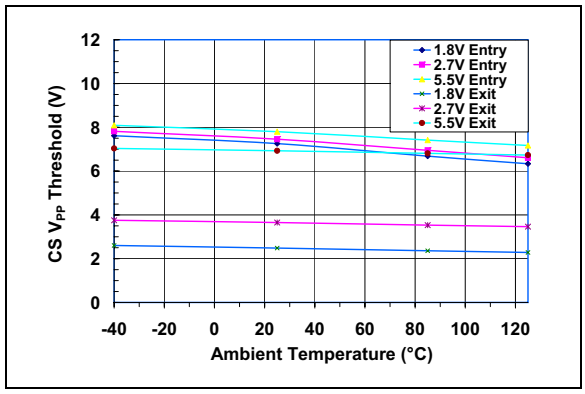

FIGURE 2-5: *$\overline{CS}$ High Input Entry/Exit Threshold vs. Ambient Temperature and V_{DD}.*

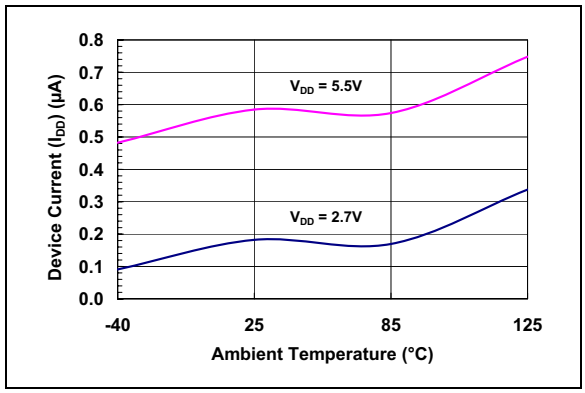

FIGURE 2-3: *Device Current (I_{SHDN}) vs. Ambient Temperature and V_{DD}. ($\overline{CS}$ = V_{DD}).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

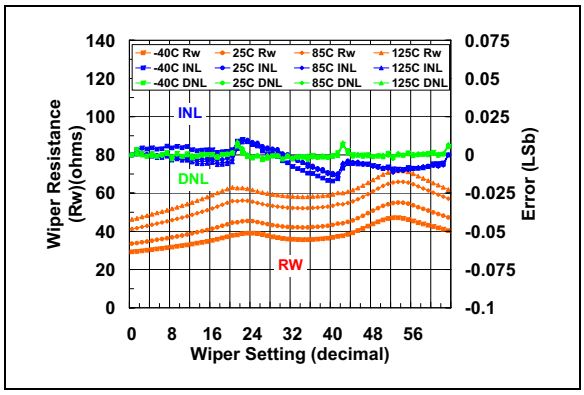

FIGURE 2-6: *2.1 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

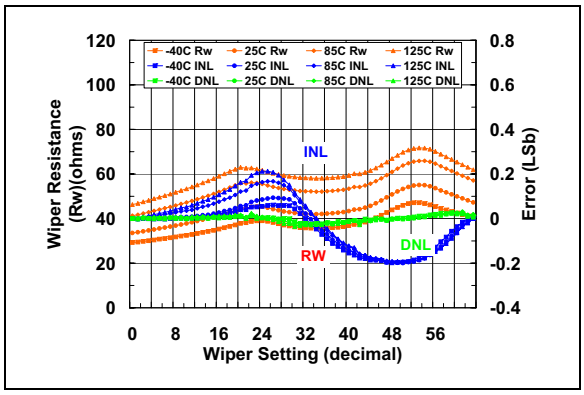

FIGURE 2-8: *2.1 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

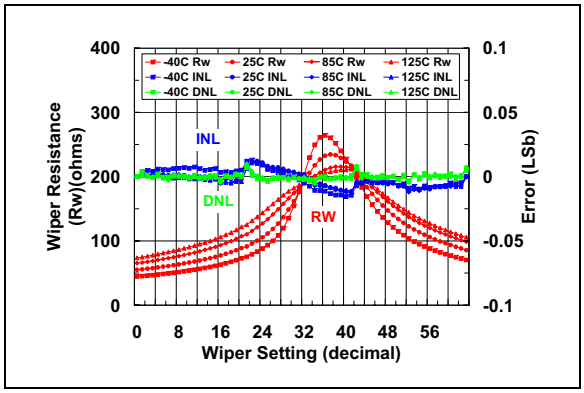

FIGURE 2-7: *2.1 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

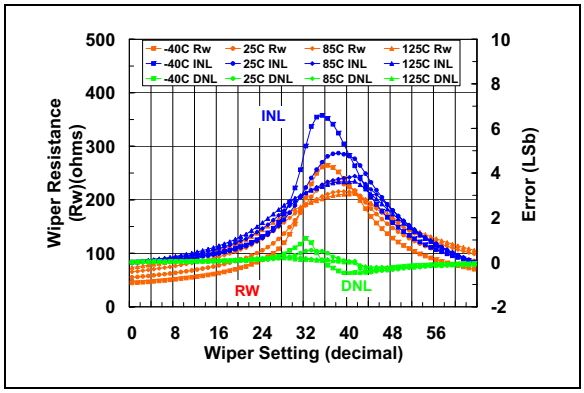

FIGURE 2-9: *2.1 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

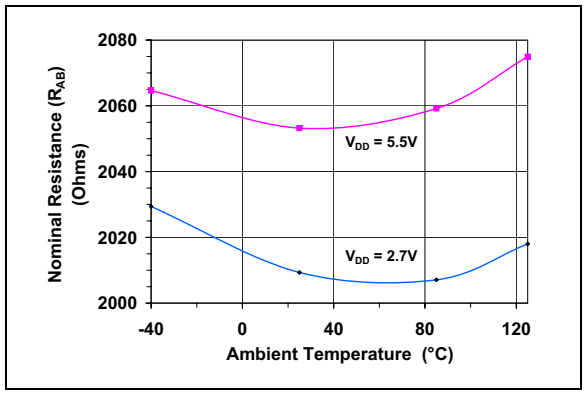

FIGURE 2-10: *2.1 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

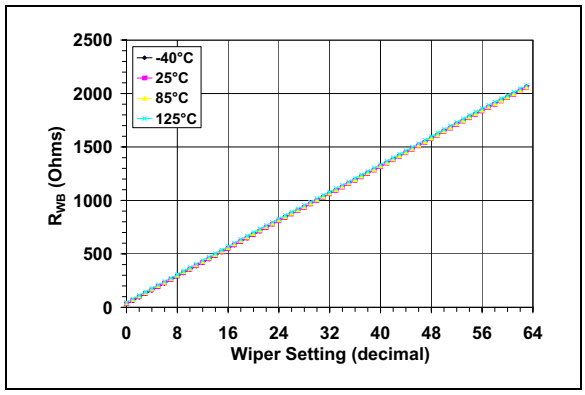

FIGURE 2-11: *2.1 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

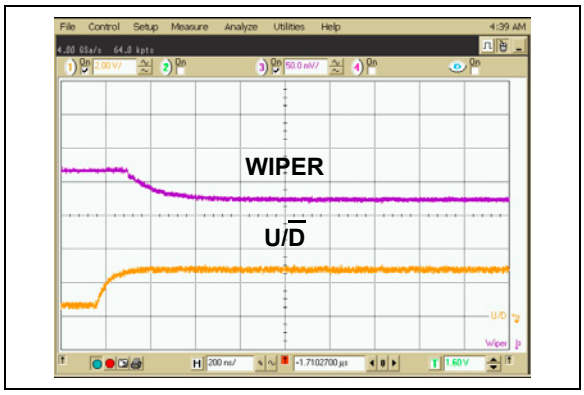

FIGURE 2-12: *2.1 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V).*

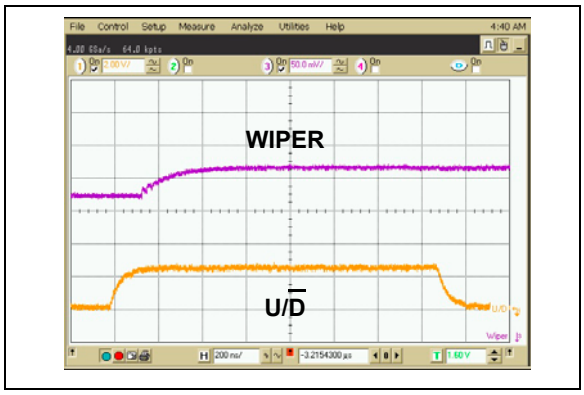

FIGURE 2-15: *2.1 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V).*

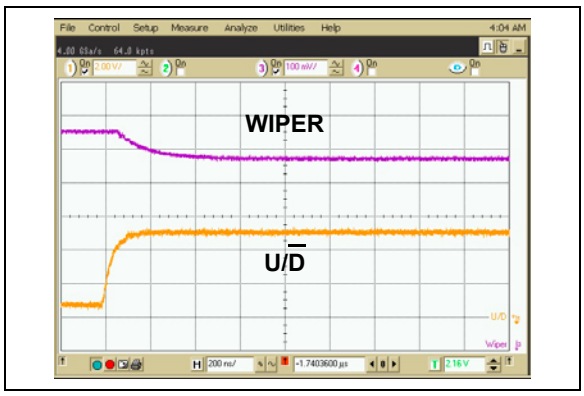

FIGURE 2-13: *2.1 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V).*

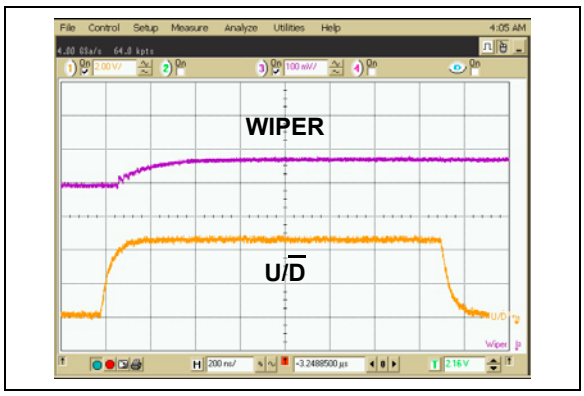

FIGURE 2-16: *2.1 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V).*

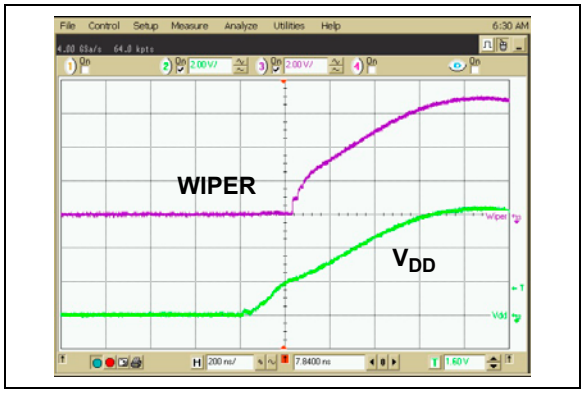

FIGURE 2-14: *2.1 kΩ – Power-Up Wiper Response Time.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

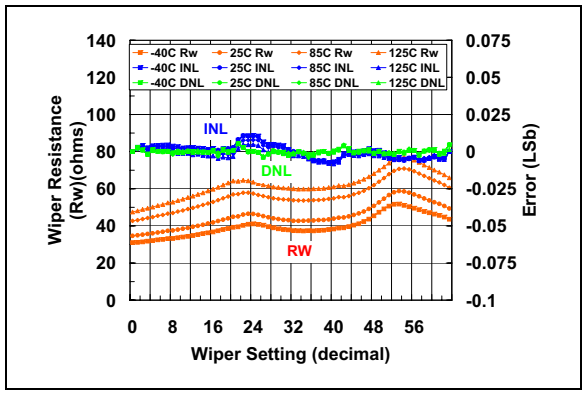

FIGURE 2-17: *5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

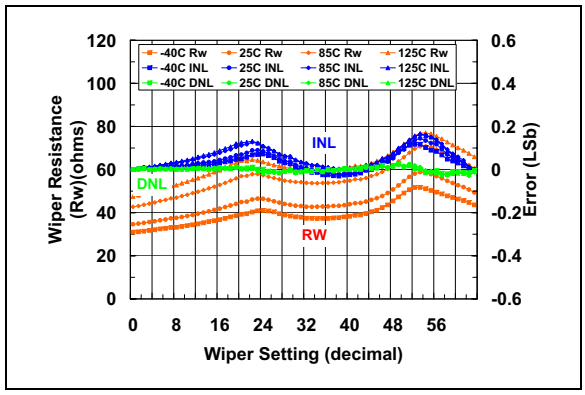

FIGURE 2-19: *5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V)*

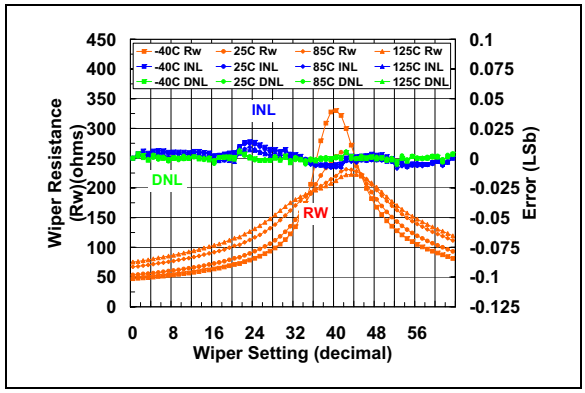

FIGURE 2-18: *5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

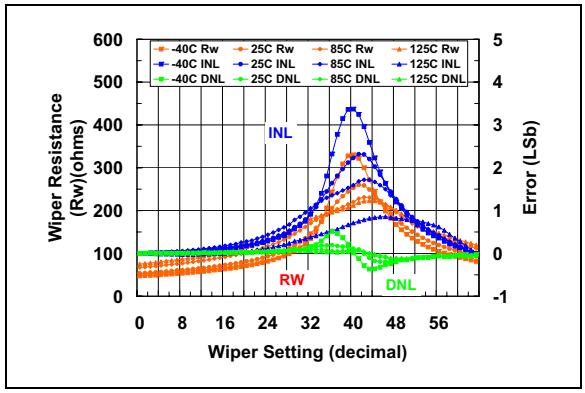

FIGURE 2-20: *5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

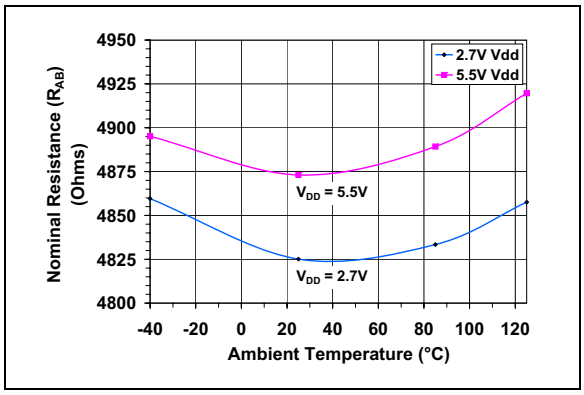

FIGURE 2-21: *5 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

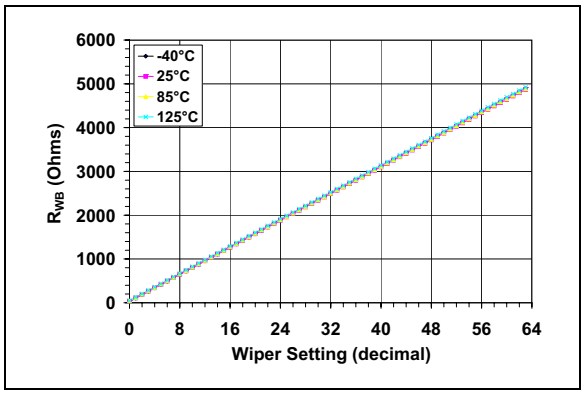

FIGURE 2-22: *5 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

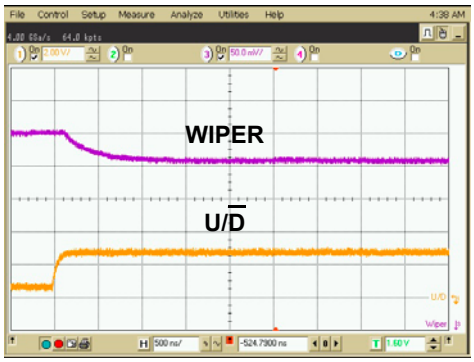

FIGURE 2-23: *5 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V).*

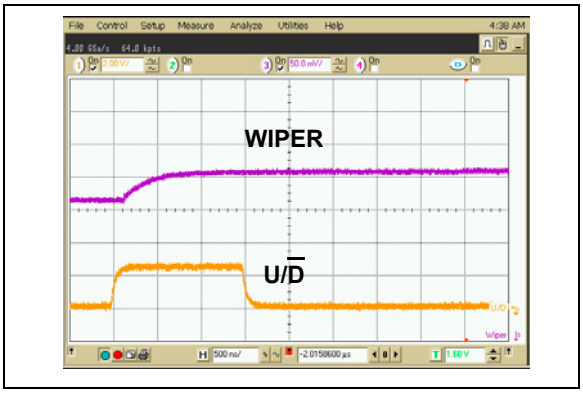

FIGURE 2-25: *5 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V).*

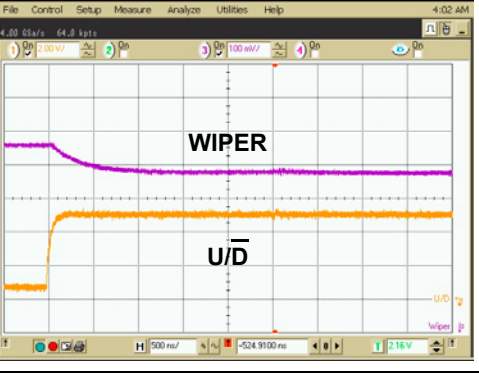

FIGURE 2-24: *5 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V).*

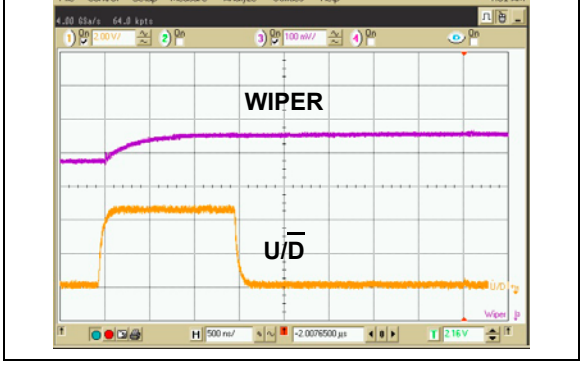

FIGURE 2-26: *5 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

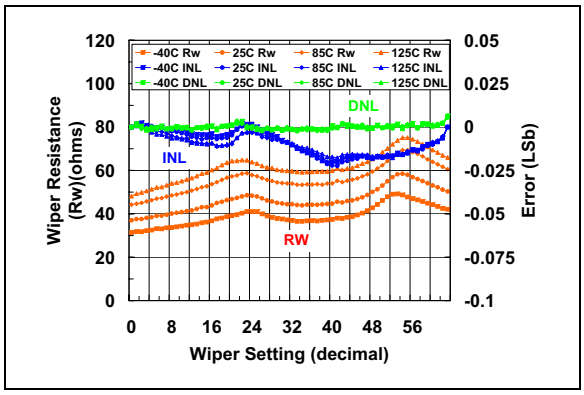

FIGURE 2-27: *10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

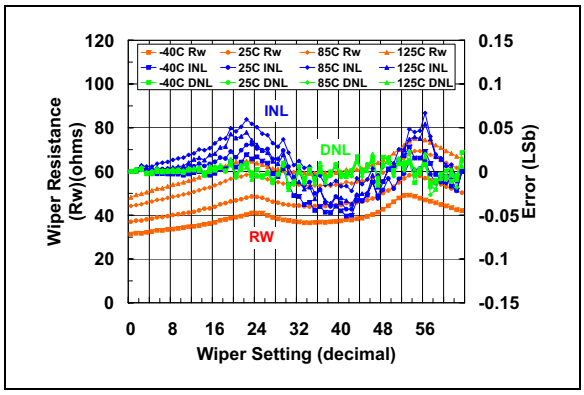

FIGURE 2-29: *10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

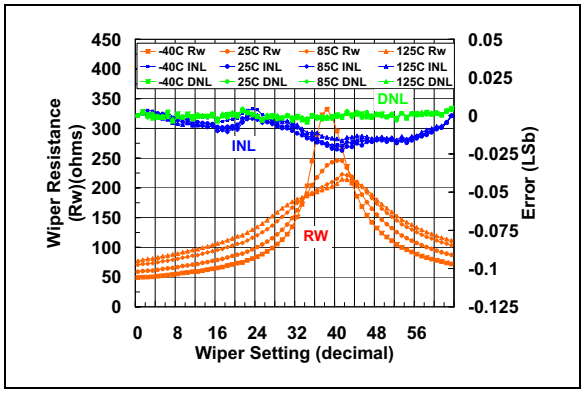

FIGURE 2-28: *10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

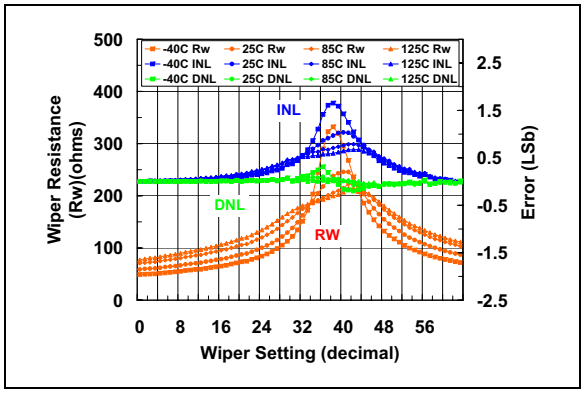

FIGURE 2-30: *10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

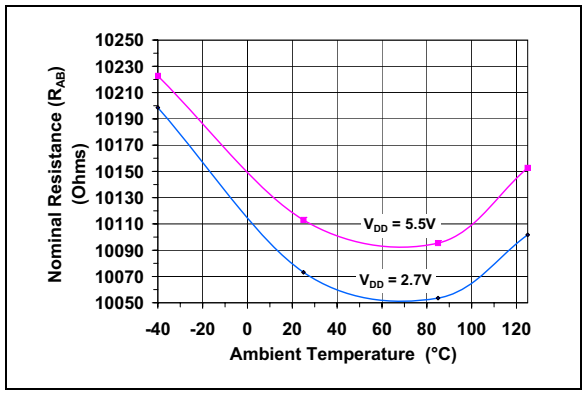

FIGURE 2-31: *10 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

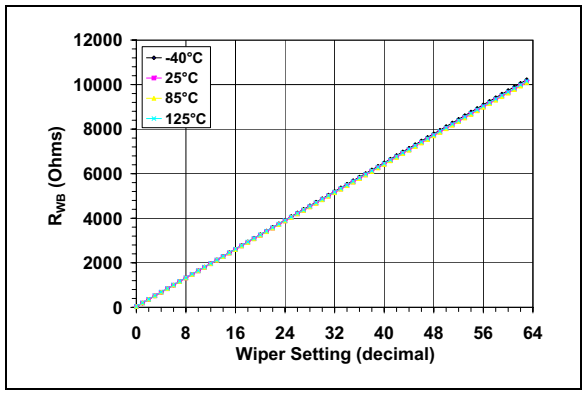

FIGURE 2-32: *10 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

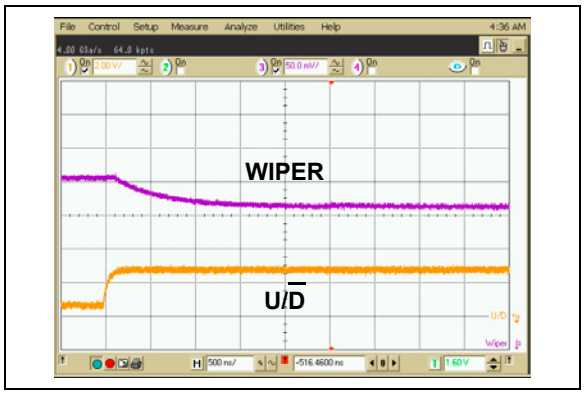

FIGURE 2-33: *10 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V).*

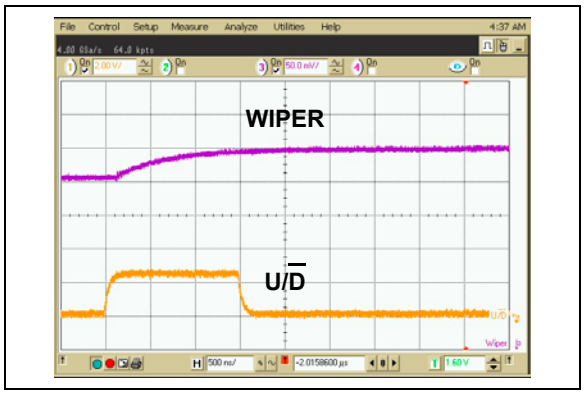

FIGURE 2-35: *10 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V).*

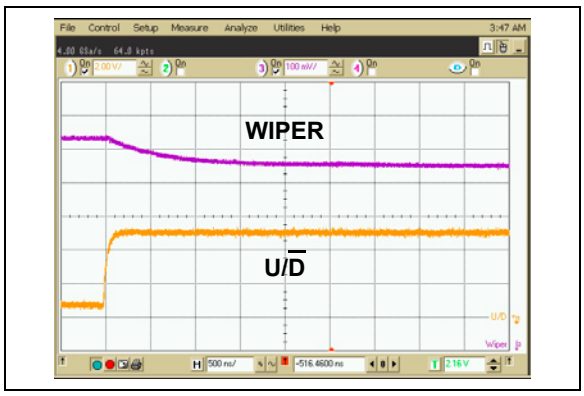

FIGURE 2-34: *10 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V).*

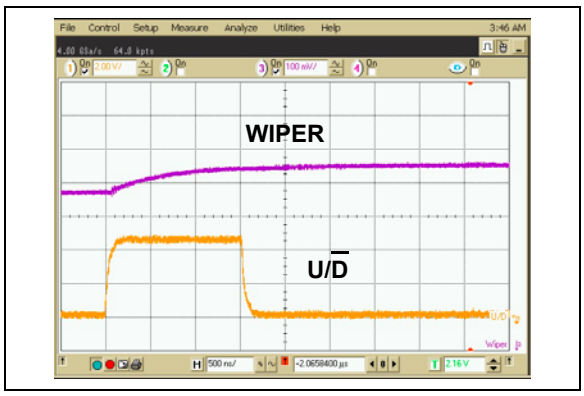

FIGURE 2-36: *10 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

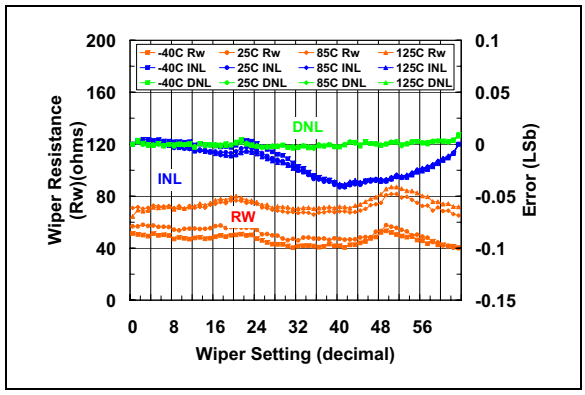

FIGURE 2-37: *50 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

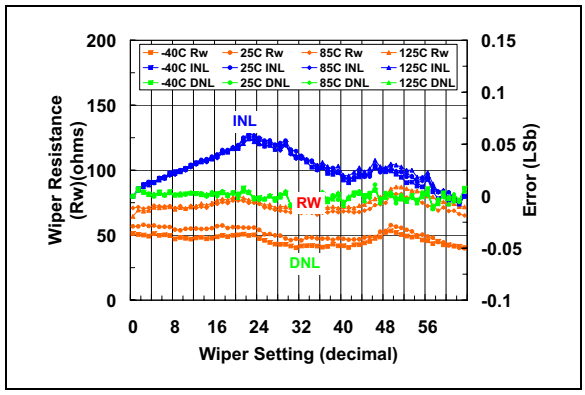

FIGURE 2-39: *50 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

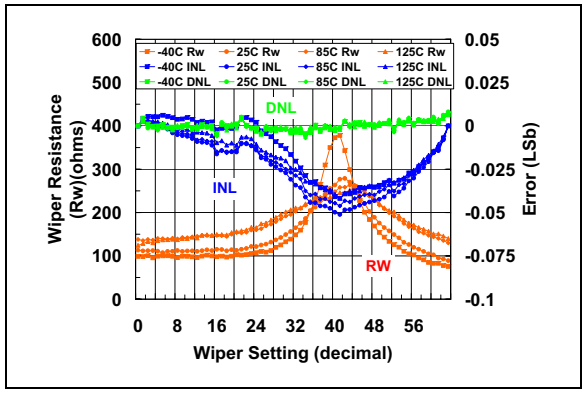

FIGURE 2-38: *50 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

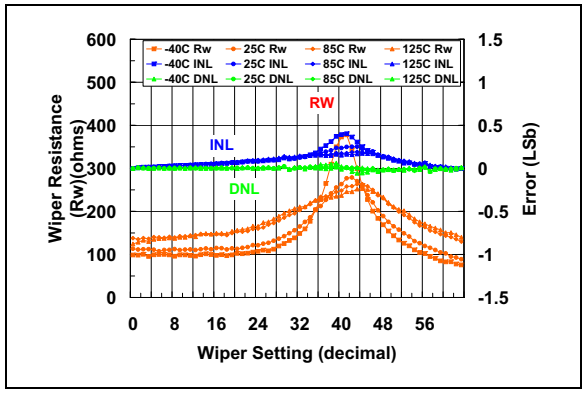

FIGURE 2-40: *50 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

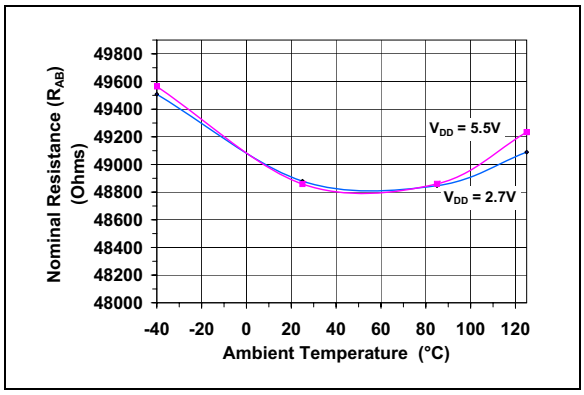

FIGURE 2-41: *50 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

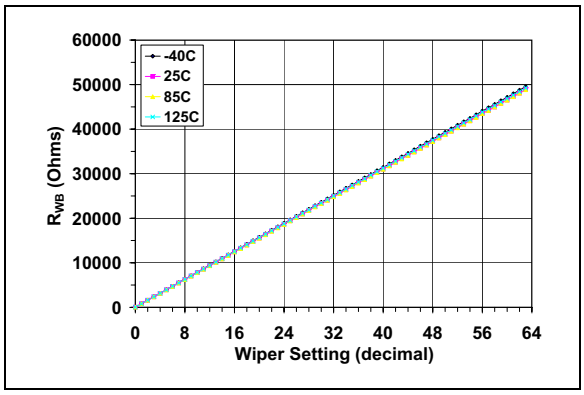

FIGURE 2-42: *50 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

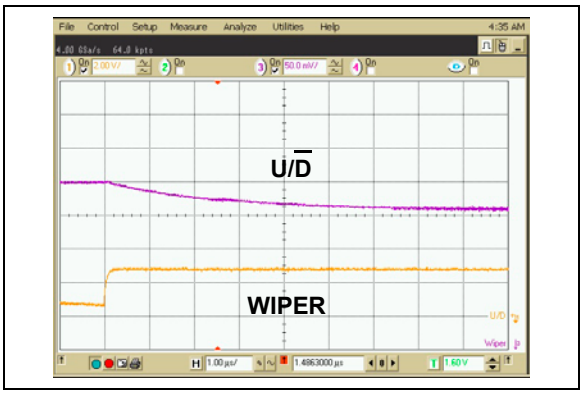

FIGURE 2-43: *50 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V).*

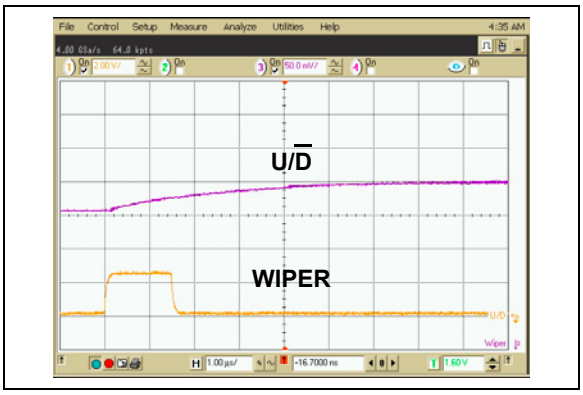

FIGURE 2-46: *50 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V).*

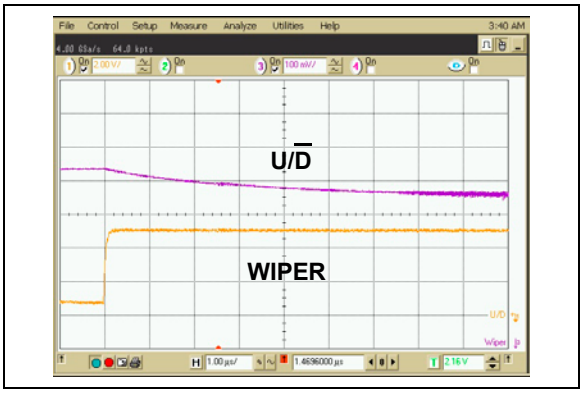

FIGURE 2-44: *50 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V).*

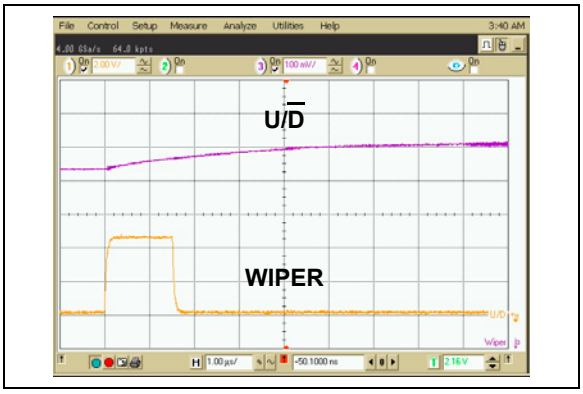

FIGURE 2-47: *50 kΩ - Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V).*

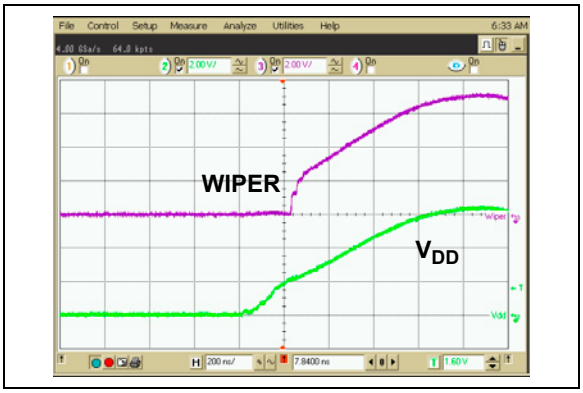

FIGURE 2-45: *50 kΩ – Power-Up Wiper Response Time.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

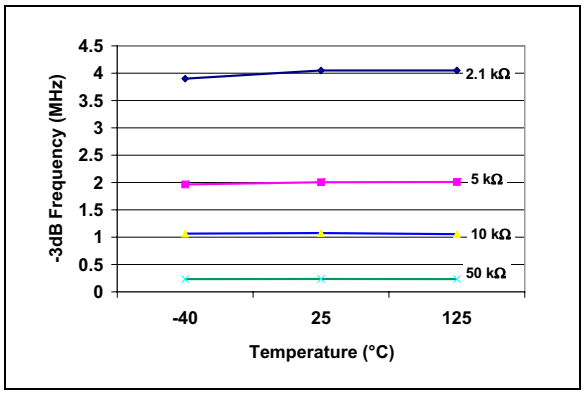

FIGURE 2-48: *-3 dB Bandwidth vs. Temperature.*

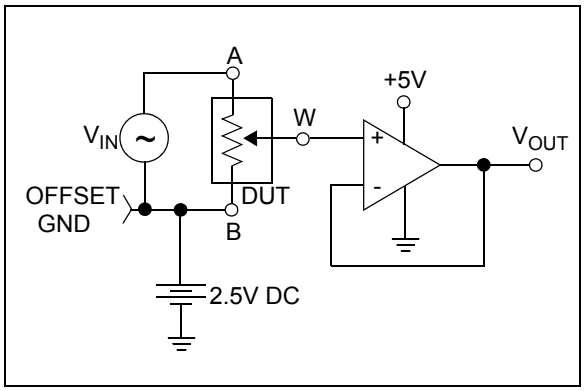

FIGURE 2-49: *-3 dB Bandwidth Test Circuit.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number			Symbol	Pin Type	Buffer Type	Function
MCP4021 (SOIC-8)	MCP4022 MCP4023 (SOT-23-6)	MCP4024 (SOT-23-5)				
1	1	1	V_{DD}	P	—	Positive Power Supply Input
2	2	2	V_{SS}	P	—	Ground
3	6	—	A	I/O	A	Potentiometer Terminal A
4	5	5	W	I/O	A	Potentiometer Wiper Terminal
5	4	4	$\overline{CS}$	I	TTL	Chip Select Input
6	—	—	B	I/O	A	Potentiometer Terminal B
7	—	—	NC	—	—	No Connection
8	3	3	U/$\overline{D}$	I	TTL	Increment/$\overline{\text{Decrement}}$ Input

Legend: TTL = TTL compatible input
A = Analog input
I = Input
O = Output
P = Power

3.1 Positive Power Supply Input (V_{DD})

The V_{DD} pin is the device's positive power supply input. The input power supply is relative to V_{SS} and can range from 2.7V to 5.5V. A decoupling capacitor on V_{DD} (to V_{SS}) is recommended to achieve maximum performance.

3.2 Ground (V_{SS})

The V_{SS} pin is the device ground reference.

3.3 Potentiometer Terminal A

The terminal A pin is connected to the internal potentiometer's terminal A (available on some devices). The potentiometer's terminal A is the fixed connection to the 0x3F terminal of the digital potentiometer.

The terminal A pin is available on the MCP4021, MCP4022 and MCP4023 devices. The terminal A pin does not have a polarity relative to the terminal W or B pins. The terminal A pin can support both positive and negative current. The voltage on teminal A must be between V_{SS} and V_{DD}.

The terminal A pin is not available on the MCP4024. The potentiometer's terminal A is internally floating.

3.4 Potentiometer Wiper (W) Terminal

The terminal W pin is connected to the internal potentiometer's terminal W (the wiper). The wiper terminal is the adjustable terminal of the digital potentiometer. The terminal W pin does not have a polarity relative to terminals A or B pins. The terminal W pin can support both positive and negative current. The voltage on teminal W must be between V_{SS} and V_{DD}.

3.5 Potentiometer Terminal B

The terminal B pin is connected to the internal potentiometer's terminal B (available on some devices). The potentiometer's terminal B is the fixed connection to the 0x00 terminal of the digital potentiometer.

The terminal B pin is available on the MCP4021 device. The terminal B pin does not have a polarity relative to the terminal W or A pins. The terminal B pin can support both positive and negative current. The voltage on teminal B must be between V_{SS} and V_{DD}.

The terminal B pin is not available on the MCP4022, MCP4023 and MCP4024 devices.

For the MCP4023 and MCP4024, the internal potentiometer's terminal B is internally connected to V_{SS}. Terminal B does not have a polarity relative to terminals W or A. Terminal B can support both positive and negative current.

For the MCP4022, terminal B is internally floating.

3.6 Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin is the chip select input. Forcing the $\overline{CS}$ pin to V_{IL} enables the serial commands. These commands can increment and decrement the wiper. Depending on the command, the wiper may (or may not) be saved to non-volatile memeory (EEPROM). Forcing the $\overline{CS}$ pin to V_{IHH} enables the high-voltage serial commands. These commands can increment and decrement the wiper and enable or disable the WiperLock technology. The wiper is saved to non-volatile memory (EEPROM).

The $\overline{CS}$ pin has an internal pull-up resistor. The resistor will become “disabled” when the voltage on the $\overline{CS}$ pin is below the V_{IH} level. This means that when the $\overline{CS}$ pin is “floating”, the $\overline{CS}$ pin will be pulled to the V_{IH} level (serial communication (the U/$\overline{D}$ pin) is ignored). And when the $\overline{CS}$ pin is driven low (V_{IL}), the resistance becomes very large to reduce the device current consumption when serial commands are occurring. See Figure 2-4 for additional information.

3.7 Increment/Decrement (U/$\overline{D}$)

The U/$\overline{D}$ pin input is used to increment or decrement the wiper on the digital potentiometer. An increment moves the wiper one step toward terminal A, while a decrement moves the wiper one step toward terminal B.

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4.0 GENERAL OVERVIEW

The MCP402X devices are general purpose digital potentiometers intended to be used in applications where a programmable resistance with moderate bandwidth is desired.

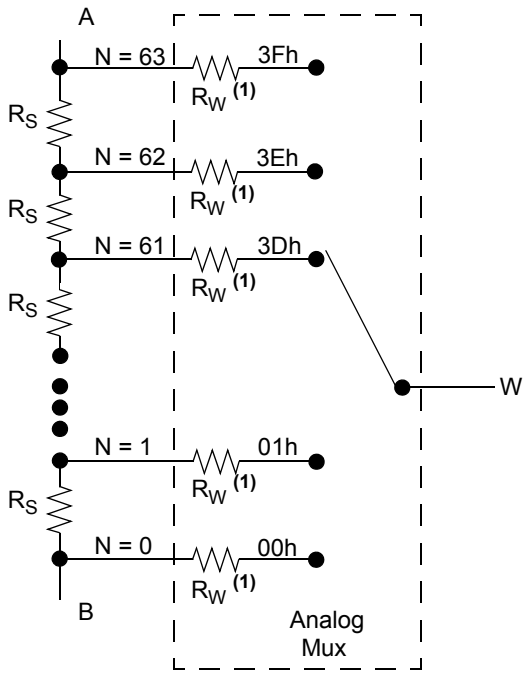
Applications generally suited for the MCP402X devices include:

- Set point or offset trimming
- Sensor calibration
- Selectable gain and offset amplifier designs
- Cost-sensitive mechanical trim pot replacement

The digital potentiometer is available in four nominal resistances (R_{AB}), where the nominal resistance is defined as the resistance between terminal A and terminal B. The four nominal resistances are 2.1 kΩ, 5 kΩ, 10 kΩ and 50 kΩ.

There are 63 resistors in a string between terminal A and terminal B. The wiper can be set to tap onto any of these 63 resistors thus providing 64 possible settings (including terminal A and terminal B).

Figure 4-1 shows a block diagram for the resistive network of the device. Equation 4-1 shows the calculation for the step resistance, while Equation 4-2 illustrates the calculation used to determine the resistance between the wiper and terminal B.



Note 1: The wiper resistance is tap dependent. That is, each tap selection resistance has a small variation. This variation effects the smaller resistance devices (2.1 kΩ) more.

FIGURE 4-1: *Resistor Block Diagram.*

EQUATION 4-1: R_S CALCULATION

$$R_S = \frac{R_{AB}}{63}$$

EQUATION 4-2: R_{WB} CALCULATION

$$R_{WB} = \frac{R_{AB}N}{63} + R_W$$

N = 0 to 63 (decimal)

1 LSb is the ideal resistance difference between two successive codes. If we use N = 1 and R_W = 0 in Equation 4-2, we can calculate the step size for each increment or decrement command.

The MCP4021 device offers a voltage divider (potentiometer) with all terminals available on pins.

The MCP4022 is a true rheostat, with terminal A and the wiper (W) of the variable resistor available on pins.

The MCP4023 device offers a voltage divider (potentiometer) with terminal B connected to ground.

The MCP4024 device is a rheostat device with terminal A of the resistor floating, terminal B connected to ground, and the wiper (W) available on pin.

The MCP4021 can be externally configured to implement any of the MCP4022, MCP4023 or MCP4024 configurations.

4.1 Serial Interface

A 2-wire synchronous serial protocol is used to increment or decrement the digital potentiometer's wiper terminal. The Increment/Decrement (U/$\overline{D}$) protocol utilizes the $\overline{CS}$ and U/$\overline{D}$ input pins. Both inputs are tolerant of signals up to 12.5V without damaging the device. The $\overline{CS}$ pin can differenciate between two high-voltage levels, V_{IH} and V_{IHH}. This enables additional commands without requiring additional input pins. The high-voltage commands (V_{IHH} on the $\overline{CS}$ pin) are similar to the standard commands, except that they control (enable, disable, ...) the state of the non-volatile WiperLock technolgy feature.

The simple U/$\overline{D}$ protocol uses the state of the U/$\overline{D}$ pin at the falling edge of the $\overline{CS}$ pin to determine if Increment or Decrement mode is desired. Subsequent rising edges of the U/$\overline{D}$ pin move the wiper.

The wiper value will not underflow or overflow. The new wiper setting can be saved to EEPROM, if desired, by selecting the state of the U/$\overline{D}$ pin during the rising edge of the $\overline{CS}$ pin.

The non-volatile wiper enables the MCP4021/2/3/4 to operate stand alone (without microcontroller control).

4.2 The WiperLock™ Technology

The MCP4021/2/3/4 device's WiperLock technology allows application-specific calibration settings to be secured in the EEPROM without requiring the use of an additional write-protect pin.

The WiperLock technology prevents the serial commands from doing the following:

- Incrementing or decrementing the wiper setting
- Writing the wiper setting to the non-volatile memory

Enabling and disabling the WiperLock technology feature requires high-voltage serial commands ($\overline{CS}$ = V_{IHH}). Incrementing and decrementing the wiper requires high-voltage commands when the feature is enabled. The high-voltage threshold (V_{IHH}) is intended to prevent the wiper setting from being altered by noise or intentional transitions on the U/$\overline{D}$ and $\overline{CS}$ pins, while still providing flexibility for production or calibration environments.

Both the $\overline{CS}$ and U/$\overline{D}$ input pins are tolerant of signals up to 12V. This allows the flexibility to multiplex the digital pot's control signals onto application signals for manufacturing/calibration.

4.3 Power-up

When the device powers up, the last saved wiper setting is restored.

While V_{DD} < V_{min} (2.7V), the electrical performance may not meet the data sheet specifications (see Figure 4-2). The wiper may be unknown or initialized to the value stored in the EEPROM. Also the device may be capable of incrementing, decrementing and writing to its EEPROM, if a valid command is detected on the $\overline{CS}$ and U/$\overline{D}$ pins.

The default settings of the MCP4021/2/3/4 device's from the factory are shown in Table 4-1.

TABLE 4-1: DEFAULT FACTORY SETTINGS SELECTION

Package Code	Default POR Wiper Setting	Wiper Code	WiperLock™ Technology Setting	Typical R_{AB} Value
-202	Mid-scale	1Fh	Disabled	2.1 kΩ
-502	Mid-scale	1Fh	Disabled	5.0 kΩ
-103	Mid-scale	1Fh	Disabled	10.0 kΩ
-503	Mid-scale	1Fh	Disabled	50.0 kΩ

It is good practice in your manufacturing flow to configure the device to your desired settings.

4.4 Brown Out

If the device V_{DD} is below the specified minimum voltage, care must be taken to ensure that the $\overline{CS}$ and U/$\overline{D}$ pins do not "create" any of the serial commands.

When the device V_{DD} drops below V_{min} (2.7V), the electrical performance may not meet the data sheet specifications (see Figure 4-2). The wiper may be unknown or initialized to the value stored in the EEPROM. Also the device may be capable of incrementing, decrementing and writing to its EEPROM if a valid command is detected on the $\overline{CS}$ and U/$\overline{D}$ pins.

4.5 Serial Interface Inactive

The serial interface is inactive any time the $\overline{CS}$ pin is at V_{IH} and all write cycles are completed.

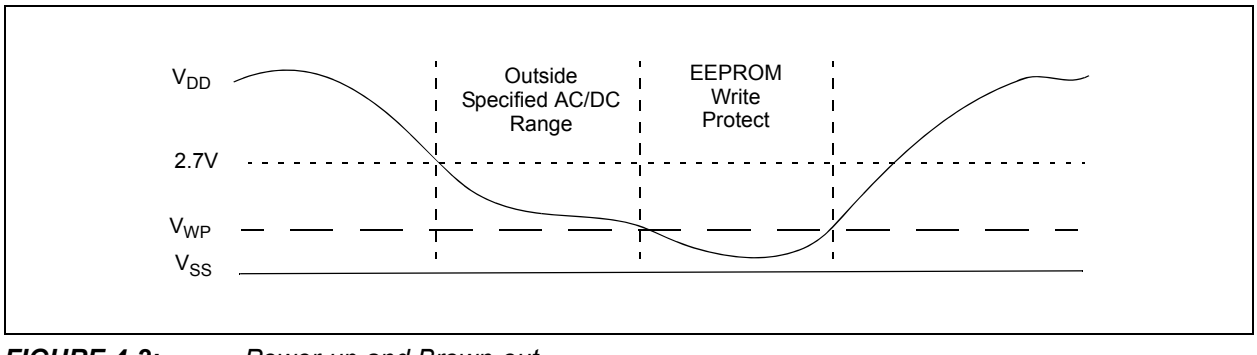


FIGURE 4-2: *Power-up and Brown-out.*

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5.0 SERIAL INTERFACE

5.1 Overview

The MCP4021/2/3/4 utilizes a simple 2-wire interface to increment or decrement the digital potentiometer's wiper terminal (W), store the wiper setting in non-volatile memory and turn the WiperLock technology feature on or off. This interface uses the Chip Select ($\overline{CS}$) pin, while the U/$\overline{D}$ pin is the Up/$\overline{Down}$ input.

The Increment/Decrement protocol enables the device to move one step at a time through the range of possible resistance values. The wiper value is initialized with the value stored in the internal EEPROM upon power-up. A wiper value of 00h connects the wiper to terminal B. A wiper value of 3Fh connects the wiper to terminal A. Increment commands move the wiper toward terminal A, but will not increment to a value greater than 3Fh. Decrement commands move the wiper toward terminal B, but will not decrement below 00h.

Refer to **Section 1.0 "Electrical Characteristics"**, AC/DC Electrical Characteristics table for detailed input threshold and timing specifications.

Communication is unidirectional. Therefore, the value of the current wiper setting cannot be read out of the MCP402X device.

5.2 Serial Commands

The MCP402X devices support 10 serial commands. The commands can be grouped into the following types:

- Serial Commands
- High-voltage Serial Commands

All the commands are shown in Table 5-1.

The command type is determined by the voltage level on the $\overline{CS}$ pin. The initial state that the $\overline{CS}$ pin must be driven is V_{IH}. From V_{IH}, the two levels that the $\overline{CS}$ pin can be driven are:

- V_{IL}
- V_{IHH}

If the $\overline{CS}$ pin is driven from V_{IH} to V_{IL}, a serial command is selected. If the $\overline{CS}$ pin is driven from V_{IH} to V_{IHH}, a high-voltage serial command is selected.

High-voltage serial commands control the state of the WiperLock technology. This is a unique feature, where the user can determine whether or not to "lock" or "unlock" the wiper state.

High-voltage serial commands increment/decrement the wiper regardless of the status of the WiperLock technology.

TABLE 5-1: COMMANDS

Command Name	Saves Wiper Value in EEPROM	High Voltage on $\overline{CS}$ pin?	After Command Wiper is "locked"/ "unlocked"	Works when Wiper is "locked"?
Increment without Writing Wiper Setting to EEPROM	—	—	unlocked	**Note 1**
Increment with Writing Wiper Setting to EEPROM	Yes	—	unlocked	**Note 1**
Decrement without Writing Wiper Setting to EEPROM	—	—	unlocked	**Note 1**
Decrement with Writing Wiper Setting to EEPROM	Yes	—	unlocked	**Note 1**
Write Wiper Setting to EEPROM	Yes	—	unlocked	**Note 1**
High-Voltage Increment and Disable WiperLock Technology	Yes	Yes	unlocked	Yes
High-Voltage Increment and Enable WiperLock Technology	Yes	Yes	locked	Yes
High-Voltage Decrement and Disable WiperLock Technology	Yes	Yes	unlocked	Yes
High-Voltage Decrement and Enable WiperLock Technology	Yes	Yes	locked	Yes
Write Wiper Setting to EEPROM and Disable WiperLock Technology	Yes	Yes	unlocked	Yes
Write Wiper Setting to EEPROM and Enable WiperLock Technology	Yes	Yes	locked	Yes

Note 1: This command will only complete if wiper is "unlocked" (WiperLock Technology is Disabled).

5.2.1 INCREMENT WITHOUT WRITING WIPER SETTING TO EEPROM

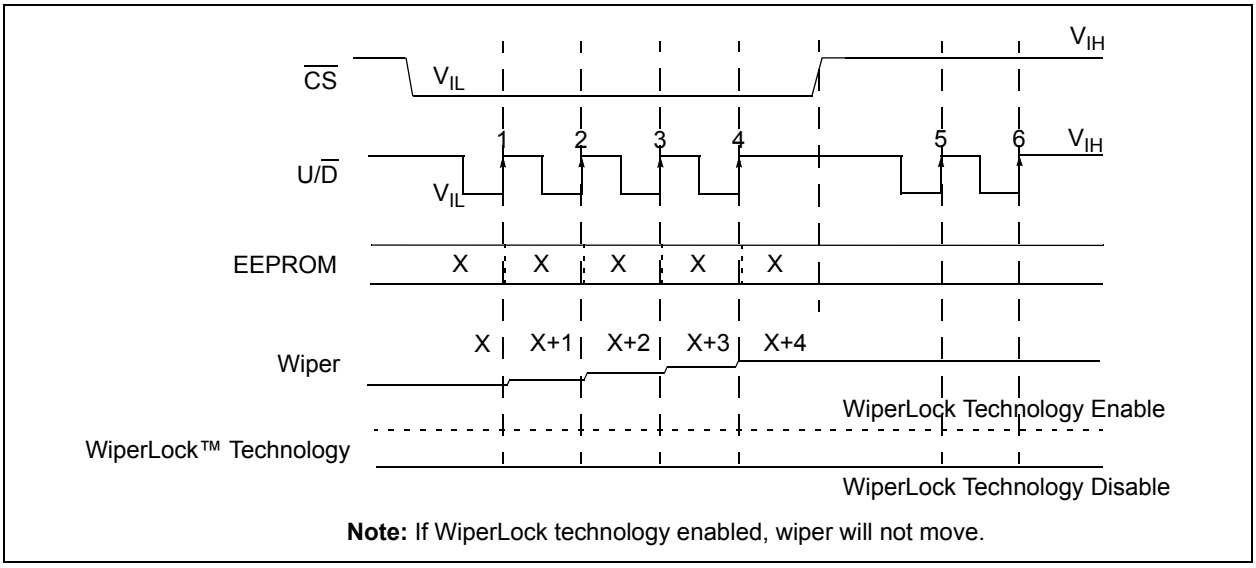
This mode is achieved by initializing the U/$\overline{D}$ pin to a high state (V_{IH}) prior to achieving a low state (V_{IL}) on the $\overline{CS}$ pin. Subsequent rising edges of the U/$\overline{D}$ pin increment the wiper setting toward terminal A. This is shown in Figure 5-1.

After the wiper is incremented to the desired position, the $\overline{CS}$ pin should be forced to V_{IH} to ensure that "unexpected" transitions (on the U/$\overline{D}$ pin do not cause the wiper setting to increment. Driving the $\overline{CS}$ pin to V_{IH} should occur as soon as possible (within device specifications) after the last desired increment occurs.

The EEPROM value has not been updated to this new wiper value, so if the device voltage is lowered below the RAM retention voltage of the device, once the device returns to the operating range, the wiper will be loaded with the wiper setting in the EEPROM.

After the $\overline{CS}$ pin is driven to V_{IH} (from V_{IL}), any other serial command may immediately be entered. This is since an EEPROM write cycle (t_{WC}) is not active.

Note:	The wiper value will not overflow. That is, once the wiper value equals 0x3F, subsequent increment commands are ignored.



Note: If WiperLock technology enabled, wiper will not move.

FIGURE 5-1: *Increment without Writing Wiper Setting to EEPROM.*

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5.2.2 INCREMENT WITH WRITING WIPER SETTING TO EEPROM

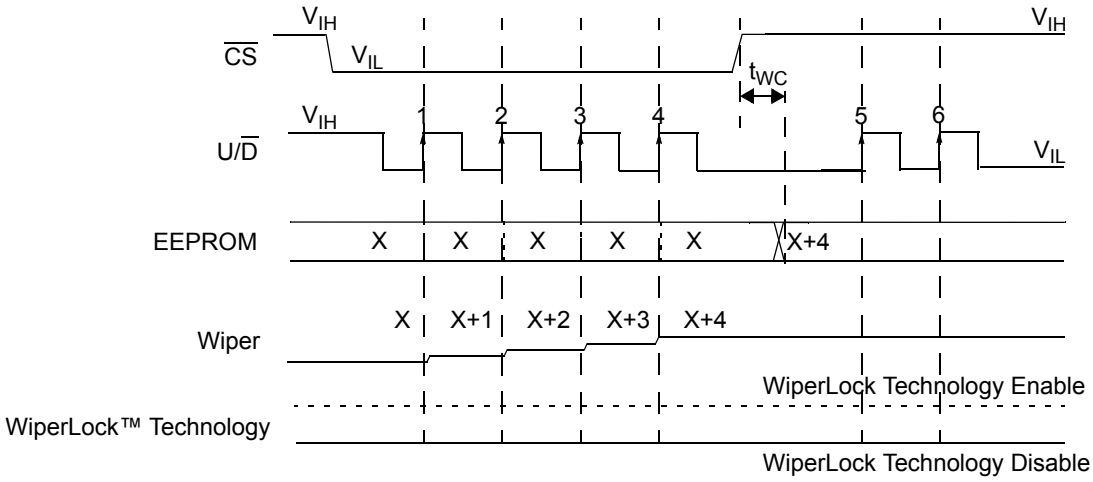
This mode is achieved by initializing the U/$\overline{D}$ pin to a high state (V_{IH}) prior to achieving a low state (V_{IL}) on the $\overline{CS}$ pin. Subsequent rising edges of the U/$\overline{D}$ pin increment the wiper setting toward terminal A. This is shown in Figure 5-2.

After the wiper is incremented to the desired position, the U/$\overline{D}$ pin should be driven low (V_{IL}). Then when the $\overline{CS}$ pin is forced to V_{IH}, the wiper value is written to the EEPROM. Therefore, if the device voltage is lowered below the RAM retention voltage of the device, once the device returns to the operating range, the wiper will be loaded with this wiper setting (stored in the EEPROM).

To ensure that "unexpected" transitions on the U/$\overline{D}$ pin do not cause the wiper setting to increment, the U/$\overline{D}$ pin should be driven low and the $\overline{CS}$ pin forced to V_{IH} as soon as possible (within device specifications) after the last desired increment occurs.

After the $\overline{CS}$ pin is driven to V_{IH} (from V_{IL}), all other serial commands are ignored until the EEPROM write cycle (t_{wc}) completes.

Note:	The wiper value will not overflow. That is, once the wiper value equals 0x3F, subsequent increment commands are ignored.



Note: If WiperLock technology enabled, wiper will not move.

FIGURE 5-2: *Increment with Writing Wiper Setting to EEPROM.*

5.2.3 DECREMENT WITHOUT WRITING WIPER SETTING TO EEPROM

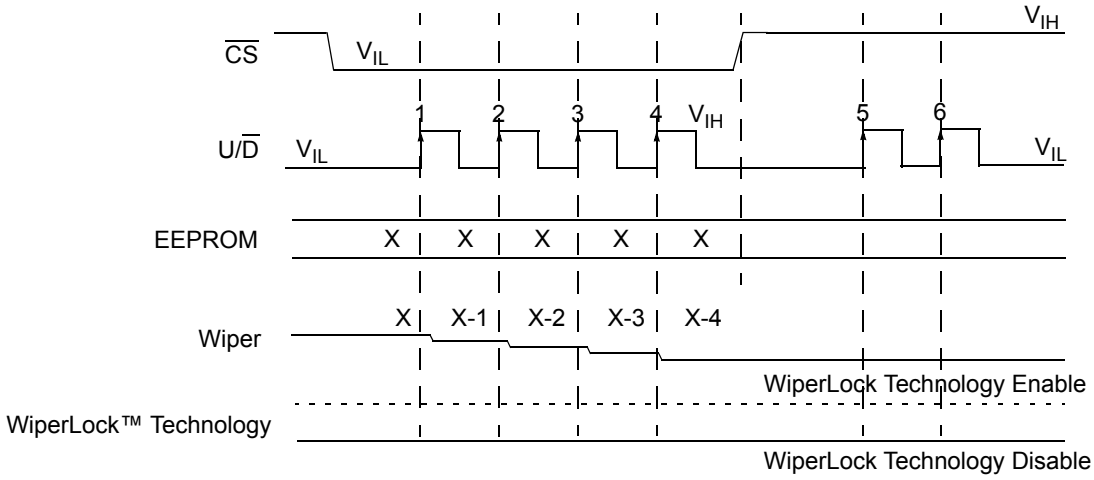
This mode is achieved by initializing the U/$\overline{D}$ pin to a low state (V_{IL}) prior to achieving a low state (V_{IL}) on the $\overline{CS}$ pin. Subsequent rising edges of the U/$\overline{D}$ pin will decrement the wiper setting toward terminal B. This is shown in Figure 5-3.

After the wiper is decremented to the desired position, the U/$\overline{D}$ pin should be forced low (V_{IL}) and the $\overline{CS}$ pin should be forced to V_{IH}. This will ensure that "unexpected" transitions on the U/$\overline{D}$ pin do not cause the wiper setting to decrement. Driving the $\overline{CS}$ pin to V_{IH} should occur as soon as possible (within device specifications) after the last desired increment occurs.

The EEPROM value has not been updated to this new wiper value, so, if the device voltage is lowered below the RAM retention voltage of the device, once the device returns to the operating range, the wiper will be loaded with the wiper setting in the EEPROM.

After the $\overline{CS}$ pin is driven to V_{IH} (from V_{IL}), any other serial command may immediately be entered, since an EEPROM write cycle (t_{WC}) is not started.

Note:	The wiper value will not underflow. That is, once the wiper value equals 0x00, subsequent decrement commands are ignored.



Note: If WiperLock technology enabled, wiper will not change.

FIGURE 5-3: *Decrement without Writing Wiper Setting to EEPROM.*

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5.2.4 DECREMENT WITH WRITING WIPER SETTING TO EEPROM

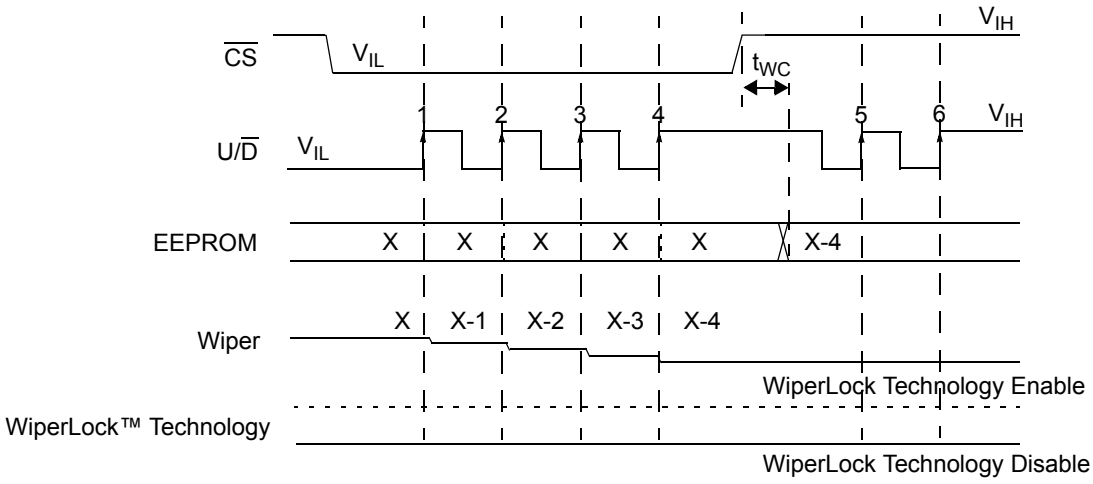
This mode is achieved by initializing the U/$\overline{D}$ pin to a low state (V_{IL}) prior to achieving a low state (V_{IL}) on the $\overline{CS}$ pin. Subsequent rising edges of the U/$\overline{D}$ pin decrement the wiper setting (toward terminal B). This is shown in Figure 5-4.

After the wiper is decremented to the desired position, the U/$\overline{D}$ pin should remain high (V_{IH}). Then when the $\overline{CS}$ pin is raised to V_{IH}, the wiper value is written to the EEPROM. Therefore, if the device voltage is lowered below the RAM retention voltage of the device, once the device returns to the operating range, the wiper will be loaded with this wiper setting (stored in the EEPROM).

To ensure that "unexpected" transitions on the U/$\overline{D}$ pin do not cause the wiper setting to decrement, the U/$\overline{D}$ pin should be driven low (V_{IL}) and the $\overline{CS}$ pin forced to V_{IH} as soon as possible (within device specifications) after the last desired increment occurs.

After the $\overline{CS}$ pin is driven to V_{IH} (from V_{IL}), all other serial commands are ignored until the EEPROM write cycle (t_{WC}) completes.

Note:	The wiper value will not underflow. That is, once the wiper value equals 0x00, subsequent decrement commands are ignored.



Note: If WiperLock technology enabled, wiper will not change.

FIGURE 5-4: *Decrement with Writing Wiper Setting to EEPROM.*

5.2.5 WRITE WIPER SETTING TO EEPROM

To write the current wiper setting to EEPROM, force both the $\overline{CS}$ pin and U/$\overline{D}$ pin to V_{IH}. Then force the $\overline{CS}$ pin to V_{IL}. Before there is a rising edge on the U/$\overline{D}$ pin, force the $\overline{CS}$ pin to V_{IH}. This causes the wiper setting value to be written to EEPROM.

Note:	After the U/$\overline{D}$ pin is forced to V_{IL}, each rising edge on the U/$\overline{D}$ pin will cause the wiper to increment. This is the same command as the "**Increment with Writing Wiper Setting to EEPROM**" command, but the U/$\overline{D}$ pin is held at V_{IL}, so the wiper is not incremented.

When the $\overline{CS}$ pin is forced to V_{IH}, the wiper value is written to the EEPROM. Therefore, if the device voltage is lowered below the RAM retention voltage of the device, once the device returns to the operating range, the wiper will be loaded with this wiper setting (stored in the EEPROM).

To ensure that "unexpected" transitions on the U/$\overline{D}$ pin do not cause the wiper setting to increment, force the $\overline{CS}$ pin to V_{IH} as soon as possible (within device specifications) after the U/$\overline{D}$ pin is forced to V_{IL}.

After the $\overline{CS}$ pin is driven to V_{IH} (from V_{IL}), all other serial commands are ignored until the EEPROM write cycle (t_{WC}) completes.

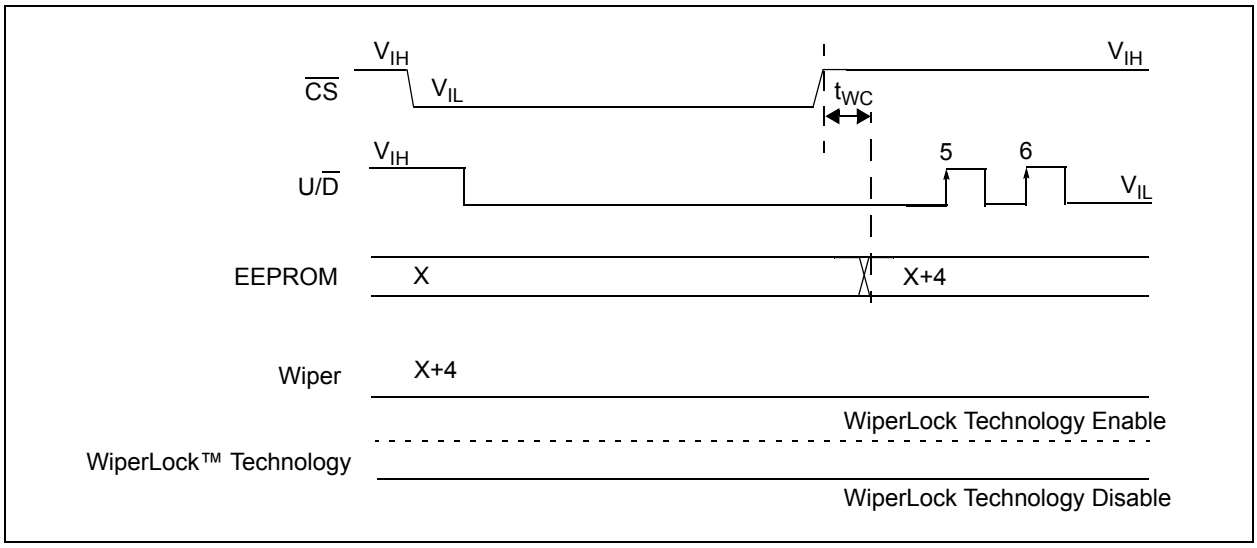


FIGURE 5-5: *Write Wiper Setting to EEPROM.*

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5.2.6 HIGH-VOLTAGE INCREMENT AND DISABLE WiperLock TECHNOLOGY

This mode is achieved by initializing the U/$\overline{D}$ pin to a high state (V_{IH}) prior to the $\overline{CS}$ pin being driven to V_{IHH}. Subsequent rising edges of the U/$\overline{D}$ pin increment the wiper setting toward terminal A. Set the U/$\overline{D}$ pin to the high state (V_{IH}) prior to forcing the $\overline{CS}$ pin to V_{IH}. This begins a write cycle and disables the WiperLock Technology feature (See Figure 5-6).

After the $\overline{CS}$ pin is driven to V_{IH} (from V_{IHH}), all other serial commands are ignored until the EEPROM write cycle (t_{WC}) completes.

Note:	The wiper value will not overflow. That is, once the wiper value equals 0x3F, subsequent increment commands are ignored.

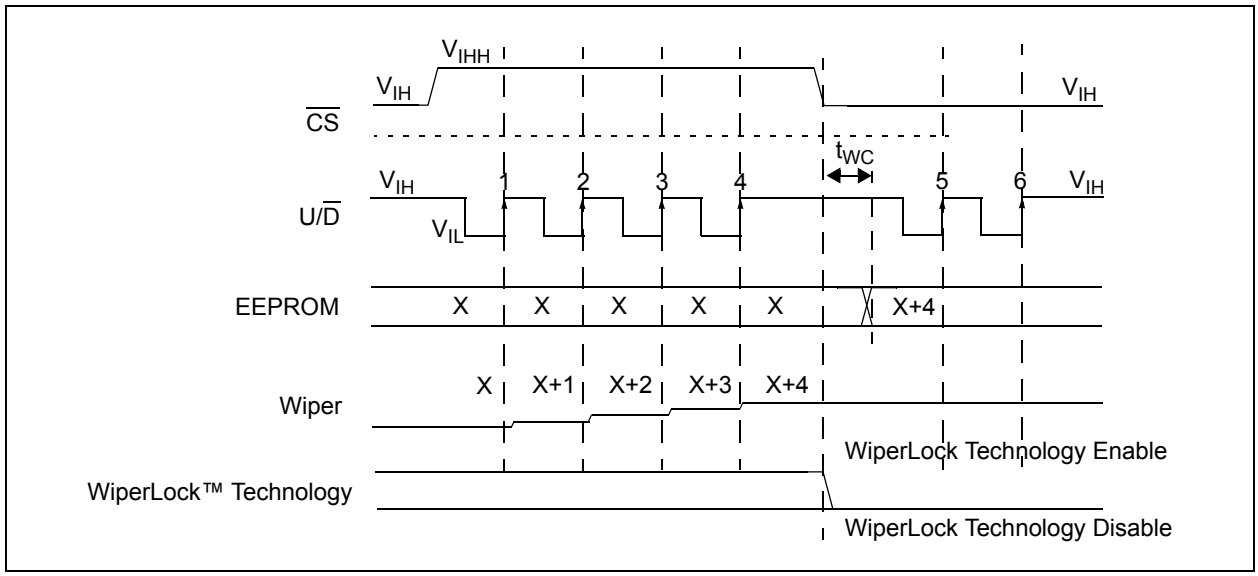

FIGURE 5-6: *High-Voltage Increment and Disable WiperLock™ Technology.*

5.2.7 HIGH-VOLTAGE INCREMENT AND ENABLE WiperLock TECHNOLOGY

This mode is achieved by initializing the U/$\overline{D}$ pin to a high state (V_{IH}) prior to the $\overline{CS}$ pin being driven to V_{IHH}. Subsequent rising edges of the U/$\overline{D}$ pin increment the wiper setting toward terminal A. Set the U/$\overline{D}$ pin to the low state (V_{IL}) prior to forcing the $\overline{CS}$ pin to V_{IH}. This begins a write cycle and enables the WiperLock Technology feature (See Figure 5-7).

After the $\overline{CS}$ pin is driven to V_{IH} (from V_{IHH}), all other serial commands are ignored until the EEPROM write cycle (t_{WC}) completes.

Note:	The wiper value will not overflow. That is, once the wiper value equals 0x3F, subsequent increment commands are ignored.

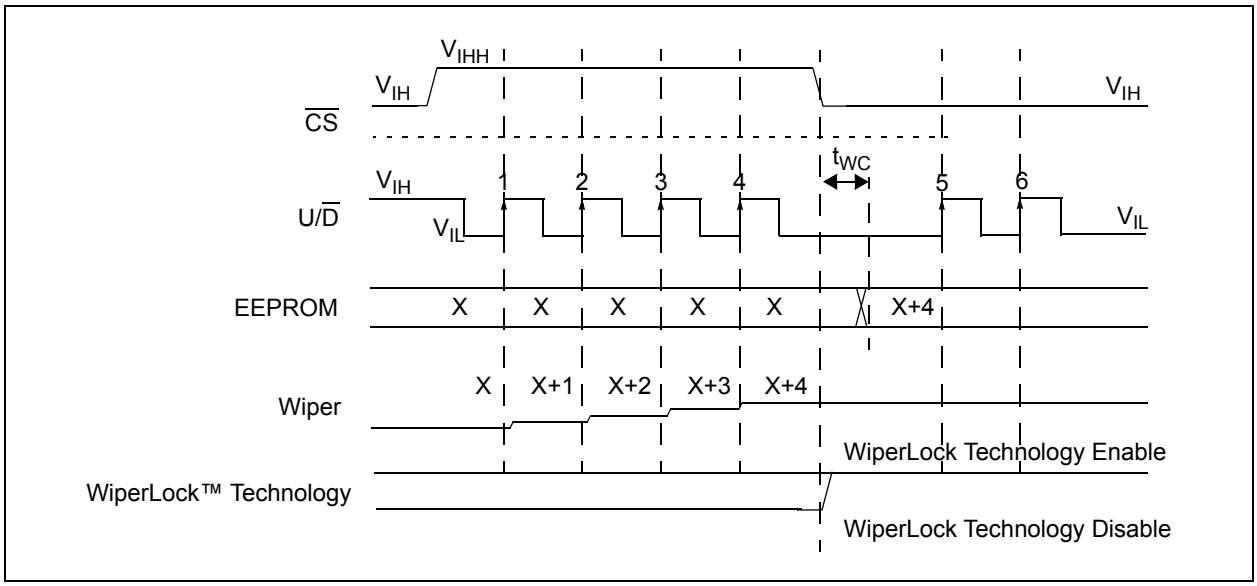

FIGURE 5-7: *High-Voltage Increment and Enable WiperLock™ Technology.*

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5.2.8 HIGH-VOLTAGE DECREMENT AND DISABLE WiperLock TECHNOLOGY

This mode is achieved by initializing the U/$\overline{D}$ pin to a low state (V_{IL}) prior to the $\overline{CS}$ pin being driven to V_{IHH}. Subsequent rising edges of the U/$\overline{D}$ pin decrement the wiper setting toward terminal B. Set the U/$\overline{D}$ pin to the low state (V_{IL}) prior to forcing the $\overline{CS}$ pin to V_{IH}. This begins a write cycle and disables the WiperLock Technology feature (See Figure 5-8).

After the $\overline{CS}$ pin is driven to V_{IH} (from V_{IHH}), all other serial commands are ignored until the EEPROM write cycle (t_{WC}) completes.

Note:	The wiper value will not underflow. That is, once the wiper value equals 0x00, subsequent decrement commands are ignored.

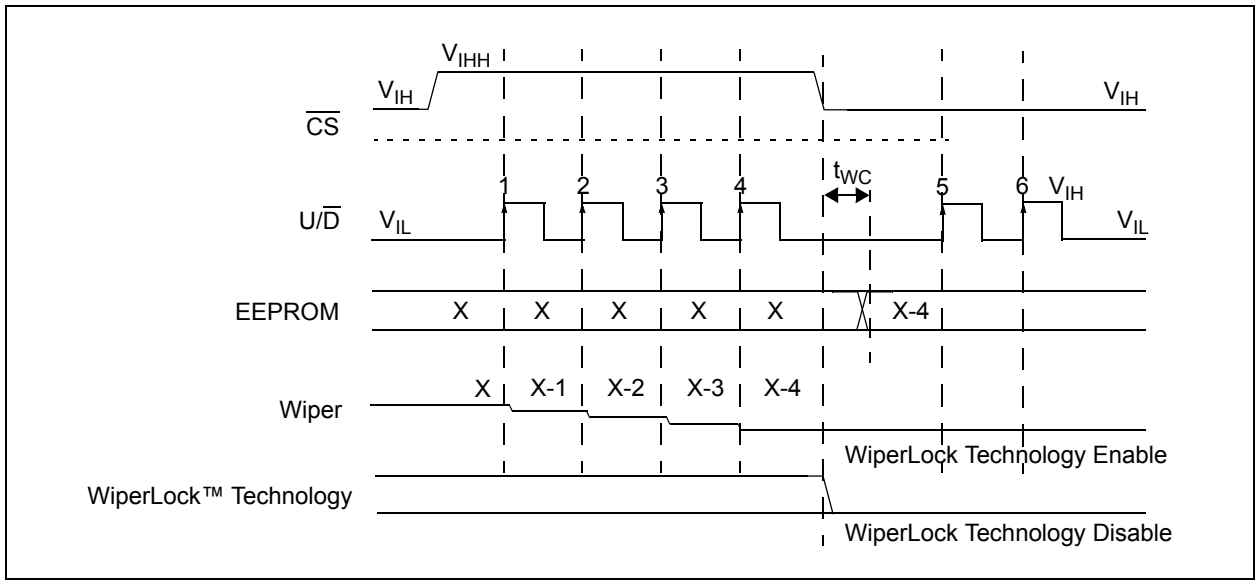

FIGURE 5-8: *High-Voltage Decrement and Disable WiperLock™ Technology.*

5.2.9 HIGH-VOLTAGE DECREMENT AND ENABLE WiperLock TECHNOLOGY

This mode is achieved by initializing the U/$\overline{D}$ pin to the low state (V_{IL}) prior to driving the $\overline{CS}$ pin to V_{IHH}. Subsequent rising edges of the U/$\overline{D}$ pin decrement the wiper setting toward terminal B. Set the U/$\overline{D}$ pin to a high state (V_{IH}) prior to forcing the $\overline{CS}$ pin to V_{IH}. This begins a write cycle and enables the WiperLock Technology feature (See Figure 5-9).

After the $\overline{CS}$ pin is driven to V_{IH} (from V_{IHH}), all other serial commands are ignored until the EEPROM write cycle (t_{WC}) completes.

Note:	The wiper value will not underflow. That is, once the wiper value equals 0x00, subsequent decrement commands are ignored.

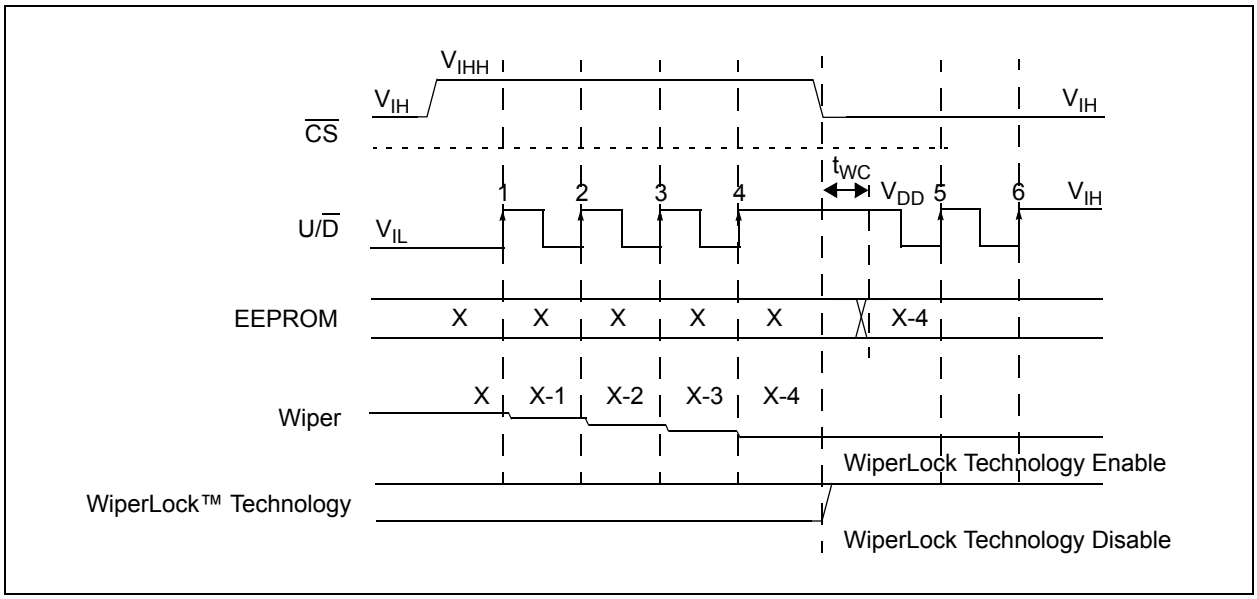

FIGURE 5-9: *High-Voltage Decrement and Enable WiperLock™ Technology.*

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5.2.10 WRITE WIPER SETTING TO EEPROM AND DISABLE WiperLock TECHNOLOGY

This mode is achieved by keeping the U/$\overline{D}$ pin static (either at V_{IL} or at V_{IH}), while the $\overline{CS}$ pin is driven from V_{IH} to V_{IHH} and then returned to V_{IH}. When the falling edge of the $\overline{CS}$ pin occurs (from V_{IHH} to V_{IH}), the wiper value is written to EEPROM and the WiperLock Technology is disabled (See Figure 5-10).

To ensure that "unexpected" transitions on the U/$\overline{D}$ pin do not cause the wiper setting to change, force the $\overline{CS}$ pin to V_{IH} as soon as possible (within device specifications) after the $\overline{CS}$ pin is forced to V_{IHH}.

After the $\overline{CS}$ pin is driven to V_{IH} (from V_{IHH}), all other serial commands are ignored until the EEPROM write cycle (t_{WC}) completes.

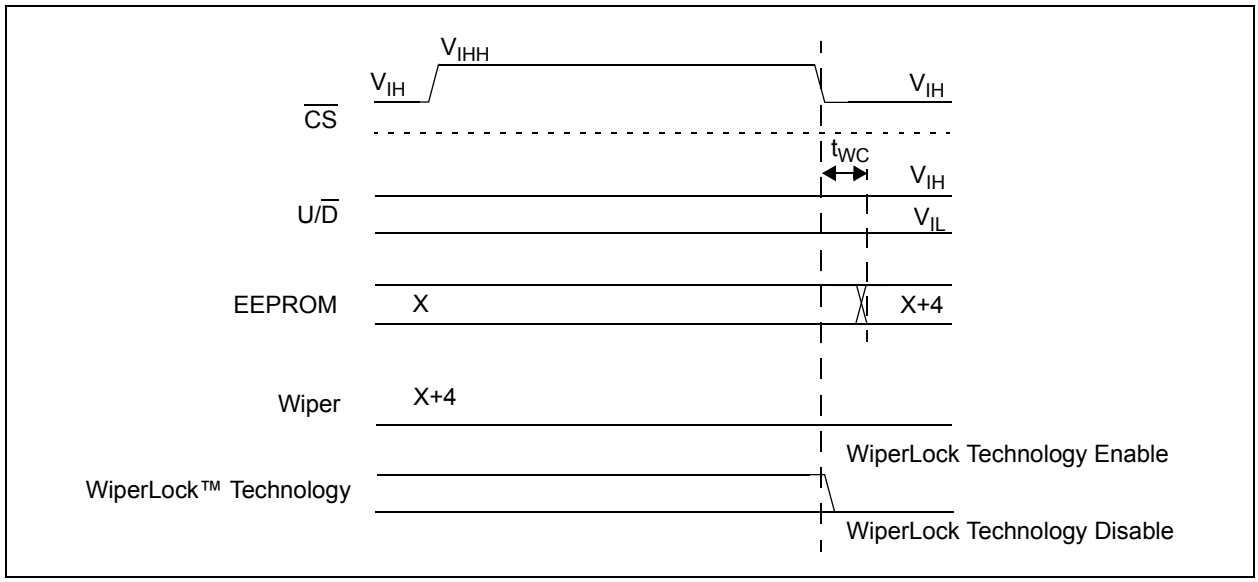

FIGURE 5-10: *Write Wiper Setting to EEPROM and Disable WiperLock™ Technology.*

5.2.11 WRITE WIPER SETTING TO EEPROM AND ENABLE WiperLock TECHNOLOGY

This mode is achieved by initializing the U/$\overline{D}$ and $\overline{CS}$ pins to a high state (V_{IH}) prior to the $\overline{CS}$ pin being driven to V_{IHH} (from V_{IH}). Set the U/$\overline{D}$ pin to a low state (V_{IL}) prior to forcing the $\overline{CS}$ pin to V_{IH} (from V_{IHH}). This begins a write cycle and enables the WiperLock Technology feature (See Figure 5-11).

To ensure that "unexpected" transitions on the U/$\overline{D}$ pin do not cause the wiper setting to increment, force the $\overline{CS}$ pin to V_{IH} as soon as possible (within device specifications) after the U/$\overline{D}$ pin is forced to V_{IL}.

After the $\overline{CS}$ pin is driven to V_{IH} (from V_{IHH}), all other serial commands are ignored until the EEPROM write cycle (t_{WC}) completes.

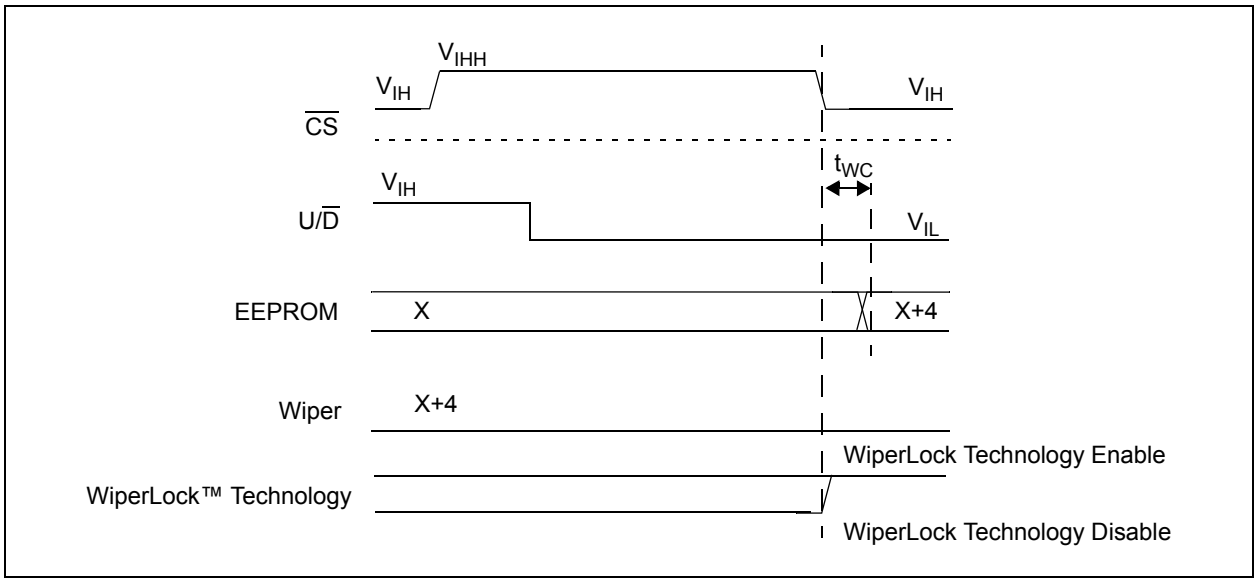

FIGURE 5-11: *Write Wiper Setting to EEPROM and Enable WiperLock™ Technology.*

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5.3 $\overline{CS}$ High Voltage

Depending on the requirements of the system, the use of high voltage (V_{IHH}) on the $\overline{CS}$ pin, may or may not be required during system operation. Table 5-2 shows possible system applications, and whether a high voltage (V_{IHH}) is required on the system.

The MCP402X supports six high-voltage commands (the $\overline{CS}$ input voltage must meet the V_{IHH} specification).

TABLE 5-2: HIGH-VOLTAGE APPLICATIONS

System Operation	High Voltage
Production calibration only - system should not update wiper setting	From Calibration Unit
WiperLock™ Technogy disabled during system operation	Not Required
Wiper setting can be updated and "locked" during system operation	Required

5.3.1 TECHNIQUES TO FORCE THE $\overline{CS}$ PIN TO V_{IHH}

The circuit in Figure 5-12 shows a method using the TC1240A doubling charge pump. When the $\overline{SHDN}$ pin is high, the TC1240A is off, and the level on the $\overline{CS}$ pin is controlled by the PIC® microcontrollers (MCUs) IO2 pin.

When the SHDN pin is low, the TC1240A is on and the V_{OUT} voltage is 2 * V_{DD}. The resistor R_1 allows the $\overline{CS}$ pin to go higher than the voltage such that the PIC MCU's IO2 pin "clamps" at approximately V_{DD}.

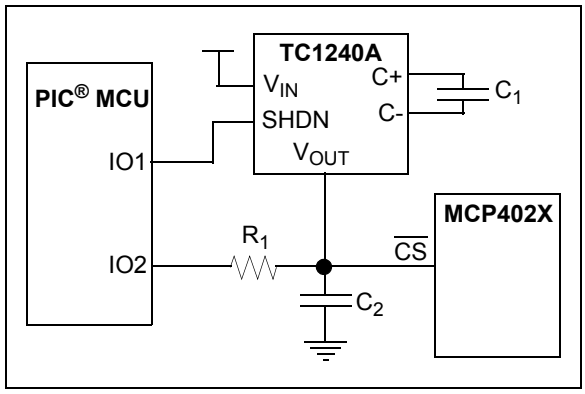


FIGURE 5-12: *Using the TC1240A to generate the V_{IHH} voltage.*

The circuit in Figure 5-13 shows the method used on the MCP402X Non-volatile Digital Potentiometer Evaluation Board. This method requires that the system voltage be approximately 5V. This ensures that when the PIC10F206 enters a brown-out condition, there is an insufficent voltage level on the $\overline{CS}$ pin to change the stored value of the wiper. The MCP402X Non-volatile Digital Potentiometer Evaluation Board User's Guide (DS51546) contains a complete schematic.

GP0 is a general purpose I/O pin, while GP2 can either be a general purpose I/O pin or it can output the internal clock.

For the serial commands, configure the GP2 pin as an input (high impedence). The output state of the GP0 pin will determine the voltage on the $\overline{CS}$ pin (V_{IL} or V_{IH}).

For high-voltage serial commands, force the GP0 output pin to output a high level (V_{OH}) and configure the GP2 pin to output the internal clock. This will form a charge pump and increase the voltage on the $\overline{CS}$ pin (when the system voltage is approximately 5V).

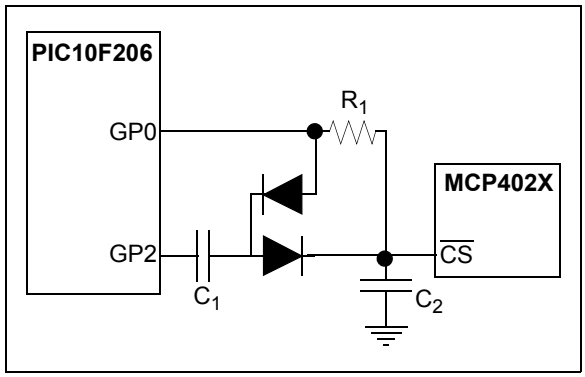


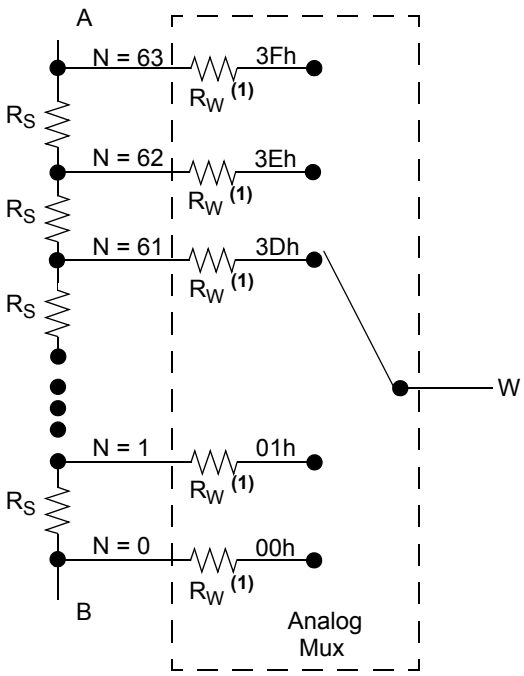
FIGURE 5-13: *MCP402X Non-volatile Digital Potentiometer Evaluation Board (MCP402XEV) implementation to generate the V_{IHH} voltage.*

6.0 RESISTOR

Digital potentiometer applications can be divided into two categories:

- Rheostat configuration
- Potentiometer (or voltage divider) configuration

Figure 6-1 shows a block diagram for the MCP402X resistors.



Note 1: The wiper resistance is tap dependent. That is, each tap selection resistance has a small variation. This variation effects the smaller resistance devices (2.1 kΩ) more.

FIGURE 6-1: *Resistor Block Diagram.*

Step resistance (R_S) is the resistance from one tap setting to the next. This value will be dependent on the R_{AB} value that has been selected. Table 6-1 shows the typical step resistances for each device.

The total resistance of the device has minimal variation due to operating voltage (see Figure 2-6, Figure 2-17, Figure 2-27 or Figure 2-37).

TABLE 6-1: TYPICAL STEP RESISTANCES

Part Number	Typical Resistance (Ω)	
	Total (R_{AB})	Step (R_S)
MCP402X-203E	2100	33.33
MCP402X-503E	5000	79.37
MCP402X-104E	10000	158.73
MCP402X-504E	50000	793.65

Terminal A and B, as well as the wiper W, do not have a polarity. These terminals can support both positive and negative current.

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6.1 Resistor Configurations

6.1.1 RHEOSTAT CONFIGURATION

When used as a rheostat, two of the three digital potentiometer's terminals are used as a resistive element in the circuit. With terminal W (wiper) and either terminal A or terminal B, a variable resistor is created. The resistance will depend on the tap setting of the wiper and the wiper's resistance. The resistance is controlled by changing the wiper setting.

The unused terminal (B or A) should be left floating. Figure 6-2 shows the two possible resistors that can be used. Reversing the polarity of the A and B terminals will not affect operation.

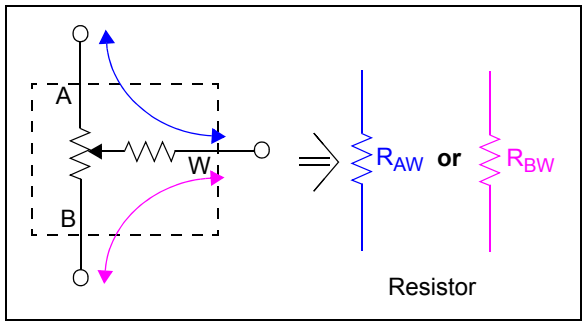


FIGURE 6-2: *Rheostat Configuration.*

This allows the control of the total resistance between the two nodes. The total resistance depends on the "starting" terminal to the wiper terminal. At the code 00h, the R_{BW} resistance is minimal (R_W), but the R_{AW} resistance in maximized ($R_{AB} + R_W$). Conversely, at the code 3Fh, the R_{AW} resistance is minimal (R_W), but the R_{BW} resistance in maximized ($R_{AB} + R_W$).

The resistance step size (R_S) equates to one LSb of the resistor.

Note:	To avoid damage to the internal wiper circuitry in this configuration, care should be taken to insure the current flow never exceeds 2.5 mA.

The change in wiper-to-end terminal resistance over temperature is shown in Figure 2-6, Figure 2-17, Figure 2-27 and Figure 2-37. The most variation over temperature will occur in the first few codes due to the wiper resistance coefficient affecting the total resistance. The remaining codes are dominated by the total resistance tempco R_{AB}.

6.1.2 POTENTIOMETER CONFIGURATION

When used as a potentiometer, all three terminals are tied to different nodes in the circuit. This allows the potentiometer to output a voltage proportional to the input voltage. This configuration is sometimes called voltage divider mode. The potentiometer is used to provide a variable voltage by adjusting the wiper position between the two endpoints as shown in Figure 6-3. Reversing the polarity of the A and B terminals will not affect operation.

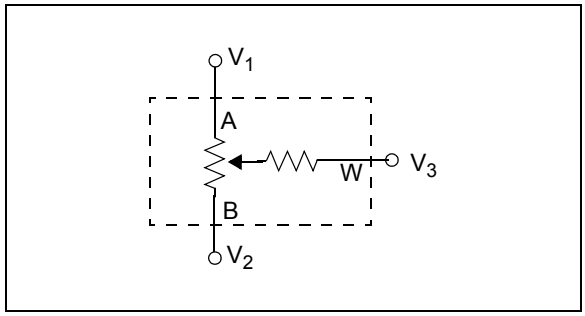


FIGURE 6-3: *Potentiometer Configuration.*

The temperature coefficient of the R_{AB} resistors is minimal by design. In this configuration, the resistors all change uniformally, so minimal variation should be seen.

The wiper resistor temperature coefficient is different from the R_{AB} temperature coefficient. The voltage at node V_3 (Figure 6-3) is not dependent on this wiper resistance, just the ratio of the R_{AB} resistors, so this temperature coefficient in most cases can be ignored.

Note:	To avoid damage to the internal wiper circuitry in this configuration, care should be taken to insure the current flow never exceeds 2.5 mA.

6.2 Wiper Resistance

Wiper resistance is the series resistance of the wiper. This resistance is typically measured when the wiper is positioned at either zero-scale (00h) or full-scale (3Fh).

The wiper resistance in potentiometer-generated voltage divider applications is not a significant source of error.

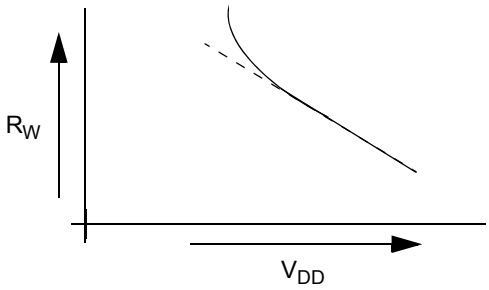
The wiper resistance in rheostat applications can create significant non-linearity as the wiper is moved toward zero-scale (00h). The lower the nominal resistance, the greater the possible error.

Wiper resistance is significant depending on the devices operating voltage. As the device voltage decreases, the wiper resistance increases (see Figure 6-4 and Table 6-2).

In a rheostat configuration, this change in voltage needs to be taken into account, particularly for the lower resistance devices. For the 2.1 kΩ device, the maximum wiper resistance at 5.5V is approximately 6% of the total resistance, while at 2.7V, it is approximately 15.5% of the total resistance.

In a potentiometer configuration, the wiper resistance variation does not effect the output voltage seen on the terminal W pin.

The slope of the resistance has a linear area (at the higher voltages) and a non-linear area (at the lower voltages), where resistance increases faster than the voltage drop (at low voltages).



Note: The slope of the resistance has a linear area (at the higher voltages) and a non-linear area (at the lower voltages).

FIGURE 6-4: *Relationship of Wiper Resistance (R_W) to Voltage*

Since there is minimal variation of the total device resistance over voltage, at a constant temperature (see Figure 2-6, Figure 2-17, Figure 2-27 or Figure 2-37), the change in wiper resistance over voltage can have a significant impact on the INL and DNL error.

TABLE 6-2: TYPICAL STEP RESISTANCES AND RELATIONSHIP TO WIPER RESISTANCE

Resistance (Ω)					R_W / R_S (%) (1)			R_W / R_{AB} (%) (2)		
Typical		Wiper (R_W)								
Total (R_{AB})	Step (R_S)	Typical	Max @ 5.5V	Max @ 2.7V	R_W = Typical	R_W = Max @ 5.5V	R_W = Max @ 2.7V	R_W = Typical	R_W = Max @ 5.5V	R_W = Max @ 2.7V
2100	33.33	75	125	325	225.0%	375.0%	975.0%	3.57%	5.95%	15.48%
5000	79.37	75	125	325	94.5%	157.5%	409.5%	1.5%	2.50%	6.50%
10000	158.73	75	125	325	47.25%	78.75%	204.75%	0.75%	1.25%	3.25%
50000	793.65	75	125	325	9.45%	15.75%	40.95%	0.15%	0.25%	0.65%

Note 1: R_S is the typical value. The variation of this resistance is minimal over voltage.

2: R_{AB} is the typical value. The variation of this resistance is minimal over voltage.

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6.3 Operational Characteristics

Understanding the operational characteristics of the device's resistor components is important to the system design.

6.3.1 ACCURACY

6.3.1.1 Integral Non-Linearity (INL)

INL error for these devices is the maximum deviation between an actual code transition point and its corresponding ideal transition point after offset and gain errors have been removed. These endpoints are from 0x00 to 0x3F. Refer to Figure 6-5.

Positive INL means higher resistance than ideal. Negative INL means lower resistance than ideal.

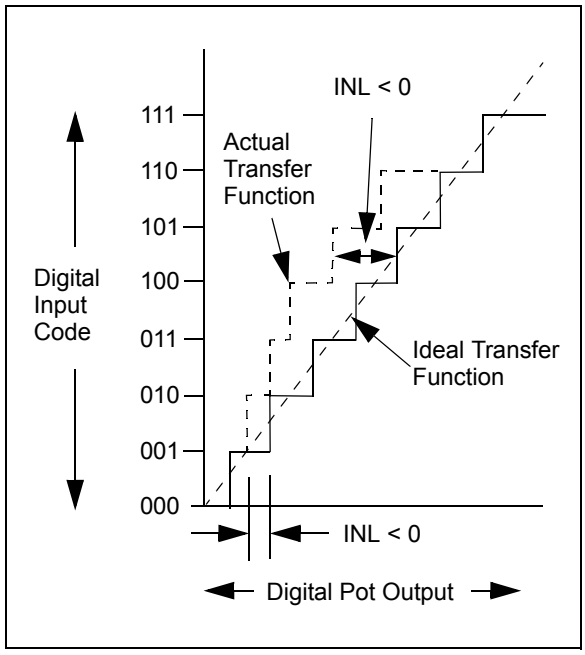

FIGURE 6-5: *INL Accuracy.*

6.3.1.2 Differential Non-Linearity (DNL)

DNL error is the measure of variations in code widths from the ideal code width. A DNL error of zero would imply that every code is exactly 1 LSb wide.

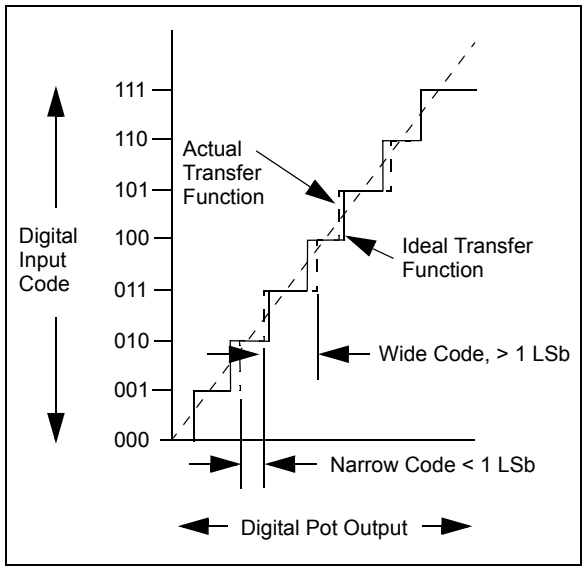

FIGURE 6-6: *DNL Accuracy.*

6.3.1.3 Ratiometric Temperature Coefficient

The ratiometric temperature coefficient quantifies the error in the ratio R_{AW}/R_{WB} due to temperature drift. This is typically the critical error when using a potentiometer device (MCP4021 and MCP4023) in a voltage divider configuration.

6.3.1.4 Absolute Temperature Coefficient

The absolute temperature coefficient quantifies the error in the end-to-end resistance (nominal resistance R_{AB}) due to temperature drift. This is typically the critical error when using a rheostat device (MCP4022 and MCP4024) in an adjustable resistor configuration.

6.3.2 MONOTONIC OPERATION

Monotonic operation means that the device's resistance increases with every step change (from terminal A to terminal B or terminal B to terminal A).

The wiper resistance is different at each tap location. When changing from one tap position to the next (either increasing or decreasing), the ΔR_W is less than the ΔR_S. When this change occurs, the device voltage and temperature are "the same" for the two tap positions.

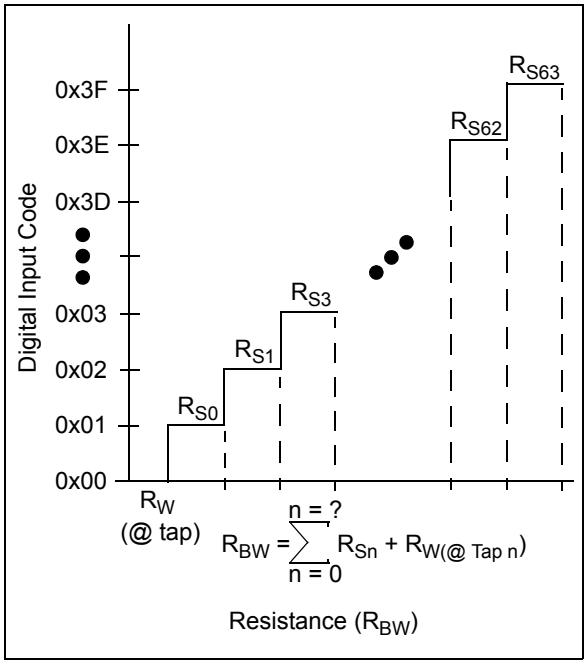

FIGURE 6-7: *Resistance, R_{BW}.*

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7.0 DESIGN CONSIDERATIONS

In the design of a system with the MCP402X devices, the following considerations should be taken into account:

- The Power Supply
- The Layout

7.1 Power Supply Considerations

The typical application will require a bypass capacitor in order to filter high-frequency noise, which can be induced onto the power supply's traces. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 7-1 illustrates an appropriate bypass strategy.

In this example, the recommended bypass capacitor value is 0.1 µF. This capacitor should be placed as close (within 4 mm) to the device power pin (V_{DD}) as possible.

The power source supplying these devices should be as clean as possible. If the application circuit has separate digital and analog power supplies, V_{DD} and V_{SS} should reside on the analog plane.

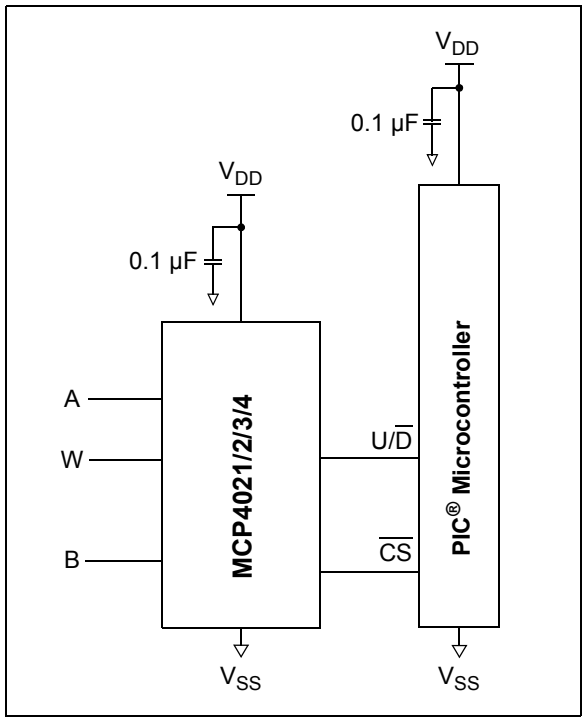

FIGURE 7-1: *Typical Microcontroller Connections.*

7.2 Layout Considerations

Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP402X's performance. Careful board layout will minimize these effects and increase the Signal-to-Noise Ratio (SNR). Bench testing has shown that a multi-layer board utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing. Particularly harsh environments may require shielding of critical signals.

If low noise is desired, breadboards and wire-wrapped boards are not recommended.

8.0 APPLICATIONS EXAMPLES

Non-volatile digital potentiometers have a multitude of practical uses in modern electronic circuits. The most popular uses include precision calibration of set point thresholds, sensor trimming, LCD bias trimming, audio attenuation, adjustable power supplies, motor control overcurrent trip setting, adjustable gain amplifiers and offset trimming. The MCP4021/2/3/4 devices can be used to replace the common mechanical trim pot in applications where the operating and terminal voltages are within CMOS process limitations (V_{DD} = 2.7V to 5.5V).

8.1 Set Point Threshold Trimming

Applications that need accurate detection of an input threshold event often need several sources of error eliminated. Use of comparators and operational amplifiers (op amps) with low offset and gain error can help achieve the desired accuracy, but in many applications, the input source variation is beyond the designer's control. If the entire system can be calibrated after assembly in a controlled environment (like factory test), these sources of error are minimized, if not entirely eliminated.

Figure 8-1 illustrates a common digital potentiometer configuration. This configuration is often referred to as a "windowed voltage divider". Note that R_1 and R_2 are not necessary to create the voltage divider, but their presence is useful when the desired threshold has limited range. It is "windowed" because R_1 and R_2 can narrow the adjustable range of V_{TRIP} to a value much less than $V_{DD} - V_{SS}$. If the output range is reduced, the magnitude of each output step is reduced. This effectively increases the trimming resolution for a fixed digital potentiometer resolution. This technique may allow a lower-cost digital potentiometer to be utilized (64 steps instead of 256 steps).

The MCP4021's and MCP4023's low DNL performance is critical to meeting calibration accuracy in production without having to use a higher precision digital potentiometer.

EQUATION 8-1: CALCULATING THE WIPER SETTING FROM THE DESIRED V_{TRIP}

$$V_{TRIP} = V_{DD}\left(\frac{R_2 + R_{WB}}{R_1 + R_{AB} + R_2}\right)$$

$$R_{AB} = R_{Nominal}$$

$$R_{WB} = R_{AB} \bullet \left(\frac{D}{63}\right)$$

$$D = \left(\left(\frac{V_{TRIP}}{V_{DD}}\right) \bullet ((R_1 + R_{AB} + R_2) - R_2)\right) \bullet 63$$

Where:

D = Digital Potentiometer Wiper Setting (0-63)

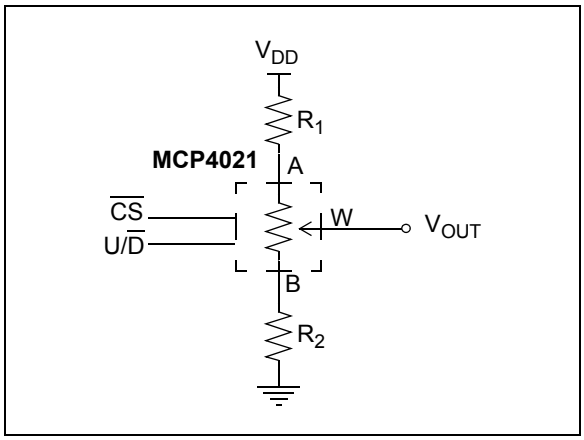

FIGURE 8-1: *Using the Digital Potentiometer to Set a Precise Output Voltage.*

8.1.1 TRIMMING A THRESHOLD FOR AN OPTICAL SENSOR

If the application has to calibrate the threshold of a diode, transistor or resistor, a variation range of 0.1V is common. Often, the desired resolution of 2 mV or better is adequate to accurately detect the presence of a precise signal. A "windowed" voltage divider, utilizing the MCP4021 or MCP4023, would be a potential solution as shown in Figure 8-2.

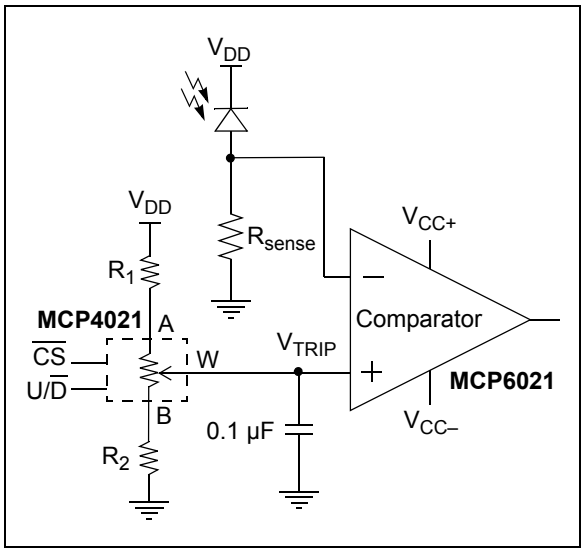

FIGURE 8-2: *Set Point or Threshold Calibration.*

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8.2 Operational Amplifier Applications

Figure 8-3, Figure 8-4 and Figure 8-5 illustrate typical amplifier circuits that could replace fixed resistors with the MCP4021/2/3/4 to achieve digitally-adjustable analog solutions.

Figure 8-4 shows a circuit that allows a non-inverting amplifier to have its' offset and gain to be independently trimmed. The MCP4021 is used along with resistors R1 and R2 to set the offset voltage. The sum of R1 + R2 resistance should be significantly greater (> 100 times) the resistance value of the MCP4021. This allows each increment or decrement in the MCP4021 to be a fine adjustment of the offset voltage. The input voltage of the op amp (V_{IN}) should be centered at the op amps V_W voltage. The gain is adjusted by the MCP4022. If the resistance value of the MCP4022 is small compared to the resistance value of R3, then this is a fine adjustment of the gain. If the resistance value of the MCP4022 is equal (or large) compared to the resistance value of R3, then this is a course adjustment of the gain. In gerneral, trim the course adjustments first and then trim the fine adjustments.

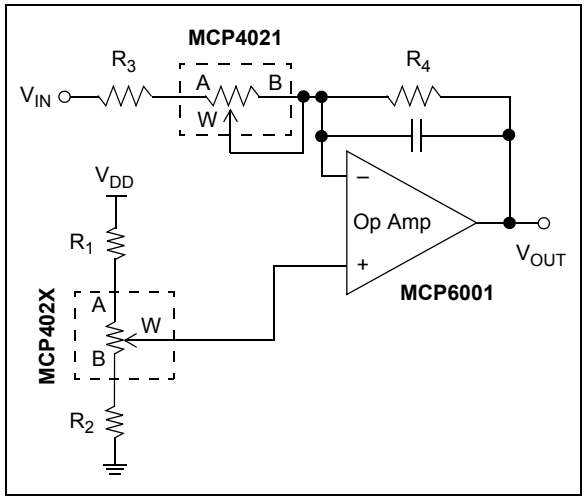

FIGURE 8-3: *Trimming Offset and Gain in an Inverting Amplifier.*

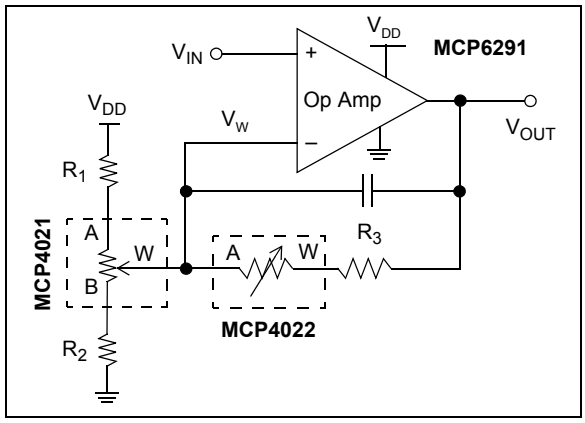

FIGURE 8-4: *Trimming Offset and Gain in a Non-Inverting Amplifier.*

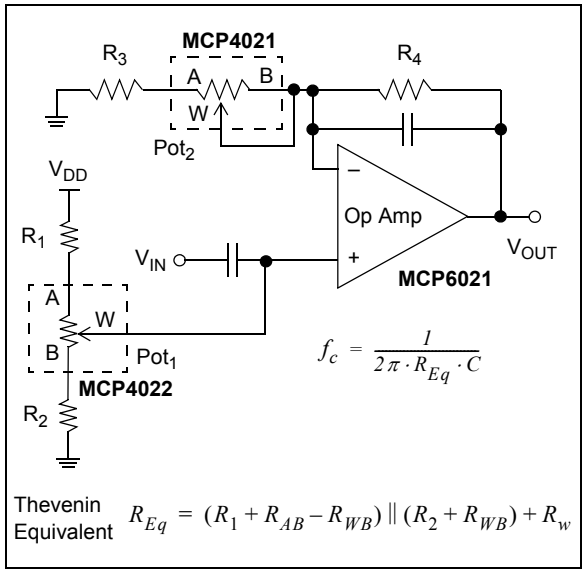

FIGURE 8-5: *Programmable Filter.*

8.3 Temperature Sensor Applications

Thermistors are resistors with very predictable variation with temperature. Thermistors are a popular sensor choice when a low-cost, temperature-sensing solution is desired. Unfortunately, thermistors have non-linear characteristics that are undesirable, typically requiring trimming in an application to achieve greater accuracy. There are several common solutions to trim and linearize thermistors. Figure 8-6 and Figure 8-7 are simple methods for linearizing a 3-terminal NTC thermistor. Both are simple voltage dividers using a Positive Temperature Coefficient (PTC) resistor (R_1) with a transfer function capable of compensating for the linearity error in the Negative Temperature Coefficient (NTC) thermistor.

The circuit, illustrated by Figure 8-6, utilizes a digital rheostat for trimming the offset error caused by the thermistor's part-to-part variation. This solution puts the digital potentiometer's R_W into the voltage divider calculation. The MCP4021/2/3/4's R_{AB} temperature coefficient is 50 ppm (-20°C to +70°C). R_W's error is substantially greater than R_{AB}'s error because R_W varies with V_{DD}, wiper setting and temperature. For the 50 kΩ devices, the error introduced by R_W is, in most cases, insignificant as long as the wiper setting is > 6. For the 2 kΩ devices, the error introduced by R_W is significant because it is a higher percentage of R_{WB}. For these reasons, the circuit illustrated in Figure 8-6 is not the most optimum method for "exciting" and linearizing a thermistor.

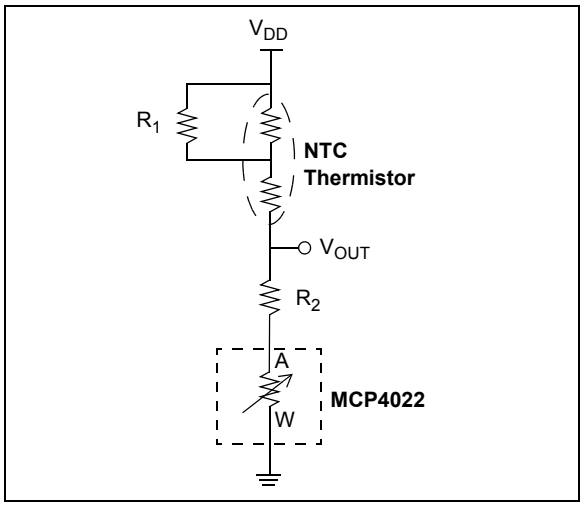

FIGURE 8-6: *Thermistor Calibration using a Digital Potentiometer in a Rheostat Configuration.*

The circuit illustrated by Figure 8-7 utilizes a digital potentiometer for trimming the offset error. This solution removes R_W from the trimming equation along with the error associated with R_W. R_2 is not required, but can be utilized to reduce the trimming "window" and reduce variation due to the digital potentiometer's R_{AB} part-to-part variability.

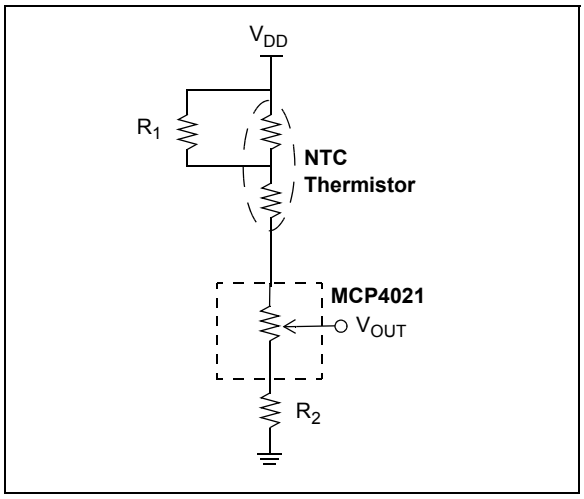

FIGURE 8-7: *Thermistor Calibration using a Digital Potentiometer in a Potentiometer Configuration.*

8.4 Wheatstone Bridge Trimming

Another common configuration to "excite" a sensor (such as a strain gauge, pressure sensor or thermistor) is the wheatstone bridge configuration. The wheatstone bridge provides a differential output instead of a single-ended output. Figure 8-8 illustrates a wheatstone bridge utilizing one to three digital potentiometers. The digital potentiometers in this example are used to trim the offset and gain of the wheatstone bridge.

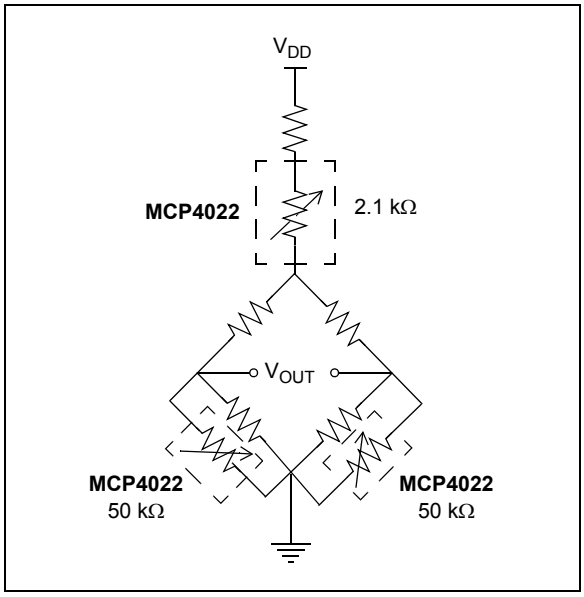

FIGURE 8-8: *Wheatstone Bridge Trimming.*

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9.0 DEVELOPMENT SUPPORT

9.1 Evaluation/Demonstration Boards

Currently there are three boards that are available that can be used to evaluate the MCP4021/2/3/4 family of devices.

1. The MCP402X Digital Potentiomenter Evaluation Board kit (MCP402XEV) contains a simple demonstration board utilizing a PIC10F206, the MCP4021 and a blank PCB, which can be populated with any desired MCP4021/2/3/4 device in a SOT-23-5, SOT-23-6 or 150 mil SOIC 8-pin package.

   This board has two push buttons to control when the PIC® microcontroller generates MCP402X serial commands. The example firmware demonstrates the following commands:

   - Increment
   - Decrement
   - High-Voltage Increment and Enable WiperLock Technology
   - High-Voltage Decrement and Enable WiperLock Technology
   - High-Voltage Increment and Disable WiperLock Technology
   - High-Voltage Decrement and Disable WiperLock Technology

   The populated board (with the MCP4021) can be used to evaluate the other MCP402X devices by appropriately jumpering the PCB pads.
2. The SOT-23-5/6 Evaluation Board (VSUPEV2) can be used to evaluate the characteristics of the MCP4022, MCP4023 and MCP4024 devices.
3. The 8-pin SOIC/MSOP/TSSOP/DIP Evaluation Board (SOIC8EV) can be used to evaluate the characteristics of the MCP4021 device in either the SOIC or MSOP package.
4. The MCP4XXX Digital Potentiometer Daughter Board allows the system designer to quickly evaluate the operation of Microchip Technology's MCP42XXX and MCP402X Digital Potentiometers. The board supports two MCP42XXX devices and an MCP402X device, which can be replaced with an MCP401X device.

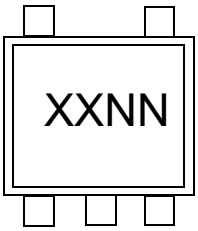
   The board also has a voltage doubler device (TC1240A), which can be used to show the WiperLock™ Technology feature of the MCP4021.

These boards may be purchased directly from the Microchip web site at www.microchip.com.

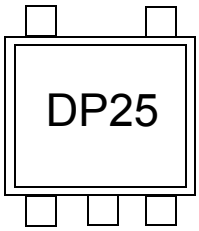
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

5-Lead SOT-23 (**MCP4024**)



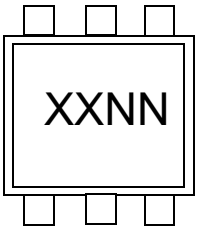
Example:



Part Number	Code
MCP4024T-202E/OT	DPNN
MCP4024T-502E/OT	DQNN
MCP4024T-103E/OT	DRNN
MCP4024T-503E/OT	DSNN

Note: Applies to 5-Lead SOT-23

6-Lead SOT-23 (**MCP4022 / MCP4023**)



Example:

Part Number	Code	
	MCP402**2**	MCP402**3**
MCP402**x**T-202E/CH	BANN	BENN
MCP402**x**T-502E/CH	BBNN	BFNN
MCP402**x**T-103E/CH	BCNN	BGNN
MCP402**x**T-503E/CH	BDNN	BHNN

Note: Applies to 6-Lead SOT-23

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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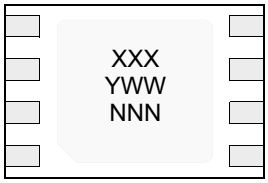
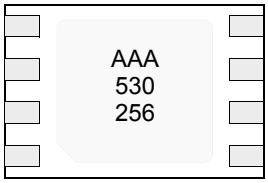
Package Marking Information

8-Lead DFN (2x3) **(MCP4021)**



Example:



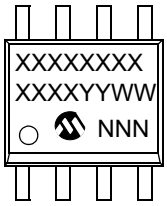
Part Number	Code
MCP4021T-202E/MC	AAA
MCP4021T-502E/MC	AAB
MCP4021T-103E/MC	AAC
MCP4021T-503E/MC	AAD

Note: Applies to 8-Lead DFN

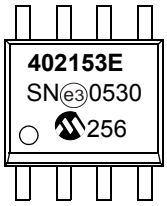
8-Lead MSOP **(MCP4021)**

Example:

8-Lead SOIC (150 mil) **(MCP4021)**



Example:



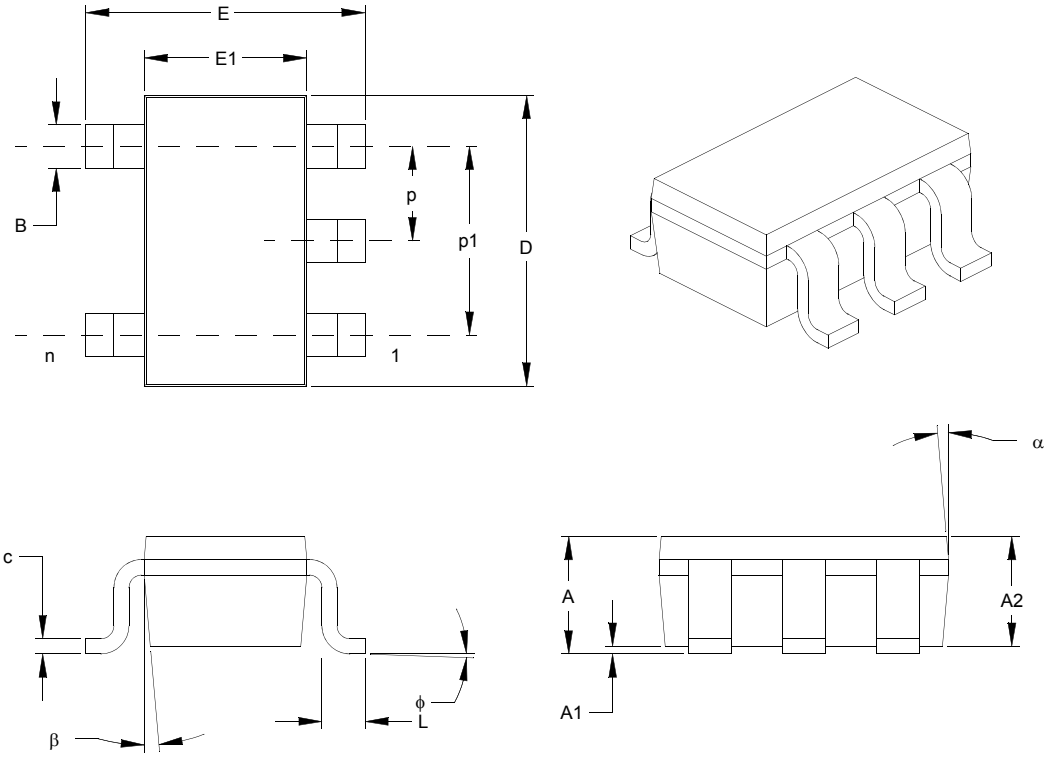
Part Numbers		Code
8L-MSOP	8L-SOIC	
MCP4021-202E/MS	MCP4021-202E/SN	22
MCP4021-502E/MS	MCP4021-502E/SN	52
MCP4021-103E/MS	MCP4021-103E/SN	13
MCP4021-503E/MS	MCP4021-503E/SN	53

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead Plastic Small Outline Transistor (OT) (SOT-23)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	f	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	a	0	5	10	0	5	10
Mold Draft Angle Bottom	b	0	5	10	0	5	10

* Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

EIAJ Equivalent: SC-74A

Drawing No. C04-091

Revised 09-12-05

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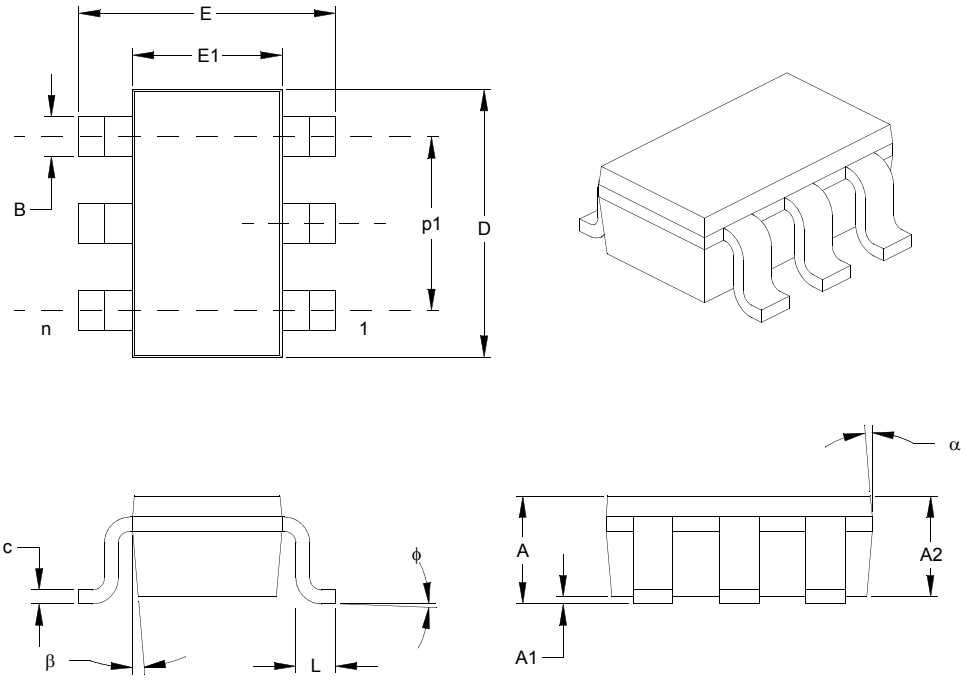
6-Lead Plastic Small Outline Transistor (CH) (SOT-23)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		6			6	
Pitch	p		.038 BSC			0.95 BSC	
Outside lead pitch	p1		.075 BSC			1.90 BSC	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	φ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

***** Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
See ASME Y14.5M

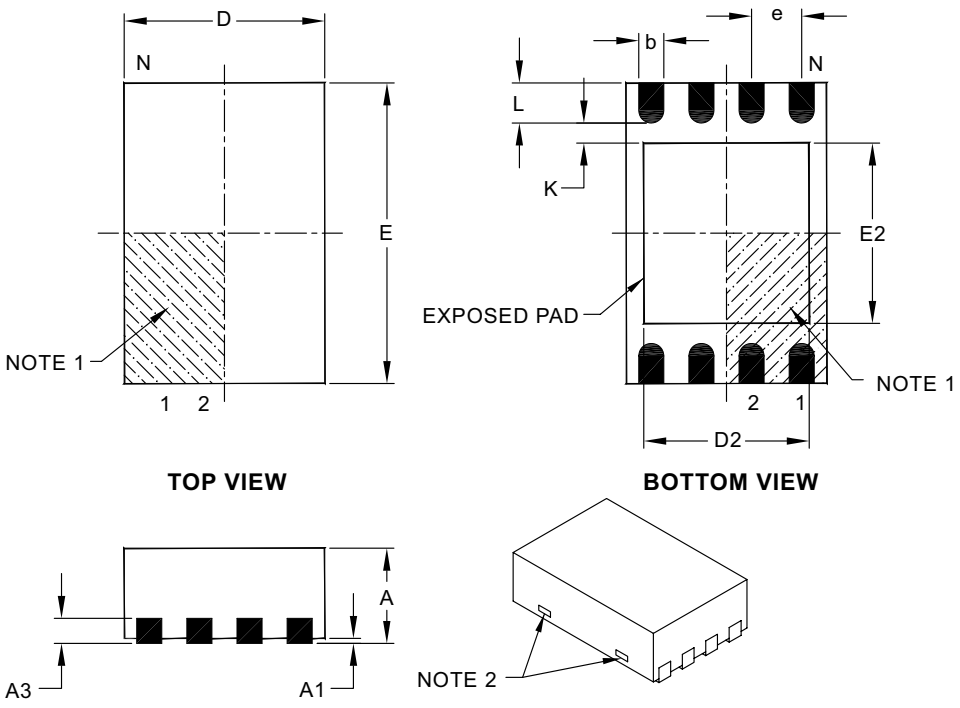
JEITA (formerly EIAJ) equivalent: SC-74A

Drawing No. C04-120

Revised 09-12-05

8-Lead Plastic Dual-Flat No-Lead Package (MC) 2x3x0.9 mm Body (DFN) – Saw Singulated

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.30	—	1.75
Exposed Pad Width	E2	1.50	—	1.90
Contact Width	b	0.18	0.25	0.30
Contact Length §	L	0.30	0.40	0.50
Contact-to-Exposed Pad §	K	0.20	—	—

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. § Significant Characteristic
4. Package is saw singulated
5. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04–123, Sept. 8, 2006

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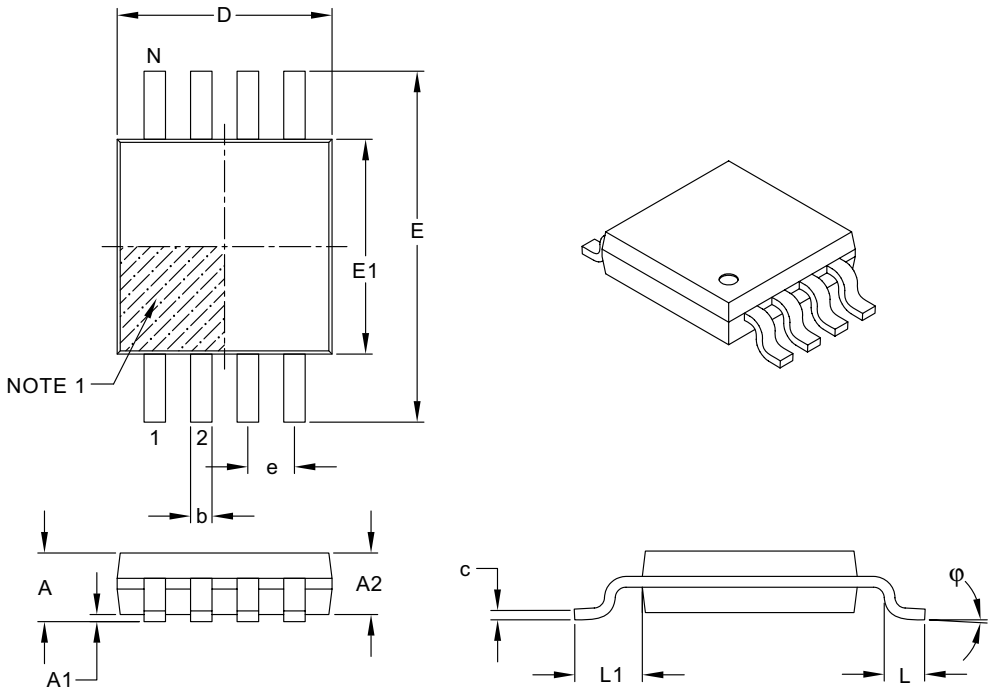
8-Lead Plastic Micro Small Outline Package (MS) (MSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	—	—	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	—	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	—	8°
Lead Thickness	c	0.08	—	0.23
Lead Width	b	0.22	—	0.40

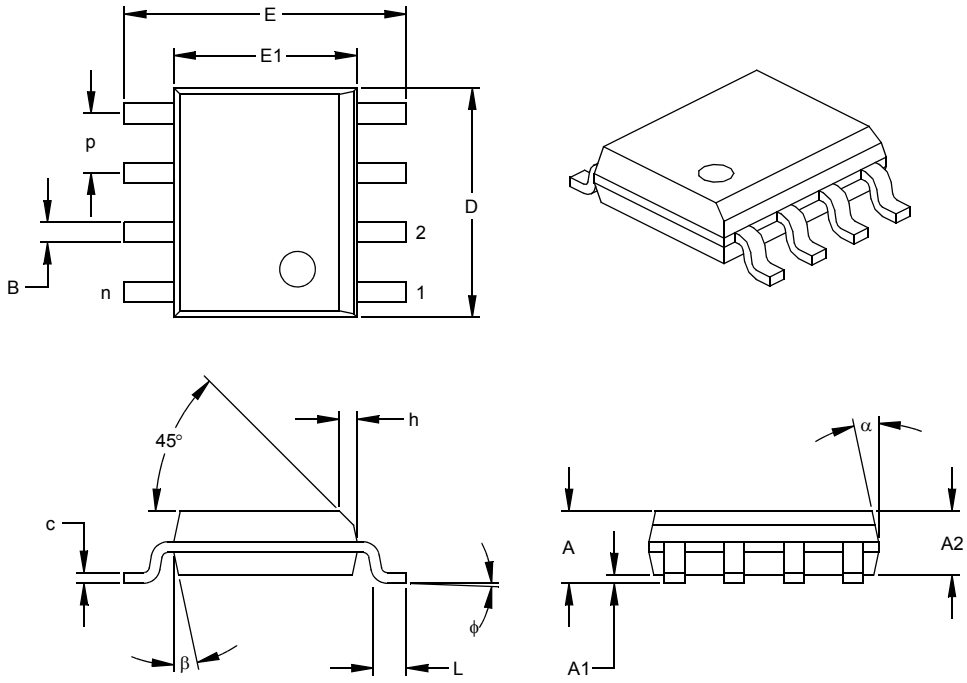
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04–111, Sept. 8, 2006

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

***** Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

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APPENDIX A: REVISION HISTORY

Revision E (December 2006)

- Added device designators in conditions column to associate units (MHz) in Bandwidth -3 dB parameter in **AC/DC Characteristics** table
- Added device designations in conditions column for R-INL and R-DNL specifications.
- Added disclaimers to package outline drawings.

Revision D (October 2006)

- Changed the EEPROM write cycle time (T_{WC}) from a maximum of 5 ms to a maximum of 10 ms (overvoltage and temperature) with a typical of 5 ms
- For the 10 kΩ device, the rheostat differential non-linearity specification at 2.7V was changed from ±0.5 LSb to ±1.0 LSb
- Figure 2-9 in **Section 2.0 "Typical Performance Curves"** was updated with the correct data.
- Added Figure 2-48 for -3 db Bandwidth information.
- Updated available Development Tools.
- Added disclaimer to package outline drawings.

Revision C (November 2005)

- Enhanced Descriptions
- Reordered Sections
- Added 8-lead MSOP and DFN packages

Revision B (April 2005)

- Updated part numbers in Product Identifcation Section (PIS)
- Added Appendix A: Revision History

Revision A (April 2005)

- Original Release of this Document

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XXX	X	/XX
Device	Resistance Version	Temperature Range	Package

Device:	MCP4021:	Single Potentiometer with U/$\overline{D}$ Interface
	MCP4021T:	Single Potentiometer with U/$\overline{D}$ Interface (Tape and Reel) (SOIC, MSOP)
	MCP4022:	Single Rheostat with U/$\overline{D}$ interface
	MCP4022T:	Single Rheostat with U/$\overline{D}$ interface (Tape and Reel) (SOT-23-6)
	MCP4023:	Single Potentiometer to GND with U/$\overline{D}$ Interface
	MCP4023T:	Single Potentiometer to GND with U/$\overline{D}$ Interface (Tape and Reel) (SOT-23-6)
	MCP4024:	Single Rheostat to GND with U/$\overline{D}$ Interface
	MCP4024T:	Single Rheostat to GND with U/$\overline{D}$ Interface (Tape and Reel)(SOT-23-5)
Resistance Version:	202 = 2.1 kΩ	
	502 = 5 kΩ	
	103 = 10 kΩ	
	503 = 50 kΩ	
Temperature Range:	E = -40°C to +125°C	
Package:	CH = Plastic Small Outline Transistor, 6-lead	
	MC = Plastic Dual Flat No Lead (2x3x0.9 mm), 8-lead	
	MS = Plastic MSOP, 8-lead	
	SN = Plastic SOIC, (150 mil Body), 8-lead	
	OT = Plastic Small Outline Transistor, 5-lead	

Examples:

a) MCP4021-103E/MS: 10 kΩ, 8-LD MSOP
b) MCP4021-103E/SN: 10 kΩ, 8-LD SOIC
c) MCP4021T-103E/MC: T/R, 10 kΩ, 8-LD DFN
d) MCP4021T-103E/MS: T/R, 10 kΩ, 8-LD MSOP
e) MCP4021T-103E/SN: T/R, 10 kΩ, 8-LD SOIC
f) MCP4021-202E/MS: 2.1 kΩ, 8-LD MSOP
g) MCP4021-202E/SN: 2.1 kΩ, 8-LD SOIC
h) MCP4021T-202E/MC: T/R, 2.1 kΩ, 8-LD DFN
i) MCP4021T-202E/MS: T/R, 2.1 kΩ, 8-LD MSOP
j) MCP4021T-202E/SN: T/R, 2.1 kΩ, 8-LD SOIC
k) MCP4021-502E/MS: 5 kΩ, 8-LD MSOP
l) MCP4021-502E/SN: 5 kΩ, 8-LD SOIC
m) MCP4021T-502E/MC: T/R, 5 kΩ, 8-LD DFN
n) MCP4021T-502E/MS: T/R, 5 kΩ, 8-LD MSOP
o) MCP4021T-502E/SN: T/R, 5 kΩ, 8-LD SOIC
p) MCP4021-503E/MS: 50 kΩ, 8-LD MSOP
q) MCP4021-503E/SN: 50 kΩ, 8-LD SOIC
r) MCP4021T-503E/MC: T/R, 50 kΩ, 8-LD DFN
s) MCP4021T-503E/MS: T/R, 50 kΩ, 8-LD MSOP
t) MCP4021T-503E/SN: T/R, 50 kΩ, 8-LD SOIC

a) MCP4022T-202E/CH 2.1 kΩ, 6-LD SOT-23
b) MCP4022T-502E/CH 5 kΩ, 6-LD SOT-23
c) MCP4022T-103E/CH 10 kΩ, 6-LD SOT-23
d) MCP4022T-503E/CH 50 kΩ, 6-LD SOT-23

a) MCP4023T-202E/CH 2.1 kΩ, 6-LD SOT-23
b) MCP4023T-502E/CH 5 kΩ, 6-LD SOT-23
c) MCP4023T-103E/CH 10 kΩ, 6-LD SOT-23
d) MCP4023T-503E/CH 50 kΩ, 6-LD SOT-23

a) MCP4024T-202E/OT 2.1 kΩ, 5-LD SOT-23
b) MCP4024T-502E/OT 5 kΩ, 5-LD SOT-23
c) MCP4024T-103E/OT 10 kΩ, 5-LD SOT-23
d) MCP4024T-503E/OT 50 kΩ, 5-LD SOT-23

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