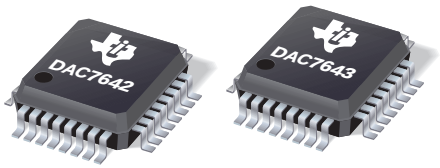


DAC7642
DAC7643

SBAS233 – DECEMBER 2001

16-Bit, Dual Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **LOW POWER: 4mW**
- **UNIPOLAR OR BIPOLAR OPERATION**
- **SETTLING TIME: 10μs to 0.003% FSR**
- **15-BIT LINEARITY AND MONOTONICITY: –40°C to +85°C**
- **RESET TO MID-SCALE (DAC7642) OR ZERO-SCALE (DAC7643)**
- **DATA READBACK**
- **DOUBLE-BUFFERED DATA INPUTS**

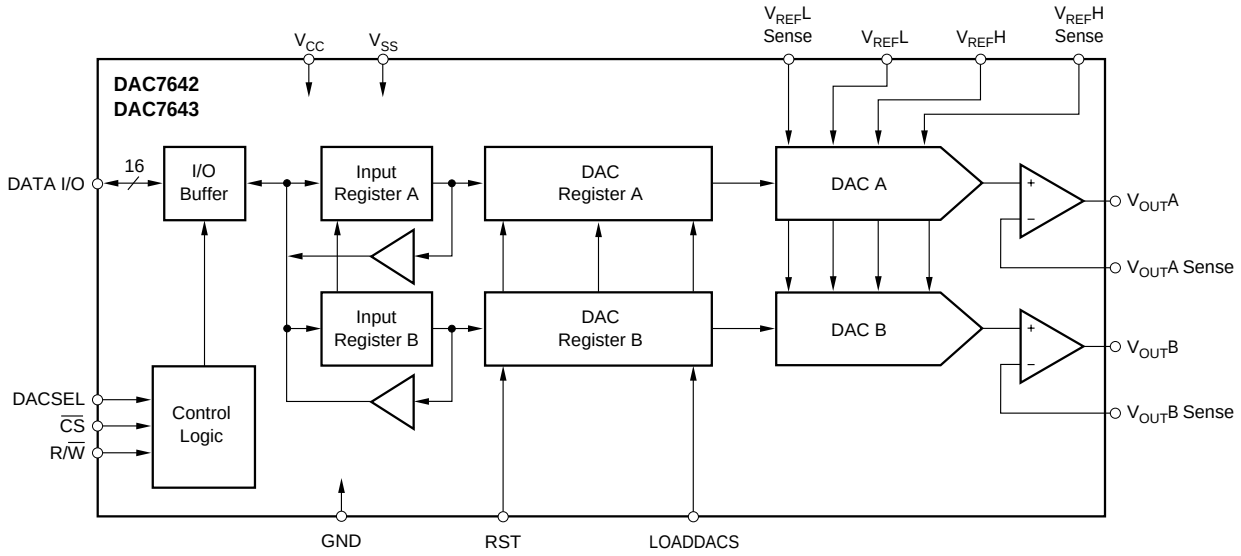
APPLICATIONS

- **PROCESS CONTROL**
- **CLOSED-LOOP SERVO-CONTROL**
- **MOTOR CONTROL**
- **DATA ACQUISITION SYSTEMS**
- **DAC-PER-PIN PROGRAMMERS**

DESCRIPTION

The DAC7642 and DAC7643 are dual channel, 16-bit, voltage output Digital-to-Analog Converters (DACs) which provide 15-bit monotonic performance over the specified temperature range. They accept 16-bit parallel input data, have double-buffered DAC input logic (allowing simultaneous update of all DACs), and provide a readback mode of the internal input registers. Programmable asynchronous reset clears all registers to a mid-scale code of 8000_H (DAC7642) or to a zero-scale code of 0000_H (DAC7643). These DACs can operate from a single +5V supply or from +5V and –5V supplies, providing an output range of 0 to +2.5V or –2.5V to +2.5V, respectively.

Low power and small size per DAC make the DAC7642 and DAC7643 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The DAC7642 and DAC7643 are available in a LQFP-32 package and specified over a –40°C to +85°C temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ABSOLUTE MAXIMUM RATINGS[1]

V_{CC} to V_{SS}	–0.3V to 11V
V_{CC} to GND	–0.3V to 5.5V
$V_{REF}L$ to V_{SS}	–0.3V to (V_{CC} – V_{SS})
V_{CC} to $V_{REF}H$	–0.3V to (V_{CC} – V_{SS})
$V_{REF}H$ to $V_{REF}L$	–0.3V to (V_{CC} – V_{SS})
Digital Input Voltage to GND	–0.3V to V_{CC} + 0.3V
Digital Output Voltage to GND	–0.3V to V_{CC} + 0.3V
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	MONOTONICITY	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC7642VF	14 Bits	LQFP-32	VF	–40°C to +85°C	DAC7642	DAC7642VFT	Tape and Reel, 250
"	"	"	"	"	"	DAC7642VFR	Tape and Reel, 1000
DAC7642VFB	15 Bits	LQFP-32	VF	–40°C to +85°C	DAC7642B	DAC7642VFBT	Tape and Reel, 250
"	"	"	"	"	"	DAC7642VFBR	Tape and Reel, 1000
DAC7643VF	14 Bits	LQFP-32	VF	–40°C to +85°C	DAC7643	DAC7643VFT	Tape and Reel, 250
"	"	"	"	"	"	DAC7643VFR	Tape and Reel, 1000
DAC7643VFB	15 Bits	LQFP-32	VF	–40°C to +85°C	DAC7643B	DAC7643VFBT	Tape and Reel, 250
"	"	"	"	"	"	DAC7643VFBR	Tape and Reel, 1000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS (Dual Supply)

At $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +5V, V_{SS} = –5V, $V_{REF}H$ = +2.5V, and $V_{REF}L$ = –2.5V, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7642VF DAC7643VF			DAC7642VFB DAC7643VFB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity Error			±3	±4		±2	±3	LSB
Linearity Match			±4			±2		LSB
Differential Linearity Error			±2	±3		±1	±2	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			Bits
Bipolar Zero Error			±1	±3		*	*	mV
Bipolar Zero Error Drift			5	10		*	*	ppm/°C
Full-Scale Error			±1	±3		*	*	mV
Full-Scale Error Drift			5	10		*	*	ppm/°C
Bipolar Zero Matching	Channel-to-Channel Matching		±1	±3		±1	±3	mV
Full-Scale Matching	Channel-to-Channel Matching		±1	±3		±1	±3	mV
Power-Supply Rejection Ratio (PSRR)	At Full-Scale		10	100		*	*	ppm/V
ANALOG OUTPUT								
Voltage Output	R_L = 10kΩ	$V_{REF}L$		$V_{REF}H$	*		*	V
Output Current		–1.25		+1.25	*		*	mA
Maximum Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			–10, +30			*		mA
Short-Circuit Duration	GND, V_{CC} or V_{SS}		Indefinite			*		
REFERENCE INPUT								
Ref High Input Voltage Range		$V_{REF}L$ + 1.25		+2.5	*		*	V
Ref Low Input Voltage Range		–2.5		$V_{REF}H$ – 1.25	*		*	V
Ref High Input Current			500			*		µA
Ref Low Input Current			–500			*		µA
DYNAMIC PERFORMANCE								
Settling Time	To ±0.003%, 5V Output Step		8	10		*	*	µs
Channel-to-Channel Crosstalk	See Figure 5		0.5			*		LSB
Digital Feedthrough			2			*		nV-s
Output Noise Voltage	f = 10kHz		60			*		nV/√Hz
DAC Glitch	$7FFF_H$ to 8000_H or 8000_H to $7FFF_H$		40			*		nV-s
DIGITAL INPUT								
V_{IH}		0.7 • V_{CC}			*			V
V_{IL}				0.3 • V_{CC}			*	V
I_{IH}				±10			*	µA
I_{IL}				±10			*	µA
DIGITAL OUTPUT								
V_{OH}	I_{OH} = –0.8mA	3.6	4.5		*	*		V
V_{OL}	I_{OL} = 1.2mA		0.3	0.4		*	*	V
POWER SUPPLY								
V_{CC}		+4.75	+5.0	+5.25	*	*	*	V
V_{SS}		–5.25	–5.0	–4.75	*	*	*	V
I_{CC}			0.7	1.1		*	*	mA
I_{SS}		–1.2	–0.8		*	*		mA
Power			7.5	11.5		*	*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Specifications same as DAC7642VF and DAC7643VF.

ELECTRICAL CHARACTERISTICS (Single Supply)

At $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +5V, V_{SS} = 0V, $V_{REF}H$ = +2.5V, and $V_{REF}L$ = 0V, unless otherwise noted.

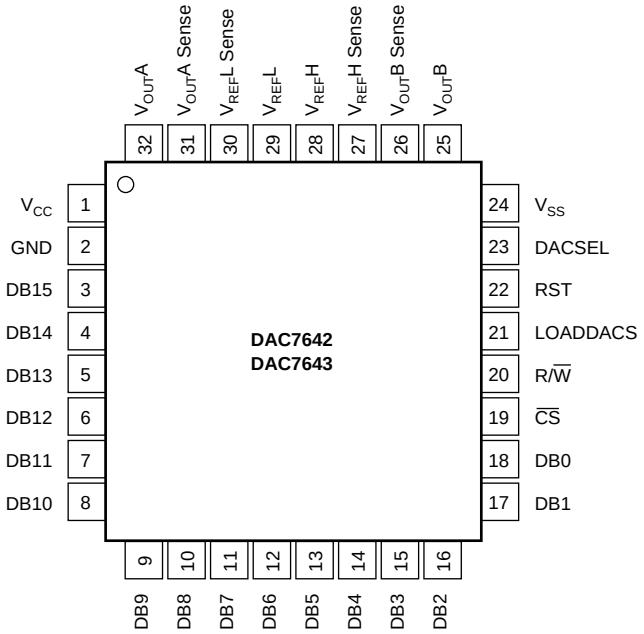
PARAMETER	CONDITIONS	DAC7642VF DAC7643VF			DAC7642VFB DAC7643VFB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity Error(1)			±3	±4		±2	±3	LSB
Linearity Match			±4			±2		LSB
Differential Linearity Error			±2	±3		±1	±2	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			Bits
Zero-Scale Error			±1	±3		*	*	mV
Zero-Scale Error Drift			5	10		*	*	ppm/°C
Full-Scale Error			±1	±3		*	*	mV
Full-Scale Error Drift			5	10		*	*	ppm/°C
Zero-Scale Matching	Channel-to-Channel Matching		±1	±3		±1	±3	mV
Full-Scale Matching	Channel-to-Channel Matching		±1	±3		±1	±3	mV
Power-Supply Rejection Ratio (PSRR)	At Full-Scale		10	100		*	*	ppm/V
ANALOG OUTPUT								
Voltage Output	R_L = 10kΩ	0		$V_{REF}H$	*		*	V
Output Current		–1.25		+1.25	*		*	mA
Maximum Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			–10, +30			*		mA
Short-Circuit Duration	GND or V_{CC}		Indefinite			*		
REFERENCE INPUT								
Ref High Input Voltage Range		$V_{REF}L$ + 1.25		+2.5	*		*	V
Ref Low Input Voltage Range		0		$V_{REF}H$ – 1.25	*		*	V
Ref High Input Current			250			*		µA
Ref Low Input Current			–250			*		µA
DYNAMIC PERFORMANCE								
Settling Time	To ±0.003%, 2.5V Output Step		8	10		*	*	µs
Channel-to-Channel Crosstalk	See Figure 6		0.5			*		LSB
Digital Feedthrough			2			*		nV-s
Output Noise Voltage, f = 10kHz			60			*		$nV/\sqrt{Hz}$
DAC Glitch	$7FFF_H$ to 8000_H or 8000_H to $7FFF_H$		40			*		nV-s
DIGITAL INPUT								
V_{IH}		0.7 • V_{CC}			*			V
V_{IL}				0.3 • V_{CC}			*	V
I_{IH}				±10			*	µA
I_{IL}				±10			*	µA
DIGITAL OUTPUT								
V_{OH}	I_{OH} = –0.8mA	3.6	4.5		*	*		V
V_{OL}	I_{OL} = 1.2mA		0.3	0.4		*	*	V
POWER SUPPLY								
V_{CC}		+4.75	+5.0	+5.25	*	*	*	V
V_{SS}		0	0	0	*	*	*	V
I_{CC}			0.5	0.9		*	*	mA
Power			2.5	4.5		*	*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Specifications same as DAC7642VF and DAC7643VF.

NOTE: (1) If V_{SS} = 0V, specification applies at Code 0040_H and above due to possible negative zero-scale error.

PIN CONFIGURATION

Top View **LQFP**



PIN DESCRIPTIONS

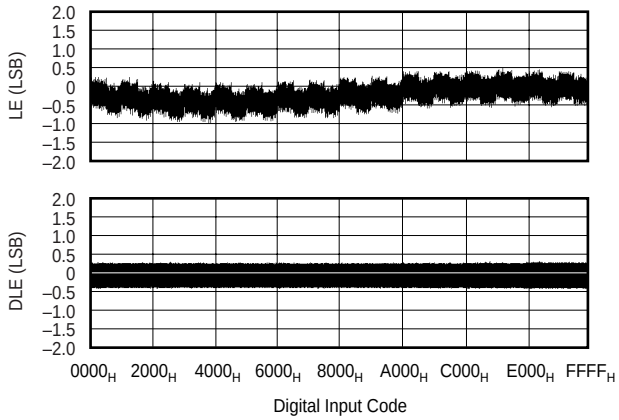
PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	V_{CC}	Positive Power Supply	20	R/$\overline{W}$	Enabled by $\overline{CS}$, Controls Data Read from and Write to the Input Registers.
2	GND	Ground	21	LOADDACS	DAC Output Registers Load Control. Rising edge triggered. Transfers Data from the Input Registers to the DAC Registers, Updating the DAC Output.
3	DB15	Data Bit 15, MSB	22	RST	Reset, Rising Edge Triggered. DAC7642 resets to mid-scale, DAC7643 resets to zero. (Resets Both Input Registers and DAC Registers)
4	DB14	Data Bit 14	23	DACSEL	Enabled by $\overline{CS}$. Selects the individual DAC Input Registers. (LOW Selects Register A, HIGH Selects Register B)
5	DB13	Data Bit 13	24	V_{SS}	Negative Power Supply
6	DB12	Data Bit 12	25	$V_{OUT}B$	DAC B Voltage Output
7	DB11	Data Bit 11	26	$V_{OUT}B$ Sense	DAC B Output Amplifier Inverting Input. Used to close the feedback loop at the load.
8	DB10	Data Bit 10	27	$V_{REF}H$ Sense	DAC A and B Reference High Sense Input
9	DB9	Data Bit 9	28	$V_{REF}H$	DAC A and B Reference High Input
10	DB8	Data Bit 8	29	$V_{OUT}L$	DAC A and B Reference Low Input
11	DB7	Data Bit 7	30	$V_{REF}L$ Sense	DAC A and B Reference Low Sense Input
12	DB6	Data Bit 6	31	$V_{OUT}A$ Sense	DAC A Output Amplifier Inverting Input. Used to close the feedback loop at the load.
13	DB5	Data Bit 5	32	$V_{OUT}A$	DAC A Output Voltage
14	DB4	Data Bit 4			
15	DB3	Data Bit 3			
16	DB2	Data Bit 2			
17	DB1	Data Bit 1			
18	DB0	Data Bit 0, LSB			
19	$\overline{CS}$	Chip Select, Active LOW			

TYPICAL CHARACTERISTICS: V_{SS} = 0V

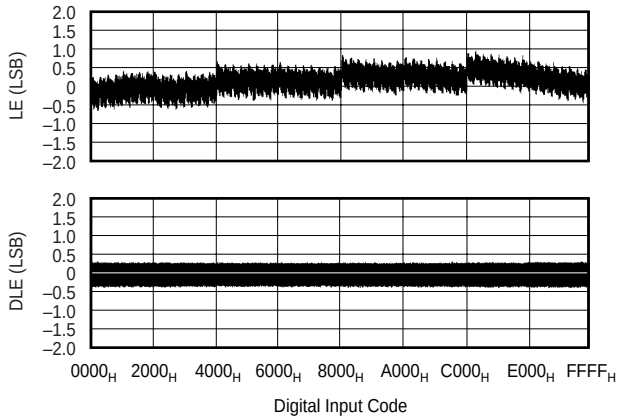
At T_A = +25°C, V_{CC} = +5V, V_{SS} = 0V, $V_{REF}H$ = +2.5V, $V_{REF}L$ = 0V, representative unit, unless otherwise specified.

+25°C

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +25°C)

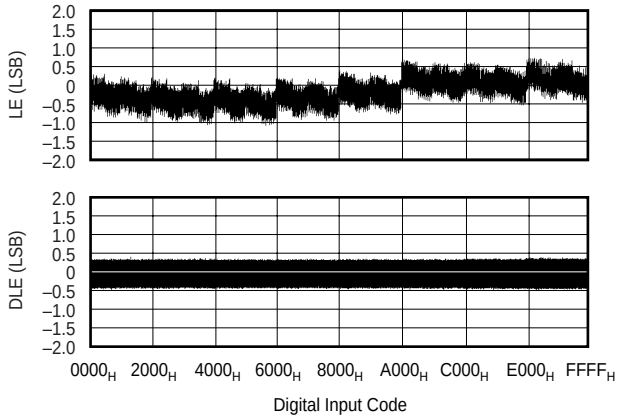


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +25°C)

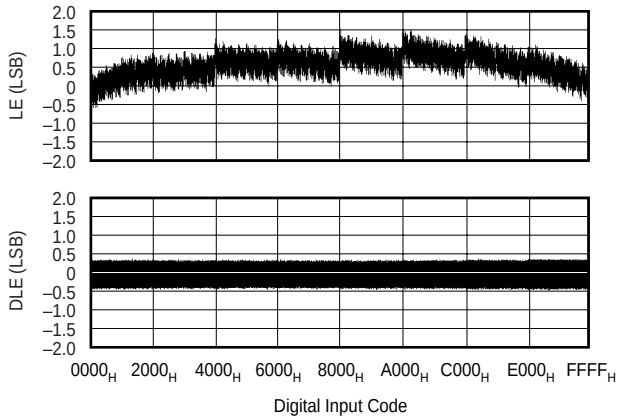


+85°C

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +85°C)

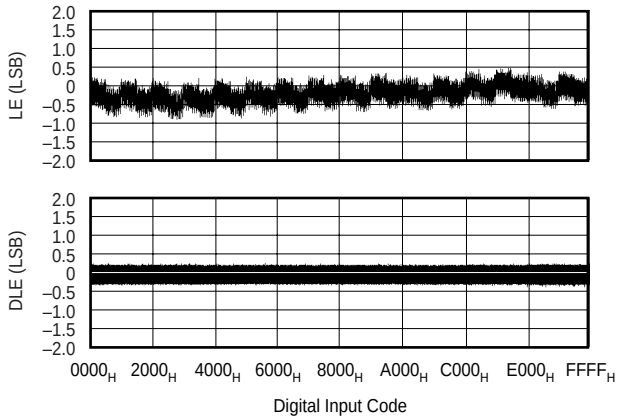


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +85°C)

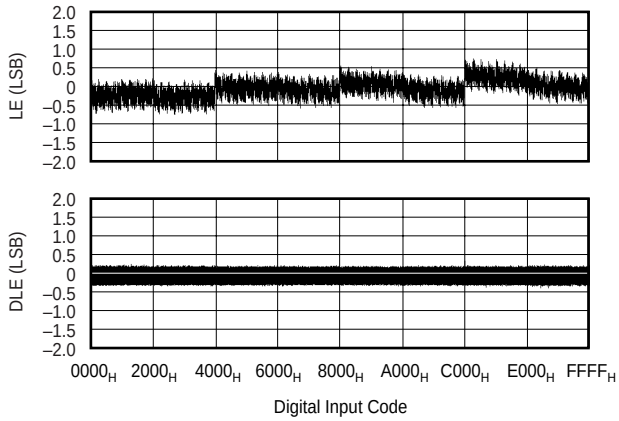


–40°C

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, –40°C)



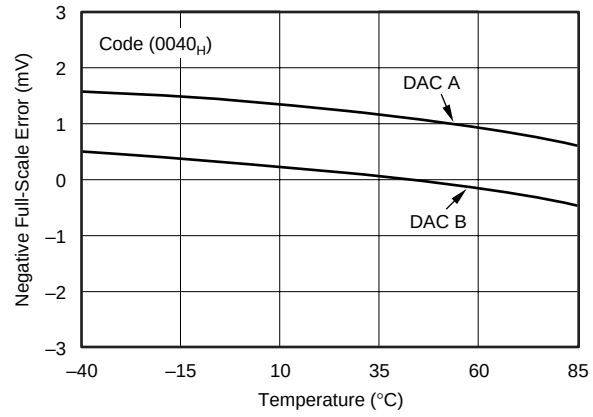
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, –40°C)



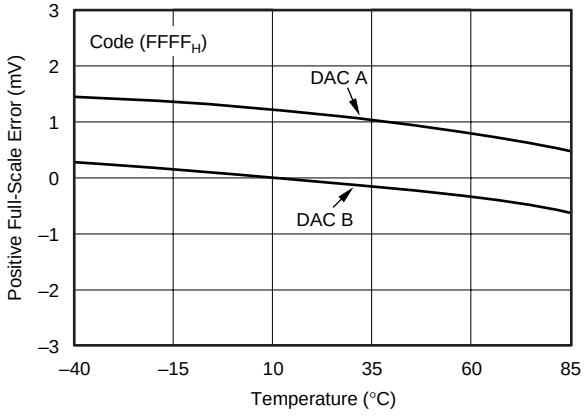
TYPICAL CHARACTERISTICS: V_{SS} = 0V (Cont.)

At T_A = +25°C, V_{CC} = +5V, V_{SS} = 0V, $V_{REF}H$ = +2.5V, $V_{REF}L$ = 0V, representative unit, unless otherwise specified.

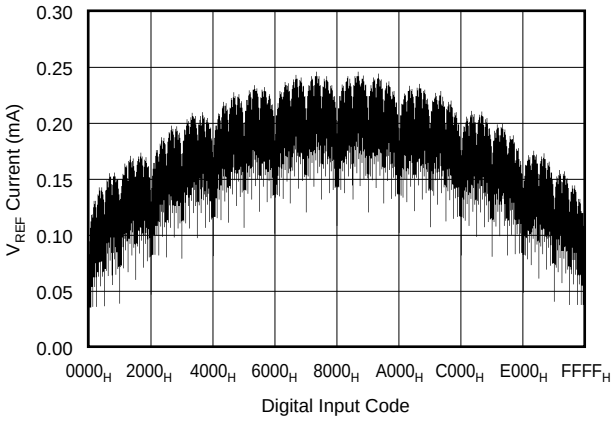
NEGATIVE FULL-SCALE ERROR vs TEMPERATURE



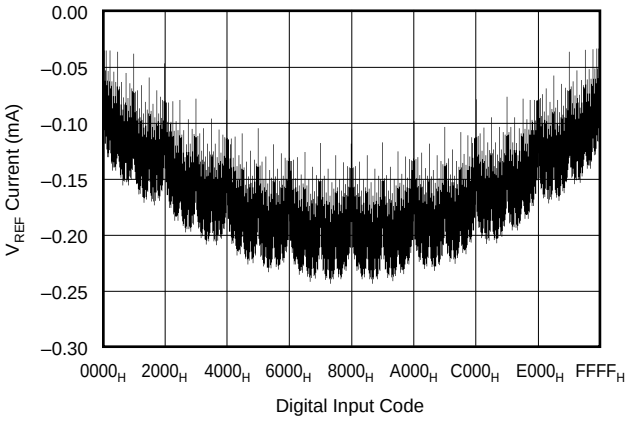
POSITIVE FULL-SCALE ERROR vs TEMPERATURE



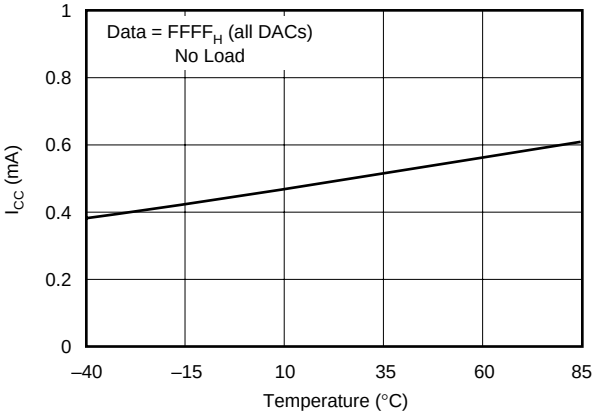
V_{REF}H CURRENT vs CODE
(all DACs sent to indicated code)



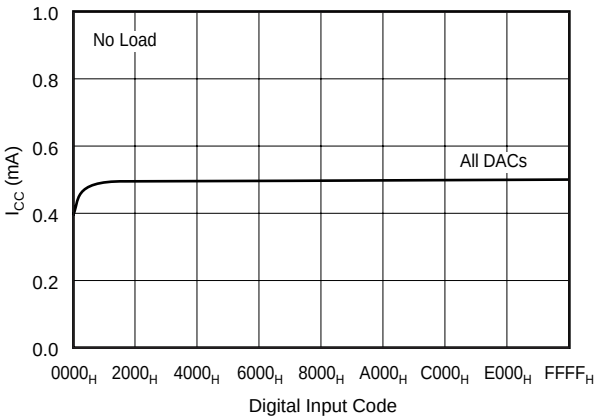
V_{REF}L CURRENT vs CODE
(all DACs sent to indicated code)



SUPPLY CURRENT vs TEMPERATURE



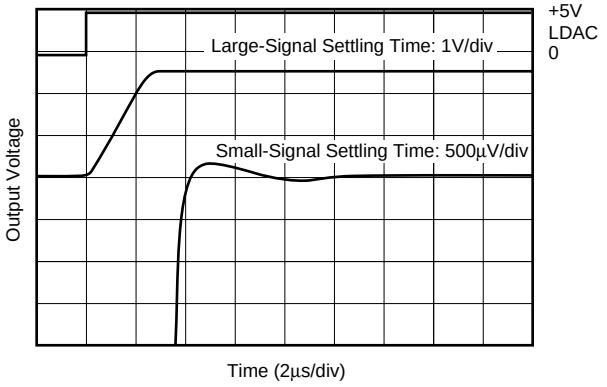
SUPPLY CURRENT vs DIGITAL INPUT CODE



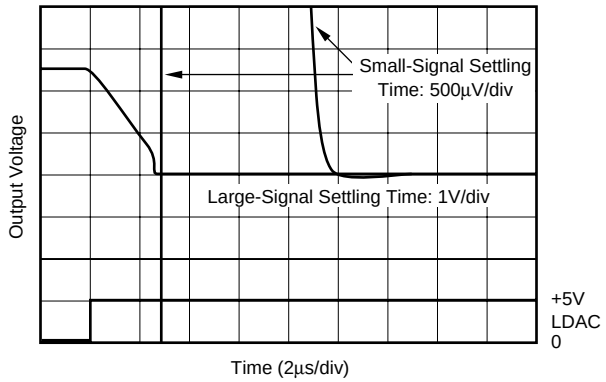
TYPICAL CHARACTERISTICS: V_{SS} = 0V (Cont.)

At T_A = +25°C, V_{CC} = +5V, V_{SS} = 0V, $V_{REF}H$ = +2.5V, $V_{REF}L$ = 0V, representative unit, unless otherwise specified.

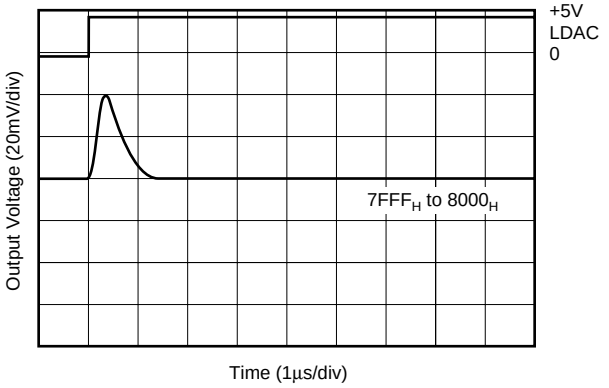
OUTPUT VOLTAGE vs SETTLING TIME
(0V to +2.5V)



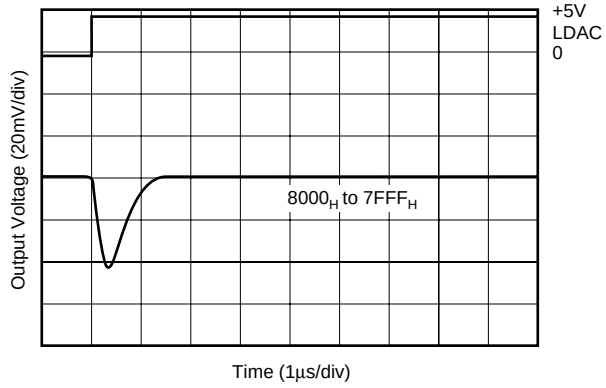
OUTPUT VOLTAGE vs SETTLING TIME
(+2.5V to 2mV)



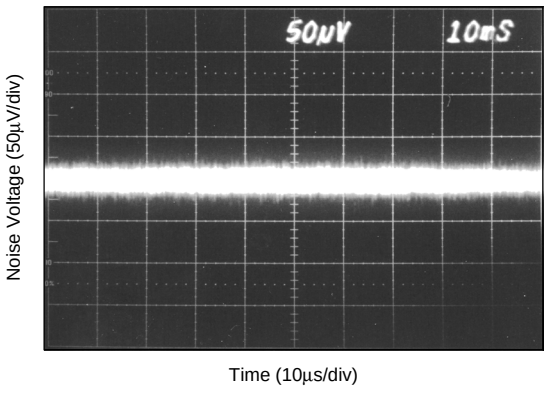
OUTPUT VOLTAGE
vs MIDSCALE GLITCH PERFORMANCE



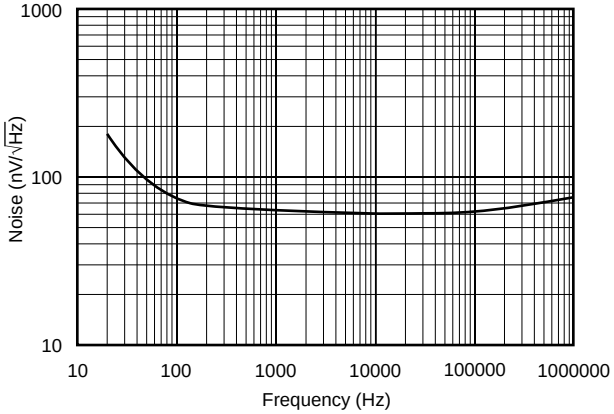
OUTPUT VOLTAGE
vs MIDSCALE GLITCH PERFORMANCE



BROADBAND NOISE



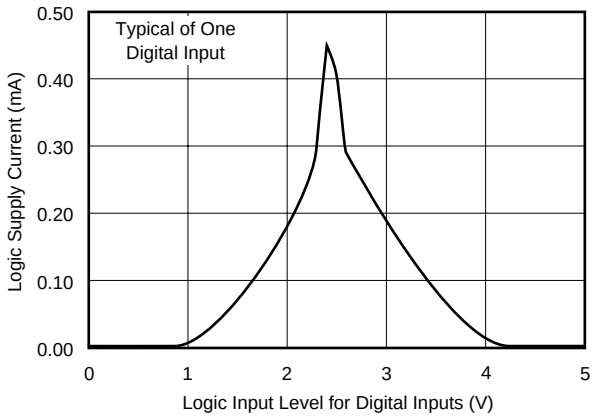
OUTPUT NOISE VOLTAGE vs FREQUENCY



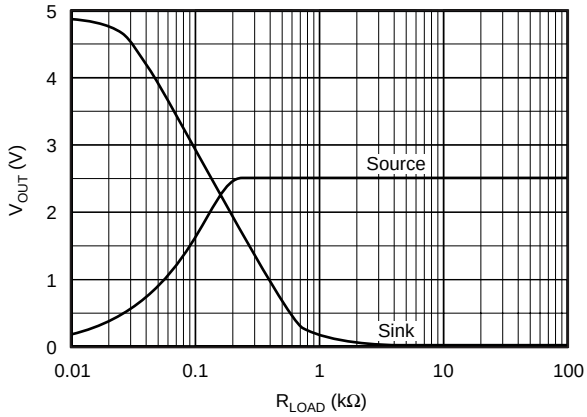
TYPICAL CHARACTERISTICS: V_{SS} = 0V (Cont.)

At T_A = +25°C, V_{CC} = +5V, V_{SS} = 0V, $V_{REF}H$ = +2.5V, $V_{REF}L$ = 0V, representative unit, unless otherwise specified.

LOGIC SUPPLY CURRENT
vs LOGIC INPUT LEVEL FOR DIGITAL INPUTS



V_{OUT} vs R_{LOAD}

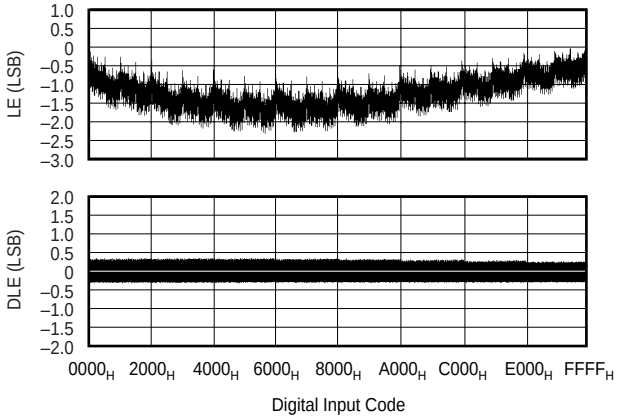


V_{SS} = –5V

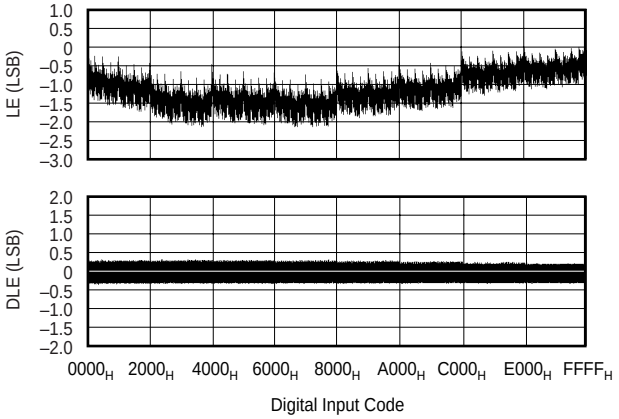
At T_A = +25°C, V_{CC} = +5V, V_{SS} = –5V, $V_{REF}H$ = +2.5V, $V_{REF}L$ = –2.5V, representative unit, unless otherwise specified.

+25°C

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +25°C)

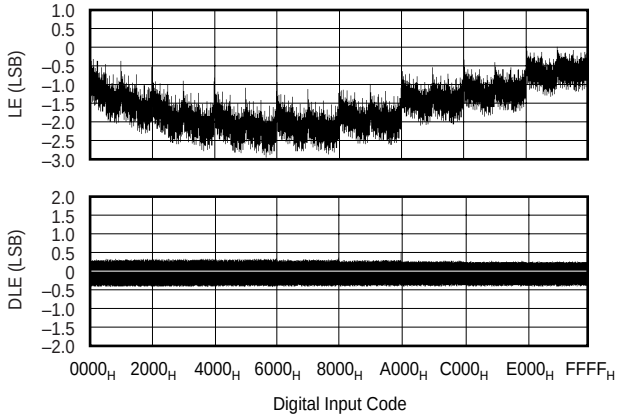


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +25°C)

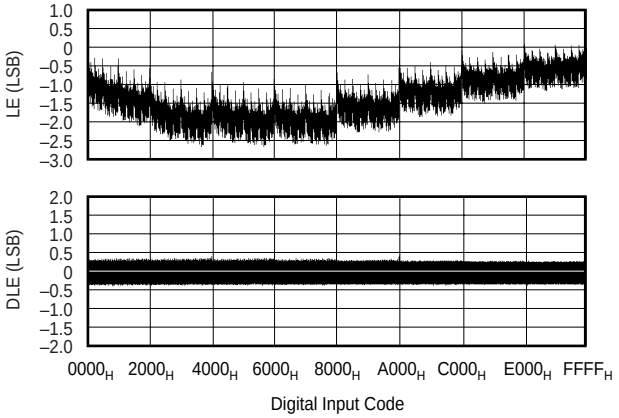


+85°C

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +85°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +85°C)

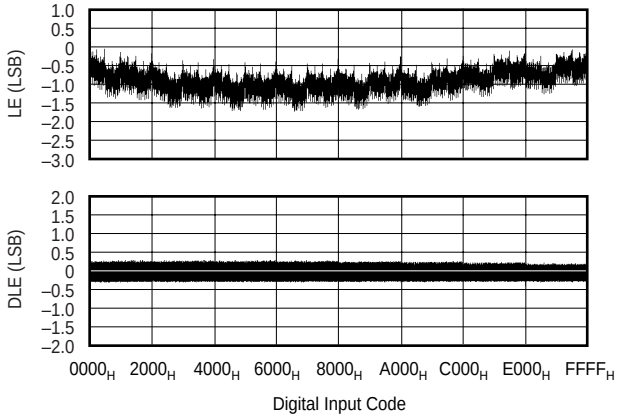


TYPICAL CHARACTERISTICS: V_{SS} = –5V (Cont.)

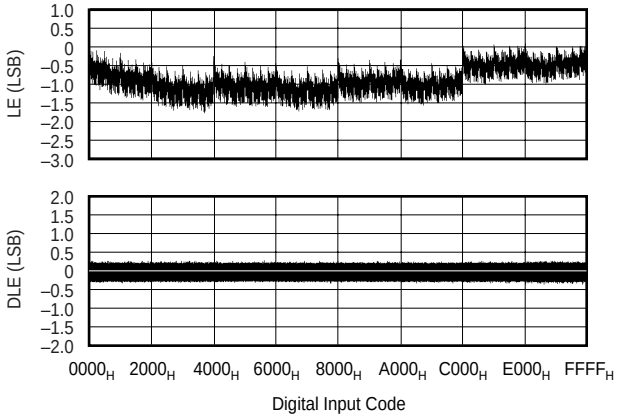
At T_A = +25°C, V_{CC} = +5V, V_{SS} = –5V, $V_{REF}H$ = +2.5V, $V_{REF}L$ = –2.5V, representative unit, unless otherwise specified.

–40°C

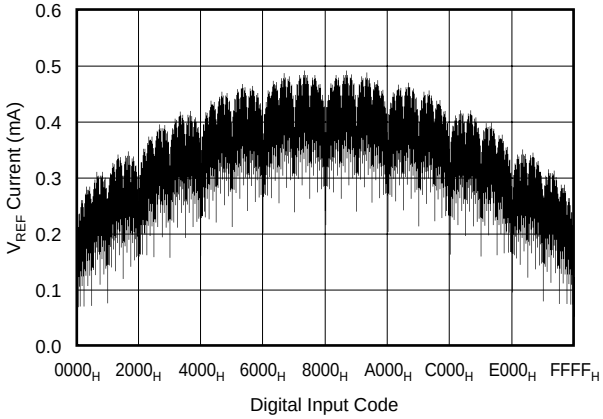
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, –40°C)



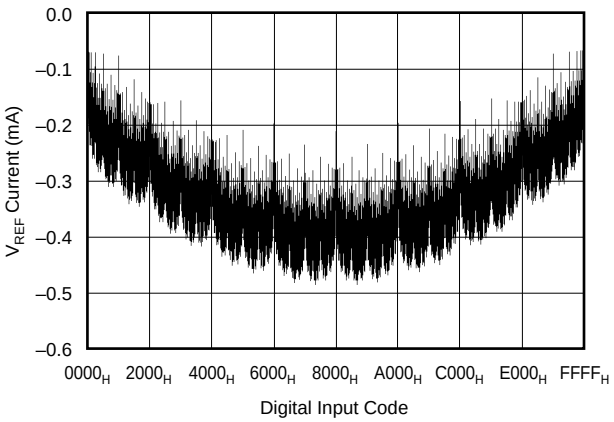
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, –40°C)



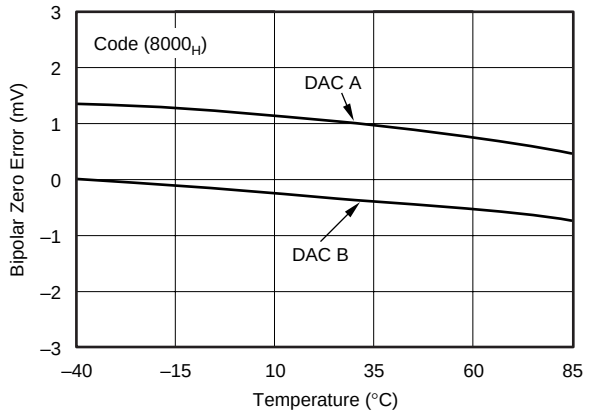
$V_{REF}H$ CURRENT vs CODE
(all DACs sent to indicated code)



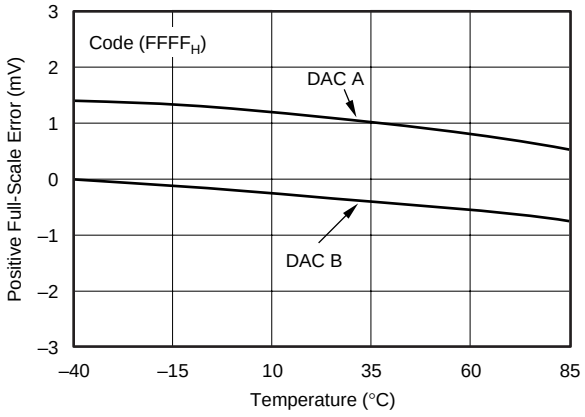
$V_{REF}L$ CURRENT vs CODE
(all DACs sent to indicated code)



BIPOLAR ZERO ERROR vs TEMPERATURE



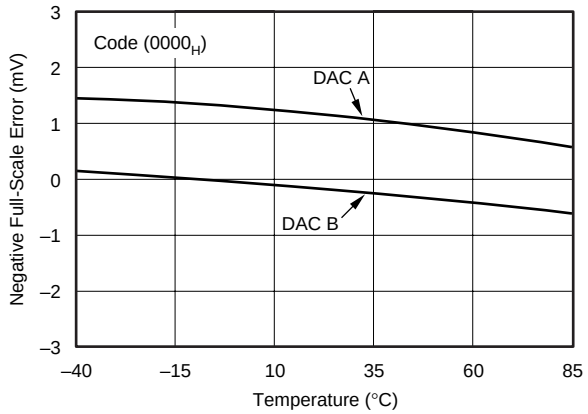
POSITIVE FULL-SCALE ERROR vs TEMPERATURE



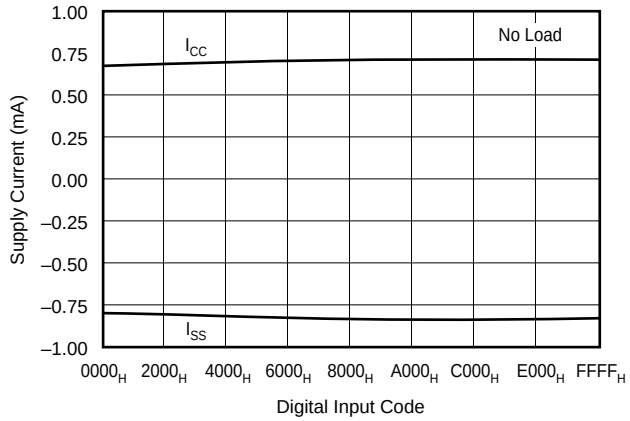
TYPICAL CHARACTERISTICS: V_{SS} = –5V (Cont.)

At T_A = +25°C, V_{CC} = +5V, V_{SS} = –5V, $V_{REF}H$ = +2.5V, $V_{REF}L$ = –2.5V, representative unit, unless otherwise specified.

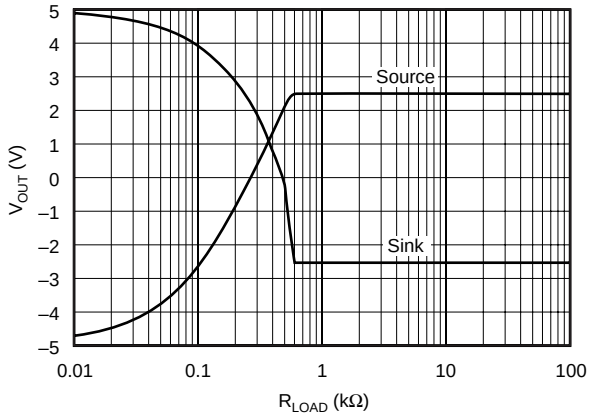
NEGATIVE FULL-SCALE ERROR vs TEMPERATURE



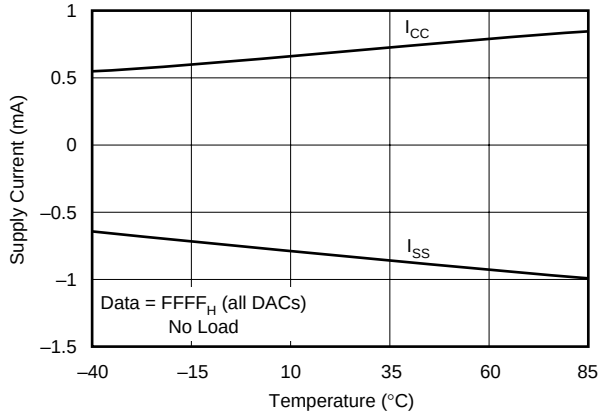
SUPPLY CURRENT vs DIGITAL INPUT CODE



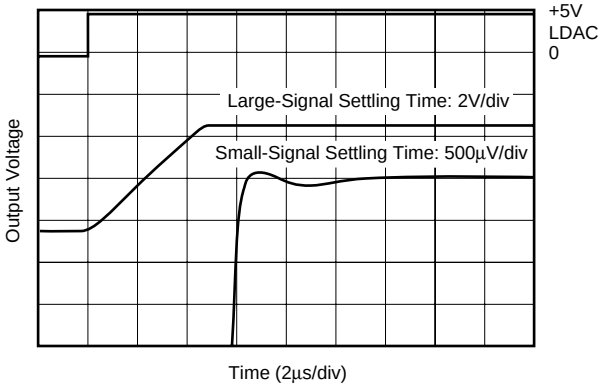
V_{OUT} vs R_{LOAD}



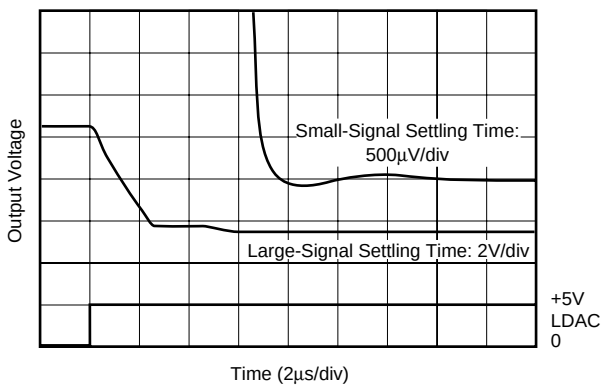
SUPPLY CURRENT vs TEMPERATURE



OUTPUT VOLTAGE vs SETTLING TIME
(–2.5V to +2.5V)

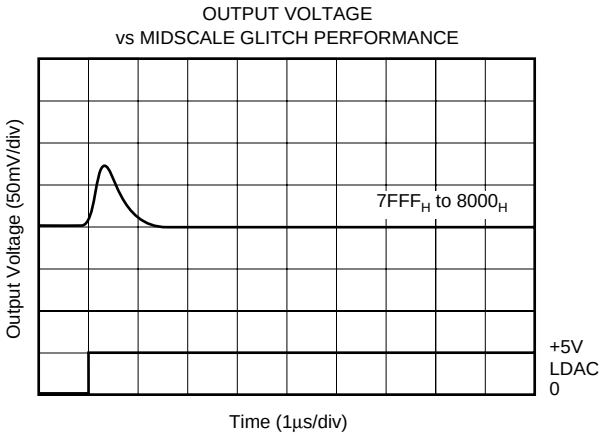


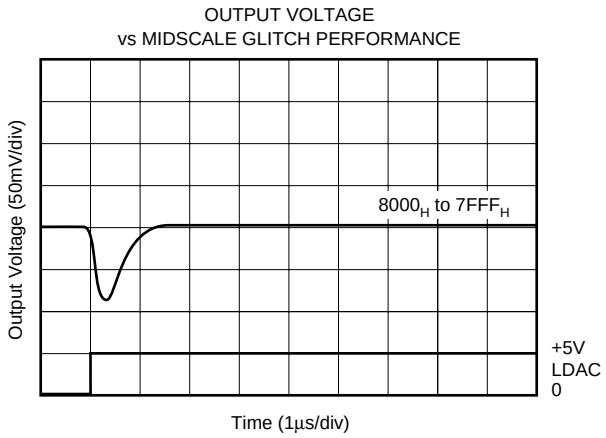
OUTPUT VOLTAGE vs SETTLING TIME
(+2.5V to –2.5V)



TYPICAL CHARACTERISTICS: V_{SS} = –5V (Cont.)

At T_A = +25°C, V_{CC} = +5V, V_{SS} = –5V, $V_{REF}H$ = +2.5V, $V_{REF}L$ = –2.5V, representative unit, unless otherwise specified.





THEORY OF OPERATION

The DAC7642 and DAC7643 are dual channel, voltage output, 16-bit DACs. The architecture is an R-2R ladder configuration with the three MSB's segmented followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network, segmented MSBs, and output op amp, as shown in Figure 1. The minimum voltage output (zero-scale) and maximum voltage output (full-scale) are set by the external voltage references $V_{REF}L$ and $V_{REF}H$, respectively. The digital input is a 16-bit parallel word and the DAC input registers offer a readback capability. The converters can be powered from either a single +5V supply or a dual ±5V supply. Each device offers a reset function which immediately sets all DAC output voltages, DAC registers and Input registers to mid-scale, code 8000$_H$ (DAC7642), or to zero-scale, code 0000$_H$ (DAC7643). See Figures 2 and 3 for the basic configurations of the DAC7642 and DAC7643.

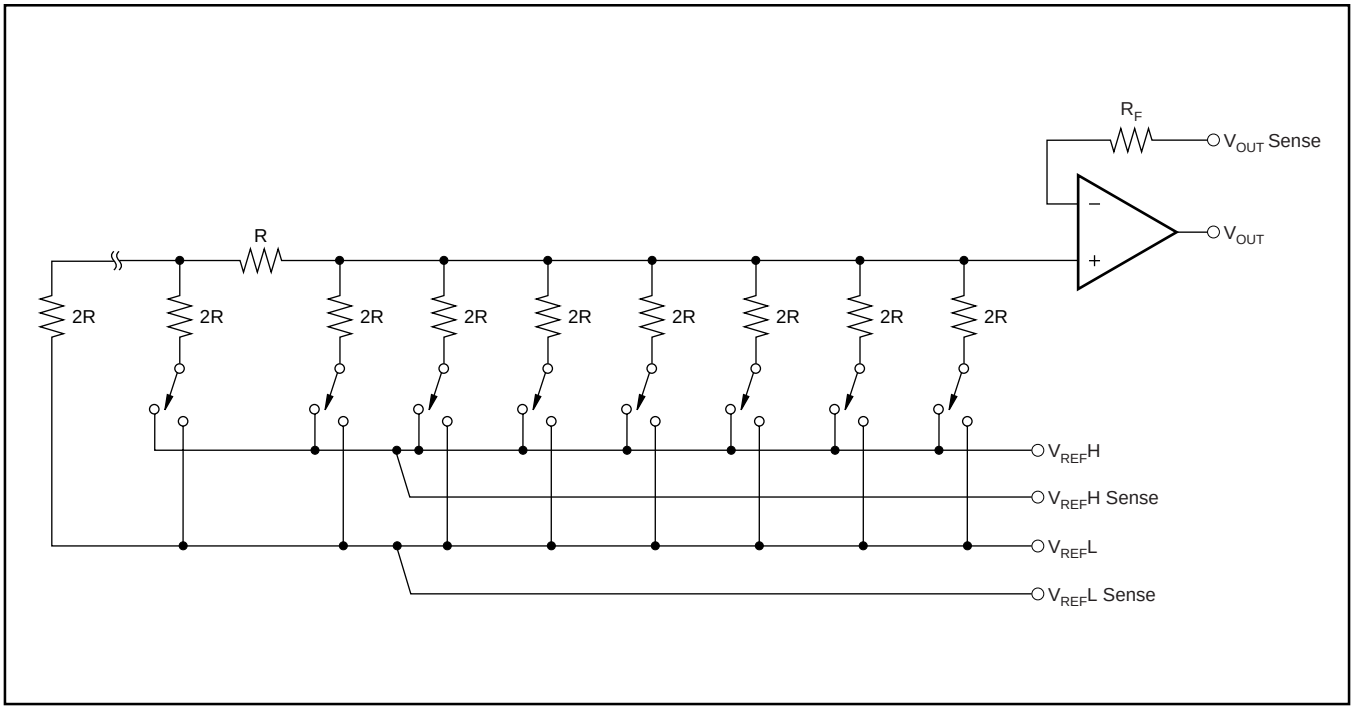


FIGURE 1. DAC7642 and DAC7643 Architecture.

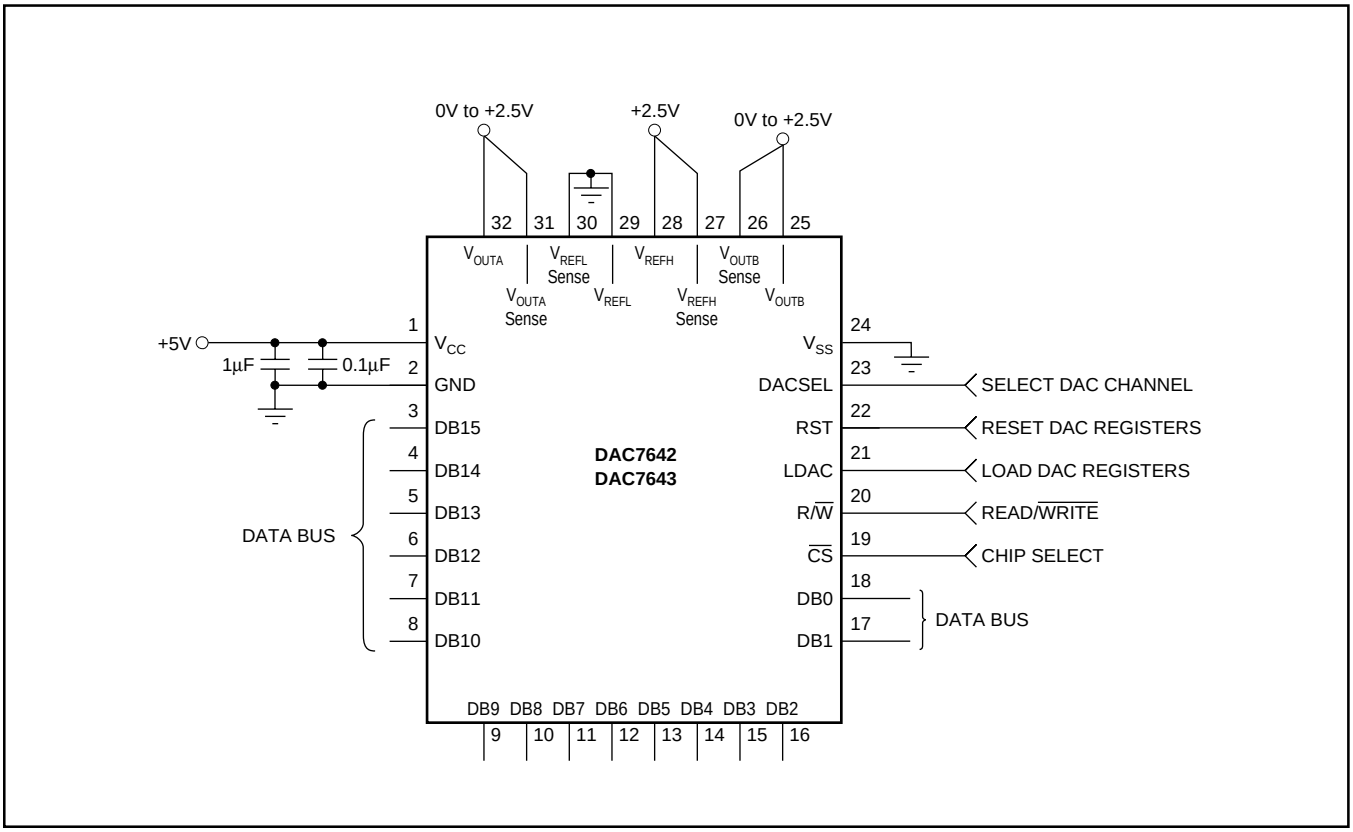


FIGURE 2. Basic Single-Supply Operation of the DAC7642 and DAC7643.

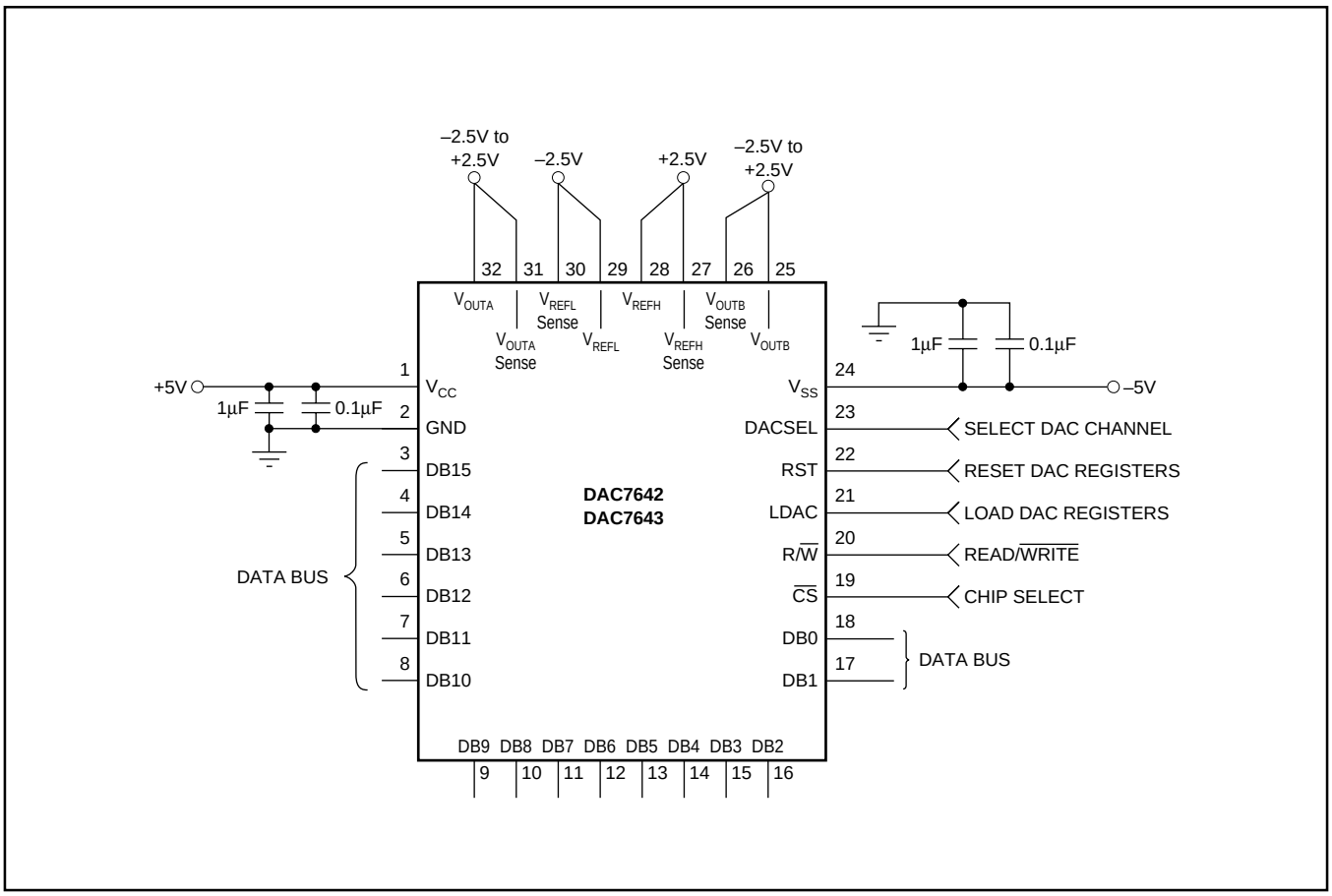


FIGURE 3. Basic Dual-Supply Operation of the DAC7642 and DAC7643.

ANALOG OUTPUTS

When V_{SS} = –5V (dual-supply operation), the output amplifier can swing to within 2.25V of the supply rails over the –40°C to +85°C temperature range. When V_{SS} = 0V (single-supply operation), and with R_{LOAD} also connected to ground, the output can swing to ground. Care must also be taken when measuring the zero-scale error when V_{SS} = 0V. Since the DAC output cannot swing below ground, the output voltage may not change for the first few digital input codes (0000_H, 0001_H, 0002_H, etc.) if the output amplifier has a negative offset. At the negative limit of –2mV, the first specified output starts at code 0040_H.

Due to the high accuracy of these DACs, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 2.5V full-scale range has a 1LSB value of 38μV. With a load current of 1mA, a series wiring and connector resistance of only 40mΩ (R_{W2}) will cause a voltage drop of 40μV, as shown in Figure 4. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 1mA load, a 10 milli-inch wide printed circuit conductor 600 milli-inches long will result in a voltage drop of 30μV.

The DAC7642 and DAC7643 offer a force and sense output configuration for the high open-loop gain output amplifiers. This feature allows the loop around the output amplifier to be closed at the load (shown in Figure 4), thus ensuring an accurate output voltage.

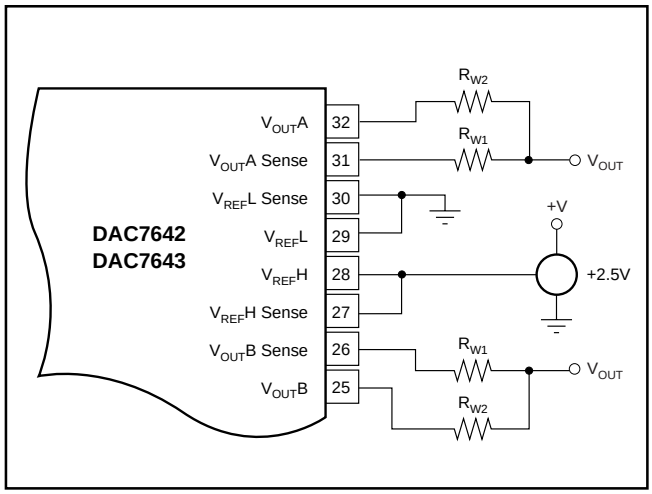


FIGURE 4. Analog Output Closed-Loop Configuration. R_W represents wiring resistances.

REFERENCE INPUTS

The reference inputs, V_{REF}L and V_{REF}H, can be any voltage between V_{SS} + 2.5V and V_{CC} – 2.5V provided that V_{REF}H is at least 1.25V greater than V_{REF}L. The minimum output of each DAC is equal to V_{REF}L plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to V_{REF}H plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of –4.75V to –5.25V. The voltage on V_{SS} sets several bias points within the converter. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device may be affected.

The current into the V_{REF}H input and out of V_{REF}L depends on the DAC output voltages and can vary from a few microamps to approximately 0.5mA. The reference input appears as a varying load to the reference. If the references applied can sink or source the required current, a reference buffer is not required. The DAC7642 and DAC7643 feature reference drive and sense connections such that the internal errors caused by the changing reference current and the circuit impedances can be minimized. Figures 5 through 13 show different reference configurations and the effect on the linearity and differential linearity.

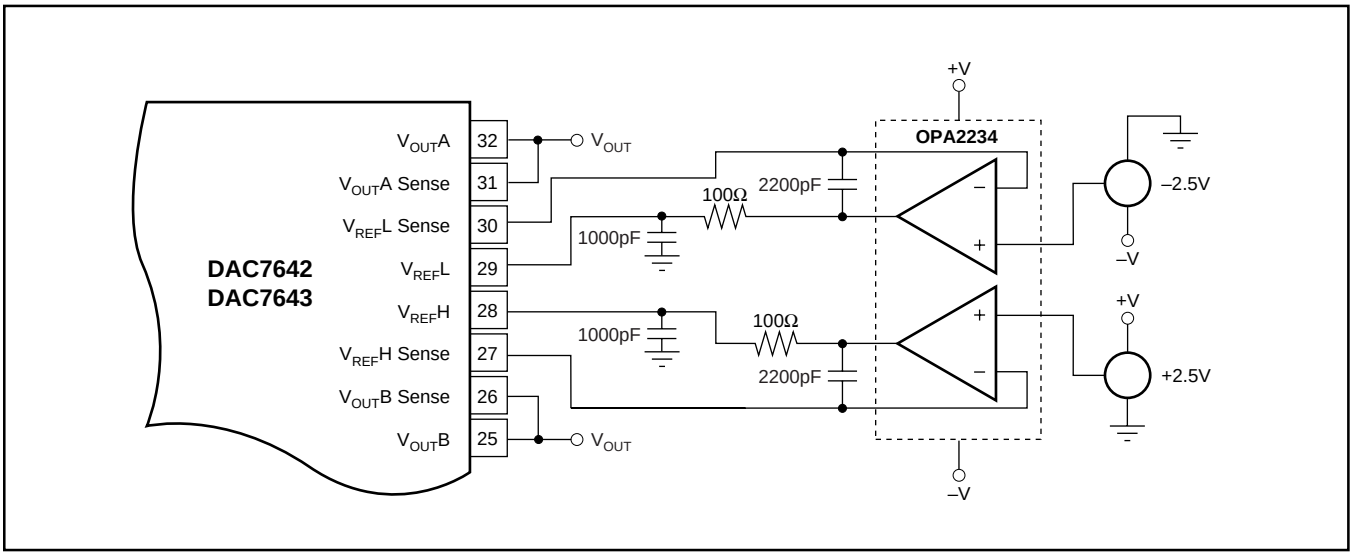


FIGURE 5. Dual Supply Configuration-Buffered References, Used for Dual-Supply Characteristic Curves.

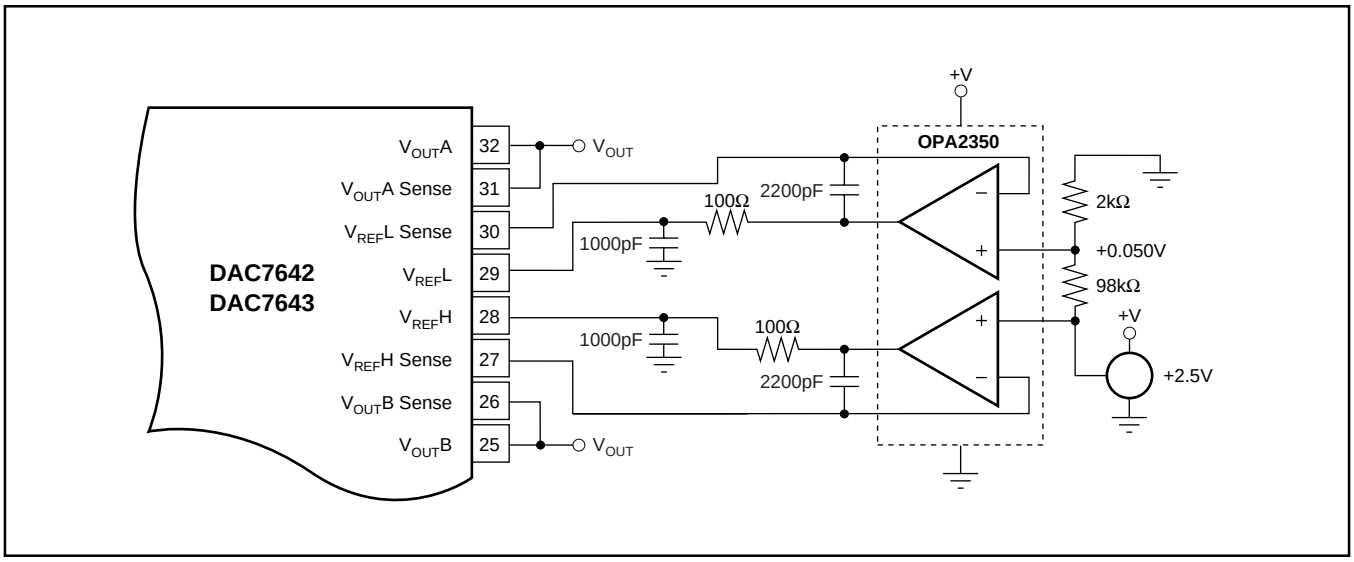


FIGURE 6. Single-Supply Buffered Reference with $V_{REF}L$ of 50mV.

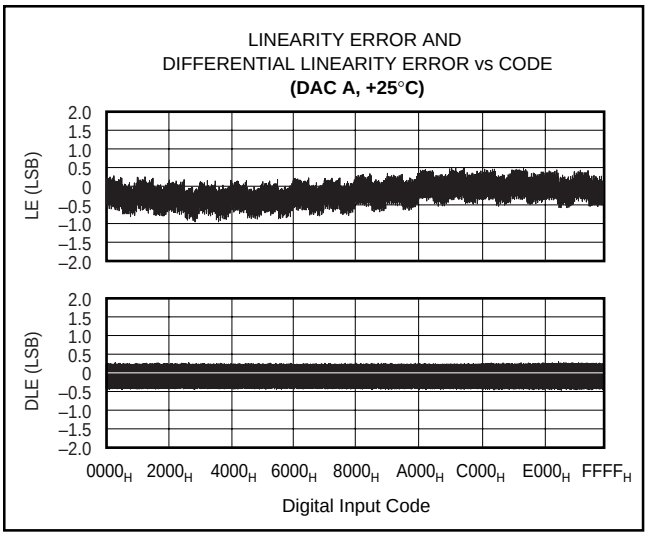


FIGURE 7. Integral Linearity and Differential Linearity Error Curves for Figure 6.

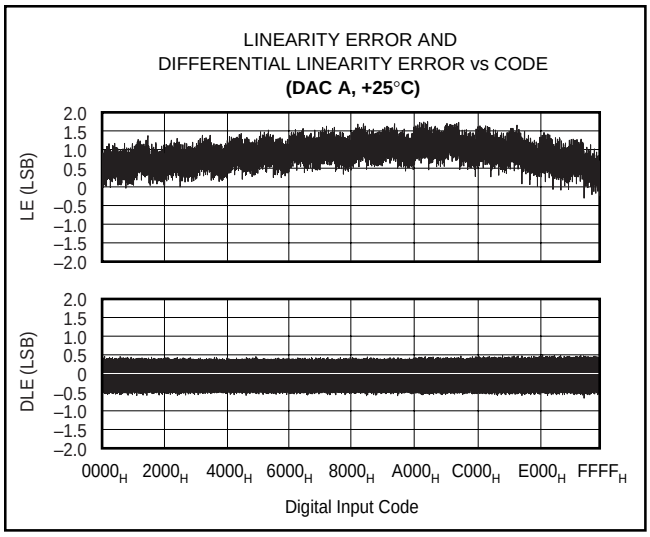


FIGURE 8. Integral Linearity and Differential Linearity Error Curves for Figure 9.

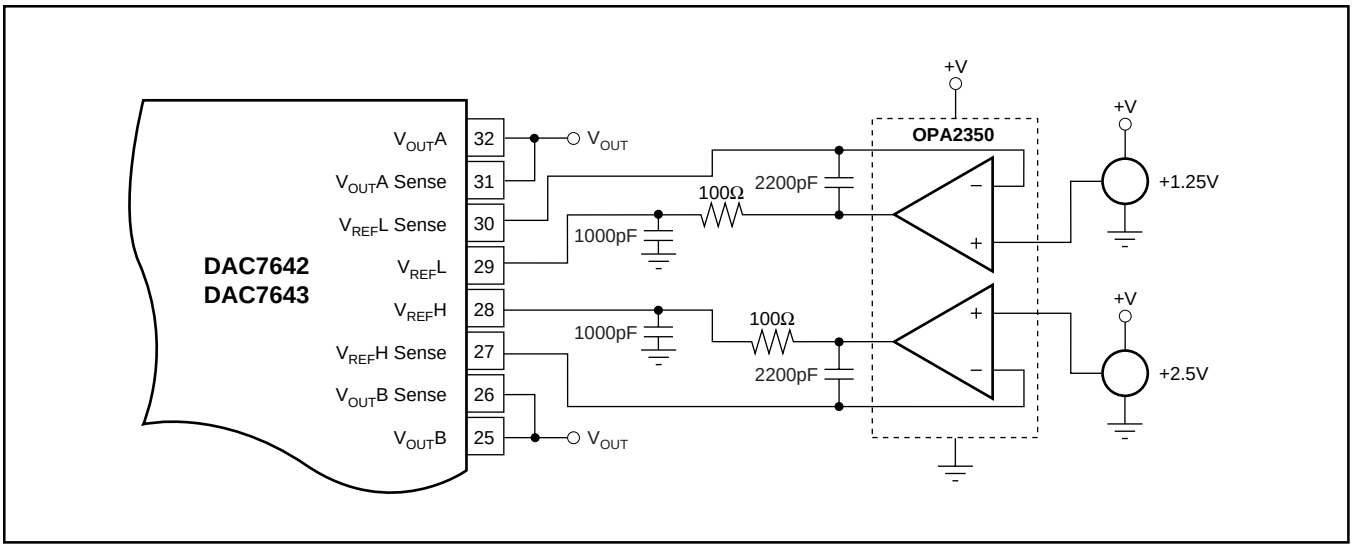


FIGURE 9. Single-Supply Buffered Reference with $V_{REF}L$ = +1.25V and $V_{REF}H$ = +2.5V.

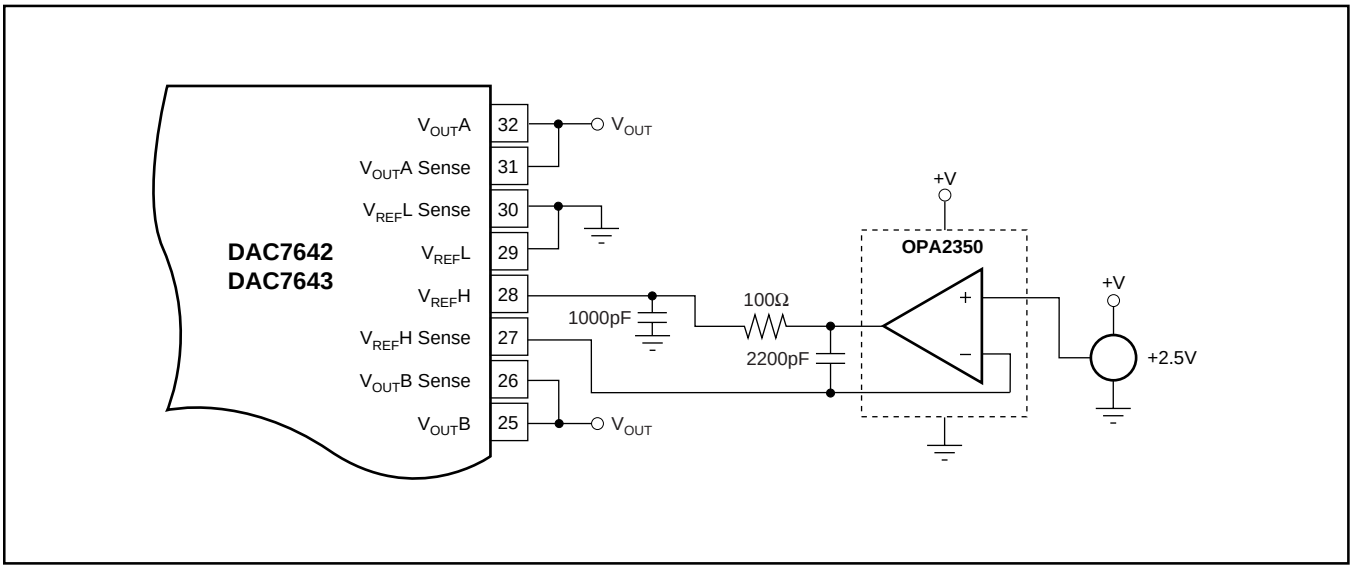


FIGURE 10. Single-Supply Buffered V_{REF}H.

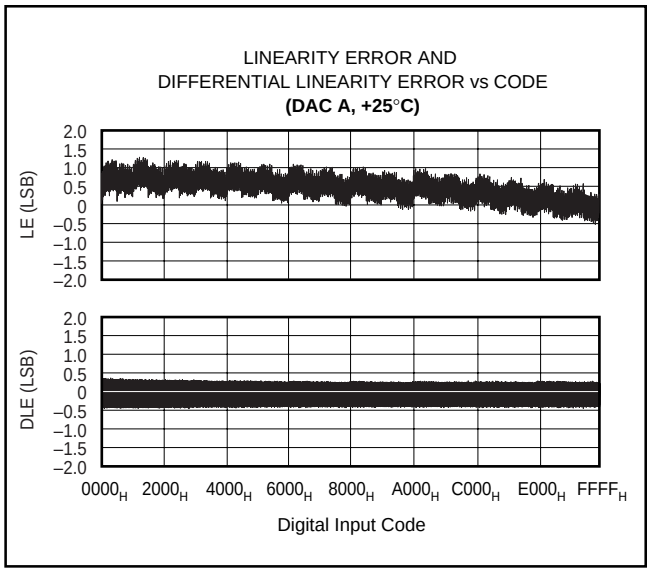


FIGURE 11. Linearity and Differential Linearity Error Curves for Figure 10.

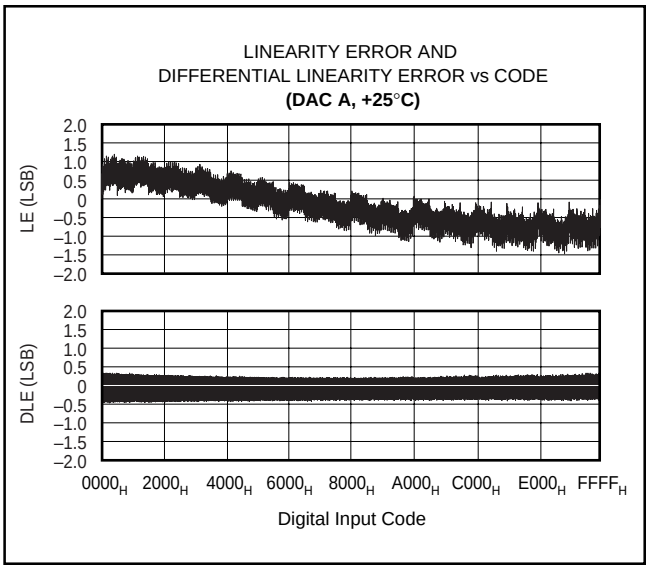


FIGURE 13. Linearity and Differential Linearity Error Curves for Figure 12.

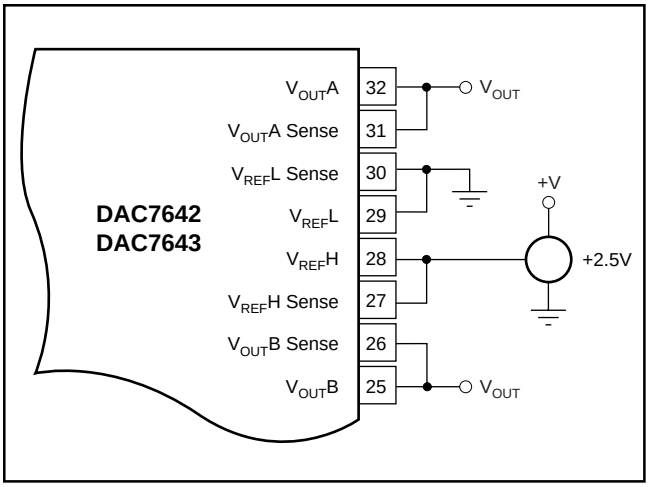


FIGURE 12. Low-Cost Single-Supply Configuration.

DIGITAL INTERFACE

See Table I for the basic control logic of the DAC7642 and DAC7643. Note that each internal register is edge triggered and not level triggered. When the LOADDACS signal is transitioned from LOW to HIGH, the digital word existing in the input register is latched into the DAC register. The first set of registers (the input registers) are triggered via the $\overline{DAC}$SEL, $\overline{R/W}$, and $\overline{CS}$ inputs. Only one of these registers can be transparent at any given time.

The double-buffered architecture is designed mainly so each DAC input register can be written to at any time without affecting the DAC outputs. All DAC voltages are updated simultaneously by the rising edge of LOADDACS. It also allows multiple devices to be updated simultaneously by sharing the LOADDACS control from the host with each device.

DACSEL	R/$\overline{W}$	$\overline{CS}$	RST	LOADDACS	INPUT REGISTER	DAC REGISTER	MODE	DAC
L	L	L	L, H	X	Write	Hold	Write Input	A
H	L	L	L, H	X	Write	Hold	Write Input	B
L	H	L	L, H	X	Read	Hold	Read Input	A
H	H	L	L, H	X	Read	Hold	Read Input	B
X	X	H	L, H	↑	Hold	Write	Update	All
X	X	H	L, H	L, H	Hold	Hold	Hold	All
X	X	X	↑	L, H	Reset	Reset	Reset	All

TABLE I. DAC7642 and DAC7643 Logic Truth Table.

DIGITAL TIMING

Figure 14 and Table II provide detailed timing for the digital interface of the DAC7642 and DAC7643.

DIGITAL INPUT CODING

The DAC7642 and DAC7643 input data is in Straight Binary format. The output voltage is given by Equation 1:

$$V_{OUT} = V_{REF}L + \frac{(V_{REF}H - V_{REF}L) \bullet N}{65,536} \quad (1)$$

where N is the digital input code. This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

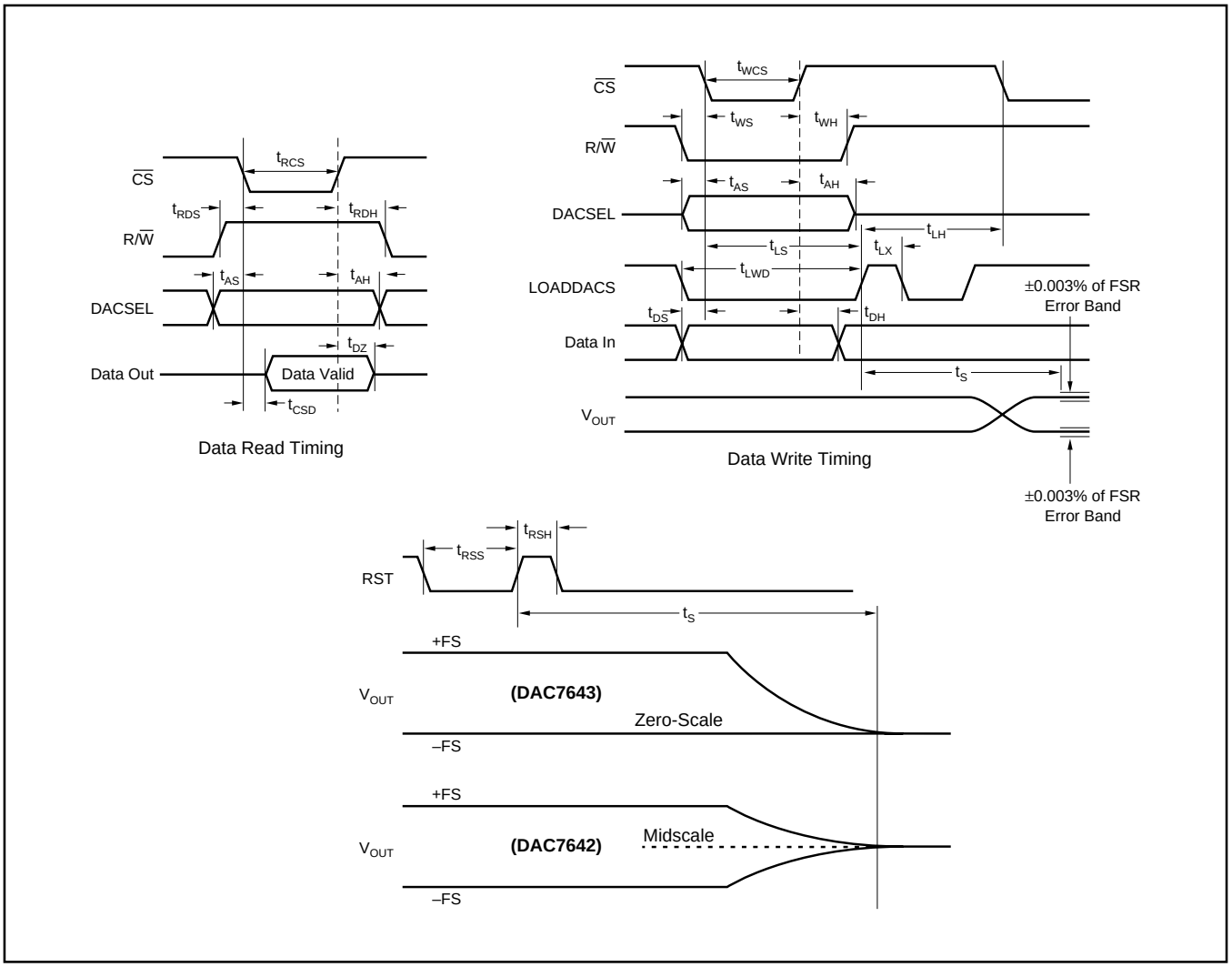


FIGURE 14. Digital Input and Output Timing.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{RCS}	$\overline{CS}$ LOW for Read	150			ns
t_{RDS}	R/$\overline{W}$ HIGH to $\overline{CS}$ LOW	10			ns
t_{RDH}	R/$\overline{W}$ HIGH after $\overline{CS}$ HIGH	10			ns
t_{DZ}	$\overline{CS}$ HIGH to Data Bus in High Impedance	10		100	ns
t_{CSD}	$\overline{CS}$ LOW to Data Bus Valid		100	150	ns
t_{WCS}	$\overline{CS}$ LOW for Write	40			ns
t_{WS}	R/$\overline{W}$ LOW to $\overline{CS}$ LOW	0			ns
t_{WH}	R/$\overline{W}$ LOW after $\overline{CS}$ HIGH	10			ns
t_{AS}	DACSEL Valid to $\overline{CS}$ LOW	0			ns
t_{AH}	DACSEL Valid after $\overline{CS}$ HIGH	10			ns
t_{LS}	$\overline{CS}$ LOW to LOADDACS HIGH	30			ns
t_{LH}	$\overline{CS}$ LOW after LOADDACS HIGH	100			ns
t_{LX}	LOADDACS HIGH	100			ns
t_{DS}	Data Valid to $\overline{CS}$ LOW	0			ns
t_{DH}	Data Valid after $\overline{CS}$ HIGH	10			ns
t_{LWD}	LOADDACS LOW	100			ns
t_{RSS}	RESET LOW	10			ns
t_{RSH}	RESET HIGH	10			ns
t_S	Settling Time			10	µs

TABLE II. Timing Specifications (T_A = –40°C to +85°C).

DIGITALLY-PROGRAMMABLE CURRENT SOURCE

The DAC7642 and DAC7643 offer a unique set of features that allows a wide range of flexibility in designing applications circuits, such as programmable current sources. The DAC7642 and DAC7643 offer both a differential reference input, as well as an open-loop configuration around the output amplifier. The open-loop configuration around the output amplifier allows a transistor to be placed within the loop to implement a digitally-programmable, unidirectional current source. The availability of a differential reference also allows programmability for both the full-scale and zero-scale currents. The output current is calculated as:

$$I_{OUT} = \left(\left(\frac{V_{REF}H - V_{REF}L}{R_{SENSE}}\right) \bullet \left(\frac{N\ Value}{65,536}\right)\right) + \left(V_{REF}L / R_{SENSE}\right) \quad (2)$$

Figure 15 shows a DAC7642 and DAC7643 in a 4-20mA current output configuration. The output current can be determined by Equation 3:

$$I_{OUT} = \left(\left(\frac{2.5V - 0.5V}{125\Omega}\right) \bullet \left(\frac{N\ Value}{65,536}\right)\right) + \left(\frac{0.5V}{125\Omega}\right) \quad (3)$$

At full-scale, the output current is 16mA plus the 4mA for the zero current. At zero scale the output current is the offset current of 4mA (0.5V/125Ω).

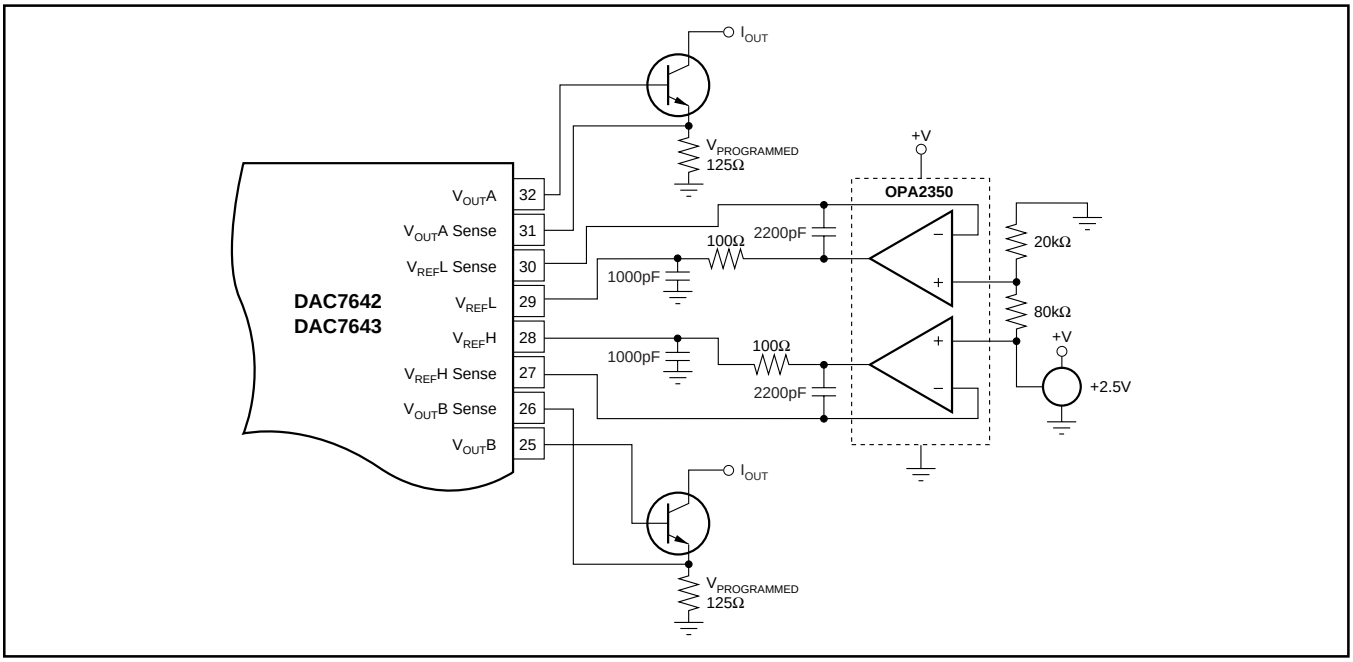
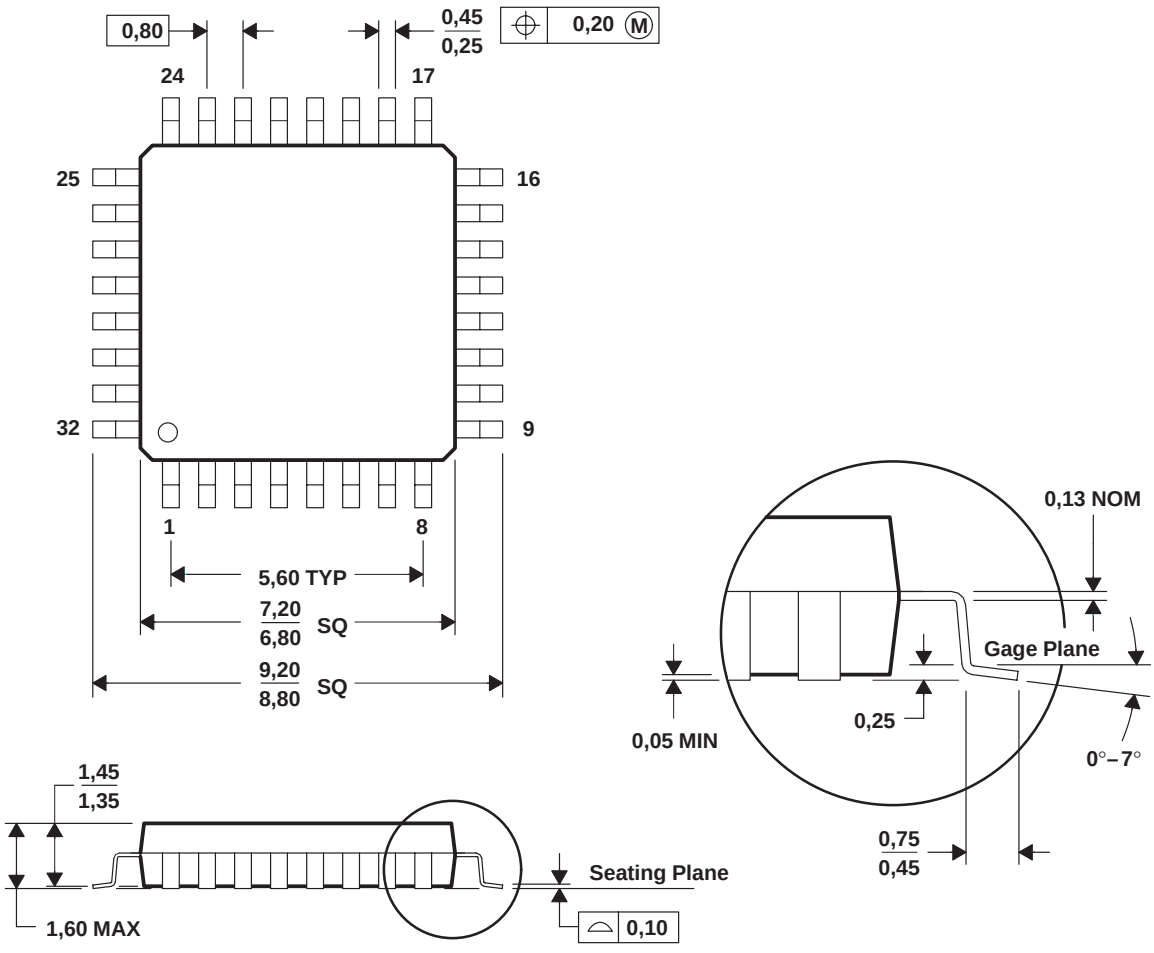


FIGURE 15. 4-20mA Digitally Controlled Current Source.

VF (S-PQFP-G32) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7642VFBT	ACTIVE	LQFP	VF	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DAC7642 B	Samples
DAC7642VFT	ACTIVE	LQFP	VF	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DAC7642	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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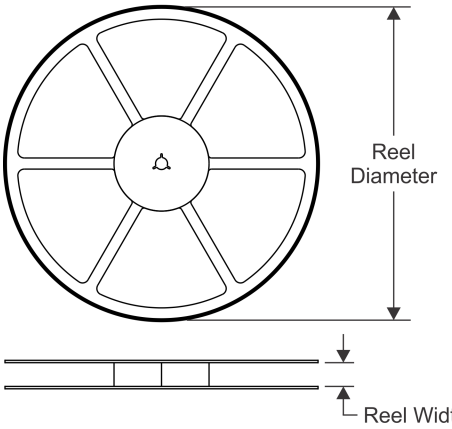
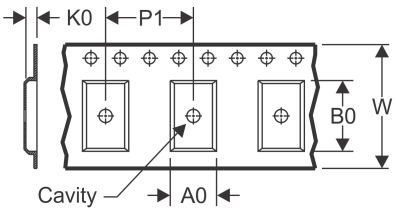
TAPE AND REEL INFORMATION

REEL DIMENSIONS

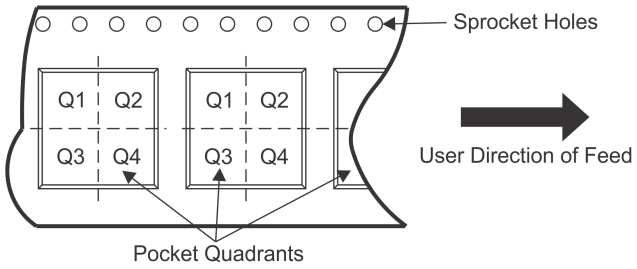


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

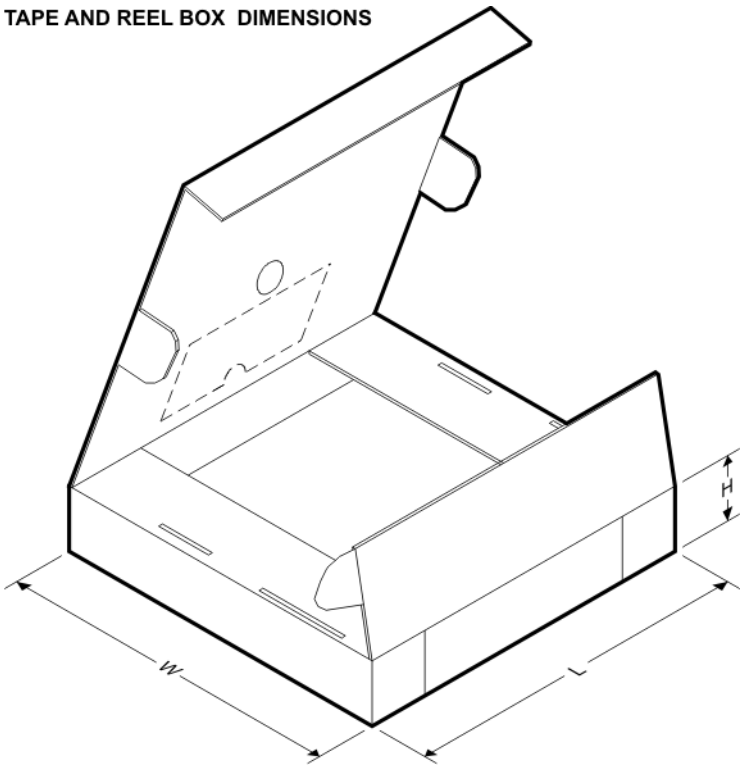
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7642VFBT	LQFP	VF	32	250	180.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
DAC7642VFT	LQFP	VF	32	250	180.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

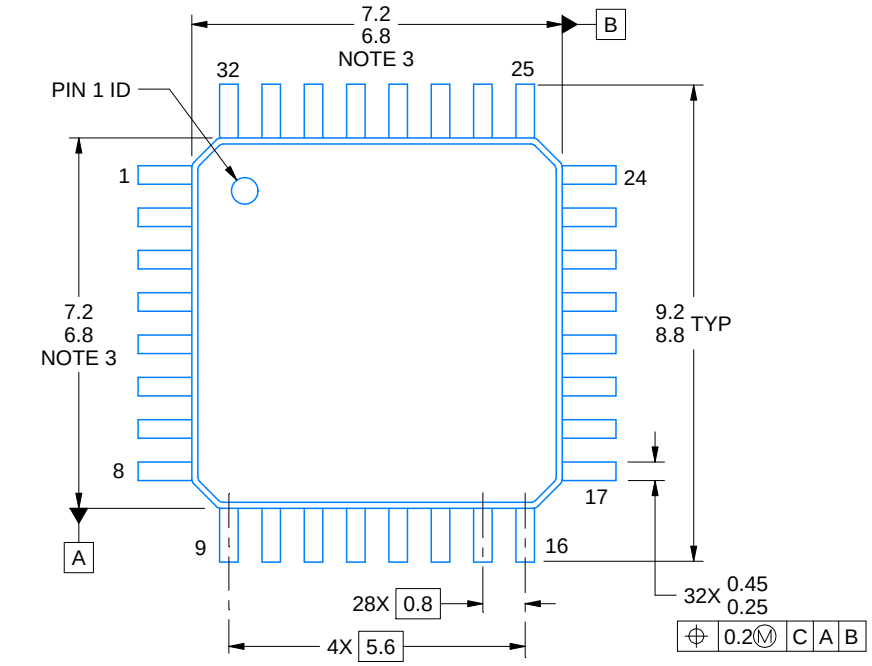
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7642VFBT	LQFP	VF	32	250	213.0	191.0	55.0
DAC7642VFT	LQFP	VF	32	250	213.0	191.0	55.0

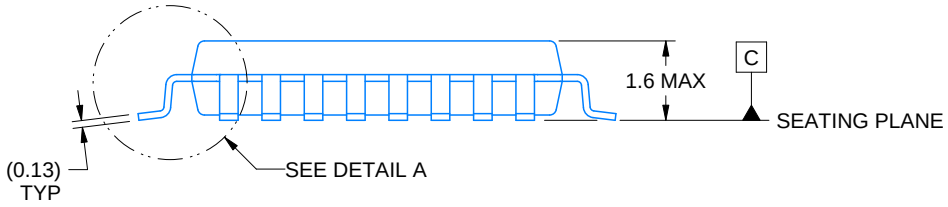
PACKAGE OUTLINE

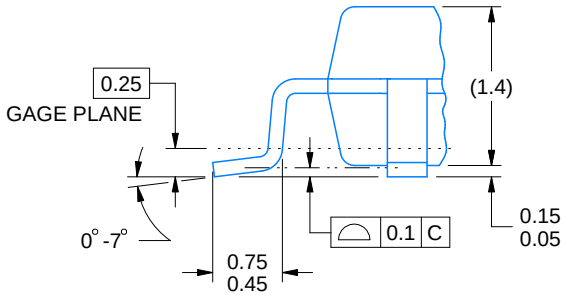
VF0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK







DETAIL A
TYPICAL

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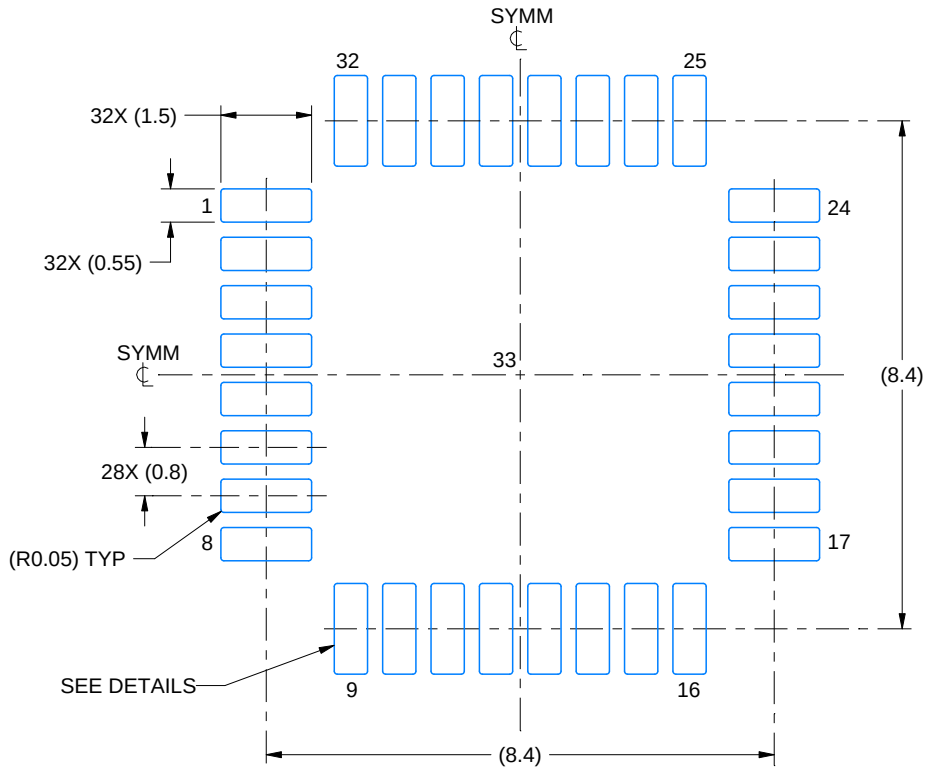
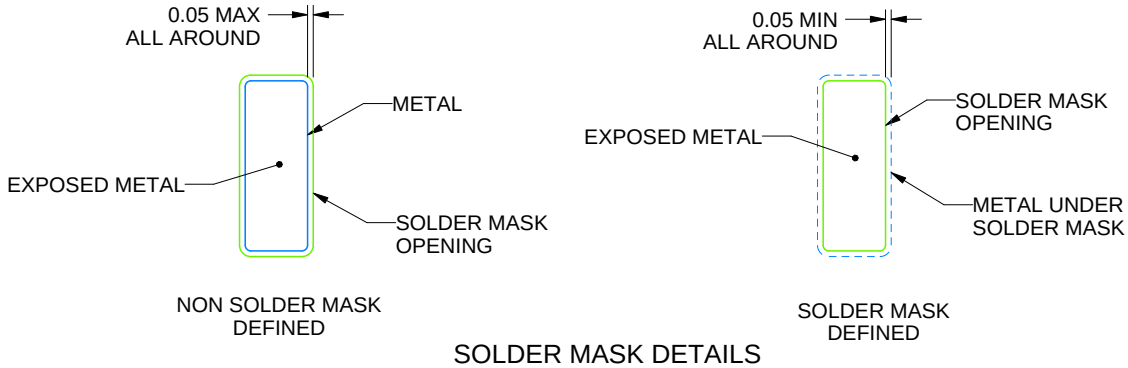
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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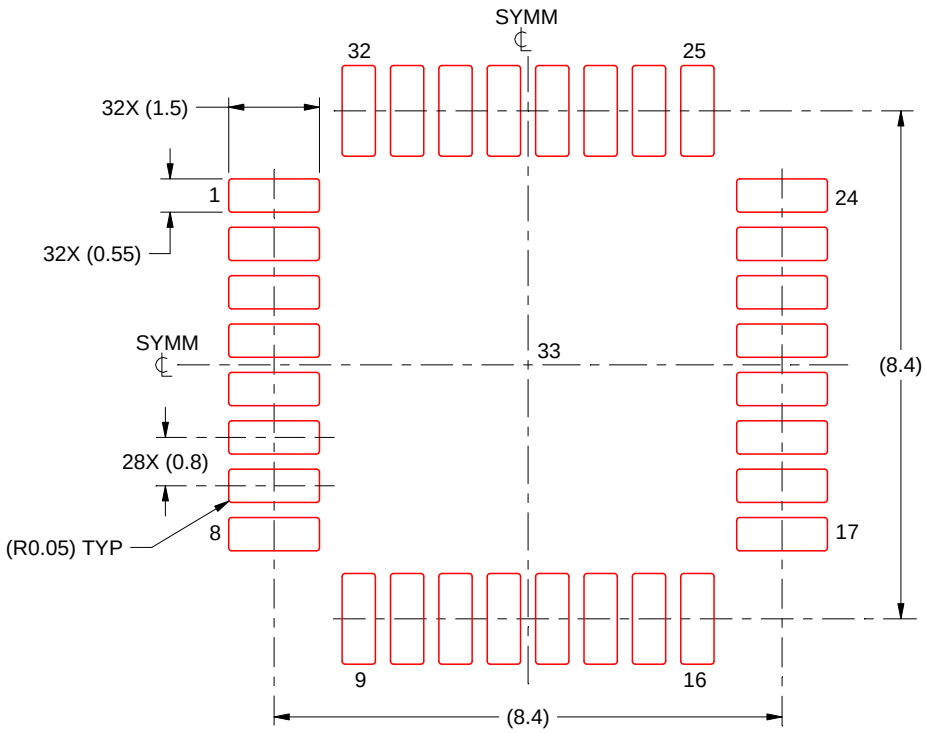
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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