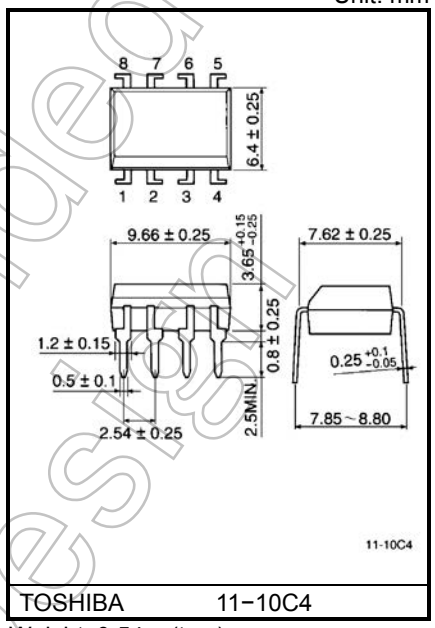
TOSHIBA Photocoupler GaAℓAs Ired & Photo IC

TLP2630

Digital Logic Isolation
Tele−Communication
Analog Data Equipment Control
Microprocessor System Interface

Unit: mm



TOSHIBA 11−10C4

Weight: 0.54 g (typ.)

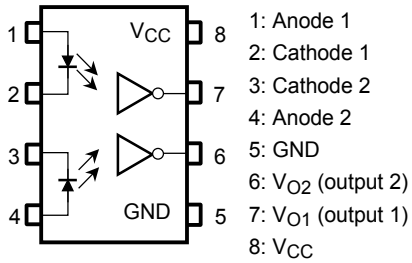
The TOSHIBA TLP2630 dual photocoupler consists of a pair of GaAℓAs light emitting diode and integrated high gain, high speed photodetector.
The output of the detector circuit is an open collector, Schottky clamped transistor. This unit is 8−lead DIP.

- Input current threshold: I_F = 5 mA (max)
- Switching speed: 10MBd
- Guaranteed performance over temperature: 0 to 70°C
- Isolation voltage: 2500 V_{rms} (min)
- UL recognized: UL1577, file no. E67349
- cUL approved :CSA Component Acceptance Service
  No. 5A, File No.E67349

Truth Table (positive logic)

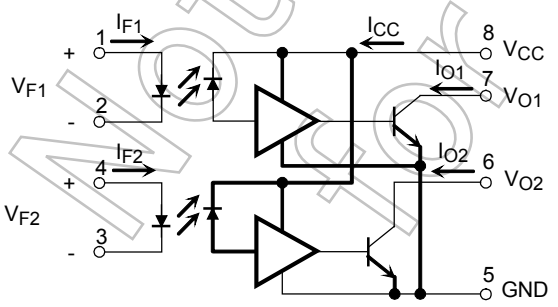
Input	Output
H	L
L	H

Pin Configuration (top view)



1: Anode 1
2: Cathode 1
3: Cathode 2
4: Anode 2
5: GND
6: V_{O2} (output 2)
7: V_{O1} (output 1)
8: V_{CC}

Schematic



Note: A 0.1μF bypass capacitor must connected between pins 8 and 5 (see Note 1).

Start of commercial production
1986-03

Absolute Maximum Ratings (no derating required up to 70°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current(each channel)	I_F	20	mA
	Pulse forward current (each channel)*	I_{FP}	30	mA
	Reverse voltage(each channel)	V_R	5	V
	Input power dissipation(each channel)	P_D	25	mW
	Input power dissipation derating (Ta ≥ 70°C) (each channel)	ΔP_D/°C	-0.45	mW/°C
Detector	Output current(each channel)	I_O	16	mA
	Output voltage(each channel)	V_O	−0.5 to 7	V
	Supply voltage (1 minute maximum)	V_{CC}	7	V
	Output power dissipation(each channel)	P_O	40	mW
	Output power dissipation derating (Ta ≥ 70°C) (each channel)	ΔP_O/°C	-0.75	mW/°C
Operating temperature range		T_{stg}	−55 to 125	°C
Storage temperature range		T_{opr}	−40 to 85	°C
Lead soldering temperature (10 s) (Note 1)		T_{sol}	260	°C
Isolation voltage (AC, 1 minute, R.H.≤ 60%, Note 3)		BVs	2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

* t ≤ 1 ms duration.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ.	Max	Unit
Input current, low level, each channel	I_{FL}	0	—	250	μA
Input current, high level, each channel	I_{FH}	6.3*	—	20	mA
Supply voltage**	V_{CC}	4.5	5	5.5	V
Fan out(TTL load, each channel)	N	—	—	8	—
Operating temperature	T_{opr}	0	—	70	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

* 6.3mA is a guard banded value which allows for at least 20% CTR degradation.
Initial input current threshold value is 5 mA or less.

**This item denotes operating ranges, not meaning of recommended operating conditions.

Electrical Characteristics (Ta = 0~70°C, unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ.*	Max	Unit
Input forward voltage (each channel)	V_F	I_F = 10mA, Ta = 25°C	—	1.65	1.75	V
Input diode temperature coefficient(each channel)	$\Delta V_F / \Delta Ta$	I_F = 10mA	—	−2.0	—	mV / °C
Input reverse breakdown voltage(each channel)	BV_R	I_R = 10μA, Ta = 25°C	5	—	—	V
Input capacitance (each channel)	C_T	V_F = 0 V, f = 1MHz	—	45	—	pF
High level output current (each channel)	I_{OH}	V_{CC} = 5.5V, V_O = 5.5V I_F = 250μA	—	1	250	μA
Low level output voltage (each channel)	V_{OL}	V_{CC} = 5.5V, I_F = 5mA I_{OL}(sinking) = 13mA	—	0.4	0.6	V
High level supply current (both channels)	I_{CCH}	V_{CC} = 5.5V, I_F = 0mA	—	14	30	mA
Low level supply current (both channels)	I_{CCL}	V_{CC} = 5.5V, I_F = 10mA	—	24	36	mA
Isolation resistance	R_S	V_S = 500V, R.H.≤ 60% (Note 3)	—	10^{14}	—	Ω
Capacitance (input−output)	C_S	f = 1MHz (Note 3)	—	0.6	—	pF
Input−input leakage current	I_{I-I}	R.H.≤ 60%, t = 5s V_{I-I} = 500V (Note 6)	—	0.005	—	μA
Resistance (input−input)	R_{I-I}	V_{I-I} = 500V (Note 6)	—	10^{11}	—	Ω
Capacitance (input−input)	C_{I-I}	f = 1MHz (Note 6)	—	0.25	—	pF

* All typical values are at V_{CC} = 5V, Ta = 25°C.

Switching Characteristics (Ta =25°C , VCC=5V)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time to low output level	t_{pHL}	1	I_F = 0→7.5mA, R_L = 350Ω C_L = 15pF (each channel)	—	60	75	ns
Propagation delay time to high output level	t_{pLH}	1	I_F = 7.5mA→0, R_L = 350Ω C_L = 15pF (each channel)	—	60	75	ns
Output rise a time,output fall time(10~90%)	t_r,t_f	1	I_F = 0⇄7.5mA, R_L = 350Ω C_L = 15pF (each channel)	—	30	—	ns
Common mode transient immunity at high output level	CM_H	2	I_F = 0 mA, R_L = 350Ω V_{CM} = 200V V_O(min) = 2V (each channel, Note 4)	—	200	—	V / μs
Common mode transient immunity at low output level	CM_L	2	I_F = 7.5mA, R_L = 350Ω V_{CM} = 200V V_O(max) = 0.8V (each channel, Note 5)	—	−500	—	V / μs

(Note 1) 2mm below seating plane.

(Note 2) The VCC supply voltage to each TLP2630 isolator must be bypassed by a 0.1μF capacitor. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package VCC and GND pins each device.

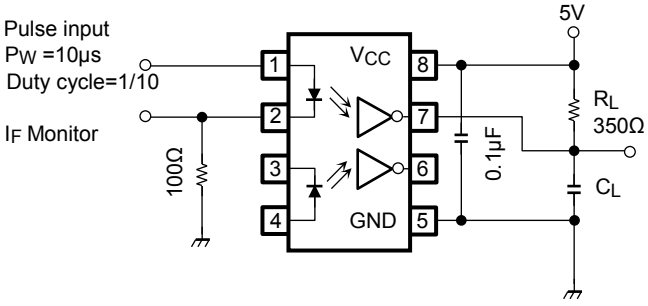
(Note 3) Device considered a two−terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

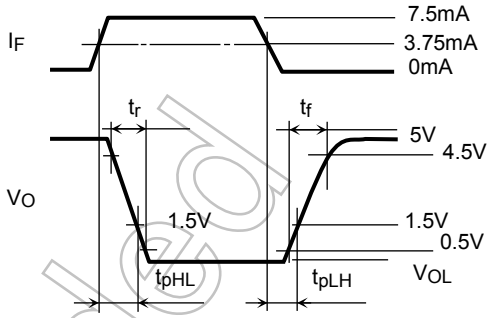
(Note 4) CM_H・the maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state(i.e. V_{OUT} > 2.0V) Measured in volts per microsecond(V / μs).

(Note 5) CM_L・the maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state(i.e. V_{OUT} < 0.8V) Measured in volts per microsecond(V / μs).

(Note 6) Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

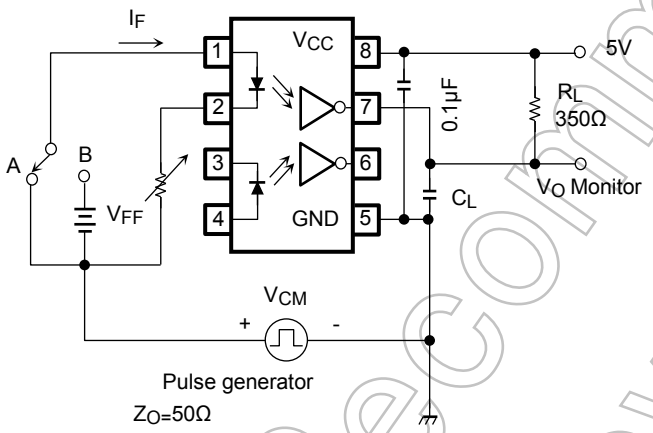
Test Circuit 1. t_{pHL} and t_{pLH}

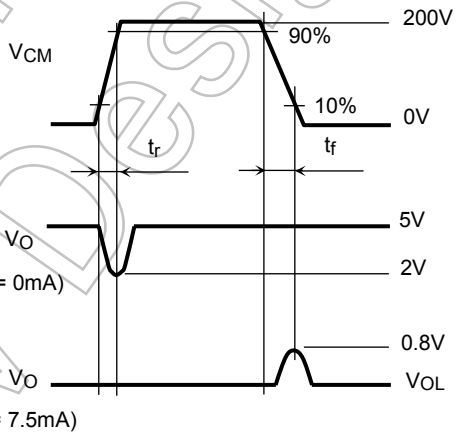




* CL is approximately 15pF which includes probe and stray wirng capacitance.

Test Circuit 2. Transient Immunity and Typical Waveforms

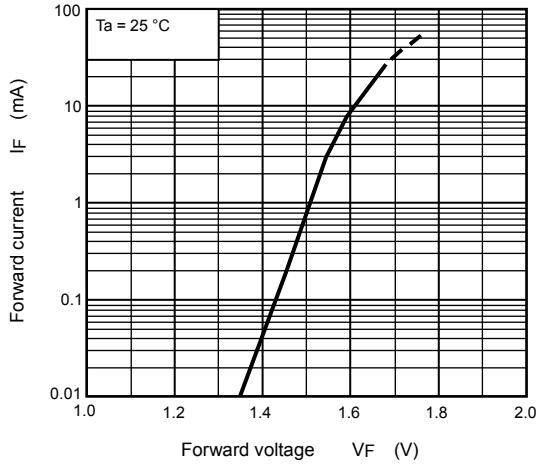




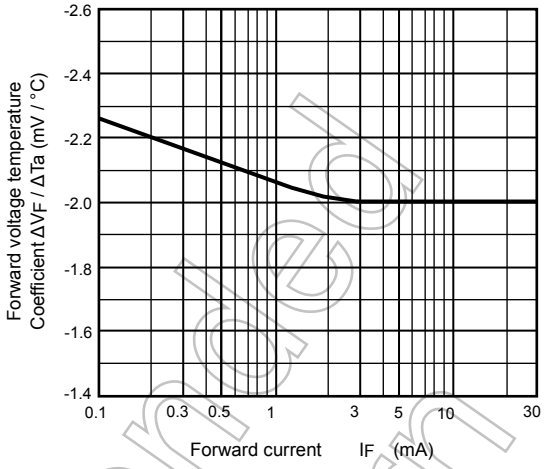
$$CM_H = \frac{160(V)}{t_r(\mu s)}, CM_L = \frac{160(V)}{t_f(\mu s)}$$

* CL is approximately 15pF which includes probe and stray wirng capacitance.

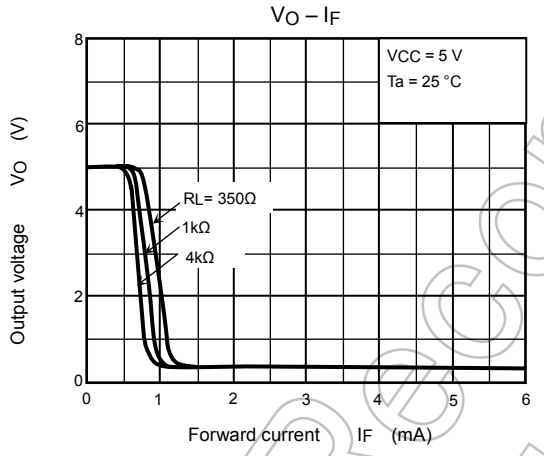
$I_F - V_F$



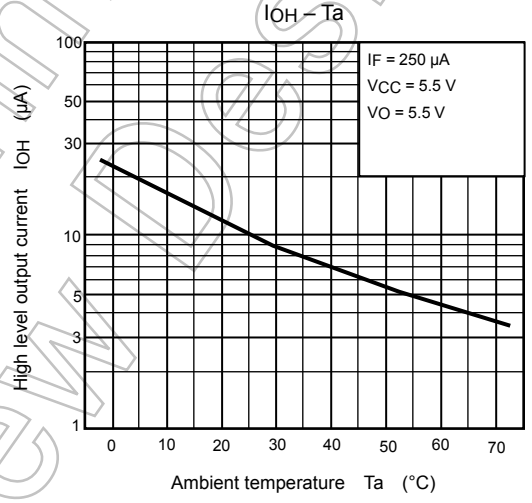
$\Delta V_F / \Delta Ta - I_F$



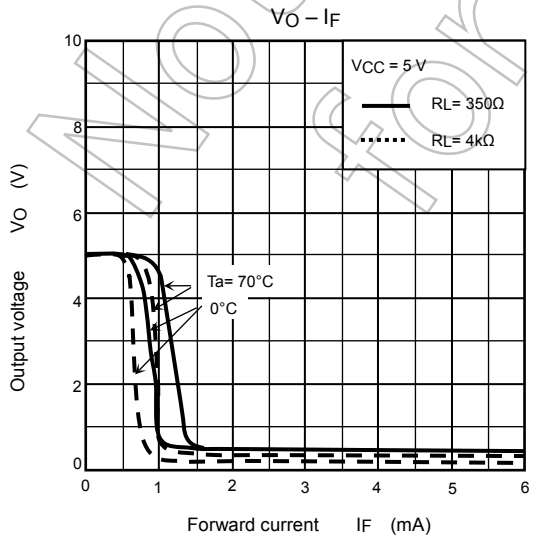
$V_O - I_F$



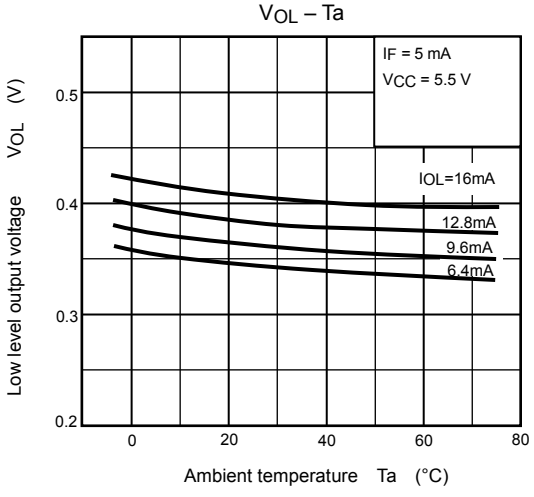
$I_{OH} - Ta$



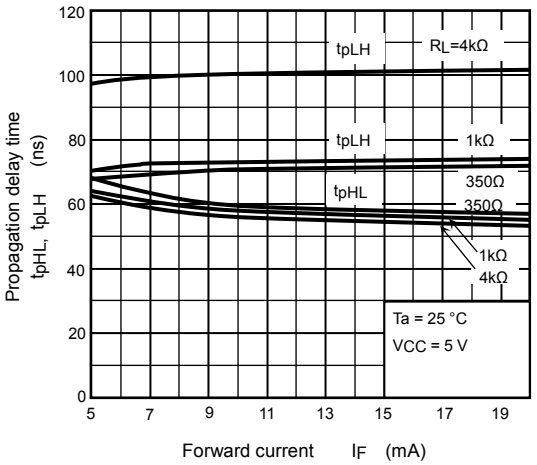
$V_O - I_F$



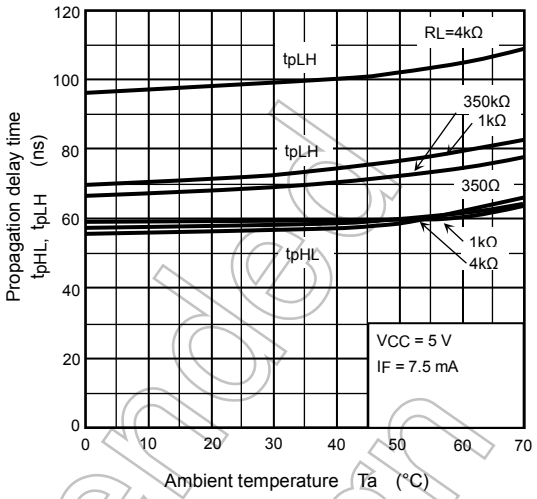
$V_{OL} - Ta$



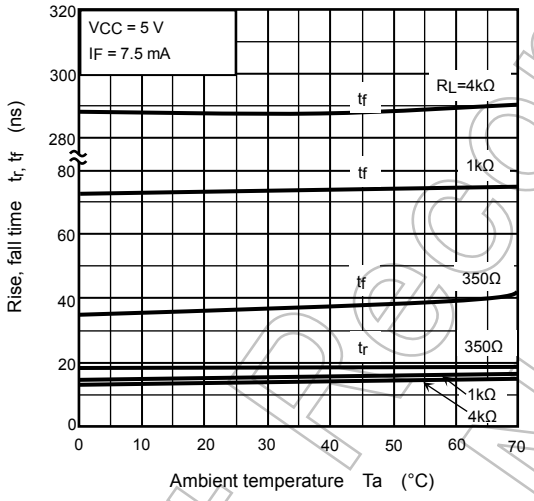
t_{pHL}, t_{pLH} – I_F



t_{pHL}, t_{pLH} – Ta



t_r, t_f – Ta



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