# **74AUP2G38**

# Low-power dual 2-input NAND gate; open drain

Rev. 10 — 3 December 2020

Product data sheet

## 1. General description

The 74AUP2G38 provides the dual 2-input NAND gate with open-drain output. The output of the device is an open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Schmitt trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire  $V_{CC}$  range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire  $V_{CC}$  range from 0.8 V to 3.6 V.

This device is fully specified for partial Power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

#### 2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- · High noise immunity
- · Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 5000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Low static power consumption; I<sub>CC</sub> = 0.9 μA (maximum)
- Latch-up performance exceeds 100 mA per JESD78B Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V<sub>CC</sub>
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



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# 3. Ordering information

**Table 1. Ordering information** 

Type number	Package	Package								
	Temperature range	Name	Description	Version						
74AUP2G38DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1						
74AUP2G38GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1						
74AUP2G38GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	SOT1116						
74AUP2G38GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	SOT1203						

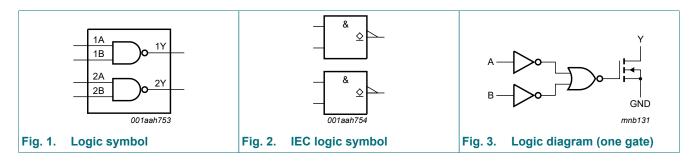
## 4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74AUP2G38DC	a38
74AUP2G38GT	a38
74AUP2G38GN	аВ
74AUP2G38GS	аВ

<sup>[1]</sup> The pin 1 indicator is located on the lower left corner of the device, below the marking code.

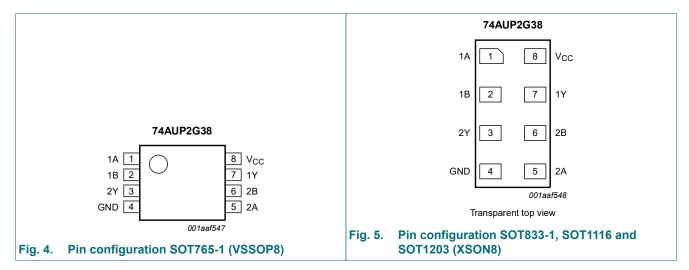
## 5. Functional diagram



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# 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A	1, 5	data input
1B, 2B	2, 6	data input
GND	4	ground (0 V)
1Y, 2Y	7, 3	data output
V <sub>CC</sub>	8	supply voltage

# 7. Functional description

#### **Table 4. Function table**

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF state.

Input	Output	
nA	nB	nY
L	L	Z
L	Н	Z
Н	L	Z
Н	Н	L

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## 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
VI	input voltage	[1]	-0.5	+4.6	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
Vo	output voltage	Active mode and Power-down mode [1]	-0.5	+4.6	V
Io	output current	$V_O = 0 V \text{ to } V_{CC}$	-	+20	mA
I <sub>CC</sub>	supply current		-	+50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$ [2]	-	250	mW

<sup>[1]</sup> The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 9. Recommended operating conditions

### **Table 6. Operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		8.0	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	Active mode and Power-down mode	0	3.6	V
T <sub>amb</sub>	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 0.8 V to 3.6 V	0	200	ns/V

<sup>[2]</sup> For SOT765-1 (VSSOP8) package: Ptot derates linearly with 4.9 mW/K above 99 °C.

For SOT833-1 (XSON8) package: Ptot derates linearly with 3.1 mW/K above 68 °C.

For SOT1116 (XSON8) package: Ptot derates linearly with 4.2 mW/K above 90 °C.

For SOT1203 (XSON8) package: Ptot derates linearly with 3.6 mW/K above 81 °C.

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## 10. Static characteristics

#### **Table 7. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T <sub>amb</sub> = 2	25 °C				1	
V <sub>IH</sub>	HIGH-level input	V <sub>CC</sub> = 0.8 V	0.70V <sub>CC</sub>	-	-	V
voltage	voltage	V <sub>CC</sub> = 0.9 V to 1.95 V	0.65V <sub>CC</sub>	-	-	V
	V <sub>CC</sub> = 2.3 V to 2.7 V	1.6	-	-	V	
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input	V <sub>CC</sub> = 0.8 V	-	-	0.30V <sub>CC</sub>	V
	voltage	V <sub>CC</sub> = 0.9 V to 1.95 V	-	-	0.35V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	0.9	V
V <sub>OL</sub>	LOW-level output	$V_I = V_{IH}$ or $V_{IL}$				
	voltage	I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 0.8 V to 3.6 V	-	-	0.1	V
		I <sub>O</sub> = 1.1 mA; V <sub>CC</sub> = 1.1 V	-	-	0.3V <sub>CC</sub>	V
		I <sub>O</sub> = 1.7 mA; V <sub>CC</sub> = 1.4 V	-	-	0.31	V
		I <sub>O</sub> = 1.9 mA; V <sub>CC</sub> = 1.65 V	-	-	0.31	V
		I <sub>O</sub> = 2.3 mA; V <sub>CC</sub> = 2.3 V	-	-	0.31	V
		I <sub>O</sub> = 3.1 mA; V <sub>CC</sub> = 2.3 V	-	-	0.44	V
		I <sub>O</sub> = 2.7 mA; V <sub>CC</sub> = 3.0 V	-	-	0.31	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.44	V
lį	input leakage current	V <sub>I</sub> = GND to 3.6 V; V <sub>CC</sub> = 0 V to 3.6 V	-	-	±0.1	μΑ
l <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH} \text{ or } V_{IL}; V_O = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	±0.1	μA
I <sub>OFF</sub>	power-off leakage current	$V_1$ or $V_0 = 0 V$ to 3.6 V; $V_{CC} = 0 V$	-	-	±0.2	μA
Δl <sub>OFF</sub>	additional power-off leakage current	$V_1$ or $V_0 = 0 V$ to 3.6 V; $V_{CC} = 0 V$ to 0.2 V	-	-	±0.2	μΑ
I <sub>CC</sub>	supply current	$V_I$ = GND or $V_{CC}$ ; $I_O$ = 0 A; $V_{CC}$ = 0.8 V to 3.6 V	-	-	0.5	μΑ
ΔI <sub>CC</sub>	additional supply current	$V_1 = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	-	-	40	μA
Cı	input capacitance	$V_{CC}$ = 0 V to 3.6 V; $V_I$ = GND or $V_{CC}$	-	0.7	-	pF
Co	output capacitance	$V_O = GND; V_{CC} = 0 V$	-	0.9	-	pF

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T <sub>amb</sub> = -4	40 °C to +85 °C				•	
V <sub>IH</sub>	HIGH-level input	V <sub>CC</sub> = 0.8 V	0.70V <sub>CC</sub>	-	-	V
	voltage	V <sub>CC</sub> = 0.9 V to 1.95 V	0.65V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.6	-	-	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input	V <sub>CC</sub> = 0.8 V	-	-	0.30V <sub>CC</sub>	V
	voltage	V <sub>CC</sub> = 0.9 V to 1.95 V	-	-	0.35V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	0.9	V
V <sub>OL</sub>	LOW-level output	$V_I = V_{IH}$ or $V_{IL}$				
	voltage	I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 0.8 V to 3.6 V	-	-	0.1	V
		I <sub>O</sub> = 1.1 mA; V <sub>CC</sub> = 1.1 V	-	-	0.3V <sub>CC</sub>	V
		I <sub>O</sub> = 1.7 mA; V <sub>CC</sub> = 1.4 V	-	-	0.37	V
		I <sub>O</sub> = 1.9 mA; V <sub>CC</sub> = 1.65 V	-	-	0.35	V
		I <sub>O</sub> = 2.3 mA; V <sub>CC</sub> = 2.3 V	-	-	0.33	V
		I <sub>O</sub> = 3.1 mA; V <sub>CC</sub> = 2.3 V	-	-	0.45	V
		I <sub>O</sub> = 2.7 mA; V <sub>CC</sub> = 3.0 V	-	-	0.33	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.45	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = GND to 3.6 V; V <sub>CC</sub> = 0 V to 3.6 V	-	-	±0.5	μΑ
l <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH} \text{ or } V_{IL}; V_O = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	±0.5	μA
I <sub>OFF</sub>	power-off leakage current	$V_1$ or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	±0.5	μΑ
Δl <sub>OFF</sub>	additional power-off leakage current	$V_1$ or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.6	μΑ
I <sub>CC</sub>	supply current	$V_I$ = GND or $V_{CC}$ ; $I_O$ = 0 A; $V_{CC}$ = 0.8 V to 3.6 V	-	-	0.9	μΑ
ΔI <sub>CC</sub>	additional supply current	$V_1 = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	-	-	50	μA

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T <sub>amb</sub> = -4	40 °C to +125 °C				-1	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 0.8 V	0.75V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	0.70V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.6	-	-	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input	V <sub>CC</sub> = 0.8 V	-	-	0.25V <sub>CC</sub>	V
	voltage	V <sub>CC</sub> = 0.9 V to 1.95 V	-	-	0.30V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	0.9	V
V <sub>OL</sub>	LOW-level output	$V_I = V_{IH}$ or $V_{IL}$				
	voltage	I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 0.8 V to 3.6 V	-	-	0.11	V
		I <sub>O</sub> = 1.1 mA; V <sub>CC</sub> = 1.1 V	-	-	0.33V <sub>CC</sub>	V
		I <sub>O</sub> = 1.7 mA; V <sub>CC</sub> = 1.4 V	-	-	0.41	V
		I <sub>O</sub> = 1.9 mA; V <sub>CC</sub> = 1.65 V	-	-	0.39	V
		I <sub>O</sub> = 2.3 mA; V <sub>CC</sub> = 2.3 V	-	-	0.36	V
		I <sub>O</sub> = 3.1 mA; V <sub>CC</sub> = 2.3 V	-	-	0.50	V
		I <sub>O</sub> = 2.7 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.50	V
l <sub>l</sub>	input leakage current	V <sub>I</sub> = GND to 3.6 V; V <sub>CC</sub> = 0 V to 3.6 V	-	-	±0.75	μΑ
l <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH} \text{ or } V_{IL}; V_O = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	±0.75	μA
I <sub>OFF</sub>	power-off leakage current	$V_1 \text{ or } V_0 = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V}$	-	-	±0.75	μA
ΔI <sub>OFF</sub>	additional power-off leakage current	$V_1$ or $V_0 = 0 \text{ V}$ to 3.6 V; $V_{CC} = 0 \text{ V}$ to 0.2 V	-	-	±0.75	μA
I <sub>CC</sub>	supply current	$V_I$ = GND or $V_{CC}$ ; $I_O$ = 0 A; $V_{CC}$ = 0.8 V to 3.6 V	-	-	1.4	μΑ
Δl <sub>CC</sub>	additional supply current	$V_1 = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	-	-	75	μA

Low-power dual 2-input NAND gate; open drain

# 11. Dynamic characteristics

#### **Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	T,	<sub>amb</sub> = 25 °	,C	T <sub>an</sub>	<sub>nb</sub> = o +85 °C	T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
C <sub>L</sub> = 5 p	F									
t <sub>pd</sub>	propagation	nA, nB to nY; see Fig. 6 [2]								
	delay	V <sub>CC</sub> = 0.8 V	-	13.5	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	1.9	4.6	10.4	1.8	11.4	1.8	12.6	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	1.5	3.3	6.5	1.4	7.4	1.4	8.2	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.2	2.9	5.1	1.1	5.9	1.1	6.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.2	3.8	0.9	4.5	0.9	4.9	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.9	2.3	4.0	0.8	4.5	0.8	4.9	ns
C <sub>L</sub> = 10	pF					'				
t <sub>pd</sub>	propagation	nA, nB to nY; see Fig. 6 [2]								
	delay	V <sub>CC</sub> = 0.8 V	-	16.3	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	2.3	5.6	12.3	2.1	13.7	2.1	15.1	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	1.8	4.1	7.6	1.7	8.8	1.7	9.7	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.6	3.8	6.1	1.4	7.1	1.4	7.8	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.4	2.9	4.6	1.2	5.4	1.2	5.9	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.3	3.2	5.7	1.1	6.4	1.1	7.0	ns
C <sub>L</sub> = 15	pF									
t <sub>pd</sub>	propagation	nA, nB to nY; see Fig. 6 [2]								
	delay	V <sub>CC</sub> = 0.8 V	-	19.0	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	2.6	6.6	14.2	2.4	15.8	2.4	17.4	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	2.1	4.8	8.7	1.9	10.1	1.9	11.1	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.9	4.6	7.6	1.7	8.5	1.7	9.3	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.6	3.6	5.6	1.5	6.3	1.5	6.9	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.6	4.1	7.5	1.4	8.3	1.4	9.1	ns
C <sub>L</sub> = 30	pF									
t <sub>pd</sub>	propagation	nA, nB to nY; see Fig. 6 [2]								
	delay	V <sub>CC</sub> = 0.8 V	-	27.0	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	3.6	9.5	19.5	3.2	21.8	3.2	24.0	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	2.9	7.0	11.5	2.6	13.6	2.6	15.0	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.6	7.0	12.1	2.3	13.3	2.3	14.6	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.4	5.4	8.9	2.1	9.9	2.1	10.9	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.3	6.5	12.7	2.1	13.9	2.1	15.3	ns

**Product data sheet** 

#### Low-power dual 2-input NAND gate; open drain

Symbol	Parameter	Conditions	T,	<sub>amb</sub> = 25	°C	T <sub>an</sub> -40 °C to	<sub>nb</sub> = o +85 °C	T <sub>am</sub> -40 °C to		Unit	
			Min	Typ [1]	Max	Min	Max	Min	Max		
C <sub>L</sub> = 5 p	F, 10 pF, 15 pl	F and 30 pF									
C <sub>PD</sub>	power	$f = 1 \text{ MHz}$ ; $V_I = \text{GND to } V_{CC}[3]$									
	dissipation capacitance	V <sub>CC</sub> = 0.8 V	-	0.6	-	-	-	-	-	pF	
	capacitarioc	V <sub>CC</sub> = 1.1 V to 1.3 V	-	0.7	-	-	-	-	-	pF	
			V <sub>CC</sub> = 1.4 V to 1.6 V	-	0.8	-	-	-	-	-	pF
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	0.9	-	-	-	-	-	pF	
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	1.1	-	-	-	-	-	pF	
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	1.4	-	-	-	-	-	pF	

- [1] All typical values are measured at nominal V<sub>CC</sub>.
- [2]  $t_{pd}$  is the same as  $t_{PZL}$  and  $t_{PLZ}$ .
- [3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N$  where:

f<sub>i</sub> = input frequency in MHz;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching.

### 11.1. Waveforms and test circuit

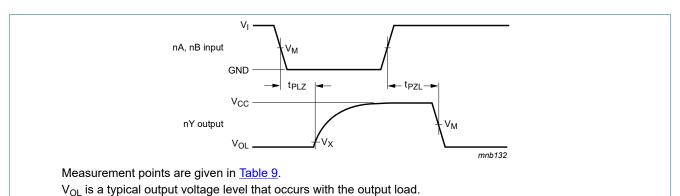
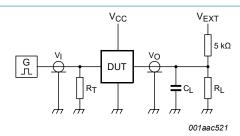


Fig. 6. The data input (nA, nB) to output (nY) propagation delays

**Table 9. Measurement points** 

Supply voltage	Input			Output	
V <sub>CC</sub>	V <sub>M</sub>	V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>	V <sub>M</sub>	V <sub>X</sub>
0.8 V to 1.6 V	0.5V <sub>CC</sub>	V <sub>CC</sub>	≤ 3.0 ns	0.5V <sub>CC</sub>	V <sub>OL</sub> + 0.1 V
1.65 V to 2.7 V	0.5V <sub>CC</sub>	V <sub>CC</sub>	≤ 3.0 ns	0.5V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V
3.0 V to 3.6 V	0.5V <sub>CC</sub>	V <sub>CC</sub>	≤ 3.0 ns	0.5V <sub>CC</sub>	V <sub>OL</sub> + 0.3 V

### Low-power dual 2-input NAND gate; open drain



Test data is given in Table 10.

Definitions for test circuit:

 $R_L$  = Load resistance.

 $C_L$  = Load capacitance including jig and probe capacitance.

 $R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

 $V_{\text{EXT}}$  = External voltage for measuring switching times.

#### Fig. 7. Test circuit for measuring switching times

#### Table 10. Test data

Supply voltage	Load		V <sub>EXT</sub>		
V <sub>CC</sub>	CL	R <sub>L</sub> [1]	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	2V <sub>CC</sub>

[1] For measuring enable and disable times  $R_L$  = 5 k $\Omega$ . For measuring propagation delays, set-up times, hold times and pulse width,  $R_L$  = 1 M $\Omega$ .

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# 12. Package outline

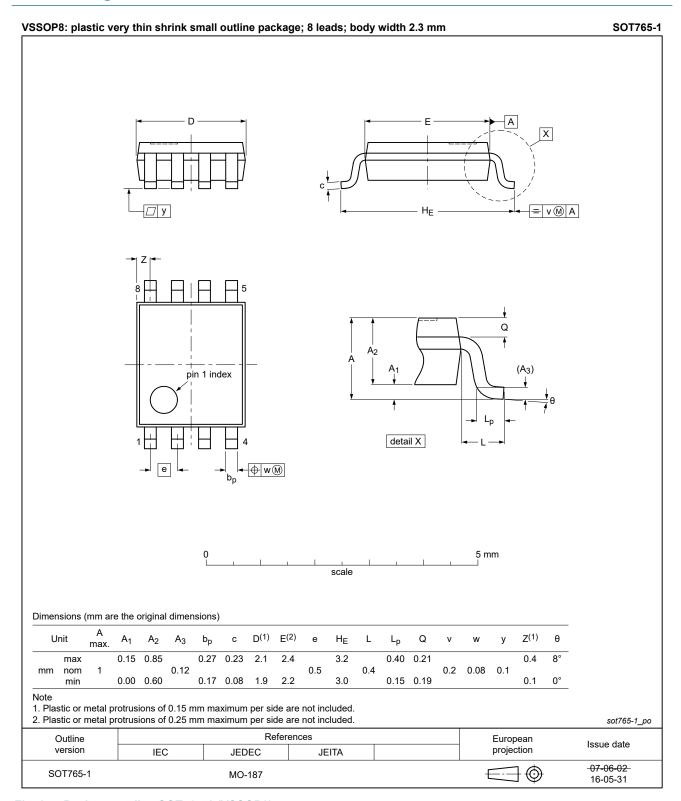


Fig. 8. Package outline SOT765-1 (VSSOP8)

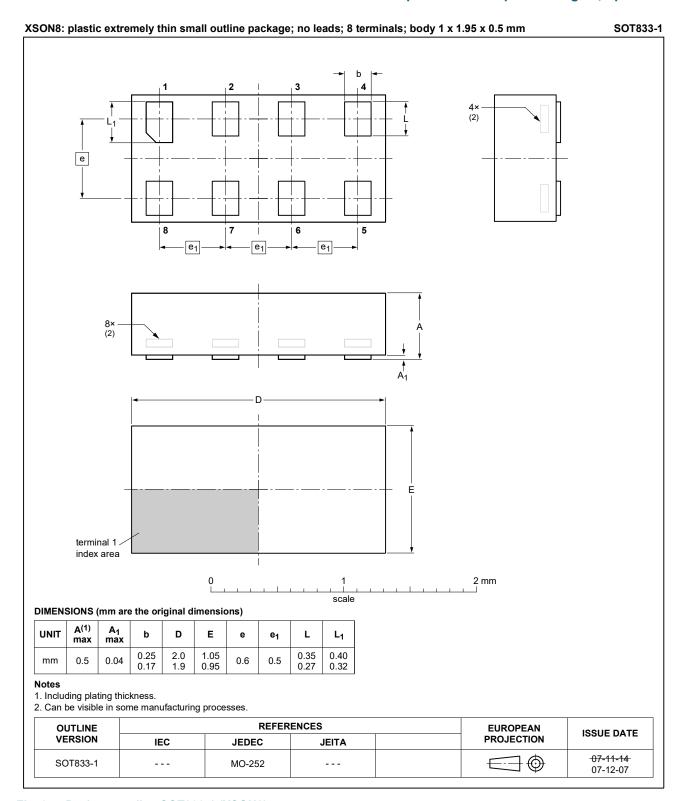


Fig. 9. Package outline SOT833-1 (XSON8)

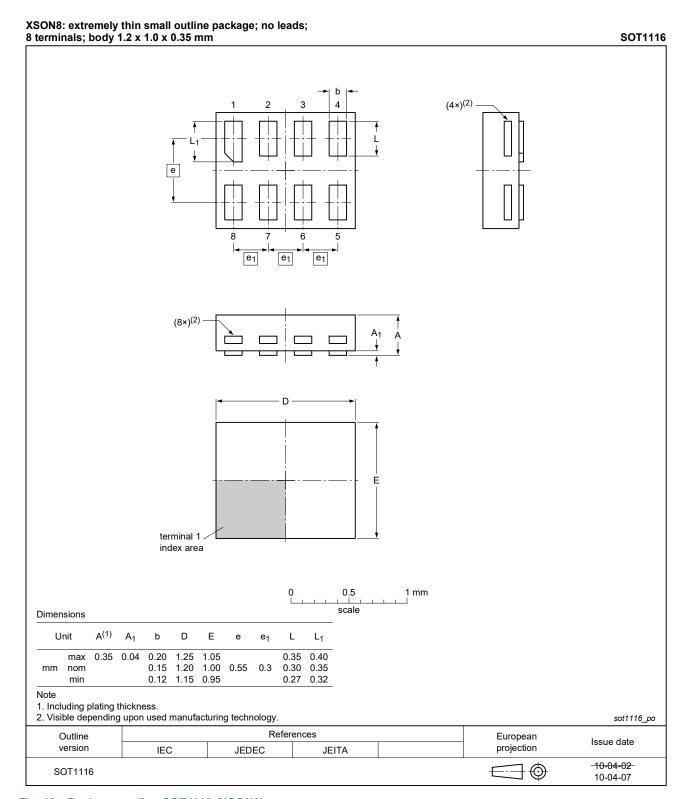


Fig. 10. Package outline SOT1116 (XSON8)

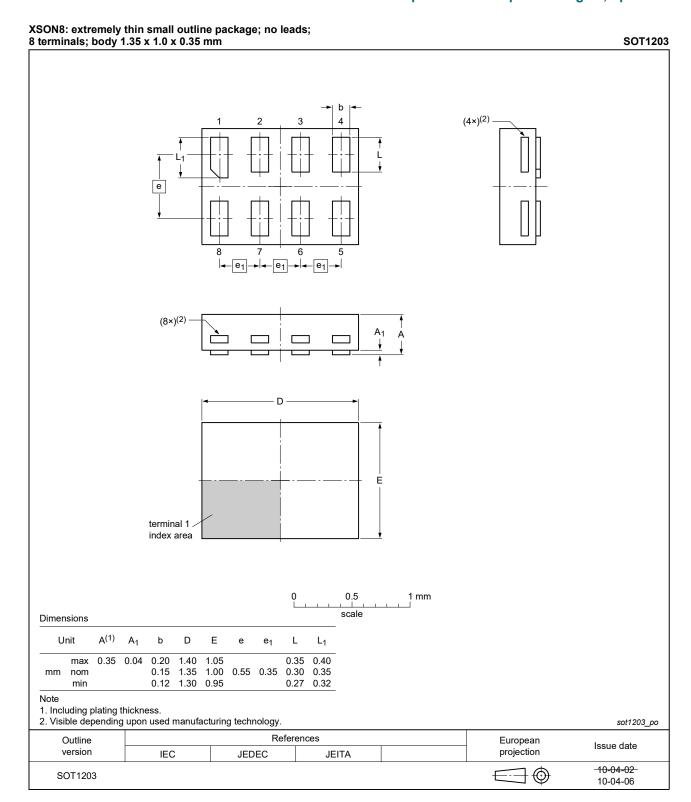


Fig. 11. Package outline SOT1203 (XSON8)

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## 13. Abbreviations

#### **Table 11. Abbreviations**

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model

# 14. Revision history

#### **Table 12. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74AUP2G38 v.10	20201203	Product data sheet	-	74AUP2G38 v.9	
Modifications:	Type numb	<ul> <li><u>Section 8</u>: Derating values for P<sub>tot</sub> total power dissipation have been updated.</li> <li>Type numbers 74AUP2G38GF (SOT1089/XSON8) and 74AUP2G38GM (SOT902-2/XQFN8) removed.</li> </ul>			
74AUP2G38 v.9	20190326	Product data sheet	-	74AUP2G38 v.8	
Modifications:	of Nexperia Legal texts Type numb Package ou		new company nam 96-2) removed. SSOP8) updated.	mply with the identity guidelines e where appropriate.	
74AUP2G38 v.8	20130211	Product data sheet	-	74AUP2G38 v.7	
Modifications:	For type nu	For type number 74AUP2G38GD XSON8U has changed to XSON8.			
74AUP2G38 v.7	20120605	Product data sheet	-	74AUP2G38 v.6	
74AUP2G38 v.6	20111209	Product data sheet	-	74AUP2G38 v.5	
74AUP2G38 v.5	20100923	Product data sheet	-	74AUP2G38 v.4	
74AUP2G38 v.4	20091008	Product data sheet	-	74AUP2G38 v.3	
74AUP2G38 v.3	20090616	Product data sheet	-	74AUP2G38 v.2	
74AUP2G38 v.2	20080312	Product data sheet	-	74AUP2G38 v.1	
74AUP2G38 v.1	20061016	Product data sheet	-	-	

### 15. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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