4-Channel, 2-Wire Bus Multiplexer with Capacitance Buffering

FEATURES

- **1:4 2-Wire Multiplexer/Switch**
- **Connect SDA and SCL Lines with 2-Wire Bus Commands**
- **Supply Independent Bidirectional Buffer for SDA and SCL Lines Increases Fan-Out**
- **Programmable Disconnect from Stuck Bus**
- Compatible with I²C and SMBus Standards
- Rise Time Accelerator Circuitry
- SMBus Compatible ALERT Response Protocol
- Two General Purpose Inputs-Outputs
- Prevents SDA and SCL Corruption During Live Board Insertion and Removal from Backplane
- ±10kV Human Body Model ESD Ruggedness
- 24-Lead QFN (4mm × 5mm) and SSOP Packages

APPLICATIONS

- Nested Addressing
- 5V/3.3V Level Translator
- Capacitance Buffer/Bus Extender

DESCRIPTION

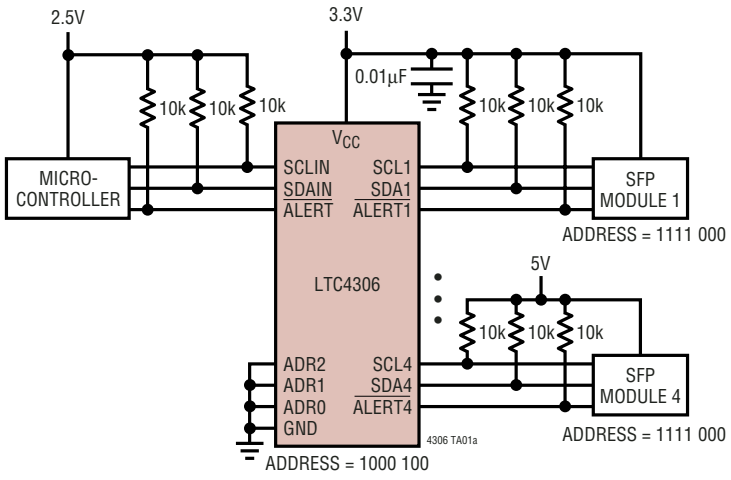
The LTC®4306 is a 4-channel, 2-wire bus multiplexer with bus buffers to provide capacitive isolation between the upstream bus and downstream buses. Through software control, the LTC4306 connects the upstream 2-wire bus to any desired combination of downstream buses. Each channel can be pulled up to a supply voltage ranging from 2.2V to 5.5V, independent of the LTC4306 supply voltage. The downstream channels are also provided with $\overline{\text{ALERT1}}$-$\overline{\text{ALERT4}}$ inputs for fault reporting.

Programmable timeout circuitry disconnects the downstream buses if the bus is stuck low. When activated, rise time accelerators source currents into the 2-wire bus pins to reduce rise time. Driving the ENABLE pin low restores all features to their default states. Three address pins provide 27 distinct addresses.

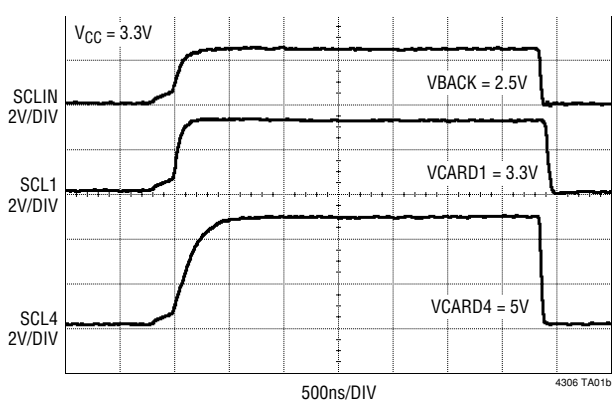
The LTC4306 is available in 24-lead QFN (4mm × 5mm) and SSOP packages.

TYPICAL APPLICATION

A Level Shifting and Nested Addressing Application



I²C Bus Waveforms

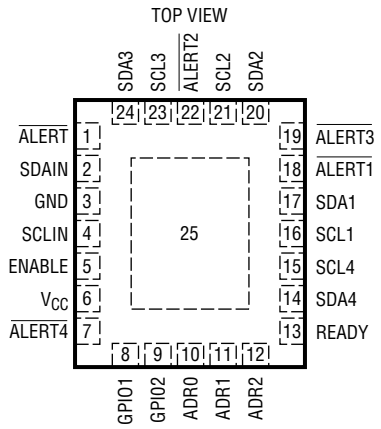


ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC}) ..... –0.3V to 7V
Input Voltages (ADR0, ADR1, ADR2, $\overline{\text{ENABLE}}$, $\overline{\text{ALERT1}}$, $\overline{\text{ALERT2}}$, $\overline{\text{ALERT3}}$, $\overline{\text{ALERT4}}$) ..... –0.3V to 7V
Output Voltages ($\overline{\text{ALERT}}$, READY) ..... –0.3V to 7V
Input/Output Voltages (SDAIN, SCLIN, SCL1, SDA1, SCL2, SDA2, SCL3, SDA3, SCL4, SDA4, GPIO1, GPIO2) ..... –0.3V to 7V
Output Sink Currents (SDAIN, SCLIN, SCL1-4, SDA1-4, GPIO1-2, $\overline{\text{ALERT}}$, READY) 10mA

Operating Temperature Range
LTC4306C ..... 0°C to 70°C
LTC4306I ..... –40°C to 85°C
Storage Temperature Range
SSOP ..... –65°C to 150°C
QFN ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
SSOP ..... 300°C

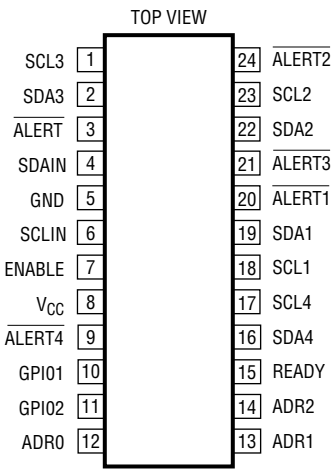
PACKAGE/ORDER INFORMATION



UFD PACKAGE
24-LEAD (4mm × 5mm) PLASTIC QFN

EXPOSED PAD (PIN 25), PCB CONNECTION OPTIONAL
MUST BE CONNECTED TO THE PCB TO OBTAIN
θ_{JA} = 43°C/W OTHERWISE θ_{JA} = 140°C/W. T_{JMAX} = 125°C

ORDER PART NUMBER
LTC4306CUFD LTC4306IUFD
UF PART MARKING*
4306



GN PACKAGE
24-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 85°C/W

ORDER PART NUMBER
LTC4306CGN LTC4306IGN

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply/Start-Up							
V_{CC}	Input Supply Range		●	2.7		5.5	V
I_{CC}	Input Supply Current	Downstream Connected, SCL Bus Low, SDA Bus High, V_{CC} = 5.5V	●		5.2	8	mA
$I_{CC\ ENABLE}$ = 0V	Input Supply Current	V_{ENABLE} = 0V, V_{CC} = 5.5V	●		1.25	2.5	mA
V_{UVLOU}	UVLO Upper Threshold Voltage		●	2.3	2.5	2.7	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{UVLOHYST}$	UVLO Threshold Hysteresis Voltage		●	100	175	250	mV
$V_{TH\ EN}$	ENABLE Falling Threshold Voltage		●	0.8	1.0	1.2	V
V_{ENHYST}	ENABLE Threshold Hysteresis Voltage				60		mV
t_{PHLEN}	ENABLE Delay, On-Off				60		ns
t_{PLHEN}	ENABLE Delay, Off-On				20		ns
I_{INEN}	ENABLE Input Leakage Current	V_{ENABLE} = 0V, 5.5V, V_{CC} = 5.5V	●		0	±1	µA
$V_{LOWREADY}$	READY Pin Logic Low Output Voltage	$I_{PULL-UP}$ = 3mA, V_{CC} = 2.7V	●		0.18	0.4	V
$I_{OFFREADY}$	READY Off State Input Leakage Current	V_{READY} = 0V, 5.5V, V_{CC} = 5.5V	●		0	±1	µA
Upstream-Downstream Buffers							
$V_{OS,BUF}$	Buffer Offset Voltage	R_{BUS} = 10k, V_{CC} = 2.7V, 5.5V (Note 4)	●	25	60	100	mV
$V_{OS,UP-BUF}$	Upstream Buffer Offset Voltage $V_{IN,\ BUFFER}$ = 0V	V_{CC} = 2.7V, R_{BUS} = 2.7k (Note 4) V_{CC} = 5.5V, R_{BUS} = 2.7k (Note 4)	● ●	40 70	80 110	120 150	mV mV
$V_{OS,DOWN-BUF}$	Downstream Buffer Offset Voltage $V_{IN,\ BUFFER}$ = 0V	V_{CC} = 2.7V, R_{BUS} = 2.7k (Note 4) V_{CC} = 5.5V, R_{BUS} = 2.7k (Note 4)	● ●	60 80	110 140	160 200	mV mV
V_{OL}	Output Low Voltage, $V_{IN,BUFFER}$ = 0V	SDA, SCL Pins; I_{SINK} = 4mA, V_{CC} = 3V, 5.5V	●			400	mV
	Output Low Voltage, $V_{IN,BUFFER}$ = 0.2V	SDA, SCL Pins; I_{SINK} = 500µA, V_{CC} = 2.7V, 5.5V	●			320	mV
$V_{IL,MAX}$	Buffer Input Logic Low Voltage	V_{CC} = 2.7V, 5.5V	●	0.4	0.52	0.64	V
$V_{THSDA,SCL}$	Downstream SDA, SCL Logic Threshold Voltage		●	0.8	1.0	1.2	V
I_{LEAK}	Input Leakage Current	SDA, SCL Pins; V_{CC} = 0V to 5.5V; Buffers Inactive	●		0	±5	µA
Rise Time Accelerators							
$V_{SDA,SCL\ slew}$	Minimum Slew Requirement to Activate Rise Time Accelerator Currents	SDAIN, SCLIN, SDA1-4, SCL1-4 Pins	●		0.4	0.8	V/µs
$V_{RISE,DC}$	Rise Time Accelerator DC Threshold Voltage	SDAIN, SCLIN, SDA1-4, SCL1-4 Pins	●	0.7	0.8	1	V
I_{BOOST}	Rise Time Accelerator Pull-Up Current	SDAIN, SCLIN, SDA1-4, SCL1-4 Pins (Note 3)		4	5.5		mA
GPIOs							
$V_{GPIO(TH)}$	GPIO Pin Input Threshold		●	0.8	1	1.2	V
$V_{GPIO(OL)}$	GPIO Pin Output Low Voltage	I_{GPIO} = 5mA, V_{CC} = 2.7V	●		0.2	0.4	V
$V_{GPIO(OH)}$	GPIO Pin Output High Voltage	I_{GPIO} = –200µA, V_{CC} = 2.7V	●	V_{CC} – 0.3			V
$I_{GPIO(IN)}$	GPIO Pin Input Leakage Current	V_{GPIO} = 0V, 5.5V, V_{CC} = 5.5V	●		0	±1	µA
Stuck Low Timeout Circuitry							
$V_{TIMER(L)}$	Stuck Low Falling Threshold Voltage	V_{CC} = 2.7V, 5.5V	●	0.4	0.52	0.64	V
$V_{TIMER(HYST)}$	Stuck Low Threshold Hysteresis Voltage				80		mV
T_{TIMER1}	Timeout Time #1	TIMSET1,0 = 01	●	25	30	35	ms
T_{TIMER2}	Timeout Time #2	TIMSET1,0 = 10	●	12.5	15	17.5	ms
T_{TIMER3}	Timeout Time #3	TIMSET1,0 = 11	●	6.25	7.5	8.75	ms
$\overline{ALERT}$							
$V_{\overline{ALERT}(OL)}$	$\overline{ALERT}$ Output Low Voltage	$I_{\overline{ALERT}}$ = 3mA, V_{CC} = 2.7V	●		0.2	0.4	V
$I_{OFF,\overline{ALERT}}$	$\overline{ALERT}$ Off State Input Leakage Current	$V_{\overline{ALERT}}$ = 0V, 5.5V	●		0	±1	µA
$I_{IN,\overline{ALERT1-4}}$	$\overline{ALERT1}$-$\overline{ALERT4}$ Input Current	$V_{\overline{ALERT1-4}}$ = 0V, 5.5V	●		0	±1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{\overline{ALERT1-4}(IN)}$	$\overline{ALERT1}$-$\overline{ALERT4}$ Pin Input Falling Threshold Voltages		●	0.8	1.0	1.2	V
$V_{\overline{ALERT1-4}(HY)}$	$\overline{ALERT1}$-$\overline{ALERT4}$ Pin Input Threshold Hysteresis Voltages				80		mV
I²C Interface							
$V_{ADR(H)}$	ADR0-2 Input High Voltage		●		0.75 • V_{CC}	0.9 • V_{CC}	V
$V_{ADR(L)}$	ADR0-2 Input Low Voltage		●	0.1 • V_{CC}	0.25 • V_{CC}		V
$I_{ADR(IN, L)}$	ADR0-2 Logic Low Input Current	ADR0-2 = 0V, V_{CC} = 5.5V	●	–30	–60	–80	µA
$I_{ADR(FLOAT)}$	ADR0-2 Allowed Input Current	V_{CC} = 2.7V, 5.5V (Note 5)	●	±5	±13		µA
$I_{ADR(IN, H)}$	ADR0-2 Logic High Input Current	ADR0-2 = V_{CC} = 5.5V	●	30	60	80	µA
$V_{SDAIN,SCLIN(TH)}$	SDAIN, SCLIN Input Falling Threshold Voltages	V_{CC} = 5.5V	●	1.4	1.6	1.8	V
$V_{SDAIN,SCLIN(HY)}$	SDAIN, SCLIN Hysteresis				30		mV
$I_{SDAIN,SCLIN(OH)}$	SDAIN, SCLIN Input Current	SCL, SDA = V_{CC}	●		0	±5	µA
C_{IN}	SDA, SCL Input Capacitance	(Note 2)			6		pF
$V_{SDAIN(OL)}$	SDAIN Output Low Voltage	I_{SDA} = 4mA, V_{CC} = 2.7V	●		0.2	0.4	V
I²C Interface Timing							
f_{SCL}	Maximum SCL Clock Frequency	(Note 2)		400			kHz
t_{BUF}	Bus Free Time Between Stop/Start Condition	(Note 2)			0.75	1.3	µs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition	(Note 2)			45	100	ns
$t_{SU,STA}$	Repeated Start Condition Set-up Time	(Note 2)			–30	0	ns
$t_{SU,STO}$	Stop Condition Set-up Time	(Note 2)			–30	0	ns
$t_{HD,DATI}$	Data Hold Time Input	(Note 2)			–25	0	ns
$t_{HD,DATO}$	Data Hold Time Output	(Note 2)		300	600	900	ns
$t_{SU,DAT}$	Data Set-up Time	(Note 2)			50	100	ns
t_f	SCL, SDA Fall Times	(Note 2)		20 + 0.1 • C_{BUS}		300	ns
t_{SP}	Pulse Width of Spikes Suppressed by the Input Filter	(Note 2)		50	150	250	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Guaranteed by design and not subject to test.

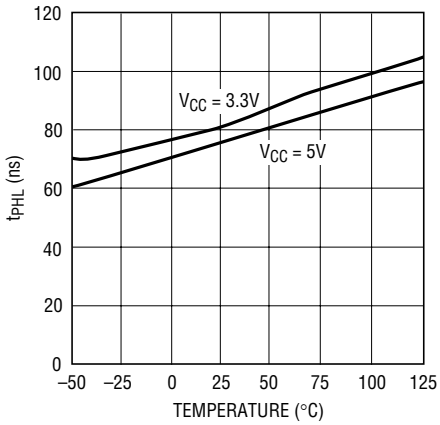
Note 3: The boosted pull-up currents are regulated to prevent excessively fast edges for light loads. See the Typical Performance Characteristics for rise time as a function of V_{CC} and parasitic bus capacitance C_{BUS} and for I_{BOOST} as a function of V_{CC} and temperature.

Note 4: When a logic low voltage, V_{LOW}, is forced on one side of the Upstream-Downstream Buffers, the voltage on the other side is regulated to a voltage $V_{LOW2} = V_{LOW} + V_{OS}$, where V_{OS} is a positive offset voltage. $V_{OS,UP-BUF}$ is the offset voltage when the LTC4306 is driving the upstream pin (e.g., SDAIN) and $V_{OS,DOWN-BUF}$ is the offset voltage when the LTC4306 is driving the downstream pin (e.g., SDA1). See the Typical Performance Characteristics for $V_{OS,UP-BUF}$ and $V_{OS,DOWN-BUF}$ as a function of V_{CC} and bus pull-up current.

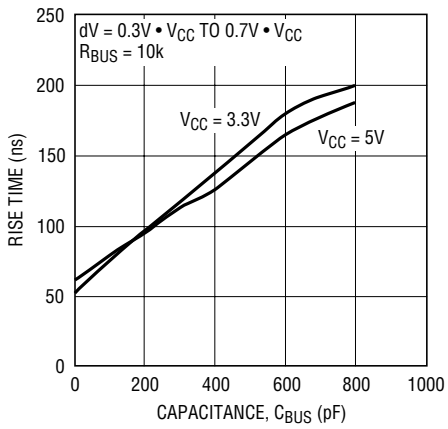
Note 5: When floating, the ADR0-ADR2 pins can tolerate pin leakage currents up to $I_{ADR(FLOAT)}$ and still convert the address correctly.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, unless otherwise indicated)

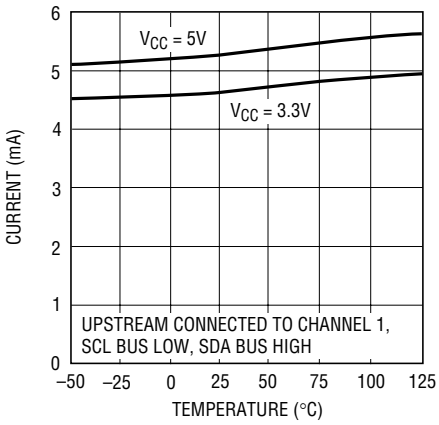
Buffer Circuitry t_{PHL} vs Temperature



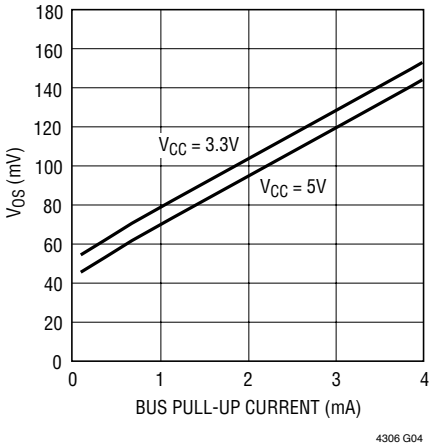
Rise Time vs C_{BUS} vs V_{CC}



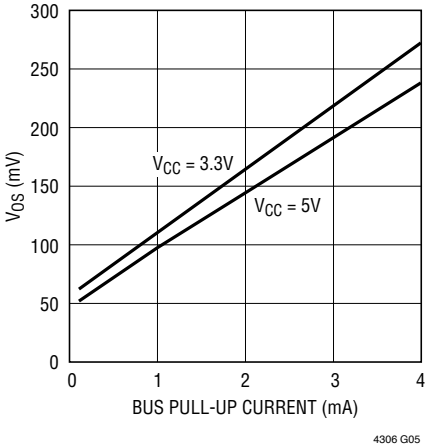
I_{CC} vs Temperature



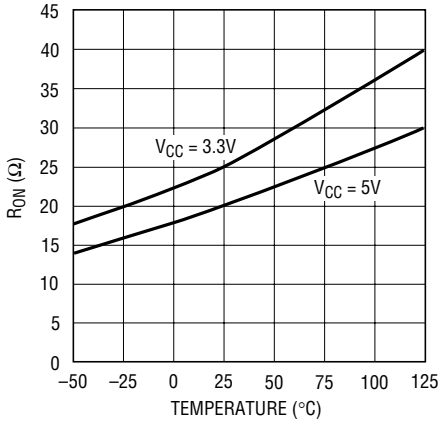
$V_{OS,UP-BUF}$ vs Bus Pull-Up Current



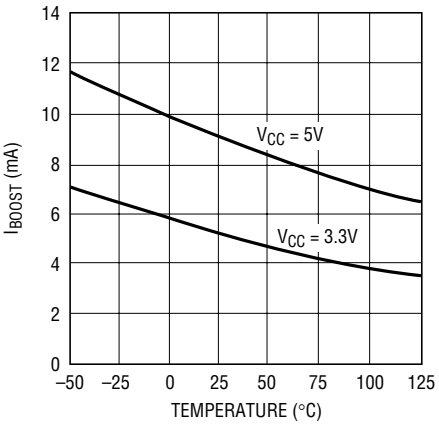
$V_{OS,DOWN-BUF}$ vs Bus Pull-Up Current



Downstream R_{FET} On Resistance vs V_{CC} and Temperature



I_{BOOST} vs Temperature



PIN FUNCTIONS (GN24 Package/UFD24 Package)

$\overline{\text{ALERT}}$ (Pin 3/Pin 1): Fault Alert Output. An open-drain output that is pulled low when a fault occurs to alert the host controller. The LTC4306 pulls $\overline{\text{ALERT}}$ low when any of the $\overline{\text{ALERT1}}$-$\overline{\text{ALERT4}}$ pins is low, when the 2-wire bus is stuck low, or when the Connection Requirement bit of Register 2 is low and a master tries to connect to a downstream channel that is low. See Operation section for the details of how $\overline{\text{ALERT}}$ is set and cleared. The LTC4306 is compatible with the SMBus Alert Response Address protocol. Connect a 10k resistor to a power supply voltage to provide the pull-up. Tie to ground if unused.

SDAIN (Pin 4/Pin 2): Serial Bus Data Input and Output. Connect this pin to the SDA line on the master side. An external pull-up resistor or current source is required.

GND (Pin 5/Pin 3): Device Ground.

SCLIN (Pin 6/Pin 4): Serial Bus Clock Input. Connect this pin to the SCL line on the master side. An external pull-up resistor or current source is required.

ENABLE (Pin 7/Pin 5): Digital Interface Enable and Register Reset. Driving ENABLE high enables I^2C communication to the LTC4306. Driving this pin low disables I^2C communication to the LTC4306 and resets the registers to their default state as shown in the Operation section. When ENABLE returns high, masters can read and write the LTC4306 again. If unused, tie ENABLE to V_{CC}.

V_{CC} (Pin 8/Pin 6): Power Supply Voltage. Connect a bypass capacitor of at least 0.01µF directly between V_{CC} and GND for best results.

GPIO1-GPIO2 (Pins 10, 11/Pins 8, 9): General Purpose Input/Output. These two pins can be used as logic inputs, open-drain outputs or push-pull outputs. The N-channel MOSFET pull-down devices are capable of driving LEDs. When used in input or open-drain output mode, the GPIOs can be pulled up to a supply voltage ranging from 1.5V to 5.5V independent of the V_{CC} voltage. GPIOs default to a high impedance open-drain output mode. There are GPIO configuration and status bits in Register 1 and Register 2. Float if unused.

ADR0-ADR2 (Pins 12, 13, 14/Pins 10, 11, 12): Three-State Serial Bus Address Inputs. Each pin may be floated, tied to ground or tied to V_{CC}. There are therefore 27 possible addresses. See Table 1 in applications information. When the pins are floated, they can tolerate ±5µA of leakage current and still convert the address correctly.

READY (Pin 15/Pin 13): Connection Ready Digital Output. An N-channel MOSFET open-drain output transistor that pulls down when none of the downstream channels is connected to the upstream bus and turns off when one or more downstream channels is connected to the upstream bus. Connect a 10k resistor to a power supply voltage to provide the pull-up. Tie to ground if unused.

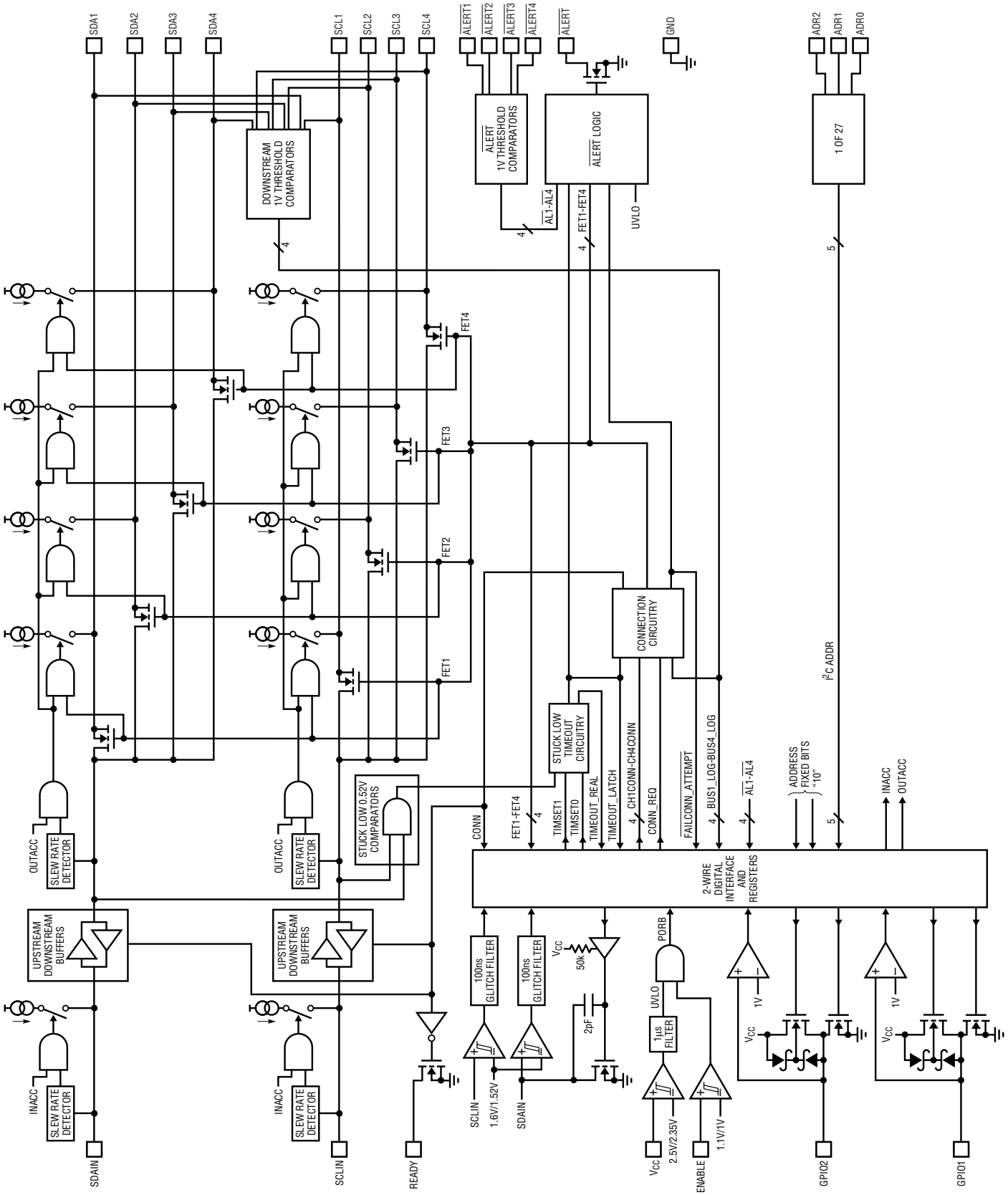
SCL1-SCL4 (Pins 18, 23, 1, 17/Pins 16, 21, 23, 15): Serial Bus Clock Outputs Channels 1-4. Connect pins SCL1-SCL4 to the SCL lines on the downstream channels 1-4, respectively. It is acceptable to float any pin that will never be connected to the upstream bus. Otherwise, an external pull-up resistor or current source is required on each pin.

SDA1-SDA4 (Pins 19, 22, 2, 16/Pins 17, 20, 24, 14): Serial Bus Data Output Channels 1-4. Connect pins SDA1-SDA4 to the SDA lines on downstream channels 1-4, respectively. It is acceptable to float any pin that will never be connected to the upstream bus. Otherwise, an external pull-up resistor or current source is required on each pin.

$\overline{\text{ALERT1}}$-$\overline{\text{ALERT4}}$ (Pins 20, 24, 21, 9/Pins 18, 22, 19, 7): Fault Alert Inputs, Channels 1-4. Devices on each of the four output channels can pull their respective pin low to indicate that a fault has occurred. The LTC4306 then pulls the $\overline{\text{ALERT}}$ low to pass the fault indication on to the host. See Operation section below for the details of how $\overline{\text{ALERT}}$ is set and cleared. Connect unused fault alert inputs to V_{CC}.

Exposed Pad (Pin 25, UFD Package Only): Power Ground. Exposed Pad may be left open or connected to device ground.

BLOCK DIAGRAM



OPERATION

Control Register Bit Definitions

Register 0 (00h)

BIT	NAME	TYPE*	DESCRIPTION
d7	Downstream Connected	R	Indicates if upstream bus is connected to any downstream buses 0 = upstream bus disconnected from all downstream buses 1 = upstream bus connected to one or more downstream buses
d6	$\overline{\text{ALERT1}}$ Logic State	R	Logic state of $\overline{\text{ALERT1}}$ pin, noninverting
d5	$\overline{\text{ALERT2}}$ Logic State	R	Logic state of $\overline{\text{ALERT2}}$ pin, noninverting
d4	$\overline{\text{ALERT3}}$ Logic State	R	Logic state of $\overline{\text{ALERT3}}$ pin, noninverting
d3	$\overline{\text{ALERT4}}$ Logic State	R	Logic state of $\overline{\text{ALERT4}}$ pin, noninverting
d2	$\overline{\text{Failed Connection Attempt}}$	R	Indicates if an attempt to connect to a downstream bus failed because the "Connection Requirement" bit in Register 2 was low and the downstream bus was low 0 = Failed connection attempt occurred 1 = No failed attempts at connection occurred
d1	Latched Timeout	R	Latched bit indicating if a timeout has occurred and has not yet been cleared. 0 = no latched timeout 1 = latched timeout
d0	Timeout Real Time	R	Indicates real-time status of Stuck Low Timeout Circuitry 0 = no timeout is occurring 1 = timeout is occurring

Note: Masters write to Register 0 to reset the fault circuitry after a fault has occurred and been resolved. Because Register 0 is Read-Only, no other functionality is affected.

* For Type, "R/W" = Read Write, "R" = Read Only

Register 1 (01h)

BIT	NAME	TYPE*	DESCRIPTION
d7	Upstream Accelerators Enable	R/W	Activates upstream rise time accelerator currents 0 = upstream rise time accelerator currents inactive (default) 1 = upstream rise time accelerator currents active
d6	Downstream Accelerators Enable	R/W	Activates downstream rise time accelerator currents 0 = downstream rise time accelerator currents inactive (default) 1 = downstream rise time accelerator currents active
d5	GPIO1 Output Driver State	R/W	GPIO1 output driver state, noninverting, default = 1
d4	GPIO2 Output Driver State	R/W	GPIO2 output driver state, noninverting, default = 1
d3-d2	Reserved	R	Not Used
d1	GPIO1 Logic State	R	Logic state of GPIO1 pin, noninverting
d0	GPIO2 Logic State	R	Logic state of GPIO2 pin, noninverting

* For Type, "R/W" = Read Write, "R" = Read Only

OPERATION

Register 2 (02h)

BIT	NAME	TYPE*	DESCRIPTION
d7	GPIO1 Mode Configure	R/W	Configures Input/Output mode of GPIO1 0 = output mode (default) 1 = input mode
d6	GPIO2 Mode Configure	R/W	Configures Input/Output Mode of GPIO2 0 = output mode (default) 1 = input mode
d5	Connection Requirement	R/W	Sets logic requirements for downstream buses to be connected to upstream bus 0 = Bus Logic State bits (see register 3) of buses to be connected must be high for connection to occur (default) 1 = Connect regardless of downstream logic state
d4	GPIO1 Output Mode Configure	R/W	Configures GPIO1 Output Mode 0 = open-drain pull-down (default) 1 = push-pull
d3	GPIO2 Output Mode Configure	R/W	Configures GPIO2 Output Mode 0 = open-drain pull-down (default) 1 = push-pull
d2	Mass Write Enable	R/W	Enable Mass Write Address using address (1011 101)b 0 = Disable Mass Write 1 = Enable Mass Write (default)
d1	Timeout Mode Bit 1	R/W	Stuck Low Timeout Set Bit 1**
d0	Timeout Mode Bit 0	R/W	Stuck Low Timeout Set Bit 0**

* For Type, “R/W” = Read Write, “R” = Read Only
**Stuck bus program table

TIMSET1	TIMSET0	TIMEOUT MODE
0	0	Timeout Disabled (Default)
0	1	Timeout After 30ms
1	0	Timeout After 15ms
1	1	Timeout After 7.5ms

Register 3 (03h)

BIT	NAME	TYPE*	DESCRIPTION
d7	Bus 1 FET State	R/W	Sets and indicates state of FET switches connected to downstream bus 1 0 = switch open (default) 1 = switch closed
d6	Bus 2 FET State	R/W	Sets and indicates state of FET switches connected to downstream bus 2 0 = switch open (default) 1 = switch closed
d5	Bus 3 FET State	R/W	Sets and indicates state of FET switches connected to downstream bus 3 0 = switch open (default) 1 = switch closed
d4	Bus 4 FET State	R/W	Sets and indicates state of FET switches connected to downstream bus 4 0 = switch open (default) 1 = switch closed
d3	Bus 1 Logic State	R	Indicates logic state of downstream bus 1; only valid when disconnected from upstream bus† 0 = SDA1, SCL1 or both are below 1V 1 = SDA1 and SCL1 are both above 1V
d2	Bus 2 Logic State	R	Indicates logic state of downstream bus 2; only valid when disconnected from upstream bus† 0 = SDA2, SCL2 or both are below 1V 1 = SDA2 and SCL2 are both above 1V
d1	Bus 3 Logic State	R	Indicates logic state of downstream bus 3; only valid when disconnected from upstream bus† 0 = SDA3, SCL3 or both are below 1V 1 = SDA3 and SCL3 are both above 1V
d0	Bus 4 Logic State	R	Indicates logic state of downstream bus 4; only valid when disconnected from upstream bus† 0 = SDA4, SCL4 or both are below 1V 1 = SDA4 and SCL4 are both above 1V

* For Type, “R/W” = Read Write, “R” = Read Only
† These bits give the logic state of disconnected downstream buses to the master, so that the master can choose not to connect to a low downstream bus. A given bit is a “don’t care” if its associated downstream bus is already connected to the upstream bus.

OPERATION

The LTC4306 is a 4-channel, 2-wire bus multiplexer/switch with bus buffers to provide capacitive isolation between the upstream bus and downstream buses. Masters on the upstream 2-wire bus (SDAIN and SCLIN) can command the LTC4306 to any combination of the 4 downstream buses. Masters can also program the LTC4306 to disconnect the upstream bus from the downstream buses if the bus is stuck low.

Undervoltage Lockout (UVLO) and ENABLE Functionality

The LTC4306 contains undervoltage lockout circuitry that maintains all of its SDA, SCL, GPIO and $\overline{\text{ALERT}}$ pins in high impedance states until the device has sufficient V_{CC} supply voltage to function properly. It also ignores any attempts to communicate with it via the 2-wire buses in this condition. When the ENABLE pin voltage is low (below 0.8V), all control bits are reset to their default high impedance states, and the LTC4306 ignores 2-wire bus commands. However, with ENABLE low, the LTC4306 still monitors the $\overline{\text{ALERT1}}$-$\overline{\text{ALERT4}}$ pin voltages and pulls the $\overline{\text{ALERT}}$ pin low if any of $\overline{\text{ALERT1}}$-$\overline{\text{ALERT4}}$ is low. When ENABLE is high, devices can read from and write to the LTC4306.

Connection Circuitry

Masters on the upstream SDAIN/SCLIN bus can write to the Bus 1 FET State through Bus 4 FET State bits of register 3 to connect to any combination of downstream channels 1 to 4. By default, the Connection Circuitry shown in the Block Diagram will only connect to downstream channels whose corresponding Bus Logic State bits in register 3 are high at the moment that it receives the connection command. If the LTC4306 is commanded to connect to multiple channels at once, it will only connect to the channels that are high. Masters can override this feature by setting the Connection Requirement bit of register 2 high. With this bit high, the LTC4306 executes connection commands without regard to the logic states of the downstream channels.

Upon receiving the connection command, the Connection Circuitry will activate the Upstream-Downstream Buffers under two conditions: first, the master must be commanding connection to one or more downstream channels, and second, there must be no stuck low condition (see Stuck Low Timeout Fault discussion). If the connection command is successful, the Upstream-Downstream Buffers pass signals between the upstream bus and the connected downstream buses. The LTC4306 also turns off its N-channel MOSFET open-drain pull-down on the READY pin, so that READY can be pulled high by its external pull-up resistor.

Upstream-Downstream Buffers

Once the Upstream-Downstream Buffers are activated, the functionality of the SDAIN and any connected downstream SDA pins is identical. A low forced on any connected SDA pin at any time results in all pins being low. **External devices must pull the pin voltages below 0.4V worst-case with respect to the LTC4306's ground pin to ensure proper operation.** The SDA pins enter a logic high state only when all devices on all connected SDA pins force a high. The same is true for SCLIN and the connected downstream SCL pins. This important feature ensures that clock stretching, clock arbitration and the acknowledge protocol always work, regardless of how the devices in the system are connected to the LTC4306.

The Upstream-Downstream Buffers provide capacitive isolation between SDAIN/SCLIN and the downstream connected buses. Note that there is no capacitive isolation between connected downstream buses; they are only separated by the series combination of their switches' on resistances.

While any combination of downstream buses may be connected at the same time, logic high levels are corrupted if multiple downstream buses are active and both the V_{CC} voltage and one or more downstream bus pull-up voltages are larger than the pull-up supply voltage for another downsteam bus. An example of this issue is shown in Figure 1. During logic highs, DC current flows from V_{BUS1} through the series combination of R1, N1, N2 and R2 and into V_{BUS2}, causing the SDA1 voltage to drop and current to be sourced into V_{BUS2}. To avoid this problem, do not activate bus 1 or any other downstream bus whose pull-up voltage is above 2.5V when bus 2 is active.

OPERATION

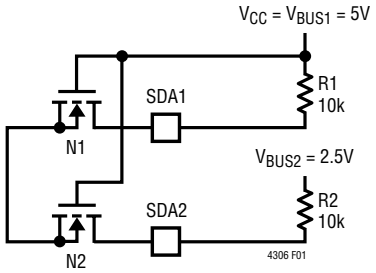


Figure 1. Example of Unacceptable Level Shifting

Rise Time Accelerators

The Upstream Accelerators Enable and Downstream Accelerators Enable bits of register 1 activate the upstream and downstream rise time accelerators, respectively. When activated, the accelerators turn on in a controlled manner and source current into the pins during positive bus transitions.

When no downstream buses are connected, an upstream accelerator turns on when its pin voltage exceeds 0.8V and is rising at a minimum slew rate of 0.8V/µs. When one or more downstream buses are connected, the accelerator on a given pin turns on when these conditions are met: first, the pin's voltage is rising at a minimum slew rate of 0.8V/µs; second, the voltages on both the upstream bus and the connected downstream buses exceed 0.8V.

Note that a downstream bus's switch must be closed in order for its rise time accelerator current to be active. See the Applications Section for choosing a bus pull-up resistor value to ensure that the rise time accelerator switches turn on. **Do not activate boost currents on a bus whose pull-up supply voltage V_{BUS} is less than V_{CC}. Doing so would cause the boost currents to source current from V_{CC} into the V_{BUS} supply during rising edges.**

Downstream Bus Connection Fault

By default, the LTC4306 will only connect to downstream channels whose SDA and SCL pins are both high (above 1V) at the moment that it receives the connection command. In this case, the LTC4306 sets the Failed Connection Attempt bit of register 0 low and pulls the ALERT pin low when the master tries to connect to a low downstream channel. Note that users can write a high to the Connection Requirement bit of register 2 high to program the LTC4306 to connect to downstream channels regardless of their logic state at the moment of connection. In this case, the downstream channel connection fault never occurs.

Stuck Low Timeout Fault

The stuck low timeout circuitry monitors the two common internal nodes of the downstream SDA and SCL switches and runs a timer whenever either of the internal node voltages is below 0.52V. The timer is reset whenever both internal node voltages are above 0.6V. If the timer ever reaches the time programmed by Timeout Mode Bits 1 and 0 of register 2, the LTC4306 pulls $\overline{\text{ALERT}}$ low and disconnects the downstream bus(es) from the upstream bus by de-biasing the Upstream-Downstream Buffers. Note that the downstream switches remain in their existing state. The Timeout Real-Time bit of register 0 indicates the real-time status of the stuck low situation. The Latched Timeout Bit of register 0 is a latched bit that is set high when a timeout occurs.

External Faults on the Downstream Channels

When a slave on downstream bus 1 pulls the $\overline{\text{ALERT1}}$ pin below 1V, the LTC4306 passes this information to the master on the upstream bus by pulling the $\overline{\text{ALERT}}$ pin low. The same is true for the other three downstream buses. Each bus has its own dedicated fault bit in Register 0, so that masters can read Register 0 to determine which buses have faults.

$\overline{\text{ALERT}}$ Functionality and Fault Resolution

When a fault occurs, the LTC4306 pulls the $\overline{\text{ALERT}}$ pin low, as described previously. The procedure for resolving faults depends on the type of fault. If a master on the upstream bus is communicating with devices on a downstream bus via the Upstream-Downstream Buffer circuitry—channel 1, for example—and a device on this bus pulls the $\overline{\text{ALERT1}}$ pin low, the LTC4306 acts transparently, and the master communicates directly with the device that caused the fault via the upstream-downstream buffer circuitry to resolve the fault.

OPERATION

In all other cases, the LTC4306 communicates with the master to resolve the fault. After the master broadcasts the Alert Response Address (ARA), the LTC4306 will respond with its address on the SDAIN line and release the $\overline{\text{ALERT}}$ pin. The $\overline{\text{ALERT}}$ line will also be released if the LTC4306 is addressed by the master.

The $\overline{\text{ALERT}}$ signal will not be pulled low again until a different type of fault has occurred or the original fault is cleared and it occurs again. Figure 2 shows the details of how the $\overline{\text{ALERT}}$ pin is set and reset. The downstream bus connection fault and faults that occur on unconnected downstream buses are grouped together and generate a single signal to drive $\overline{\text{ALERT}}$. The stuck low timeout fault has its own dedicated pathway to $\overline{\text{ALERT}}$; however, once a stuck low occurs, another one will not occur until the first one is cleared. For these reasons, once the master has established the LTC4306 as the source of the fault, it should read register 0 to determine the specific problem, take action to solve the problem, and clear the fault promptly. All faults are cleared by writing a dummy data byte to register 0, which is a read-only register.

For example, assume that a fault occurs, the master sends out the ARA, and the LTC4306 successfully writes its address onto SDAIN and releases its $\overline{\text{ALERT}}$ pin. The master reads register 0 and learns that the $\overline{\text{ALERT2}}$ logic state bit is low. The master now knows that a device on downstream bus 2 has a fault and writes to register 3 to connect to bus 2, so that it can communicate with the source of the fault. At this point, the master writes to register 0 to clear the LTC4306 fault register.

I²C Device Addressing

Twenty-seven distinct bus addresses are configurable using the three state ADR0, ADR1 and ADR2 pins. Table 1 shows the correspondence between pin states and addresses. Note that address bits a6 and a5 are internally configured to 1 and 0 respectively. In addition, the LTC4306 responds to two special addresses. Address (1011 101) is a mass write used to write all LTC4306's, regardless of their individual address settings. The mass write can be masked by setting the Mass Write Enable bit of register 2 to zero. Address (0001 100) is the SMBus Alert Response Address. Figure 3 shows data transfer over a 2-wire bus.

Supported Commands

Users must write to the LTC4306 using the SMBus Write Byte protocol and read from it using the Read Byte protocol. During fault resolution, the LTC4306 also supports the Alert Response Address protocol. The formats for these protocols are shown in Figure 4. Users must follow the Write Byte protocol exactly to write to the LTC4306; if a Repeated Start Condition is issued before a Stop Condition, the LTC4306 ignores the attempted write, and its control bits remain in their preexisting state. When

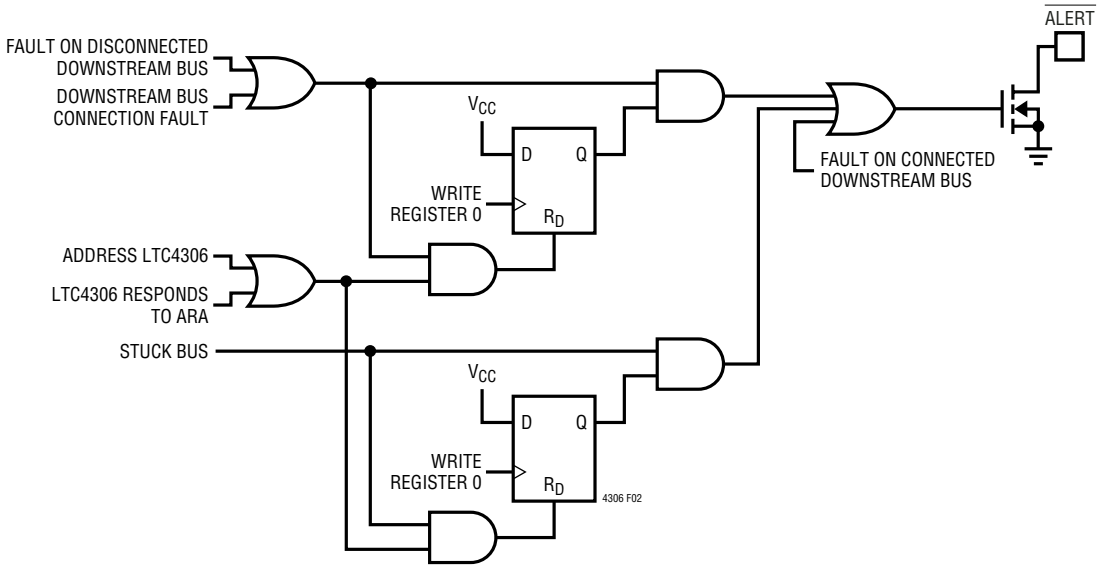


Figure 2. Setting and Resetting the $\overline{\text{ALERT}}$ Pin

OPERATION

Table 1. LTC4306 I²C Device Addressing

DESCRIPTION	HEX DEVICE ADDRESS	BINARY DEVICE ADDRESS								LTC4306 ADDRESS PINS		
	h	a6	a5	a4	a3	a2	a1	a0	R/$\overline{W}$	ADR2	ADR1	ADR0
Mass Write	BA	1	0	1	1	1	0	1	0	X	X	X
Alert Response	19	0	0	0	1	1	0	0	1	X	X	X
0	80	1	0	0	0	0	0	0	X	L	NC	L
1	82	1	0	0	0	0	0	1	X	L	H	NC
2	84	1	0	0	0	0	1	0	X	L	NC	NC
3	86	1	0	0	0	0	1	1	X	L	NC	H
4	88	1	0	0	0	1	0	0	X	L	L	L
5	8A	1	0	0	0	1	0	1	X	L	H	H
6	8C	1	0	0	0	1	1	0	X	L	L	NC
7	8E	1	0	0	0	1	1	1	X	L	L	H
8	90	1	0	0	1	0	0	0	X	NC	NC	L
9	92	1	0	0	1	0	0	1	X	NC	H	NC
10	94	1	0	0	1	0	1	0	X	NC	NC	NC
11	96	1	0	0	1	0	1	1	X	NC	NC	H
12	98	1	0	0	1	1	0	0	X	NC	L	L
13	9A	1	0	0	1	1	0	1	X	NC	H	H
14	9C	1	0	0	1	1	1	0	X	NC	L	NC
15	9E	1	0	0	1	1	1	1	X	NC	L	H
16	A0	1	0	1	0	0	0	0	X	H	NC	L
17	A2	1	0	1	0	0	0	1	X	H	H	NC
18	A4	1	0	1	0	0	1	0	X	H	NC	NC
19	A6	1	0	1	0	0	1	1	X	H	NC	H
20	A8	1	0	1	0	1	0	0	X	H	L	L
21	AA	1	0	1	0	1	0	1	X	H	H	H
22	AC	1	0	1	0	1	1	0	X	H	L	NC
23	AE	1	0	1	0	1	1	1	X	H	L	H
24	B0	1	0	1	1	0	0	0	X	H	H	L
25	B2	1	0	1	1	0	0	1	X	L	H	L
26	B4	1	0	1	1	0	1	0	X	NC	H	L

users follow the Write Byte protocol exactly, the new data contained in the Data Byte is written into the register selected by bits r1 and r0 on the Stop Bit.

General Purpose Input/Outputs (GPIOs)

The LTC4306 provides two general purpose input/output pins (GPIOs) that can be configured as logic inputs, open-drain outputs or push-pull outputs. The GPIO1 and GPIO2 Mode Configure bits in register 2 determine whether the GPIOs are used as inputs or outputs. When the GPIOs are used as outputs, the GPIO1 and GPIO2 Output Mode Configure bits of register 2 configure the GPIO outputs either as open-drain N-channel MOSFET pull-downs or push-pull stages.

In push-pull mode, at V_{CC} = 3.3V, the typical pull-up impedance is 670Ω and the typical pull-down impedance

OPERATION

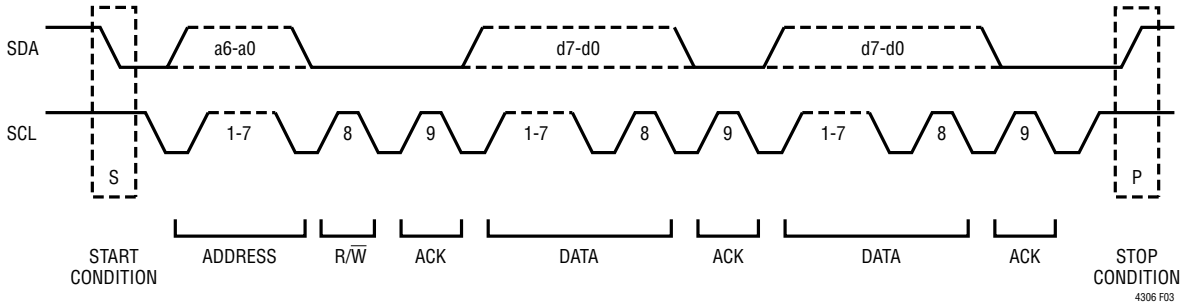


Figure 3. Data Transfer Over I²C or SMBus

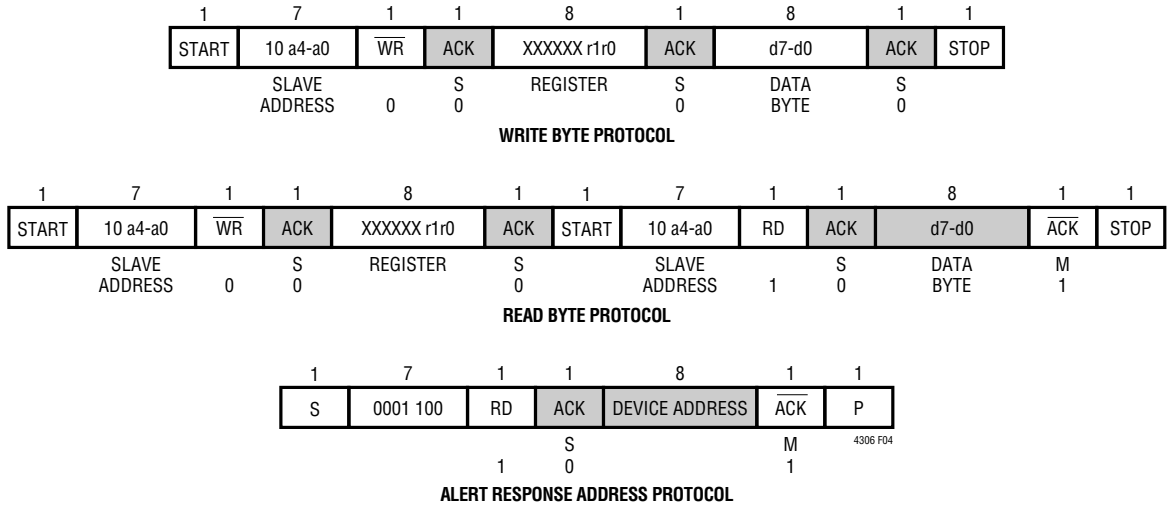


Figure 4. Protocols Accepted by LTC4306

is 35Ω, making the GPIO pull-downs capable of driving LEDs. At V_{CC} = 5V, the typical pull-up impedance is 320Ω and the typical pull-down impedance is 20Ω. In open-drain output mode, the user provides the logic high by connecting a pull-up resistor between the GPIO pin and an external supply voltage. The external supply voltage can range from 1.5V to 5.5V independent of the V_{CC} voltage. In input mode, the GPIO input threshold voltage is 1V.

The GPIO1 and GPIO2 Logic State bits in register 1 indicate the logic state of the two GPIO pins. The logic-level threshold voltage for each pin is 1V. The GPIO1 and GPIO2 Output Driver State bits in register 1 indicate the logic state that the LTC4306 is attempting to write to the GPIO pins. This is useful when the GPIOs are being used in open-drain output mode and one or more external devices are connected to the GPIOs. If the LTC4306 is trying to write a high to a GPIO pin, but the pin's actual logic state is low, then the LTC4306 knows that the low is being forced by an external device.

Glitch Filters

The LTC4306 provides glitch filters on the SDAIN and SCLIN pins as required by the I²C Fast Mode (400kHz) Specification. The filters prevent signals of up to 50ns (minimum) time duration and rail-to-rail voltage magnitude from passing into the two-wire bus digital interface circuitry.

OPERATION

Fall Time Control

Per the I^2C Fast Mode (400kHz) Specification, the two-wire bus digital interface circuitry provides fall time control when forcing logic lows onto the SDAIN bus. The fall time always meets the limits:

$(20 + 0.1 \bullet C_B) < t_f < 300ns$

where t_f is the fall time in ns and C_B is the equivalent bus capacitance in pF. Whenever the Upstream-Downstream Buffer Circuitry is active, its output signal will meet the fall time requirements, provided that its input signal meets the fall time requirements.

APPLICATIONS INFORMATION

Design Example

A typical LTC4306 application circuit is shown in Figure 5. The circuit illustrates the level-shifting, multiplexer/switch and capacitance buffering features of the LTC4306. In this application, the LTC4306 V_{CC} voltage and downstream bus 1 are powered from a 3.3V supply voltage; downstream bus 4 is powered from 5V, and the upstream bus is powered from 2.5V. Channels 2 and 3 are omitted for simplicity. The following sections describe a methodology for choosing the external components in Figure 5.

SDA, SCL Pull-Up Resistor Selection

The pull-up resistors on the SDA and SCL pins must be strong enough to provide a minimum of 100µA pull-up current, per the SMBus Specification. In most systems, the required minimum strength of the pull-up resistors is determined by the minimum slew requirement to guarantee that the LTC4306's rise time accelerators are activated during rising edges. At the same time, the pull-up value should be kept low to maximize the logic low noise margin and minimize the offset voltage of the Upstream-Downstream Buffer circuitry. The LTC4306 is designed to function for a maximum DC pull-up current of 4mA. If multiple downstream channels are active at the same time, this means that the sum total of the pull-up currents from these channels must be less than 4mA. At supply voltages of 2.7V and 5.5V, pull-up resistor values of 10k work well for capacitive loads up to 215pF and 420pF, respectively. For larger bus capacitances, refer to equation (1) below. The LTC4306 works with capacitive loads up to 2nF.

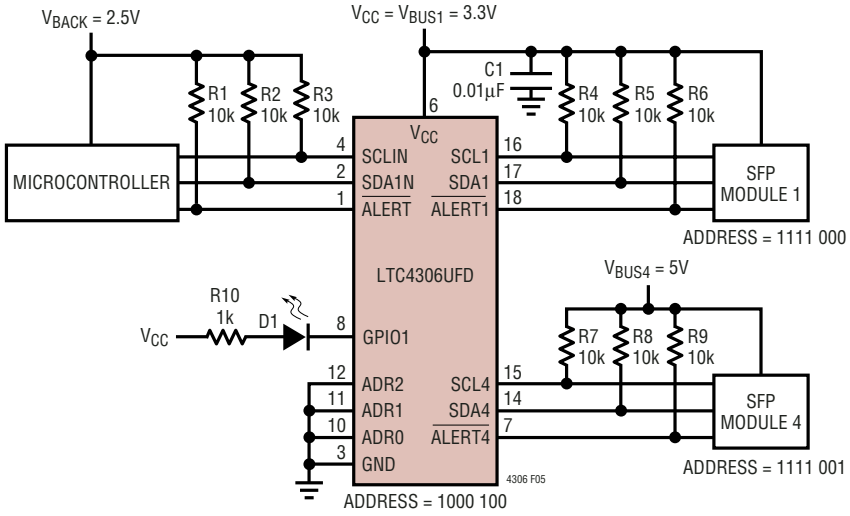


Figure 5. A Level Shifting Circuit

APPLICATIONS INFORMATION

Assume in Figure 5 that the total parasitic bus capacitance on SDA1 due to trace and device capacitance is 100pF. To ensure that the boost currents are active during rising edges, the pull-up resistor must be strong enough to cause the SDA1 pin voltage to rise at a rate of 0.8V/µs as the pin voltage is rising above 0.8V. The equation is:

$$R_{PULL-UP,MAX}\,[k\Omega] = \frac{\left\{(V_{BUSMIN} - 0.8V) \bullet 1250\left[\frac{ns}{V}\right]\right\}}{C_{BUS}\,[pF]} \quad (1)$$

where V_{BUSMIN} is the minimum operating pull-up supply voltage, and C_{BUS} is the bus parasitic capacitance. In our example, $V_{BUS1} = V_{CC} = 3.3V$, and assuming ±10% supply tolerance, $V_{BUS1MIN}$ = 2.97V. With C_{BUS} = 100pF, $R_{PULL-UP,MAX}$ = 27.1k. Therefore, we must choose a pull-up resistor smaller (i.e., stronger pull-up) than 27.1k, so a 10k resistor works fine.

$\overline{\text{ALERT}}$, READY and GPIO Component Selection

The pull-up resistors on the $\overline{\text{ALERT}}$ and READY pins must provide a maximum pull-up current of 3mA, so that the LTC4306 is capable of holding the pin at logic low voltages below 0.4V. When choosing LEDs to be driven by the LTC4306's GPIO pins, make sure that the required LED sinking current is less than 5mA, and add a current-limiting resistor in series with the LED.

Level Shifting Considerations

In the design example of Figure 5, the LTC4306 V_{CC} voltage is less than or equal to both of the downstream bus pull-up voltages, so buses 1 and 4 can be active at the same time. Likewise, the rise time accelerators can be turned on for the downstream buses, but must never be activated on SCLIN and SDAIN, because doing so would result in significant current flow from V_{CC} to V_{BACK} during rising edges.

Other Application Circuits

Figure 6 illustrates how the LTC4306 can be used to expand the number of devices in a system by using nested addressing. Each I/O card contains a temperature sensor having device address 1001 000. If the four I/O cards were plugged directly into the backplane, the four sensors would require four unique addresses. However, if masters use the LTC4306 in multiplexer mode, where only one downstream channel is connected at a time, then each I/O card can have a device with address 1001 000 and no problems will occur.

Figures 7 and 8 show two different methods for hot-swapping I/O cards onto a live two-wire bus using the LTC4306. The circuitry of Figure 7 consists of an LTC4306 residing on the edge of an I/O card having four separate downstream buses. Connect a 200k resistor to ground from the ENABLE pin and make the ENABLE pin the shortest pin on the connector, so that the ENABLE pin remains at a constant logic low while all other pins are connecting. This ensures that the LTC4306 remains in its default high impedance state and ignores connection transients on its SDAIN and SCLIN pins until they have established solid contact with the backplane 2-wire bus. In addition, make sure that the $\overline{\text{ALERT}}$ connector pin is shorter than the V_{CC} pin, so that V_{CC} establishes solid contact with the I/O card pull-up supply pin and powers the pull-up resistors on $\overline{\text{ALERT1}}$–$\overline{\text{ALERT4}}$ before ALERT makes contact.

Figure 8 illustrates an alternate SDA and SCL hot-swapping technique, where the LTC4306 is located on the backplane and an I/O card plugs into downstream channel 4. Before plugging and unplugging the I/O card, make sure that channel 4's downstream switch is open, so that it does not disturb any 2-wire transaction that may be occurring at the moment of connection/disconnection. Note that pull-up resistor, R17, on $\overline{\text{ALERT4}}$ should be located on the backplane and not the I/O card to ensure proper operation of the LTC4306 when the I/O card is not present. The pull-up resistors on SCL4 and SDA4, R15 and R16 respectively, may be located on the I/O card, provided that downstream bus 4 is never activated when the I/O card is not present. Otherwise, locate R15 and R16 on the backplane.

APPLICATIONS INFORMATION

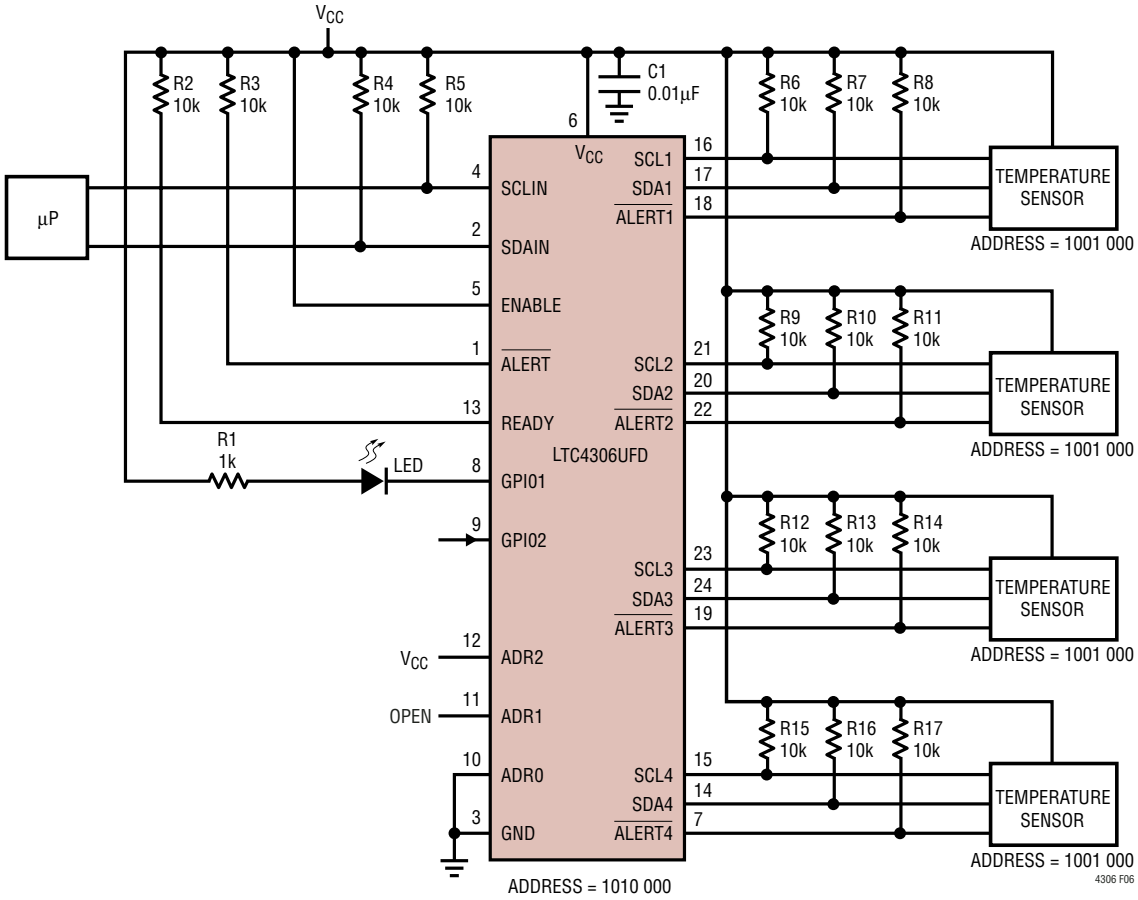


Figure 6. Nested Addressing Application

APPLICATIONS INFORMATION

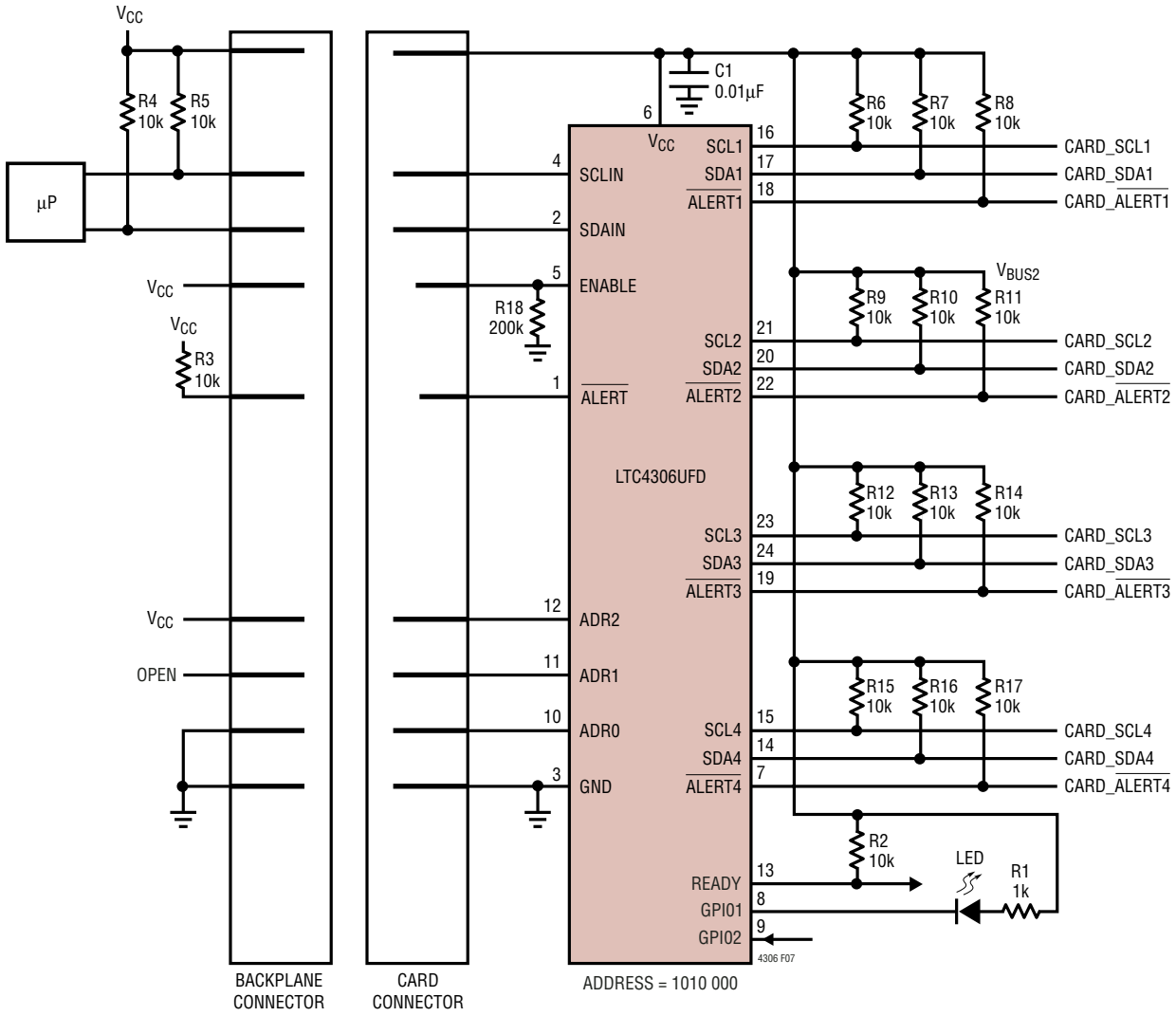
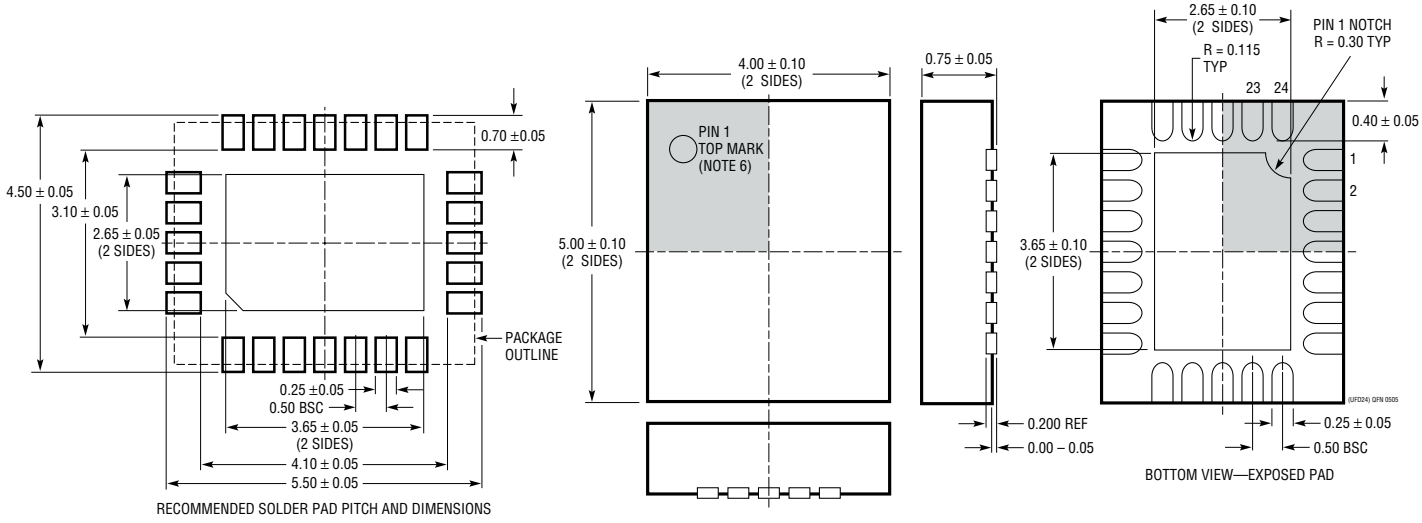


Figure 7. Hot-Swapping Application

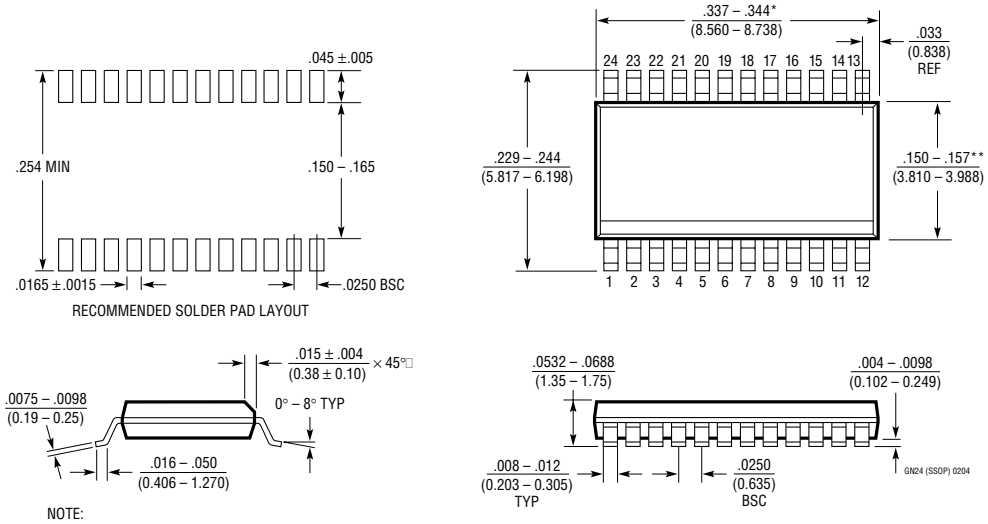
PACKAGE DESCRIPTION

UFD Package
24-Lead Plastic QFN (4mm x 5mm)
(Reference LTC DWG # 05-08-1696)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

GN Package
24-Lead Plastic SSOP
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

APPLICATIONS INFORMATION

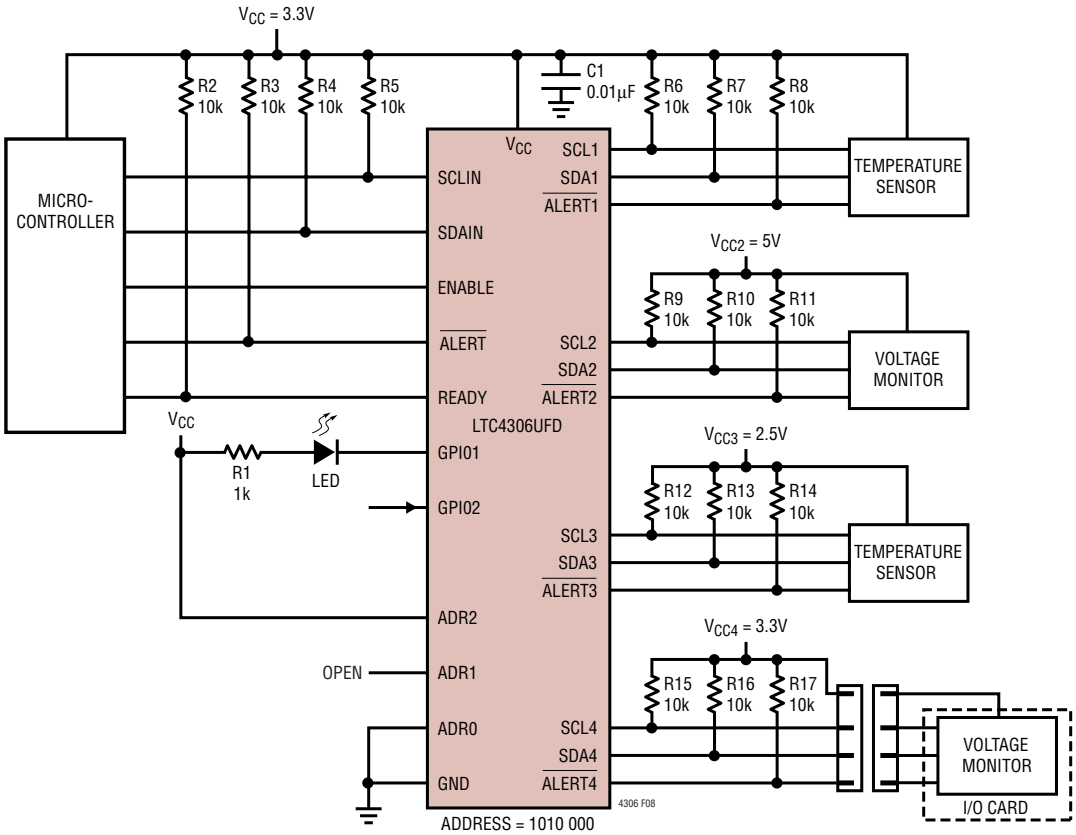


Figure 8. Downstream Side Hot-Swapping Application

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1380/LTC1393	Single-Ended 8-Channel/Diffierential 4-Channel Analog Mux with SMBus Interface	Low R_{ON}: 35Ω Single-Ended/70Ω Differential, Expandable to 32 Single or 16 Differential Channels
LTC1427-50	Micropower, 10-Bit Current Output DAC with SMBus Interface	Precision 50µA ±2.5% Tolerance Over Temperature, 4 Selectable SMBus Addresses, DAC Powers Up at Zero or Midscale
LTC1694/LTC1694-1	SMBus Accelerator	Improved SMBus/I²C Rise Time, Ensures Data Integrity with Multiple SMBus/I²C Devices
LT®1786F	SMBus Controlled CCFL Switching Regulator	1.25A, 200kHz, Floating or Grounded Lamp Configurations
LTC1695	SMBus/I²C Fan Speed Controller in ThinSOT™	0.75Ω PMOS 180mA Regulator, 6-Bit DAC
LTC1840	Dual I²C Fan Speed Controller	Two 100µA 8-Bit DACs, Two Tach Inputs, Four GPIO
LTC4300A-1/LTC4300A-2	Hot Swappable 2-Wire Bus Buffer	Isolates Backplane and Card Capacitances
LTC4300A-3	Hot Swappable 2-Wire Bus Buffer	Provides Level Shifting and Enable Functions
LTC4301	Supply Independent Hot Swappable 2-Wire Bus Buffer	Supply Independent
LTC4301L	Hot Swappable 2-Wire Bus Buffer with Low Voltage Level Translation	Allows Bus Pull-Up Voltages as Low as 1V on SDAIN and SCLIN
LTC4303/LTC4304	How Swappable Bus Buffers with Stuck Bus Recovery	Recover Stuck Buses with Automatic Clocking
LTC4305	2-Channel 2-Wire Multiplexer with Capacitance Buffering	2 Selectable Downstream Buses, Stuck Bus Disconnect, Rise Time Accelerators, Fault Reporting, ±10kV HBM ESD Tolerance

ThinSOT is a trademark of Linear Technology Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT/LWI/TP 0805 500 • PRINTED IN USA

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

LTC4306IGN#PBF LTC4306IUFD LTC4306CGN#TR LTC4306CGN LTC4306IUFD#PBF LTC4306IGN#TR LTC4306CUFD LTC4306IUFD#TR LTC4306CUFD#PBF LTC4306CUFD#TRPBF LTC4306IGN LTC4306IUFD#TRPBF LTC4306CUFD#TR LTC4306CGN#TRPBF LTC4306IGN#TRPBF LTC4306CGN#PBF