PAC1710/20

Single and Dual High-Side Current-Sense Monitor with Power Calculation

Features

- Single and Dual High-Side Current Sensor
  - Current measurement is integrated over 2.5 ms to 2.6 seconds with up to 11-bit resolution
  - 1% current measurement accuracy in positive range
  - Measures V_{SOURCE} voltages
- Calculates Power
- V_{SOURCE} Voltage Range 0V to 40V
- Bidirectional Current Sensing
- Auto-Zero Input Offset Voltage
- Digital Averaging
  - Adjustable sampling time and resolution
- 5 µA Typical Standby Current
- Programmable Sense Voltage Range
  - ±10 mV, ±20 mV, ±40 mV, and ±80 mV
- Power Supply Range 3.0V to 5.5V
- Wide Temperature Operating Range: -40°C to +85°C
- $\overline{\text{ALERT}}$ Output for Voltage and Current out of Limit Transients Between Sampling Interval
- SMBus 2.0 Communications Interface
  - Block Read and Block Write
  - Address selectable by resistor decode
- Sample Time Configurable from 2.5 ms to 320 ms
  - With averaging effective sampling times up to 2.6 seconds
- 10-Lead 3 x 3 mm VDFN package

Applications

- Notebook and Desktop Computers
- Industrial
- Power Management Systems
- Embedded Applications
- Servers

Description

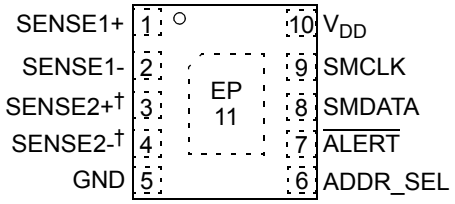
The PAC1710/20 are single and dual high-side bidirectional current sensing monitors with precision voltage measurement capabilities. Each sensor measures the voltage developed across an external sense resistor to represent the high-side current of a battery or voltage regulator. The PAC1710/20 also measures the SENSE+ pin voltage and calculates average power over the integration period. The $\overline{\text{ALERT}}$ pin can be programmed to assert when high and low limits are exceeded for Current Sense and Bus Voltage.

The PAC1710/20 device is good for measuring dynamic power. The long integration time allows for extending system polling cycles without losing any power consumption information. In addition the alert ensures that transient events are captured between the polling cycles.

Available in a RoHS compliant 3 x 3 mm 10-pin VDFN package.

Package Types

PAC1710/20
3x3 VDFN*

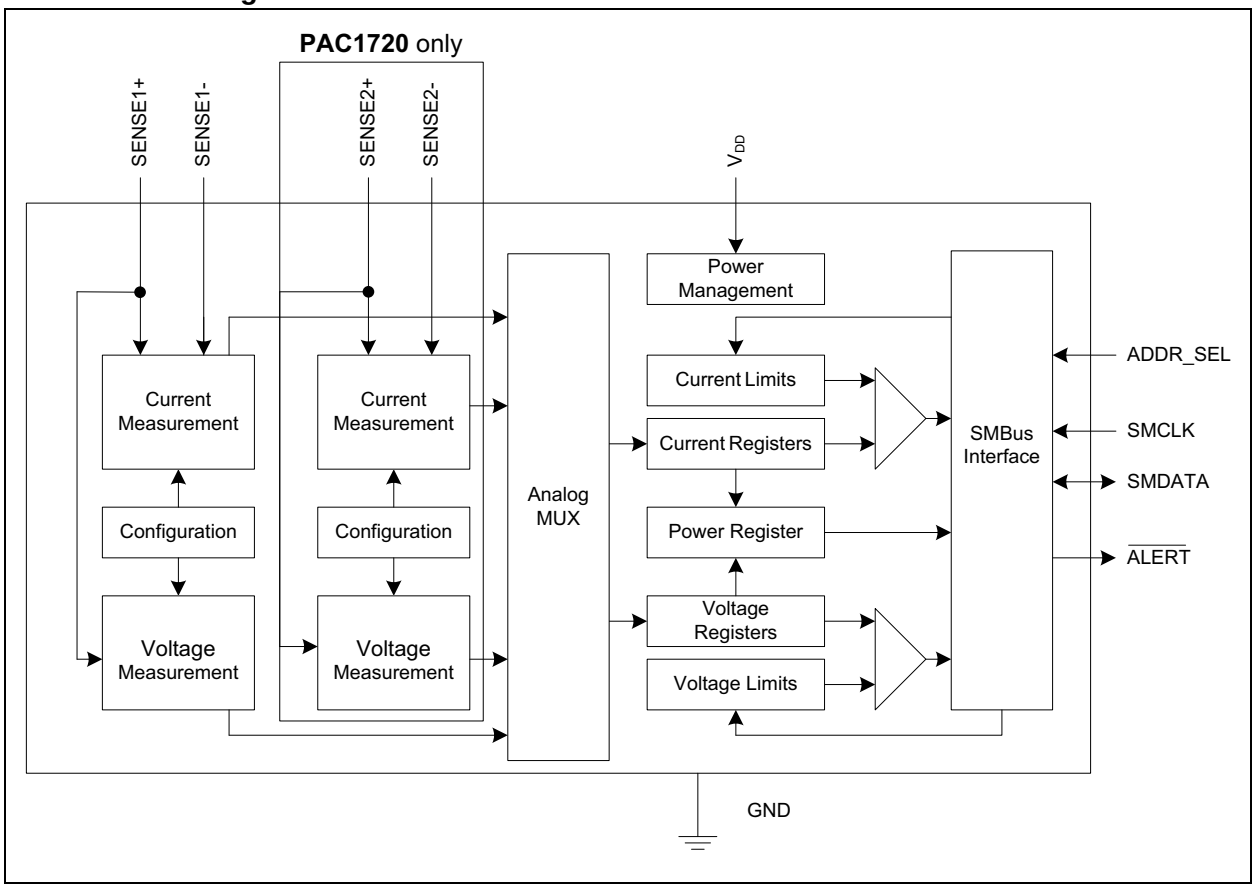


*Includes Exposed Thermal Pad (EP), see Table 3-1

†PAC1720 only.

© 2015-2016 Microchip Technology Inc.

Device Block Diagram



© 2015-2016 Microchip Technology Inc.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Electrical Specifications

Absolute Maximum Ratings(†)

V_{DD} pin ..... -0.3 to 6.0V

Voltage on SENSE- and SENSE+ pins ..... -42 to 42V

Voltage on any other pin to GND ..... -GND-0.3 to V_{DD}+0.3V

Voltage between Sense pins (|(SENSE+ – SENSE-)|) 40V

Input current to any pin except V_{DD} ..... +10 mA

Output short-circuit current ..... Continuous

Package Power Dissipation (Note) ..... 0.5W up to T_A = 85°C/W

Junction to Ambient (θ_{J-A}) ..... 78°C/W

Operating Ambient Temperature Range ..... -40 to 85°C

Storage Temperature Range ..... -55 to 150°C

ESD Rating – SMCLK, SMDATA, and $\overline{\text{ALERT}}$ pins – HBM 8000V

SD Rating – all other pins – HBM 2000V

† **Notice**: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

Note:	The Package Power Dissipation specification assumes a recommended thermal via design consisting of a 2 x 3 matrix of 0.3 mm (12 mil) vias at 0.9 mm pitch connected to the ground plane with a 1.6 mm x 2.3 mm thermal landing.

TABLE 1-1: DC CHARACTERISTICS

Electrical Characteristics: Unless otherwise specified, maximum values are at T_A = -40°C to +85°C, V_{DD} = 3V to 5.5V, V_{SOURCE} = 0V to 40V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{SOURCE} = 24V, V_{SENSE} = (SENSE+ – SENSE-) = 0V; Current Sense Full Scale Range = 80 mV unless otherwise noted

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Supply						
Voltage on SENSE+	V_{SOURCE}	0	—	40	V	
V_{DD} Range	V_{DD}	3.0	—	5.5	V	
V_{DD} Pin Supply Current (PAC1720)	I_{DD}	—	0.525	1.3	mA	Both measurement channels enabled. Continuous conversions (see Table 4-1)
		—	13	50	µA	Both measurement channels enabled. One conversion per second (see Table 4-1). VSRC_SAMP_TIME = 2.5 ms CS_SAMP_TIME = 2.5 ms No SMBus communications
V_{DD} Pin Supply Current (PAC1710)	I_{DD}	—	360	900	µA	Continuous Conversions (see Table 4-1)
		—	10	35	µA	One conversion per second (see Table 4-1). VSRC_SAMP_TIME = 2.5 ms CS_SAMP_TIME = 2.5 ms No SMBus communications
V_{DD} Rise Rate	V_{DD_RISE}	0.03			V/ms	0 to 3V in 100 ms
V_{DD} Standby Current	I_{DD_STBY}	—	5.5	15	µA	Standby state
Analog Input Characteristics						
SENSE+/SENSE- Pins Common-Mode Voltage Range	V_{CM}	0	—	40	V	Common-mode voltage on SENSE pins, referenced to ground
V_{SENSE} Differential Input Voltage Range	V_{DIFF}	-80	—	+80	mV	Voltage between SENSE+ and SENSE- pins
Current-Sense Power Supply Rejection Ratio	PSRR_CS	—	10	—	µV/V	3.0V < V_{DD} < 5.5V
Full-Scale Range (±) (see **Section 4.4 "Current Measurement"**)	FSR	-10	—	10	mV	1 LSB = 4.885 µV 11-bit data resolution
		-20	—	20	mV	1 LSB = 9.77 µV 11-bit data resolution
		-40	—	40	mV	1 LSB = 19.54 µV 11-bit data resolution
		-80	—	80	mV	1 LSB = 39.08 µV 11-bit data resolution
Common-Mode Rejection	V_{SENSE_CMRR}	80	100	—	dB	Common-Mode Rejection, 0V < V_{SOURCE} < 40V
SENSE+/SENSE- Pins Common-Mode Voltage Range	V_{CM}	0	—	40	V	Common-mode voltage on SENSE pins, referenced to ground
V_{BUS} Gain Accuracy	$V_{BUS\_GAIN\_ERR}$	—	—	±0.4	%	Measured at ADC output, Gain = 1

© 2015-2016 Microchip Technology Inc.

TABLE 1-1: DC CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, maximum values are at T_A = -40°C to +85°C, V_{DD} = 3V to 5.5V, V_{SOURCE} = 0V to 40V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{SOURCE} = 24V, V_{SENSE} = (SENSE+ – SENSE-) = 0V; Current Sense Full Scale Range = 80 mV unless otherwise noted						
Characteristic	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
SENSE+, SENSE- Pin Leakage Current	I_{SENSE+}, I_{SENSE-}	—	—	1.0	µA	V_{BUS} = 24V, V_{SENSE} = 0V Sleep state
SENSE+, SENSE- Pin Leakage Current	I_{SENSE+}, I_{SENSE-}	—	—	1.0	µA	V_{DD} = 0V
SENSE+ Pin Bias Current	I_{SENSE+}	—	100	150	µA	-80 mV < V_{SENSE} < 80 mV Active state
SENSE- Pin Bias Current	I_{SENSE-}	—	0.1	1	µA	-80 mV < V_{SENSE} < 80 mV Active state
Current-Sense Offset Error Voltage						
Offset Error Voltage (referred to input)	V_{OS}	—	±15	—	µV	FSR = ±10 mV
		—	±15	—	µV	FSR = ±20 mV
		—	±20	—	µV	FSR = ±40 mV
		—	±40	—	µV	FSR = ±80 mV
Current-Sense Total Measurement Error						
Total Error (positive range) (see **Section 4.4 "Current Measurement"**)	$V_{SENSE\_TOT\_ERR}$	—	±0.5	±1	% FSR	FSR = 0 to +10 mV
		—	±0.3	±0.6	% FSR	FSR = 0 to +20 mV
		—	±0.2	±0.4	% FSR	FSR = 0 to +40 mV
		—	±0.2	±0.4	% FSR	FSR = 0 to +80 mV
Total Error (negative range) (see **Section 4.4 "Current Measurement"**)	$V_{SENSE\_TOT\_ERR}$	-1	-1.3	-1.6	% FSR	FSR = -10 mV to 0
		-1	-1.3	-1.6	% FSR	FSR = -20 mV to 0
		-1	-1.3	-1.6	% FSR	FSR = -40 mV to 0
		-1.6	-2	-2.4	% FSR	FSR = -80 mV to 0
V_{SOURCE} Voltage Measurement						
Power Supply Rejection Ratio	PSRR	—	10	—	mV/V	3.0V < V_{DD} < 5.5V
V_{SOURCE} Error (±)	V_{SOURCE_ERR}	—	0.15	0.3	% FSV	

TABLE 1-1: DC CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, maximum values are at T_A = -40°C to +85°C, V_{DD} = 3V to 5.5V, V_{SOURCE} = 0V to 40V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{SOURCE} = 24V, V_{SENSE} = (SENSE+ – SENSE-) = 0V; Current Sense Full Scale Range = 80 mV unless otherwise noted						
Characteristic	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Power Ratio						
Total Power Ratio Measurement Error (±) (positive range)	P_{RATIO_ERR}	—	—	1	% FSR	FSR = 0 to +10 mV, 0 to +20 mV, 0 to +40 mV, or 0 to +80 mV
Total Power Ratio Measurement Error (±) (negative range)	P_{RATIO_ERR}	—	—	2	% FSR	FSR = -10 mV to 0, -20 mV to 0, -40 mV to 0, or -80 mV to 0
First Power Ratio Ready	t_{CONV_P}	—	—	220	ms	Time after power-up before P_{RATIO} updated
Digital I/O Pins (SMCLK, SMDATA, $\overline{\text{ALERT}}$)						
Pull-up Voltage Range	V_{PULLUP}	3.0	—	5.5	V	Pull-up voltage for SMBus and $\overline{\text{ALERT}}$ pins
Time to First Communications	t_{COMM}	—	—	25	ms	
Input High Voltage	V_{IH}	2.0	—	—	V	SMCLK, SMDATA OD pins pulled up to V_{PULLUP}
Input Low Voltage	V_{IL}	—	—	0.8	V	
Output Low Voltage	V_{OL}	—	—	0.4	V	OD pin pulled to V_{PULLUP} 3 mA current sink
Leakage Current (±)	I_{LEAK}	—	—	5	µA	Powered or unpowered T_A < +85°C

© 2015-2016 Microchip Technology Inc.

TABLE 1-2: SMBUS MODULE SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, maximum values are at T_A = -40°C to +85°C, V_{DD} = 3V to 5.5V, V_{BUS} = 0V to 32V; Typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 24V, V_{SENSE} = (SENSE+ – SENSE-) = 0V						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
SMBus Interface						
Input Capacitance	C_{IN}	—	4	10	pF	
SMBus Timing						
Clock Frequency	f_{SMB}	10	—	400	kHz	
Spike Suppression	t_{SP}	—	—	100	ns	
Bus Free Time Stop to Start	t_{BUF}	1.3	—	—	µs	
Start Setup Time	$t_{SU:STA}$	0.6	—	—	µs	
Start Hold Time	$t_{HD:STA}$	0.6	—	—	µs	
Stop Setup Time	$t_{SU:STO}$	0.6	—	—	µs	
Data Hold Time	$t_{HD:DAT}$	0	—	—	µs	When transmitting to the master
Data Hold Time	$t_{HD:DAT}$	0.3	—	—	µs	When receiving from the master
Data Setup Time	$t_{SU:DAT}$	0.6	—	—	µs	
Clock Low Period	t_{LOW}	1.3	—	—	µs	
Clock High Period	t_{HIGH}	0.6	—	—	µs	
Clock/Data Fall Time	t_{FALL}	—	—	300	ns	Min = 20 + 0.1 C_{LOAD} ns
Clock/Data Rise Time	t_{RISE}	—	—	300	ns	Min = 20 + 0.1 C_{LOAD} ns
Capacitive Load	C_{LOAD}	—	—	400	pF	Total per bus line

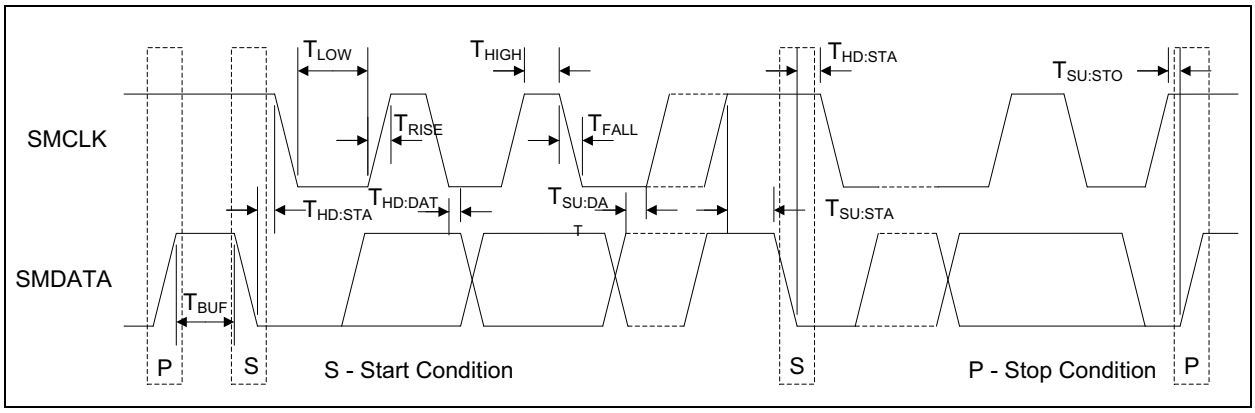


FIGURE 1-1: *SMBus Timing.*

NOTES:

© 2015-2016 Microchip Technology Inc.

2.0 TYPICAL OPERATING CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, maximum values are at T_A = -40°C to +85°C, V_{DD} = 3V to 5.5V, V_{SOURCE} = 0V to 40V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{SOURCE} = 24V, V_{SENSE} = (SENSE+ – SENSE-) = 0V.

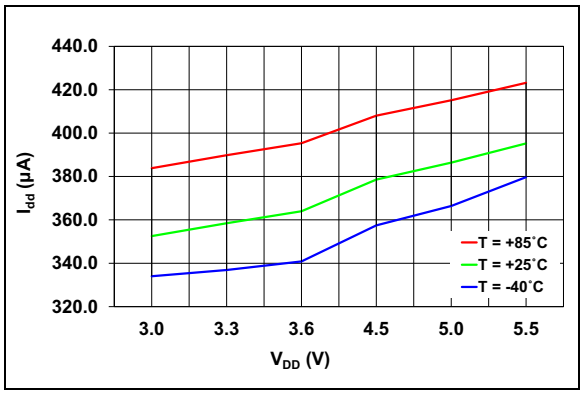


FIGURE 2-1: *I_{DD} vs. V_{DD}, Continuous Conversions (**PAC1710**).*

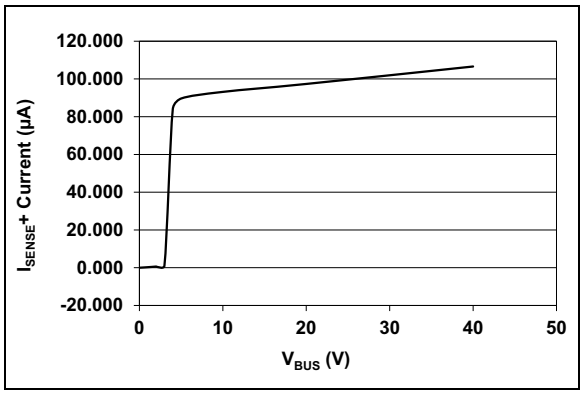


FIGURE 2-4: *I_{SENSE}+ Pin Current vs. V_{BUS} (T_A = -40°C to +85°C).*

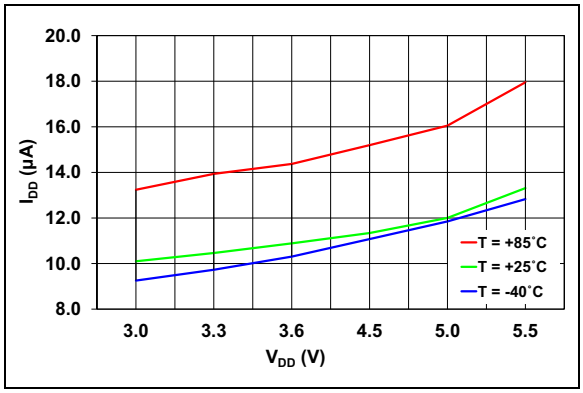


FIGURE 2-2: *I_{DD} vs. V_{DD}, One Conversion per Second, Lowest Resolution (**PAC1710**).*

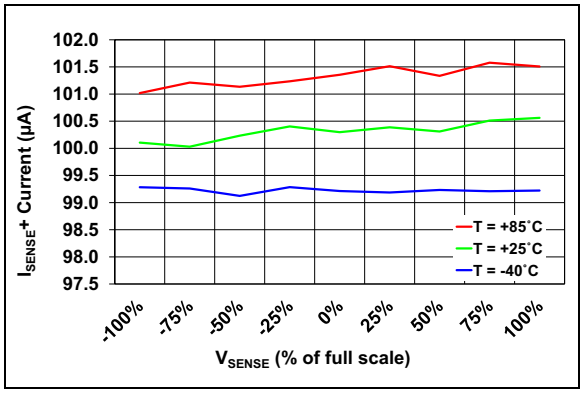


FIGURE 2-5: *I_{SENSE}+ Pin Bias Current (80 mV Range).*

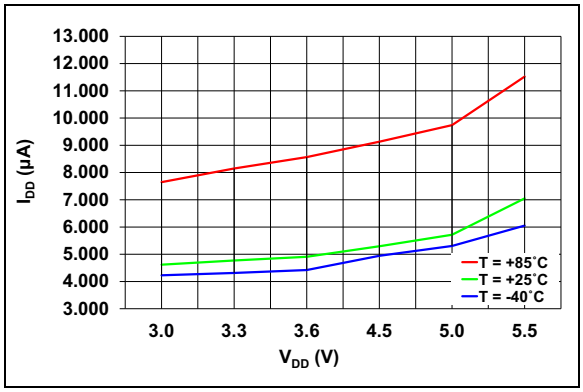


FIGURE 2-3: *I_{DD} vs. V_{DD}, Standby Mode (**PAC1710**)*

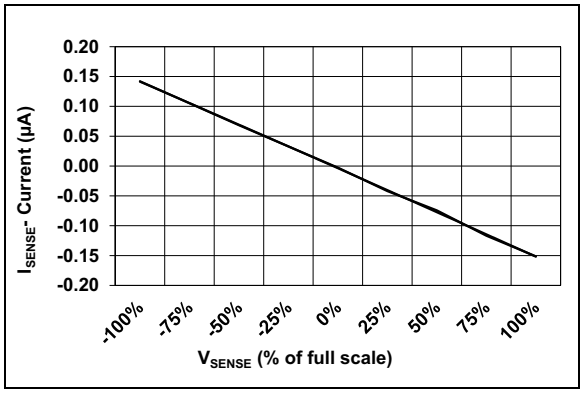


FIGURE 2-6: *I_{SENSE}- Pin Bias Current (80 mV Range, T_A = -40°C to +85°C).*

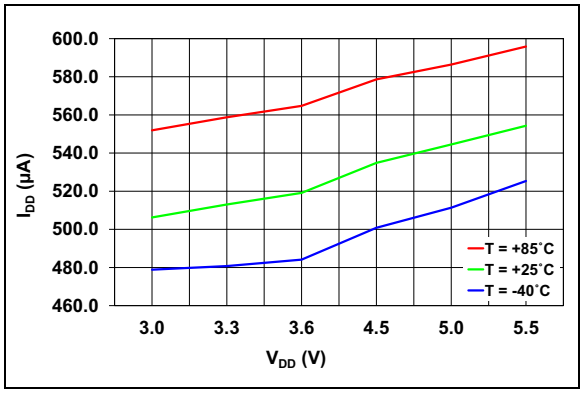


FIGURE 2-7: *I_{DD} vs. V_{DD}, Continuous Conversions (**PAC1720**).*

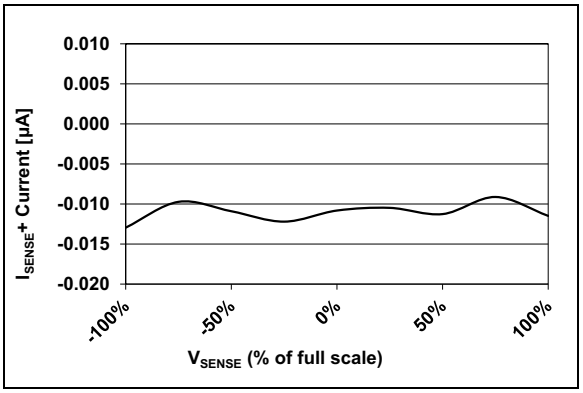


FIGURE 2-10: *I_{SENSE}+ Pin Leakage Current, T_A = -40°C to +85°C.*

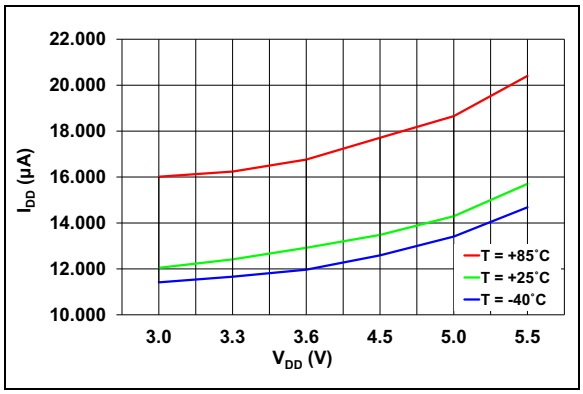


FIGURE 2-8: *I_{DD} vs. V_{DD}, One Conversion per Second, Lowest Resolution (**PAC1720**).*

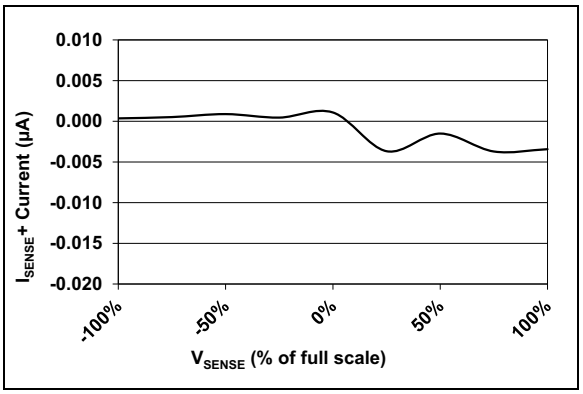


FIGURE 2-11: *I_{SENSE}- Pin Leakage Current, T_A = -40°C to +85°C.*

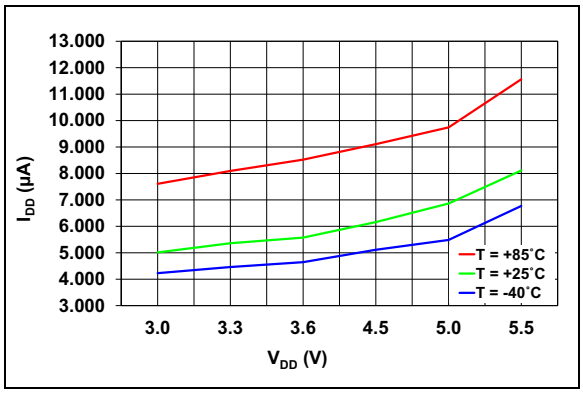


FIGURE 2-9: *I_{DD} vs. V_{DD}, Standby Mode (**PAC1720**).*

© 2015-2016 Microchip Technology Inc.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN DESCRIPTIONS

PAC1710/20 3x3 VDFN	Symbol	Type (See Table 3-2)	Description
1	SENSE1+	AIO40	VBUS1/VSENSE1+ input
2	SENSE1-	AIO40	VSENSE1- input
3	SENSE2+	AIO40	VBUS2/VSENSE2+ input
4	SENSE2-	AIO40	VSENSE2- input
5	GND	Power	Ground
6	ADDR_SEL	AIO	Selects SMBus/I²C™ address
7	$\overline{\text{ALERT}}$	DO	SMBus Alert Pin
8	SMDATA	DIOD	SMDATA: SMBus - requires pull-up resistor
9	SMCLK	DI	SMCLK: SMBus - requires pull-up resistor
10	V_{DD}	Power	Positive power supply voltage
11	EP	—	Not internally connected, but recommend grounding.

TABLE 3-2: PIN TYPES DESCRIPTION

Pin Type	Description
Power	This pin is used to power the device
AIO40	Analog Input/Output – this pin is used as an I/O for analog signals. Maximum voltage is 40V.
AIO5	Analog Input/Output – this pin is used as an I/O for analog signals. Maximum voltage is 5V.
DI	Digital Input – this pin is used for digital inputs
DIOD	Digital Input/Output Open Drain – this pin is used for digital I/O and is open drain

3.1 Sense1+/Sense1-

These two pins form the differential input for measuring voltage across a sense resistor in the application. The positive input (Sense1+) also acts as the input pin for bus voltage.

3.2 Sense2+/Sense2- (PAC1720 only)

These two pins form the differential input for measuring voltage across a sense resistor in the application. The positive input (Sense2 +) also acts as the input pin for bus voltage.

3.3 Ground (GND)

System ground.

3.4 Address Selection (ADDR_SEL)

Address selection for the SMBus Slave address, based on the pull-down resistor.

3.5 SMBus ALERT ($\overline{\text{ALERT}}$)

This pin is the SMBus ALERT pin that is asserted under fault conditions.

3.6 SMBus Data (SMDATA)

This is the bidirectional SMBus data pin. This pin is open drain, and requires a pull-up resistor.

3.7 SMBus Clock (SMCLK)

This is the SMBus clock pin. This pin is open drain, and requires a pull-up resistor.

3.8 Positive Power Supply Voltage (V_{DD})

Power supply input pin for the device.

3.9 Exposed Thermal Pad (EP)

This pad should be connected to ground for noise immunity.

NOTES:

© 2015-2016 Microchip Technology Inc.

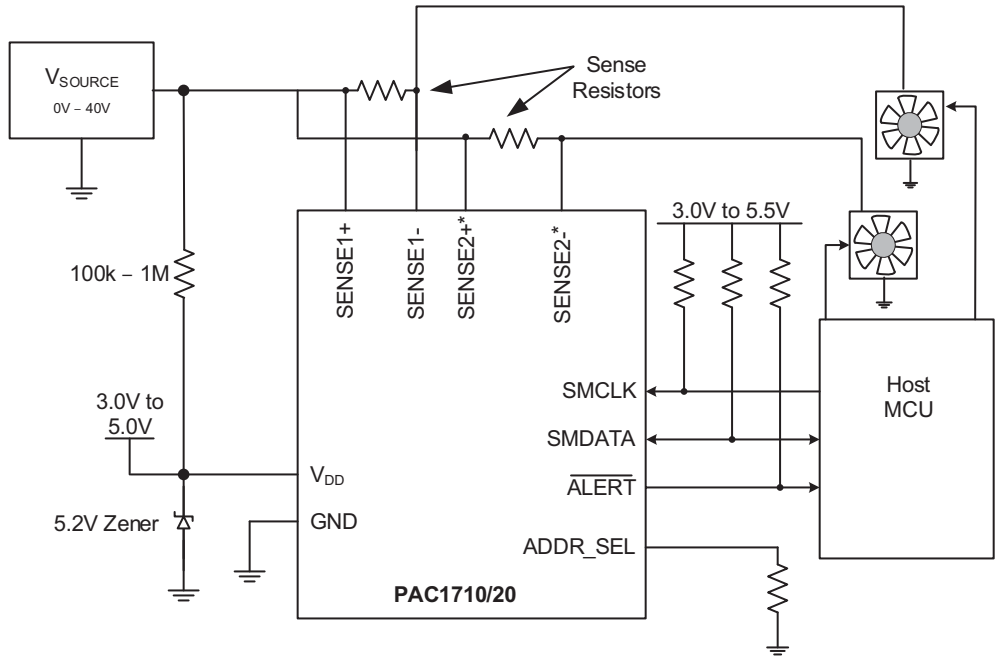
4.0 GENERAL DESCRIPTION

The PAC1710/20 is a bidirectional high-side current-sensing device with precision voltage measurement capabilities. It measures the voltage developed across an external sense resistor to represent the high-side current of a battery or voltage regulator. The PAC1710/20 also measures the SENSE1+ and SENSE2+ pin voltages (V_{SOURCE}) and calculates average power over the integration period.

The PAC1710/20 measures the differential voltage across an external sense resistor, digitizes it with a variable resolution (6-bit to 11-bit plus sign) Sigma-Delta ADC, and transmits via the SMBus or the I^2C™ protocol. The current range allows for large variations in measured current with high accuracy and low voltage drop across the resistor.

The PAC1710/20 has programmable high and low limits for current sense and bus voltage with a maskable $\overline{ALERT}$ signal to the host when an out-of-limit measurement occurs.

A system diagram is shown in Figure 4-1.



Note 1: The device MUST be biased PRIOR to applying V_{SOURCE}. Failure to do so will result in damage.

2: The unpowered bias on V_{DD} must be greater than V_{DD}, if V_{DD} will be removed prior to V_{SOURCE}.

*__PAC1720__ only.

FIGURE 4-1: *PAC1710/20 System Diagram.*

4.1 Power States

The PAC1710/20 has three states of operation:

- Active – The PAC1710/20 initiates conversion cycles for the programmed conversion rate.
- Standby – This is the lowest power state. There are no conversion cycles. The majority of circuitry is powered-down to reduce supply current to a minimum. The SMBus is active and the part will return requested data. To enter the Standby state, disable all measurements (see Register 6-1).
- One-Shot – While the device is in the Standby state, the host can initiate a conversion cycle on demand (see Register 6-3). After the conversion cycle is complete, the device will return to the Standby state.

4.2 Conversion Cycle

The conversion cycle is the period of time in which the measurements are taken and the data is updated. In the Active state, individual measurement can be disabled. In the Standby state, all measurements are updated.

During the conversion cycle, both channels on the PAC1720 begin taking measurements at the same time. In both devices, the V_{SENSE} sample is taken first for its programmed sample time. Then, the V_{SOURCE} sample is taken for its programmed sample time. Digital averaging may be applied to average the last 2-8 samples. Sample time and digital averaging have separate controls for V_{SENSE} and V_{SOURCE} as well as for each channel, in the case of PAC1720. (see Register 6-7 and Register 6-8).

At the end of the conversion cycle, the enabled measurements are updated. The Power Ratio, High Limit Status (which includes a CONV_DONE status bit), and Low Limit Status registers are always updated. The $\overline{ALERT}$ pin will be asserted, by default, if any out-of-limit conditions exist (see **Section 4.7 "ALERT Output"**).

4.3 Conversion Rate

For power management in the Active state, a conversion rate can be programmed. Conversion rate specifies how often measurement data should be updated. Once per second is the lowest setting (see Register 6-2).

If the actual sampling time for both measurements (V_{SOURCE} and V_{SENSE}) is greater than 1/conversion rate for either channel, the PAC1710/20 will override the programmed conversion rate and operate in continuous mode.

4.4 Current Measurement

The PAC1710/20 includes one or two high-side current sensing circuits. These circuits measure the voltage (V_{SENSE}) induced across a fixed external current sense resistor (R_{SENSE}) and stores the voltage as a signed 11-bit (by default) number in the Sense Voltage registers.

The PAC1710/20 current sensing operates in one of four bipolar Full-Scale Ranges (FSR): ±10 mV, ±20 mV, ±40 mV, or ±80 mV (see **Section 4.4 "Current Measurement"**). The default FSR is ±80 mV.

Full-Scale Current (FSC) can be calculated from Equation 4-1.

EQUATION 4-1: FULL-SCALE CURRENT

$$FSC = \frac{FSR}{R_{SENSE}}$$

Where:

FSC	=	Full-scale current
FSR	=	±10 mV, ±20 mV, ±40 mV, or ±80 mV (see Table 4-6)
R_{SENSE}	=	External sense resistor value

The actual current through R_{SENSE} can then be calculated using Equation 4-2.

EQUATION 4-2: BUS CURRENT

$$I_{BUS} = FSC \times \frac{V_{SENSE}}{Denominator}$$

Where:

I_{BUS}	=	Actual bus current
FSC	=	Full-scale current value (from Equation 4-1)
V_{SENSE}	=	The value read from the Sense Voltage Registers (in decimal), ignoring the four lowest bits which are always zero (see Register 6-10 and Register 6-11 for PAC1720)
Denominator	=	Determined by the sample time, as shown in Table 4-5.

As an example, suppose the system is drawing 1.65A through a 10 mΩ resistor, the FSR is set for ±20 mV, and sample time is 80 ms. Using Equation 4-1, the FSC is 2A. The measured V_{SENSE} is 1.65A * 10 mΩ = 16.5 mV. This value of V_{SENSE} is represented in the Sense Voltage Registers as 69_8h (0110_1001_1000b or 1688d) ignoring the 4 lower bits of the low byte as these are always 0. This value, when applied to Equation 4-2, results in an I_{BUS} current of 1.649A.

© 2015-2016 Microchip Technology Inc.

For a negative voltage, the Sense Voltage Registers are read as 96_0h (again ignoring the lower 4 bits of the low byte as these are always 0). To calculate current, the binary value is first converted from two's complement by inverting the bits and adding one:

96_80h = 1001_0110_1000b. Inverting equals 0110_1001_0111b (69_7h) and adding one gives 0110_1001_1000b (69_8h).

This results in the same calculated value as in the positive voltage case.

4.5 Voltage Measurement

The pin voltage is measured on the supply side of the appropriate SENSE+ pin and stored as an unsigned 11-bit number in the V_{SOURCE} Voltage Registers as V_{SOURCE} (see Register 6-12).

Full-Scale Voltage (FSV) is given by the maximum value of the V_{SENSE} Voltage Registers:

EQUATION 4-3: FULL-SCALE VOLTAGE

$$FSV = 40 - \frac{40}{Denominator}$$

Where:

FSV	=	Full scale voltage
Denominator	=	determined by the sample time, as shown in Table 4-2

Actual voltage at SENSE+ can be calculated using Equation 4-4.

EQUATION 4-4: BUS VOLTAGE

$$V_{SOURCE\_PIN} = FSV \times \frac{V_{SOURCE}}{Denominator}$$

Where:

V_{SOURCE_PIN}	=	The actual voltage on the SENSE1+/SENSE2+ pin
FSV	=	The full-scale voltage (from Equation 4-3)
V_{SOURCE}	=	The value read from the V_{SOURCE} Voltage Registers (in decimal), ignoring the lowest five bits which are always zero (see **Section 4.11 "VSOURCE Data representation"**).
Denominator	=	Determined by the sample time, as shown in Table 4-2

As an example using 10-bit resolution, suppose that the actual pin voltage is 24V. The V_{SOURCE} Voltage Registers will report a value of 99_80h (1001_1001_10XX_XXXXb) in 10-bit resolution (default). When reading the data, the lower 5 bits are always ignored. Because the default operation is to measure the V_{SOURCE} voltage with 10-bit resolution, the sixth bit is likewise ignored. Therefore, decoding the upper 10 bits results in a decimal value of 614. This value, when applied in Equation 4-3, results in V_{SOURCE_PIN} equal to 23.98V.

As an example using 11-bit resolution, suppose that the actual pin voltage is 10.65V. The V_{SOURCE} Voltage Registers will report a value of 44_10h (0100_0100_001X_XXXXb). Because the lower 5 bits are ignored, the decimal result is 545d. This value, when applied in Equation 4-4, results in V_{SOURCE_PIN} equal to 10.64V.

The V_{SOURCE} voltage may also be determined by scaling each bit set by the indicated bit weighting as described in **Section 4.11 "VSOURCE Data representation"**.

4.6 Power Calculation

The PAC1710/20 may be used to determine the average power provided at the source side of SENSE+ (SENSE1+ and SENSE2+) using the value P_{RATIO}, contained in the Power Ratio Registers (see Register 6-14). The value represents the percentage of maximum calculable power.

P_{RATIO} is mathematically generated by multiplying the absolute values of V_{SENSE} and V_{SOURCE} (see **Section 4.4 "Current Measurement"** and **Section 4.5 "Voltage Measurement"**) and is stored as a 16-bit number. P_{RATIO} is updated whenever either V_{SENSE} or V_{SOURCE} is updated.

Full-scale power can be calculated from Equation 4-5.

EQUATION 4-5: FULL-SCALE POWER

$$FSP = FSC \times FSV$$

Where:

FSP	=	The full-scale power
FSC	=	The full-scale current (from Equation 4-1)
FSV	=	The full-scale voltage (from Equation 4-3)

Actual power drawn from the source can be calculated using Equation 4-6.

EQUATION 4-6: BUS POWER

$$P_{BUS} = FSP \times \frac{P_{RATIO}}{65,535}$$

Where:

P_{BUS} = The actual power provided by the source measured at SENSE+

FSP = the full-scale power (from Equation 4-5)

P_{RATIO} = the value read from the Power Ratio Registers (in decimal). See Register 6-14 and Register 6-15

As an example, suppose that the actual pin voltage is 10.65V, the current through a 10 mΩ resistor is 1.65A, the FSR is set for ±20 mV, and the sample times are the defaults. The FSC value is 2A per Equation 4-1. The FSV value is 39.96V per Equation 4-4. Using Equation 4-5, the FSP value is 79.92W. Applying P = V ∗ I, the expected power is 17.57W which is 21.98% of the FSP value.

Reading the Power Ratio Registers will report P_{RATIO} as 38_47h (0011_1000_0100_0111b or 14,407d). Using Equation 4-6, this value results in a calculated bus power of 17.57W which is ~21.98% of the FSP value.

4.7 $\overline{\text{ALERT}}$ Output

The $\overline{\text{ALERT}}$ pin is an open-drain output and requires a pull-up resistor to V_{PULLUP}.

The $\overline{\text{ALERT}}$ pin is used as an interrupt signal or as an SMBus Alert signal that allows an SMBus slave to communicate an error condition to the master. One or more SMBus Alert outputs can be hardwired together.

The $\overline{\text{ALERT}}$ pin will be asserted (by default) if the measured V_{SOURCE} voltage or V_{SENSE} voltage are out of limit (≥ high limit or < low limit). The $\overline{\text{ALERT}}$ pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the $\overline{\text{ALERT}}$ pin will remain asserted until the appropriate status bits are cleared.

The $\overline{\text{ALERT}}$ pin can be masked for all out-of-limit measurements by setting the MASK_ALL bit (see Register 6-1) or for an individual out-of-limit measurement (see Register 6-5). Once the $\overline{\text{ALERT}}$ pin has been masked, it will be de-asserted if no unmasked out-of-limit conditions exist. Any interrupt conditions that occur while the $\overline{\text{ALERT}}$ pin is masked will update the status registers normally.

The $\overline{\text{ALERT}}$ pin can be asserted for 5 µs when all measurements are finished (if enabled by setting CONV_DONE_EN, see Register 6-1).

4.8 Conversion Rate

The Conversion Rate controls how often V_{SENSE}, V_{SOURCE}, P_{RATIO} and the status bits are updated in the Active state (see Table 4-1). The conversion rate should only be updated when the PAC1710/20 is in the Standby state. To do this, disable the measurements in the Configuration Register 00h, wait for the conversion cycle to complete by monitoring the XMEAS_DIS bits in 00h until they stay set to '1', change the conversion rate, and then enable the desired measurements.

TABLE 4-1: CONVERSION RATE FOR MEASUREMENT

CONV_RATE<2:0>		Conversion Rate
1	0	
0	0	1 per sec
0	1	2 per sec
1	0	4 per sec
1	1	Continuous (default)

4.9 Sampling Time and Resolution

The PAC1710/20 sampling interval and resolution for measuring V_{SOURCE} and V_{SENSE} are register controlled. The V_{SOURCE} settings based on register values are shown in Table 4-2 and Table 4-3. The V_{SENSE} measurements have an additional parameter: Full-Scale Resolution of the differential input. The V_{SENSE} settings based on register values are shown in Table 4-4, Table 4-5 and Table 4-6.

TABLE 4-2: VOLTAGE SOURCE SAMPLING TIME SETTINGS

VSRC_SAMP_TIME		V_{SOURCE} Sample Time	Equation 4-3 Denominator	Equation 4-4 Denominator
0	0	2.5 ms (data = 8 bits)	256	255
0	1	5 ms (data = 9 bits)	512	511
1	0	10 ms (data = 10 bits) (Default)	1024	1023
1	1	20 ms (data = 11 bits)	2048	2047

TABLE 4-3: VOLTAGE SOURCE AVERAGING SETTINGS

VSRC_AVG		Samples to Average
0	0	Disabled (default)
0	1	2
1	0	4
1	1	8

© 2015-2016 Microchip Technology Inc.

TABLE 4-4: CURRENT-SENSING AVERAGING SETTINGS

CS_SAMP_AVG<1:0>		Samples to Average
0	0	Disabled (default)
0	1	2
1	0	4
1	1	8

TABLE 4-5: CURRENT-SENSING SAMPLING TIME SETTINGS

CS_SAMP_TIME<2:0>			Current Sensor Sample Time	Equation 4-2 Denominator
0	0	0	2.5 ms (Data = sign + 6 bits)	63
0	0	1	5 ms (Data = sign + 7 bits)	127
0	1	0	10 ms (Data = sign + 8 bits)	255
0	1	1	20 ms (Data = sign + 9 bits)	511
1	0	0	40 ms (Data = sign + 10 bits)	1023
1	0	1	80 ms (Data = sign + 11 bits) (default)	2047
1	1	0	160 ms (Data = sign + 11 bits)	2047
1	1	1	320 ms (Data = sign + 11 bits)	2047

Note 1: 160 ms sampling time has built-in 2X analog oversampling using ADC at 12-bit resolution.

2: 320 mx sampling time has built-in 4X analog oversampling using ADC at 13-bit resolution.

TABLE 4-6: CURRENT-SENSING RANGE SETTINGS

CS_RNG<1:0>		Full Scale Range
0	0	-10 mV to 10 mV
0	1	-20 mV to 20 mV
1	0	-40 mV to 40 mV
1	1	-80 mV to 80 mV (default)

4.10 Sense Voltage measurement Resolution

The Sense Voltage Registers store the measured V_{SENSE} value (see **Section 4.4 "Current Measurement"**). Note that the bit weighting values are for representation of the voltage relative to full scale. There is no internal scaling of data and all normal binary bit weightings still apply.

The Sense Voltage Registers data format is standard two's complement format with the positive full-scale value (7F_Fh) and negative full-scale value (80_0h) equal to the programmed FSR.

The Sign bit indicates the direction of current flow. If the Sign bit is '0', the current is flowing through R_{SENSE} from the SENSE+ pin to the SENSE- pin. If the Sign bit is '1', the current is flowing through R_{SENSE} from the SENSE- pin to the SENSE+ pin.

Data resolution is dependent upon sampling time as shown in Table 4-8. The data format (assuming 11-bit resolution) is shown in Table 4-7**.** This data will scale directly with the sampling time.

TABLE 4-7: V_{SENSE} DATA FORMAT

V_{SENSE}	Binary	Hex (as read by registers)
- Full-Scale	1000_0000_0000	80_0h
-2 LSB	1111_1111_1110	FF_Eh
-1 LSB	1111_1111_1111	FF_Fh
0	0000_0000_0000	00_0h
+1 LSB	0000_0000_0001	00_1h
+2 LSB	0000_0000_0010	00_2h
+Full-Scale -1 LSB	0111_1111_1111	7F_Fh

TABLE 4-8: V_{SENSE} DATA RESOLUTION

Sampling Time	Resolution (±)			
	±10 mV	±20 mV	±40 mV	±80 mV
2.5 ms	156.3 µV	312.5 µV	625.0 µV	1.250 mV
5 ms	78.13 µV	156.3 µV	312.5 µV	625.0 µV
10 ms	39.06 µV	78.13 µV	156.3 µV	312.5 µV
20 ms	19.53 µV	39.06 µV	78.13 µV	156.3 µV
40 ms	9.76 µV	19.53 µV	39.06 µV	78.13 µV
≥ 80 ms	4.88 µV	9.76 µV	19.53 µV	39.06 µV

© 2015-2016 Microchip Technology Inc.

4.11 V_{SOURCE} Data representation

The V_{SOURCE} Voltage Registers store the measured V_{SOURCE} value (see **Section 4.5 "Voltage Measurement"**). The measured voltage is determined by summing the bit weights of each bit set. For example, if V_{SOURCE} was 7.4V, the V_{SOURCE} Voltage Registers would read `0010_1111` for the high byte and `0100_0000b` for the low byte corresponding to 5V + 1.25V + 0.625V + 0.3125V + 0.1563V + 0.0390V = 7.3828V.

The bit weightings are assigned for human interpretation. They should be disregarded when translating the information via a computing system, as shown in **Section 4.5 "Voltage Measurement"**.

The V_{SOURCE} Voltage Registers cannot support negative values, so all values less than 0V will be recorded as 0V.

4.12 Power Ratio Data Representation

The Power Ratio Registers store a power factor value, P_{RATIO}, that is used to determine the final average power delivered to the system (see **Section 4.6 "Power Calculation"**). P_{RATIO} is the result of the multiplication of the V_{SENSE} reading and the V_{SOURCE} reading values shifted to a 16-bit number. It represents the ratio of delivered power with respect to maximum power.

4.13 Limit Registers

These registers are used in concordance with the $\overline{ALERT}$ pin to indicate when high or low limits have been exceeded.

4.13.1 V_{SENSE} LIMITS

The V_{SENSE} Limit Registers store a high and low limit for V_{SENSE}. V_{SENSE} is compared against both limits after each conversion cycle.

The data format for the limit is a raw binary form that is relative to the maximum V_{SENSE} that has been programmed.

If the measured sense voltage meets or exceeds the high limit or drops below the low limit, the $\overline{ALERT}$ pin is asserted (by default, see **Section 4.7 "ALERT Output"**) and the VSENSE_HIGH or VSENSE_LOW status bits are set in the High Limit Status or Low Limit Status registers (see Register 6-16 and Register 6-18).

4.13.2 V_{SOURCE} LIMITS

The V_{SOURCE} Voltage Limit registers store the high and low limits for V_{SOURCE}. V_{SOURCE} is compared against both limits after each conversion cycle.

If V_{SOURCE} meets or exceeds the corresponding high limit or drops below the low limit, the $\overline{ALERT}$ pin is asserted (by default, see **Section 4.7 "ALERT Output"**) and the VSRC_HIGH or VSRC_LOW status bits are set in the High Limit Status or Low Limit Status registers (see Register 6-20 and Register 6-22).

© 2015-2016 Microchip Technology Inc.

5.0 SMBUS COMMUNICATION

5.0.1 SMBus START BIT

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic '1' state to a logic '0' state while the SMBus Clock line is in a logic '1' state.

5.0.2 SMBus ADDRESS AND RD/$\overline{WR}$ BIT

The SMBus Address Byte consists of the 7-bit client address followed by a 1-bit RD/$\overline{WR}$ indicator. If this RD/$\overline{WR}$ bit is a logic '0', the SMBus host is writing data to the client device. If this RD/$\overline{WR}$ bit is a logic '1', the SMBus host is reading data from the client device.

The PAC1710/20 SMBus address is determined by a single resistor connected between ground and the ADDR_SEL pin as shown in Table 5-1.

TABLE 5-1: ADDR_SEL RESISTOR SETTING

RES (5%)	SMBus Address	RES (5%)	SMBus Address
0	1001_100(r/w)	1600	0101_000(r/w)
100	1001_101(r/w)	2000	0101_001(r/w)
180	1001_110(r/w)	2700	0101_010(r/w)
300	1001_111(r/w)	3600	0101_011(r/w)
430	1001_000(r/w)	5600	0101_100(r/w)
560	1001_001(r/w)	9100	0101_101(r/w)
750	1001_010(r/w)	20000	0101_110(r/w)
1270	1001_011(r/w)	Open	0011_000(r/w)

All SMBus Data bytes are sent most significant bit first and composed of 8 bits of information.

5.0.3 SMBus ACK AND NACK BITS

The SMBus client will acknowledge all data bytes that it receives (as well as the client address if it matches and the ARA address if the $\overline{ALERT}$ pin is asserted). This is done by the client device pulling the SMBus Data line low after the eigth bit of each byte that is transmitted.

The host will not acknowledge (NACK) the data received from the client by holding the SMBus data line high after the eigth data bit has been sent.

5.0.4 SMBus STOP BIT

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the PAC1710/20 detects an SMBus Stop bit, and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

5.0.5 SMBus TIMEOUT

The PAC1710/20 includes an SMBus timeout feature. Following a 30 ms period of inactivity on the SMBus, the device will time out and reset the SMBus interface.

The time-out functionality defaults to disabled and can be enabled by writing to the TIMEOUT bit (see Register 6-1).

5.1 SMBus and I^{2}C Compliance

The major differences between SMBus and I^{2}C devices are highlighted below. For more information, refer to the SMBus 2.0 and I^{2}C specifications.

- PAC1710/20 supports I^{2}C fast mode at 400 kHz. This covers the SMBus maximum time of 100 kHz.
- Minimum frequency for SMBus communications is 10 kHz.
- The SMBus client protocol will reset if the clock is held at a logic '0' for longer than 30 ms. This time-out functionality is disabled by default in the PAC1710/20 and can be enabled by writing to the TIMEOUT bit. I^{2}C does not have a timeout.
- The SMBus client protocol will reset if both the clock and data lines are held at a logic '1' for longer than 200 µs (idle condition). This function is disabled by default in the PAC1710/20 and can be enabled by setting the TIMEOUT bit. I^{2}C does not have an idle condition.
- I^{2}C devices do not support the Alert Response Address functionality (which is optional for SMBus).
- I^{2}C devices support Block Read and Block Write differently. I^{2}C protocol allows for unlimited number of bytes to be sent in either direction. The SMBus protocol requires that an additional data byte indicating number of bytes to read/write is transmitted. The PAC1710/20 supports I^{2}C formatting only.

5.2 SMBUS PROTOCOLS

The PAC1710/20 communicates with a host controller through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 1-1. Stretching of the SMCLK signal is supported; however, the PAC1710/20 will not stretch the clock signal.

All of the below protocols use the convention in Table 5-2.

TABLE 5-2: PROTOCOL FORMAT

Data Sent to Device	Data Sent to the Host
# of bits sent	# of bits sent

5.2.1 WRITE BYTE

The Write Byte is used to write one byte of data to the registers, as shown in Table 5-3.

TABLE 5-3: WRITE BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	Register Data	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 → 1

5.2.2 READ BYTE

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 5-4.

TABLE 5-4: READ BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data	NACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	1 → 0	YYYY_YYY	1	0	XXh	1	0 → 1

5.2.3 SEND BYTE

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 5-5.

TABLE 5-5: SEND BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	0 → 1

5.2.4 RECEIVE BYTE

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 5-6.

TABLE 5-6: RECEIVE BYTE PROTOCOL

START	Slave Address	RD	ACK	Register Address	NACK	STOP
1 → 0	YYYY_YYY	1	0	XXh	1	0 → 1

© 2015-2016 Microchip Technology Inc.

5.2.5 ALERT RESPONSE ADDRESS

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert when configured to operate as an interrupt.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of `0001_100xb`. All devices with active interrupts will respond with their client address, as shown in Table 5-7.

TABLE 5-7: ALERT RESPONSE ADDRESS PROTOCOL

START	Alert Response Address	RD	ACK	Device Address	NACK	STOP
1 → 0	0001_100	1	0	YYYY_YYY	1	0 → 1

The PAC1710/20 will respond to the ARA in the following way if the $\overline{\text{ALERT}}$ pin is asserted:

- Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
- Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

5.3 I²C Protocols

The PAC1710/20 supports I²C Block Read and Block Write.

The protocols listed below use the convention in Table 5-1.

5.3.1 BLOCK WRITE

The Block Write is used to write multiple data bytes to a group of contiguous registers, as shown in Table 5-8.

TABLE 5-8: BLOCK WRITE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	Register Data	ACK
1 → 0	YYYY_YYY	0	0	XXh	0	XXh	0
Register Data	**ACK**	**Register Data**	**ACK**	**Register Address**	**Register Data**	**ACK**	**STOP**
XXh	0	XXh	0		XXh	0	0 → 1

5.3.2 BLOCK READ

The Block Read is used to read multiple data bytes from a group of contiguous registers, as shown in Table 5-9.

TABLE 5-9: BLOCK READ PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data
1→ 0	YYYY_YYY	0	0	XXh	0	1 → 0	YYYY_YYY	1	0	XXh
ACK	**Register Data**	**ACK**	**Register Data**	**ACK**	**Register Data**	**ACK**	**...**	**Register Data**	**NACK**	**STOP**
0	XXh	0	XXh	0	XXh	0	...	XXh	1	0 → 1

© 2015-2016 Microchip Technology Inc.

6.0 REGISTERS IN HEXADECIMAL ORDER

The registers shown in Table 6-1 are accessible through the SMBus. In the individual register tables that follow, an entry of '—' indicates that the bit is not used and will always read '0'.

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER

Register Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
00h	Configuration	—	CDEN	MSKAL	C2IDS	C2VDS	TOUT	C1IDS	C1VDS	00h
01h	Conversion Rate	—	—	—	—	—	—	CONV1	CONV0	03h
02h	One-Shot	OS7	OS6	OS5	OS4	OS3	OS2	OS1	OS0	00h
03h	Channel Mask Register	—	—	—	—	C2VS	C2VSR	C1VS	C1VSR	00h
04h	High-Limit Status	CVDN	—	—	—	C2VSH	C2VRH	C1VSH	C1VRH	00h
05h	Low-Limit Status	—	—	—	—	C2VSL	C2VRL	C1VSL	C1VRL	00h
0Ah	V_{SOURCE} Sampling Configuration	C2RS1	C2RS0	C2RA1	C2RA0	C1RS1	C1RS0	C1RA1	C1RA0	88h
0Bh	CH1 V_{SENSE} Sampling Configuration	—	C1SS2	C1SS1	C1SS0	C1SA1	C1SA0	C1SR1	C1SR0	53h
0Ch	CH2 V_{SENSE} Sampling Configuration	—	C2SS2	C2SS1	C2SS0	C2SA1	C2SA0	C2SR1	C2SR0	53h
0Dh	CH1 Sense Voltage High Byte	C1SR11	C1SR10	C1SR9	C1SR8	C1SR7	C1SR6	C1SR5	C1SR4	00h
0Eh	CH1 Sense Voltage Low Byte	C1SR3	C1SR2	C1SR1	C1SR0	—	—	—	—	00h
0Fh	CH2 Sense Voltage High Byte	C2SR11	C2SR10	C2SR9	C2SR8	C2SR7	C2SR6	C2SR5	C2SR4	00h
10h	CH2 Sense Voltage Low Byte	C2SR3	C2SR2	C2SR1	C2SR0	—	—	—	—	00h
11	CH1 V_{SOURCE} Voltage High Byte	C1VR10	C1VR9	C1VR8	C1VR7	C1VR6	C1VR5	C1VR4	C1VR3	00h
12	CH1 V_{SOURCE} Voltage Low Byte	C1VR2	C1VR1	C1VR0	—	—	—	—	—	00h
13h	CH2 V_{SOURCE} Voltage High Byte	C2VR10	C1VR9	C2VR8	C2VR7	C2VR6	C2VR5	C2VR4	C2VR3	00h
14h	CH2 V_{SOURCE} Voltage Low Byte	C2VR2	C2VR1	C2VR0	—	—	—	—	—	00h

© 2015-2016 Microchip Technology Inc.

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
15h	CH1 Power Ratio High Byte	C1P15	C1P14	C1P13	C1P12	C1P11	C1P10	C1P8	C1P7	00h
16h	CH1 Power Ratio Low Byte	C1P7	C1P6	C1P5	C1P4	C1P3	C1P2	C1P1	C1P0	00h
17h	CH2 Power Ratio High Byte	C2P15	C2P14	C2P13	C2P12	C2P11	C2P10	C2P8	C2P7	00h
18h	CH2 Power Ratio Low Byte	C2P7	C2P6	C2P5	C2P4	C2P3	C2P2	C2P1	C2P0	00h
19h	CH1 Sense Voltage High Limit	C1SH7	C1SH6	C1SH5	C1SH4	C1SH3	C1SH2	C1SH1	C1SH0	7Fh
1Ah	CH2 Sense Voltage High Limit	C2SH7	C2SH6	C2SH5	C2SH4	C2SH3	C2SH2	C2SH1	C2SH0	7Fh
1Bh	CH1 Sense Voltage Low Limit	C1SL7	C1SL6	C1SL5	C1SL4	C1SL3	C1SL2	C1SL1	C1SL0	80h
1Ch	CH2 Sense Voltage Low Limit	C2SL7	C2SL6	C2SL5	C2SL4	C2SL3	C2SL2	C2SL1	C2SL0	80h
1Dh	CH1 V_{SOURCE} Voltage High Limit	C1VH7	C1VH6	C1VH5	C1VH4	C1VH3	C1VH2	C1VH1	C1VH0	FFh
1Eh	CH2 V_{SOURCE} Voltage High Limit	C2VH7	C2VH6	C2VH5	C2VH4	C2VH3	C2VH2	C2VH1	C2VH0	FFh
1Fh	CH1 V_{SOURCE}Voltage Low Limit	C1VL7	C1VL6	C1VL5	C1VL4	C1VL3	C1VL2	C1VL1	C1VL0	00h
20h	CH2 V_{SOURCE} Voltage Low Limit	C2VL7	C2VL6	C2VL5	C2VL4	C2VL3	C2VL2	C2VL1	C2VL0	00h
FDh	Product ID	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0	57h/58h
FEh	Manufacturer ID	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	5Dh
FFh	Revision	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	81h

© 2015-2016 Microchip Technology Inc.

6.1 Read Multiple Data Bytes

When any measurement high-byte register is read (V_{SOURCE} or V_{SENSE}), the corresponding low byte is copied into an internal “shadow” register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from the same high byte register again will automatically refresh this stored low byte data.

6.2 Detailed Register Description

REGISTER 6-1: CONFIGURATION REGISTER (ADDRESS 00H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CDEN	MSKAL	C2IDS	C2VDS	TOUT	C1IDS	C1VDS
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **CDEN**: Enables the $\overline{\text{ALERT}}$ pin to be asserted when the conversion cycle is finished.
1 = $\overline{\text{ALERT}}$ pin will be asserted for 5 µs when the conversion cycle is finished.
0 = $\overline{\text{ALERT}}$ pin is not masked. If any of the appropriate status bits are set, the $\overline{\text{ALERT}}$ pin will be asserted.

bit 5 **MSKAL**: Masks the $\overline{\text{ALERT}}$ pin from asserting due to out-of-limit conditions.
1 = $\overline{\text{ALERT}}$ pin is masked. It will not be asserted for any interrupt condition. The Status Registers will be updated normally.
0 = $\overline{\text{ALERT}}$ pin is not masked. It will be asserted for any interrupt condition not masked by Register 6-4. The Status Registers will be updated normally.

bit 4 **C2IDS**: Disables the V_{SENSE} measurement for channel 2 (PAC1720)
1 = The device is not measuring the sense voltage. It will update CH2 Sense Voltage Registers when a One-Shot command is given.
0 = The device is measuring sense voltage for CH2
Unimplemented: Read as ‘0’ (PAC1710)

bit 3 **C2VDS**: Disables the V_{SOURCE} measurement for channel 2 (PAC1720)
1 = The device is not measuring the Source voltage. It will update CH2 Source Voltage Registers when a One-Shot command is given.
0 = The device is measuring Source voltage for CH2
Unimplemented: Read as ‘0’ (PAC1710)

bit 2 **TOUT**: Enables the time-out and idle reset functionality of the communications protocol (see **Section 5.0.5 “SMBus Timeout”**).
1 = Time out enabled
0 = Time out disabled

bit 1 **C1IDS**: Disables the V_{SENSE} measurement for channel 1
1 = The device is not measuring the sense voltage. It will update CH1 Sense Voltage Registers when a One-Shot command is given.
0 = The device is measuring sense voltage for CH1

bit 0 **C1VDS**: Disables the V_{SOURCE} measurement for channel 1
1 = The device is not measuring the Source voltage. It will update CH1 Source Voltage Registers when a One-Shot command is given.
0 = The device is measuring source voltage for CH1

REGISTER 6-2: CONVERSION RATE REGISTER (ADDRESS 01H)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1
—	—	—	—	—	—	CONV<1:0>	
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7-2 **Unimplemented**: Read as '0'

bit 1-0 **CONV<1:0>**: Determines the conversion rate as shown in Table 4-1.
00b = 1 Sample/Second
01b = 2 Samples/Second
01b = 4 Samples/Second
11b = Continuous

REGISTER 6-3: ONE-SHOT REGISTER (ADDRESS 02H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OS<7:0>							
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7-0 **OS<7:0>**: When the device is in the Standby state, writing to the One-Shot Register will initiate a conversion cycle and update all measurements.

REGISTER 6-4: CHANNEL MASK REGISTER (ADDRESS 03H)

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	C2VS	C2VSR	C1VS	C1VSR
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7-4 **Unimplemented**: Read as '0'

bit 3 **C2VS**: Masks the $\overline{\text{ALERT}}$ pin from asserting when the channel 2 V_{SENSE} value meets or exceeds the high limit or drops below the low limit (PAC1720).
1 = The channel 2 V_{SENSE} voltage measurement cannot cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
0 = The channel 2 V_{SENSE} voltage measurement can cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
Unimplemented: Read as '0' (PAC1710)

bit 2 **C2VSR**: Masks the $\overline{\text{ALERT}}$ pin from asserting when the channel 2 V_{SOURCE} value meets or exceeds the high limit or drops below the low limit (PAC1720).
1 = The channel 2 V_{SOURCE} voltage measurement cannot cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
0 = The channel 2 V_{SOURCE} voltage measurement can cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
Unimplemented: Read as '0' (PAC1710)

© 2015-2016 Microchip Technology Inc.

REGISTER 6-4: CHANNEL MASK REGISTER (ADDRESS 03H) (CONTINUED)

bit 1 **C1VS:** Masks the $\overline{\text{ALERT}}$ pin from asserting when the channel 1 V_{SENSE} value meets or exceeds the high limit or drops below the low limit.
1 = The channel 1 V_{SENSE} voltage measurement cannot cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
0 = The channel 1 V_{SENSE} voltage measurement can cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).

bit 0 **C1VSR**: Masks the $\overline{\text{ALERT}}$ pin from asserting when the channel 1 V_{SOURCE} value meets or exceeds the high limit or drops below the low limit.
1 = The channel 1 V_{SOURCE} voltage measurement cannot cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
0 = The channel 1 V_{SOURCE} voltage measurement can cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).

REGISTER 6-5: HIGH-LIMIT STATUS REGISTER (ADDRESS 04H)

RC-0	U-0	U-0	U-0	RC-0	RC-0	RC-0	RC-0
CVDN	—	—	—	C2VSH	C2VRH	C1VSH	C1VRH
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7 **CVDN**: Indicates that the conversion cycle (see **Section 4.2 "Conversion Cycle"**) is complete. This bit is cleared when read.
1 = Conversion complete
0 = Conversion not complete

bit 6-4 **Unimplemented**: Read as '0'

bit 3 **C2VSH**: This bit is set when the channel 2 V_{SENSE} value meets or exceeds its programmed high limit (PAC1720).
1 = The channel 2 V_{SOURCE} voltage measurement caused the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
0 = Normal operation
Unimplemented: Read as '0' (PAC1710)

bit 2 **C2VRH**: This bit is set when the channel 2 V_{SOURCE} value meets or exceeds its programmed high limit (PAC1720).
1 = The channel 2 V_{SOURCE} voltage measurement caused the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
0 = Normal Operation
Unimplemented: Read as '0' (PAC1710)

bit 1 **C1VSH**: This bit is set when the channel 1 V_{SENSE} value meets or exceeds its programmed high limit.
1 = The channel 1 V_{SENSE} voltage measurement caused the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
0 = Normal Operation

bit 0 **C1VRH**: This bit is set when the channel 1 V_{SOURCE} value meets or exceeds its programmed high limit.
1 = The channel 1 V_{SOURCE} voltage measurement caused the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
0 = Normal Operation

REGISTER 6-6: LOW-LIMIT STATUS REGISTER (ADDRESS 05H)

U-0	U-0	U-0	U-0	RC-0	RC-0	RC-0	RC-0
—	—	—	—	C2VSL	C2VRL	C1VSL	C1VRL
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7-4 **Unimplemented**: Read as '0'

bit 3 **C2VSL**: This bit is set when the channel 2 V_{SENSE} falls below its programmed low limit (PAC1720)
1 = The channel 2 V_{SENSE} voltage measurement caused the $\overline{ALERT}$ pin to be asserted (if enabled).
0 = Normal operation
Unimplemented: Read as '0' (PAC1710)

bit 2 **C2VRL**: This bit is set when the channel 2 V_{SOURCE} value falls below its programmed low limit.
1 = The channel 2 V_{SOURCE} voltage measurement caused the $\overline{ALERT}$ pin to be asserted (if enabled).
0 = Normal Operation
Unimplemented: Read as '0' (PAC1710)

bit 1 **C1VSL**: This bit is set when the channel 1 V_{SENSE} value falls below its programmed low limit.
1 = The channel 1 V_{SENSE} voltage measurement caused the $\overline{ALERT}$ pin to be asserted (if enabled).
0 = Normal Operation

bit 0 **C1VRL**: This bit is set when the channel 1 V_{SOURCE} value falls below its programmed low limit.
1 = The channel 1 V_{SOURCE} voltage measurement caused the $\overline{ALERT}$ pin to be asserted (if enabled).
0 = Normal Operation

REGISTER 6-7: V_{SOURCE} SAMPLING CONFIGURATION REGISTER (ADDRESS 0AH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2RS<1:0>		C2RA<1:0>		C1RS<1:0>		C1RA<1:0>	
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7-6 **C2RS<1:0>**: Determines the channel 2 V_{SOURCE} measurement sample time, as shown in Table 4-2 (PAC1720). This will affect the resolution of the data presented in the V_{SOURCE} Voltage Registers.
Unimplemented: Read as '0' (PAC1710)

bit 5-4 **C2RA<1:0>**: Controls the digital averaging that is applied to the channel 2 V_{SOURCE} measurement, as shown in Table 4-3 (PAC1720). This determines the number of consecutive samples that are averaged.
Unimplemented: Read as '0' (PAC1710)

bit 3-2 **C1RS<1:0>**: Determines the channel 1 V_{SOURCE} measurement sample time, as shown in Table 4-2. This will affect the resolution of the data presented in the V_{SOURCE} Voltage Registers.

bit 1-0 **C1RA<1:0>**: Controls the digital averaging that is applied to the channel 1 V_{SOURCE} measurement, as shown in Table 4-3. This determines the number of consecutive samples that are averaged.

© 2015-2016 Microchip Technology Inc.

REGISTER 6-8: CHANNEL 1 V_{SENSE} SAMPLING CONFIGURATION REGISTER (ADDRESS 0BH)

R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1
—	C1CSS<2:0>			C1SA<1:0>		C1SR<1:0>	
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7 **Unimplemented**: Read as '0'

bit 6-4 **C1CSS<2:0>**: Determines the Channel 1 V_{SENSE} voltage measurement sample time, as shown in Table 4-5. This will affect the resolution of the data in the CH1 Sense Voltage Registers.

bit 3-2 **C1SA<1:0>**: Controls the digital averaging that is applied to the channel 1 V_{SENSE} measurement, as shown in Table 4-4. This determines the number of consecutive samples that are averaged.

bit 1-0 **C1SR<1:0>**: Determines the Current Sense full scale range for channel 1 V_{SENSE} measurement as shown in Table 4-6.

REGISTER 6-9: CHANNEL 2 V_{SENSE} SAMPLING CONFIGURATION REGISTER (ADDRESS 0CH)

R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1
—	C2CSS<2:0>			C2SA<1:0>		C2SR<1:0>	
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7 **Unimplemented**: Read as '0'

bit 6-4 **C2CSS<2:0>**: Determines the Channel 2 V_{SENSE} voltage measurement sample time, as shown in Table 4-5 (PAC1720). This will affect the resolution of the data in the CH2 Sense Voltage Registers.
Unimplemented: Read as '0'(PAC1710).

bit 3-2 **C2SA<1:0>**: Controls the digital averaging that is applied to the Channel 2 V_{SENSE} measurement, as shown in Table 4-4 (PAC1720). This determines the number of consecutive samples that are averaged.
Unimplemented: Read as '0' (PAC1710)

bit 1-0 **C2SR<1:0>**: Determines the Channel 2 Current Sense full scale range channel 2 V_{SENSE} measurement as shown in Table 4-6 (PAC1720).
Unimplemented: Read as '0' (PAC1710)

REGISTER 6-10: CHANNEL 1 V_{SENSE} RESULT REGISTER (ADDRESSES 0DH AND 0EH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
C1SR<15:8>							
bit 15							bit 8

R-0	R-0	R-0	R-0	U-0	U-0	U-0	U-0
C1SR<7:4>				—	—	—	—
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

bit 15-4 **C1SR<15:4>**: These registers contain the most recent digitized value Channel 1 V_{SENSE} samples.
bit 3-0 **Unimplemented**: Read as ‘0’

REGISTER 6-11: CHANNEL 2 V_{SENSE} RESULT REGISTER (ADDRESSES 0FH AND 10H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
C2SR<15:8>							
bit 15							bit 8

R-0	R-0	R-0	R-0	U-0	U-0	U-0	U-0
C2SR<7:4>				—	—	—	—
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

bit 15-4 **C2SR<15:4>**: These registers contain the most recent digitized value channel 2 V_{SENSE} samples (PAC1720).
Unimplemented: Read as ‘0’ (PAC1710)
bit 3-0 **Unimplemented**: Read as ‘0’

© 2015-2016 Microchip Technology Inc.

REGISTER 6-12: CHANNEL 1 VSOURCE RESULT REGISTER (ADDRESSES 11H AND 12H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
C1VR<15:8>							
bit 15							bit 8

R-0	R-0	R-0	U	U-0	U-0	U-0	U-0
C1VR<7:5>			—	—	—	—	—
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 15-5 **C1VR<15:5>**: These registers contain the most recent digitized value Channel 1 V_{SOURCE} samples.
400h = 20V
200h = 10V
100h = 5V
080h = 2.5V
040h = 1.25V
020h = 625 mV
010h = 312.5 mV
008h = 156.25 mV
004h = 78.125 mV
002h = 39.063 mV
001h = 19.531 mV

bit 4-0 **Unimplemented**: Read as '0'

REGISTER 6-13: CHANNEL 2 VSOURCE RESULT REGISTER (ADDRESSES 13H AND 14H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
C2VR<15:8>							
bit 15							bit 8

R-0	R-0	R-0	U-0	U-0	U-0	U-0	U-0
C2VR<7:5>			—	—	—	—	—
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

bit 15-5 **C2VR<10:0>**: These registers contain the most recent digitized value Channel 2 V_{SOURCE} samples (PAC1720).
400h = 20V
200h = 10V
100h = 5V
080h = 2.5V
040h = 1.25V
020h = 625 mV
010h = 312.5 mV
008h = 156.25 mV
004h = 78.125 mV
002h = 39.063 mV
001h = 19.531 mV
Unimplemented: Read as ‘0’ (PAC1710)

bit 4-0 **Unimplemented**: Read as ‘0’

REGISTER 6-14: CHANNEL 1 POWER RATIO REGISTER (ADDRESSES 15H AND 16H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
C1P<15:8>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
C1P<7:0>							
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

bit 15-0 **C1P<15:0>**: These registers contain the most recent channel 1 Power ratio calculations. This is a 16-bit binary number representing a ratio based on Power FSR.

© 2015-2016 Microchip Technology Inc.

REGISTER 6-15: CHANNEL 2 POWER RATIO REGISTER (ADDRESS 17H AND 18H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
C2P<15:8>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
C2P<7:0>							
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 15-0 **C2P<15:0>**: These registers contain the most recent channel 2 power ratio calculations (PAC1720). This is a 16-bit binary number representing a ratio based on Power FSR
Unimplemented: Read as '0' (PAC1710)

REGISTER 6-16: CHANNEL 1 V_{SENSE} HIGH LIMIT REGISTER (ADDRESS 19H)

R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
C1SH<7:0>							
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7-0 **C1SH<7:0>**: Two's complement high-limit channel 1 V_{SENSE}
0100_000 = 1024
0010_0000 = 512
0001_0000 = 256
0000_1000 = 128
0000_0100 = 64
0000_0010 = 32
0000_0001 = 16
1111_1111 = -1
1000_000 = -1024

REGISTER 6-17: CHANNEL 2 V_{SENSE} HIGH-LIMIT REGISTER (ADDRESS 1AH)

R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
C2SH<7:0>							
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7-0 **C2SH<7:0>**: Two's complement high-limit channel 2 V_{SENSE} (PAC1720)
0100_000 = 1024
0010_0000 = 512
0001_0000 = 256
0000_1000 = 128
0000_0100 = 64
0000_0010 = 32
0000_0001 = 16
1111_1111 = -1
1000_000 = -1024
Unimplemented: Read as '0' (PAC1710)

REGISTER 6-18: CHANNEL 1 V_{SENSE} LOW-LIMIT REGISTER (ADDRESS 1BH)

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C1SL<7:0>							
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7-0 **C1SL<7:0>**: Two's complement low-limit channel 1 V_{SENSE}
0100_000 = 1024
0010_0000 = 512
0001_0000 = 256
0000_1000 = 128
0000_0100 = 64
0000_0010 = 32
0000_0001 = 16
1111_1111 = -1
1000_000 = -1024

© 2015-2016 Microchip Technology Inc.

REGISTER 6-19: CHANNEL 2 V_{SENSE} LOW-LIMIT REGISTER (ADDRESS 1CH)

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2SL<7:0>							
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7-0 **C2SL<7:0>**: Two's complement low-limit channel 2 V_{SENSE} (PAC1720)
0100_000 = 1024
0010_0000 = 512
0001_0000 = 256
0000_1000 = 128
0000_0100 = 64
0000_0010 = 32
0000_0001 = 16
1111_1111 = -1
1000_000 = -1024
Unimplemented: Read as '0' (PAC1710)

REGISTER 6-20: CHANNEL 1 V_{SOURCE} HIGH-LIMIT REGISTER (ADDRESS 1DH)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
C1VH<7:0>							
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7-0 **C1VH<7:0>**: Two's complement high-limit channel 1 V_{SOURCE}
80h = 20V
40h = 10V
20h = 5V
10h = 2.5V
08h = 1.25V
04h = 625 mV
02h = 312.5 mV
01h = 156.25 mV

© 2015-2016 Microchip Technology Inc.

REGISTER 6-21: CHANNEL 2 V_{SOURCE} HIGH-LIMIT REGISTER (ADDRESS 1EH)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
C2VH<7:0>							
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7-0 **C2VH**: Two's complement high-limit channel 2 V_{SOURCE} (PAC1720)
0h = 20V
40h = 10V
20h = 5V
10h = 2.5V
08h = 1.25V
04h = 625 mV
02h = 312.5 mV
01h = 156.25 mV
Unimplemented: Read as '0' (PAC1710)

REGISTER 6-22: CHANNEL 1 V_{SOURCE} LOW-LIMIT REGISTER (ADDRESS 1FH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C1VL<7:0>							
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7-0 **C1VL<7:0>**: Two's complement low-limit channel 1 V_{SOURCE}
0h = 20V
40h = 10V
20h = 5V
10h = 2.5V
08h = 1.25V
04h = 625 mV
02h = 312.5 mV
01h = 156.25 mV

© 2015-2016 Microchip Technology Inc.

REGISTER 6-23: CHANNEL 2 V_{SOURCE} LOW-LIMIT REGISTER (ADDRESS 20H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2VL<7:0>							
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7-0 **C2VL<7:0>**: Two's complement low-limit channel 2 V_{SOURCE}
0h = 20V
40h = 10V
20h = 5V
10h = 2.5V
08h = 1.25V
04h = 625 mV
02h = 312.5 mV
01h = 156.25 mV

REGISTER 6-24: PRODUCT REGISTER (ADDRESS FDH)

R-0	R-1	R-0	R-1	R-0	R-1	R-1	R-1
PID<7:0>							
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7-0 **PID<7:0>**: Product ID for PAC1710/20
57h = PAC1720
58H = PAC1710

REGISTER 6-25: MCHP ID REGISTER (ADDRESS FEH)

R-0	R-1	R-0	R-1	R-1	R1	R-0	R-1
MID<7:0>							
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

bit 7-0 **MID<7:0>**: Manufacturer ID

REGISTER 6-26: REVISION REGISTER (ADDRESS FFH)

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
REV<7:0>							
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

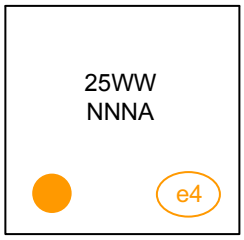
bit 7-0 **REV<7:0>**: Silicon Revision

© 2015-2016 Microchip Technology Inc.

7.0 PACKAGE DESCRIPTION

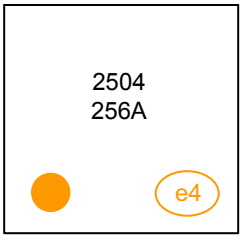
7.1 Package Marking Information

10-Lead VDFN (3x3x0.9 mm)



Part Number	Code
PAC1710-1-AIA-TR	25WW
PAC1720-1-AIA-TR	26WW

Example

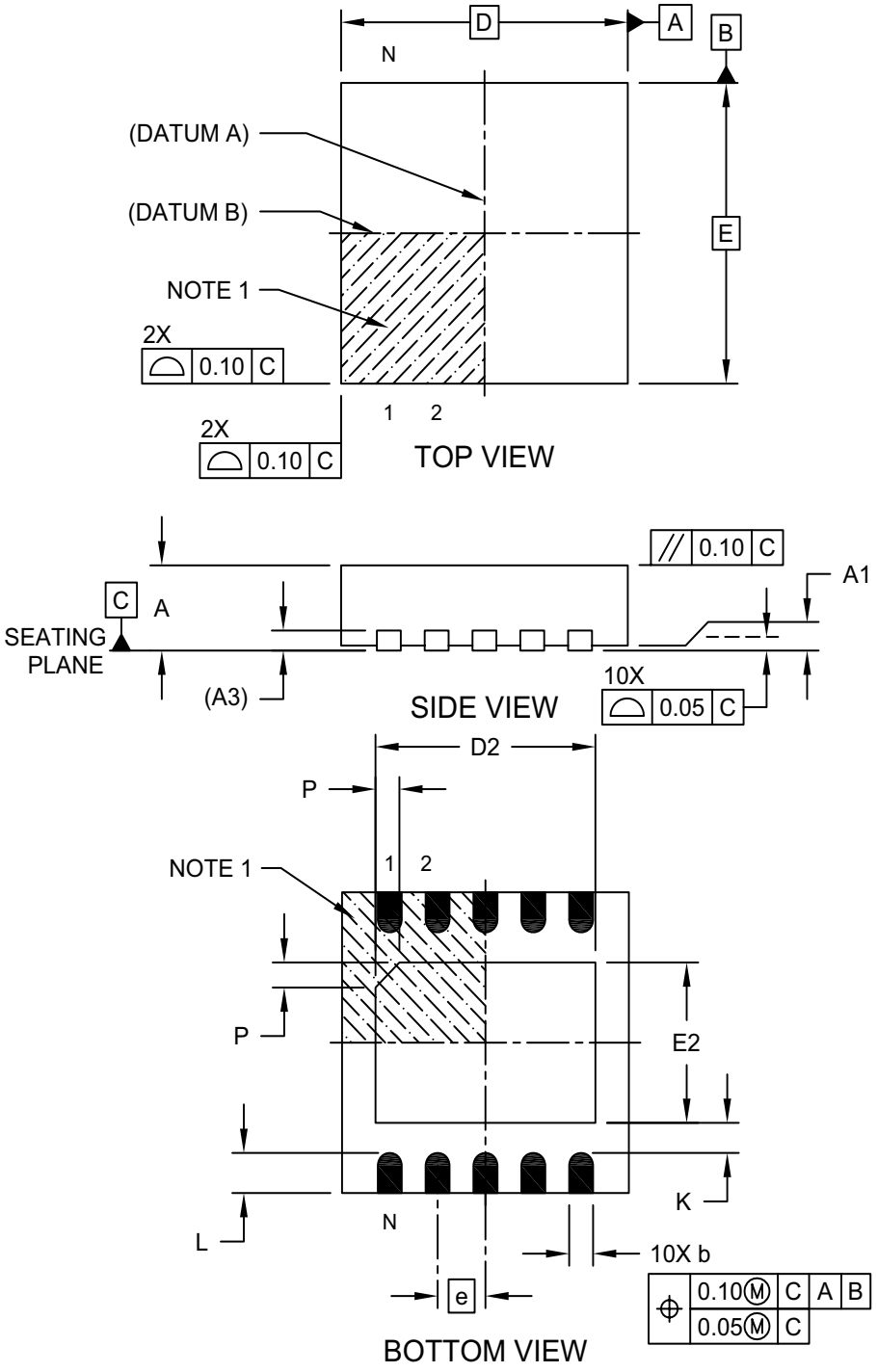


Legend:	Y	Year code (last digit of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	<R>	Package
	<COO>	Country of origin

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

10-Lead Very Thin Plastic Dual Flat, No Lead Package (9Q) - 3x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

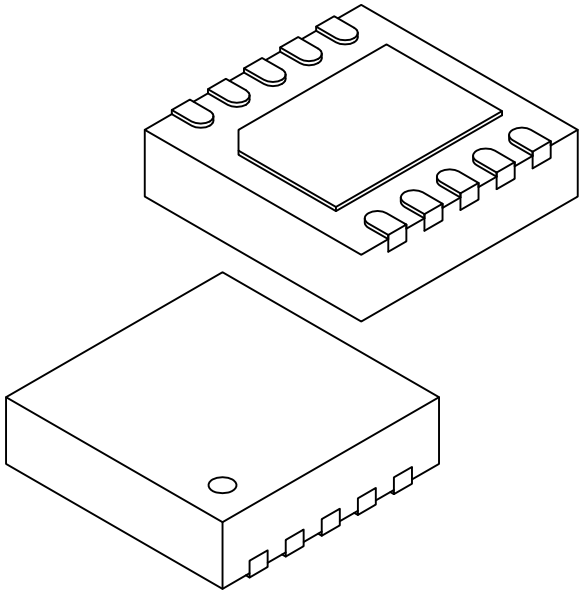


Microchip Technology Drawing C04-206B Sheet 1 of 2

© 2015-2016 Microchip Technology Inc.

10-Lead Very Thin Plastic Dual Flat, No Lead Package (9Q) - 3x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	(A3)		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.20	2.30	2.40
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.60	1.70
Exposed Pad Chamfer	P	-	0.25	-
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.25	0.30	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

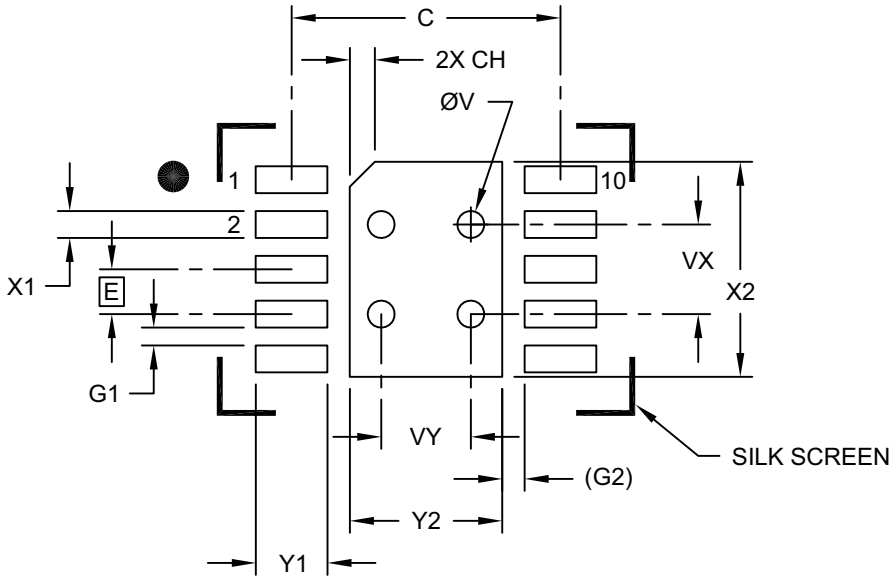
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-206B Sheet 2 of 2

10-Lead Very Thin Plastic Dual Flat, No Lead Package (9Q) - 3x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	Y2			1.70
Optional Center Pad Length	X2			2.40
Contact Pad Spacing	C		3.00	
Center Pad Chamfer	CH		0.28	
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			0.80
Contact Pad to Contact Pad (X8)	G1	0.20		
Contact Pad to Center Pad (X10)	G2	0.25 REF		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	VX		1.00	
Thermal Via Pitch	VY		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerances, for reference only.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2206B

© 2015-2016 Microchip Technology Inc.

APPENDIX A: REVISION HISTORY

Revision B (February 2016)

The following was modified:

1. Updated the package drawings in **Section 7.0, Package Description**

Revision A (May 2015)

- Replaces previous SMSC version 1.1 (12-08-11)
- Updated the Absolute Maximum Ratings in **Section 1.1, Electrical Specifications**
- Added information for the dual high-side current sensor (PAC1720)

Revision 1.1 (December 2011)

- Initial release

NOTES:

© 2015-2016 Microchip Technology Inc.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	-XXX	-XX
Device	SMBus Address	Package	Tape and Reel

Device:	PAC1710/20: High-side power/current monitor with analog output	
SMBus Address:	-1	= selectable address
Package:	AIA	= 10-lead 3 mm x 3 mm VDFN
Shipping Pack:	TR	=4,000 piece Tape and Reel

Examples:

a) PAC1710-1-AIA-TR: Single-channel high-side current monitor 3x3 VDFN 8-lead package, shipped in a 4,000 piece Tape and Reel

NOTES:

© 2015-2016 Microchip Technology Inc.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE**.** Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949 ==

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KeeLoq, KeeLoq logo, Kleer, LANCheck, LINK MD, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC32 logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, ETHERSYNCH, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and QUIET-WIRE are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KleerNet, KleerNet logo, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PureSilicon, RightTouch logo, REAL ICE, Ripple Blocker, Serial Quad I/O, SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2015-2016, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-5224-0276-3

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110

Canada - Toronto
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Dusseldorf
Tel: 49-2129-3766400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Venice
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Poland - Warsaw
Tel: 48-22-3325737

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

07/14/15

© 2015-2016 Microchip Technology Inc.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Microchip:

PAC1710-1-AIA-TR