AN2448
Application note

EVALTSM1052: Ultra small battery charger using TSM1052

Introduction

This document describes a low power adapter that can be used in travel battery charger applications. It uses the new Constant Voltage Constant Current (CVCC) controller TSM1052, which is housed in one of the smallest packages available (SOT23-6L). Thanks to its low consumption and low operating voltage, good electrical performance is achieved. Another important feature of this SMPS is the absence of the Y1 safety capacitor between primary and secondary grounds.

Figure 1. EVALTSM1052 demo board

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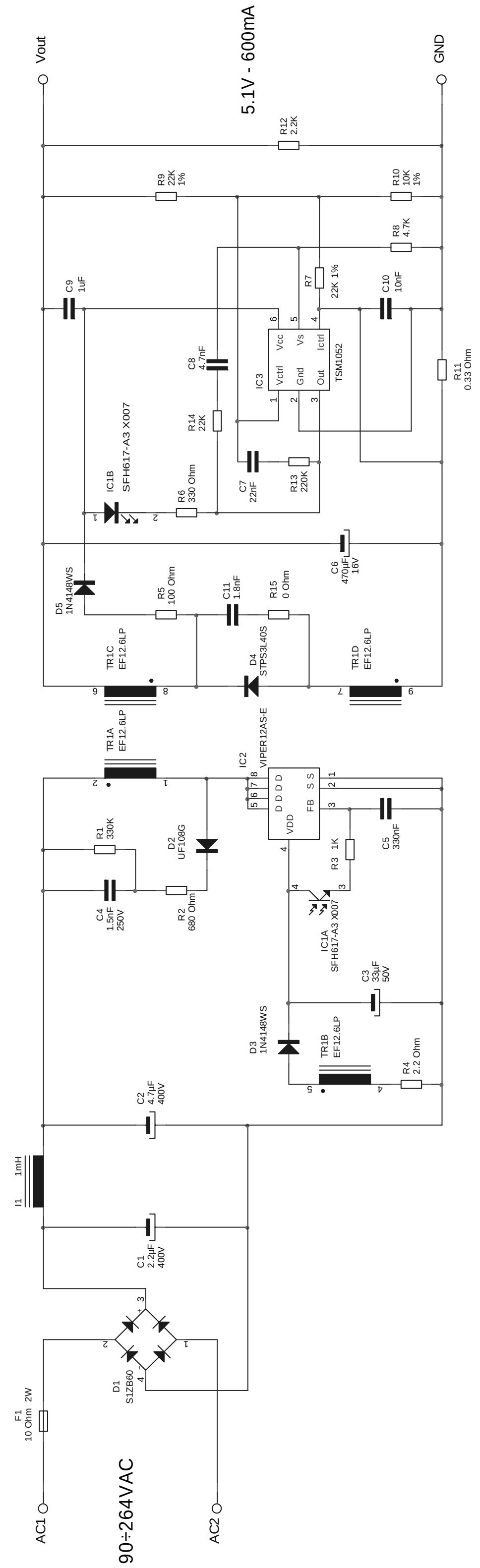
1 Adapter features

1.1 Main characteristics

- Input:
  - V_{in}: 90 ~ 264 Vrms
  - f: 45 ~ 66 Hz
- Output:
  - 5.1Vdc ± 2%
  - 600 mA
  - Cable drop compensation (0.33 mV/mA)
- No-load:
  - Pin below 0.3 W
- Short circuit: protected with nominal current regulation
- PCB type & size:
  - CEM-1
  - Single side 35 µm
  - 48 x 18 mm
- Safety: according to EN60065
- EMI: according to EN55022 - class B

Figure 2. Electrical diagram



1.2 Circuit description

The circuit used implements a flyback topology, which is ideal for a low power, low cost isolated converter.

At primary side a VIPer12A-E has been used. This IC includes a current mode PWM controller and a Power MOSFET in a small SO-8 package. The converter works in both continuous and discontinuous conduction mode depending on the input voltage (the circuit has a wide range input) and the output load. The switching frequency is internally fixed at 60 KHz. The design has been developed to reduce overall component count and adapter cost.

The input section includes a resistor for inrush current limiting, a diode bridge, two electrolytic bulk capacitors and an inductor as front-end ac-dc converter and EMC filter. The transformer is a layer type, uses a standard EF12.6 ferrite core and is designed to have a reflected voltage of about 90 V. The peculiarity of this transformer is the winding technique which allows the elimination of the usual Y1 safety capacitor between the primary and the secondary. A RCD clamp network is used for leakage inductance demagnetization. The power supply for the VIPer12A-E is obtained with a self supply winding from the transformer connected in forward configuration. This circuit provides a voltage that is directly proportional to the input rectified voltage and independent from the load voltage. In this way even in short circuit condition ($V_{OUT} = 0$), the IC is correctly supplied. The wide V_{DD} operating range (9 V to 38 V) of the VIPer12A-E allows a wide range mains input voltage.

At secondary side, the TSM1052 constant voltage constant current (CVCC) controller is used. Like the VIPer12A-E, the TSM1052 is also supplied with a forward configuration, in order to obtain the same benefit. The voltage is taken on one half of the secondary winding (between pins 8 and 6), rectified with diode D5 and added to the output voltage. Under all working conditions, the voltage supply for the TSM1052 and the photodiode IC1B is equal to the output voltage plus forward rectified voltage on half secondary. With this configuration a correct supply is provided over the whole input range, even with the output short circuited.

With this configuration a small ripple at twice line frequency is present at the output. This is due to the supply of the photodiode IC1B, which is a replica of the voltage on C2. Usually this is not a problem in battery chargers. There are two ways to eliminate this phenomenon if necessary:

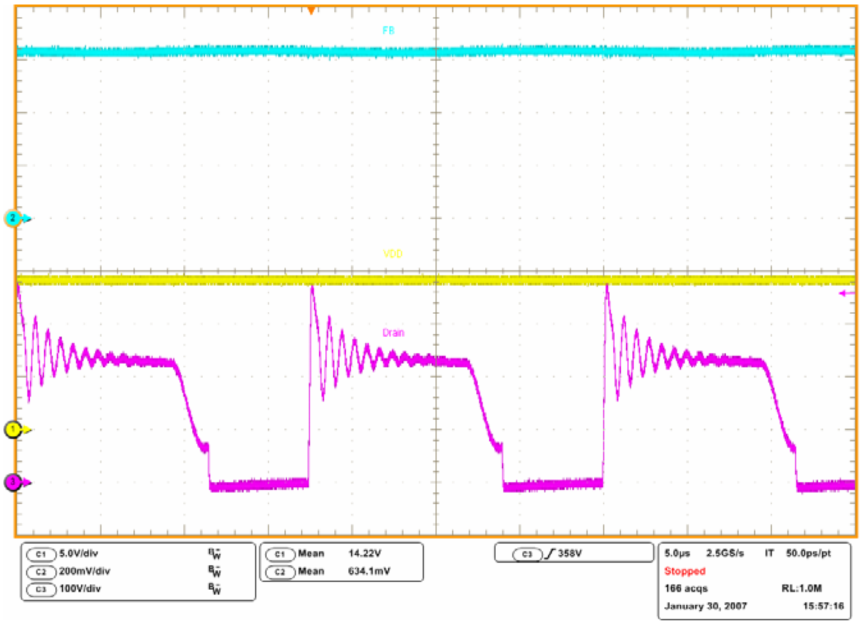
- C9 can be substituted by an electrolytic capacitor (at least 47 µF)
- The TSM1052 and IC1B can be attached directly to the output voltage. In this case the current regulation is guaranteed only for output voltages down to 1.7 V

Resistor R7 has been added for cable drop compensation (the higher the output current the higher the output voltage). R7 has been chosen according to the cable characteristics (it has about 0.3 Ω of resistance).

2 Electrical behavior

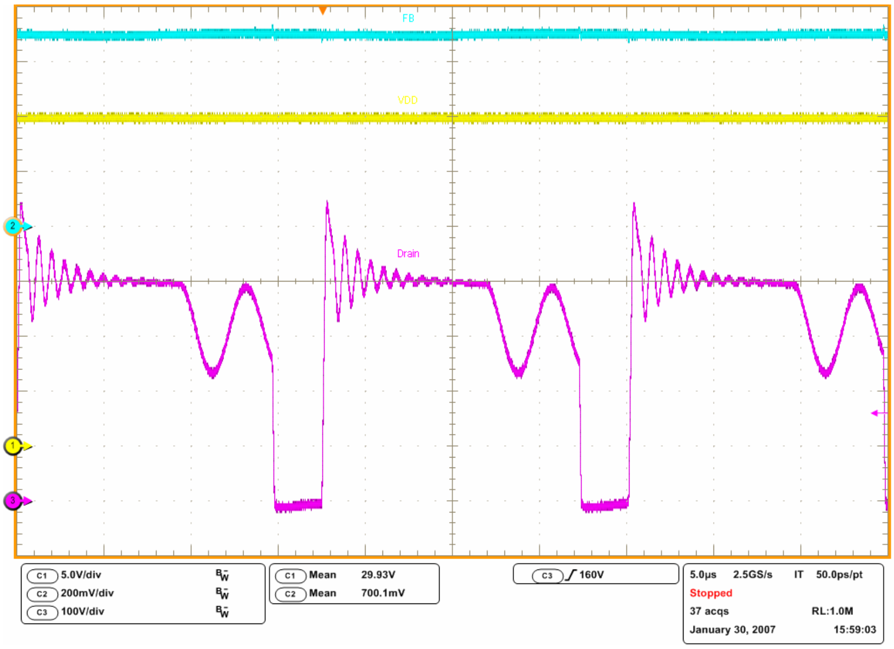
Figure 3 and *Figure 4* show all the VIPer12A-E waveforms during normal operation at full load. The converter operates in DCM at both 115 Vrms and 230 Vrms:

Figure 3. **V_{in} = 115 Vrms - 60 Hz**



CH1: VIPer12A-E supply voltage (yellow)
CH2: VIPer12A-E feedback pin (red)
CH3: VIPer12A-E drain voltage (green)

Figure 4. V_{in} = 230 Vrms - 50 Hz



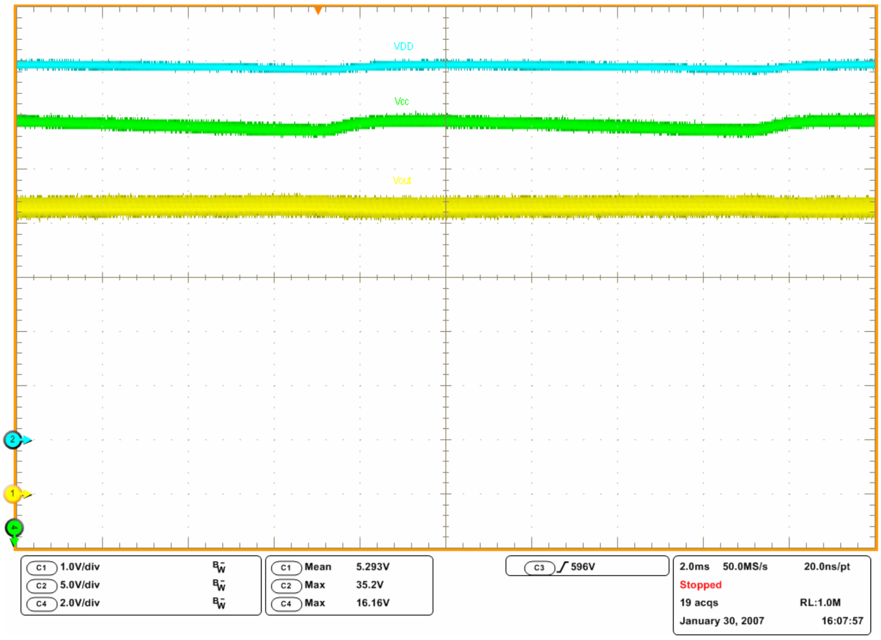
CH1: VIPer12A-E supply voltage (yellow)
CH2: VIPer12A-E feedback pin (light blue)
CH3: VIPer12A-E drain voltage (purple)

Due to the forward supply, the V_{DD} voltage is directly proportional to the input voltage, so it is nearly double at 230 V_{ac} with respect to 115 V_{ac}.

The worst case (maximum / minimum) supply voltages for both primary and secondary sides are shown in *Figure 5* and *Figure 6*.

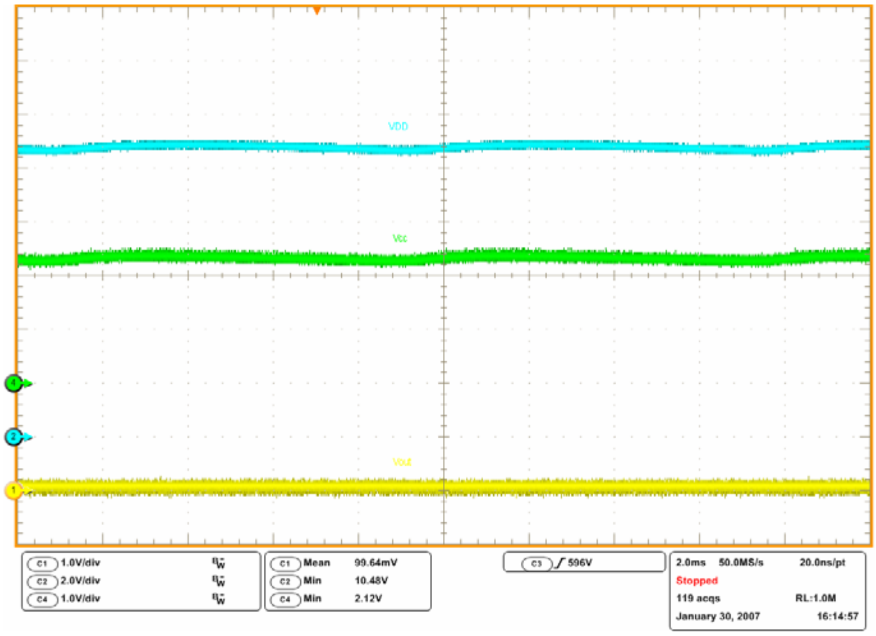
For the maximum voltages, the converter operates with the maximum load in CV mode (that is, the maximum output voltage is present, thanks to the cable drop compensation) and with the maximum input voltage (264 V_{ac}). In this condition the VIPer12A-E has a maximum supply voltage of 35.2 V and the TSM1052 16.16 V. Minimum voltages are taken with short circuit on the output (CC regulation) and minimum input voltage (90 V_{ac}). Given this condition the VIPer12A-E has a minimum supply voltage of 10.48 V and the TSM1052 2.12 V.

Figure 5. Maximum supply voltages



CH1: output voltage (yellow)
CH2: VIPer12A-E supply voltage (light blue)
CH3: TSM1052 supply voltage (green)

Figure 6. Minimum supply voltages

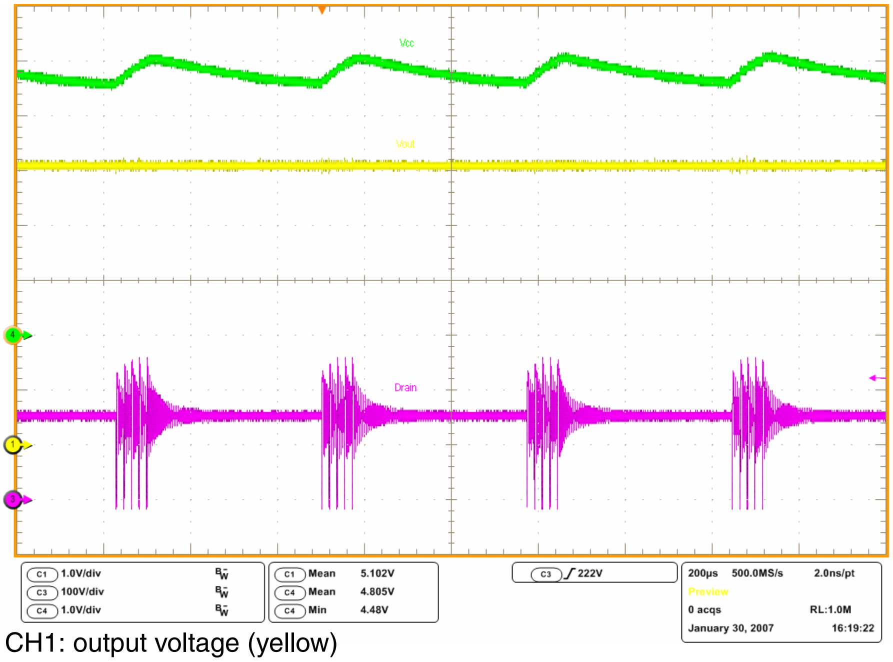


CH1: output voltage (yellow)
CH2: VIPer12A-E supply voltage (light blue)
CH3: TSM1052 supply voltage (green)

Let's see what happens at the extreme conditions: no load and short circuit.

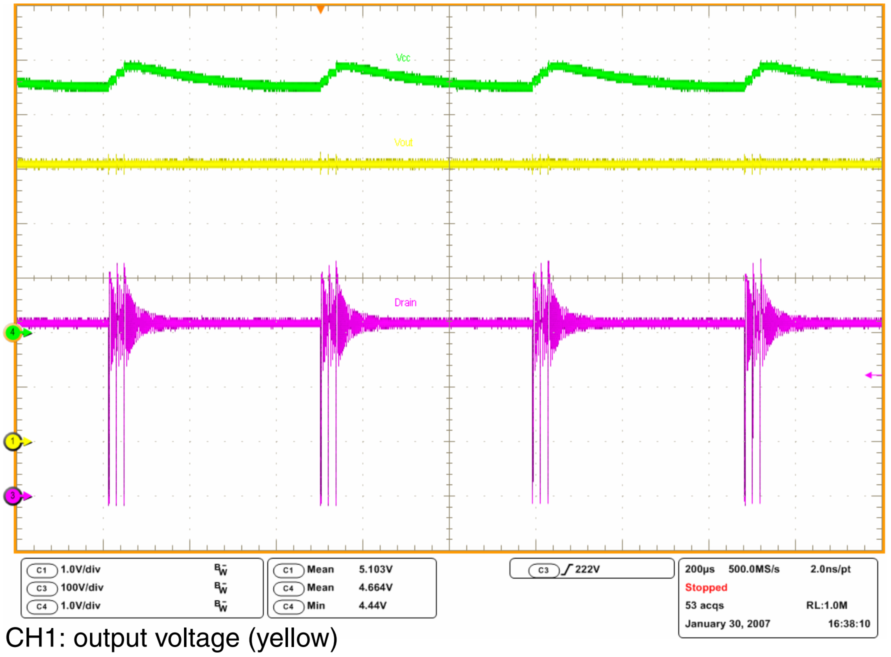
During no load conditions, the circuit operates in burst mode allowing an input power of less than 300 mW over the whole input voltage range.

Figure 7. V_{in} = 115 V_{ac} - no-load



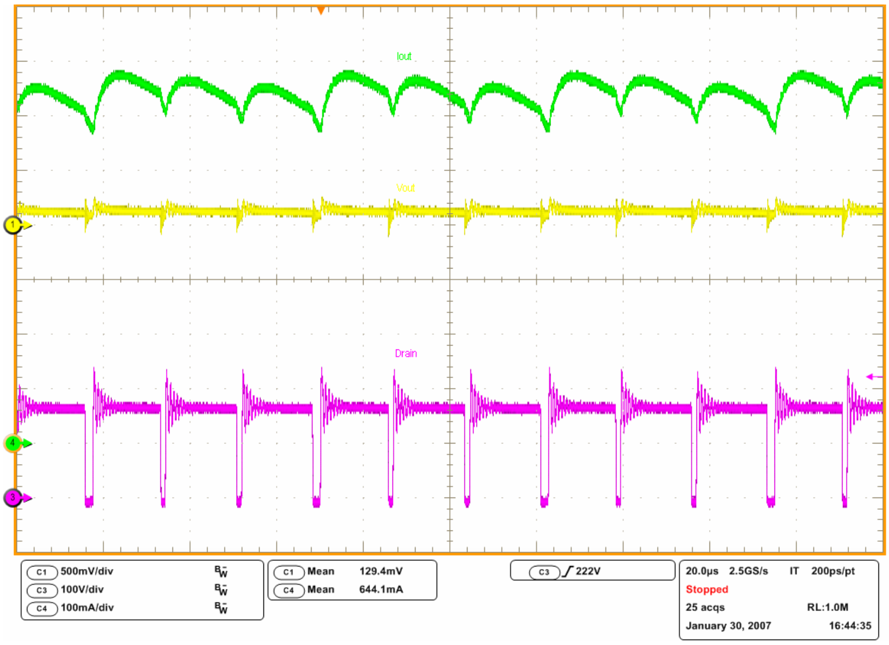
CH1: output voltage (yellow)
CH2: VIPer12A-E drain pin (purple)
CH3: TSM1052 supply voltage (green)

Figure 8. V_{in} = 230 V_{ac} - no-load



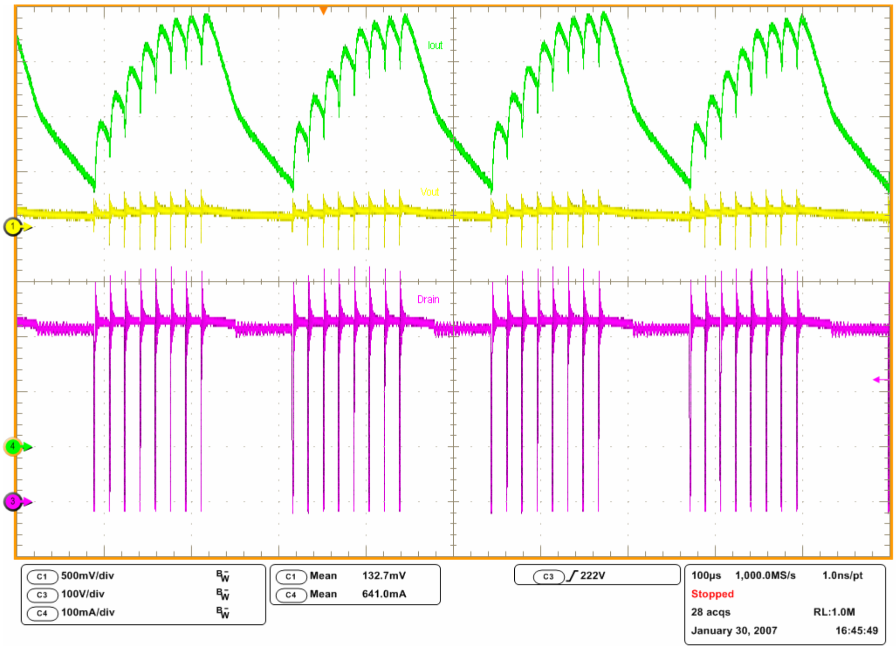
CH1: output voltage (yellow)
CH2: VIPer12A-E drain pin (purple)
CH3: TSM1052 supply voltage (green)

Figure 9. V_{in} = 115 V_{ac} - short circuit



CH1: output voltage (yellow)
CH2: VIPer12A-E drain pin (purple)
CH3: TSM1052 supply voltage (green)

Figure 10. V_{in} = 230 V_{ac} - short circuit



CH1: output voltage (yellow)
CH2: VIPer12A-E drain pin (purple)
CH3: output current (green)

With the circuit used in this evaluation board, when the output current has rapid variation from maximum to zero and the input voltage is low (< 105 V_{ac}), the VIPer12A-E loses the supply for about 400-500 ms. The output voltage thereby decreases. After that time the IC turns on again and the output returns to the nominal value. This behavior is not problematic in this kind of application and has not been modified, in order to have a smaller and cheaper solution. If this phenomenon must be avoided, however, it is enough to increase C3 to 100 µF.

3 Electrical performance

3.1 Efficiency

Table 1 and *Table 2* show the board efficiency at the two nominal voltages.

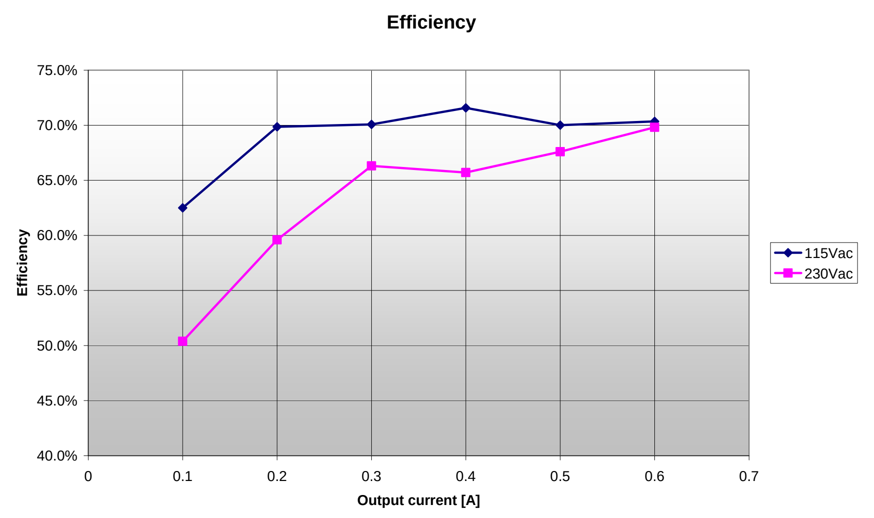
Table 1. Efficiency at 115 Vrms

Io [A]	Vo [V]	Po [W]	Iin [mA]	Pin [W]	Efficiency
0.1	5.153	0.520	16.9	0.832	62.5%
0.2	5.185	1.036	27.4	1.483	69.9%
0.3	5.217	1.566	38.2	2.235	70.1%
0.4	5.248	2.096	47.6	2.928	71.6%
0.5	5.280	2.638	58.7	3.769	70.0%
0.6	5.310	3.187	68.5	4.530	70.3%

Table 2. Efficiency at 230 Vrms

Io [A]	Vo [V]	Po [W]	Iin [mA]	Pin [W]	Efficiency
0.1	5.158	0.520	12.8	1.033	50.4%
0.2	5.190	1.037	20.1	1.740	59.6%
0.3	5.222	1.568	25.5	2.364	66.3%
0.4	5.254	2.098	32.6	3.193	65.7%
0.5	5.286	2.641	38.4	3.908	67.6%
0.6	5.319	3.192	43.6	4.572	69.8%

Figure 11. Efficiency vs. output current



As indicated in *Table 3*, the no-load consumption is always below 300 mW, and therefore complies with the more restrictive standards (European Code Of Conduct).

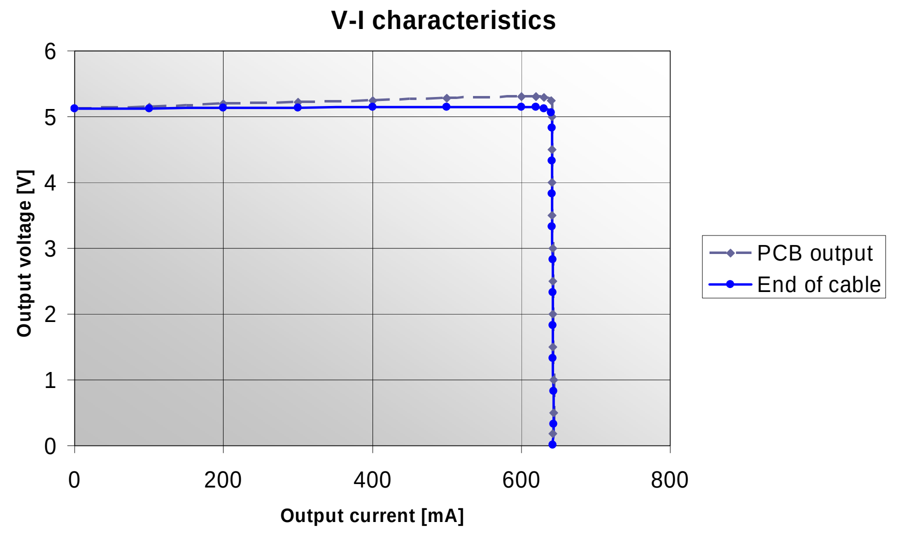
Table 3. No-load consumption

Value	$90V_{ac}$	$115V_{ac}$	$230V_{ac}$	$264V_{ac}$
Pin [W]	0.106	0.131	0.239	0.273
V_{OUT} [V]	5.12	5.12	5.12	5.12

3.2 Output characteristics

Figure 12 shows the output characteristics (taken with 115 V_{ac} mains input) on PCB pads and at the end of the output cable. Values are very close also at 230 V_{ac}. It is interesting to note that, while in the constant current region, the output voltage can reach zero.

Figure 12. Output characteristics at 115 V_{ac} with CDC (cable drop compensation)



The effect of the cable drop compensation is also worthy of note. *Table 4* shows the output voltage at various load amounts measured at the output connector, after the output cable. 115 V_{ac} and 230 V_{ac} mains input give very similar results. With the cable drop compensation the output voltage is nearly constant while, without this feature, at maximum load the output voltage goes down to 4.96 V (about -3.1%). The effect of this feature is also clearly visible in the output characteristic (*Figure 12*), with a flat line while in the constant voltage regulation region.

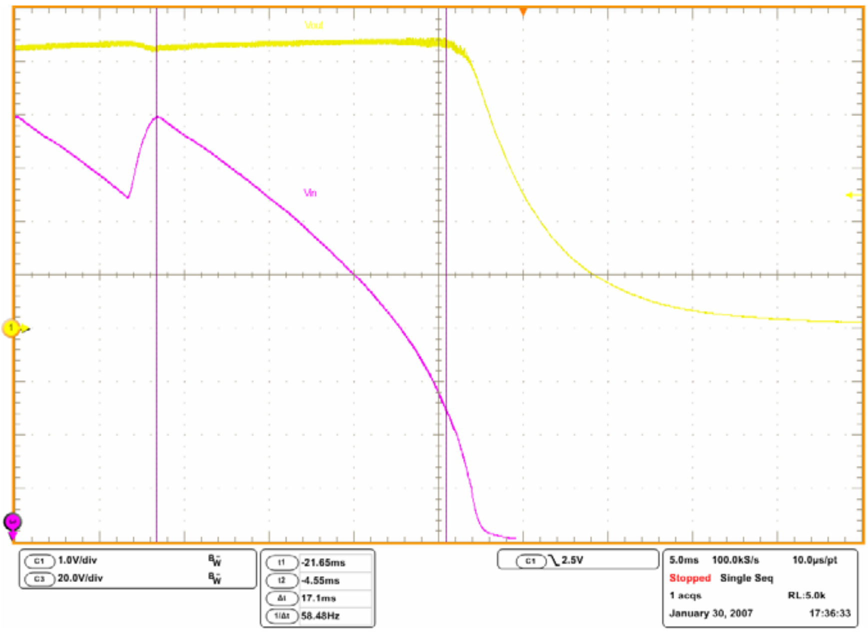
Table 4. Output voltage at output connector

Iout [A]	0	0.1	0.2	0.3	0.4	0.5	0.6
Vout [V] with CDC	5.12	5.13	5.13	5.14	5.14	5.15	5.15
Vout [V] without CDC	5.12	5.09	5.07	5.04	5.01	4.98	4.96

3.3 Hold-up time

During power down phase the output voltage undergoes a clean transition without restart trials or glitches. By observing the waveforms it is possible to measure the hold-up time. In *Figure 13* and *Figure 14* this condition is shown for the two nominal voltages of 115 V_{ac} and 230 V_{ac}. In the worst case, 115 V_{ac}, a hold-up time of about 17.1 ms is measured.

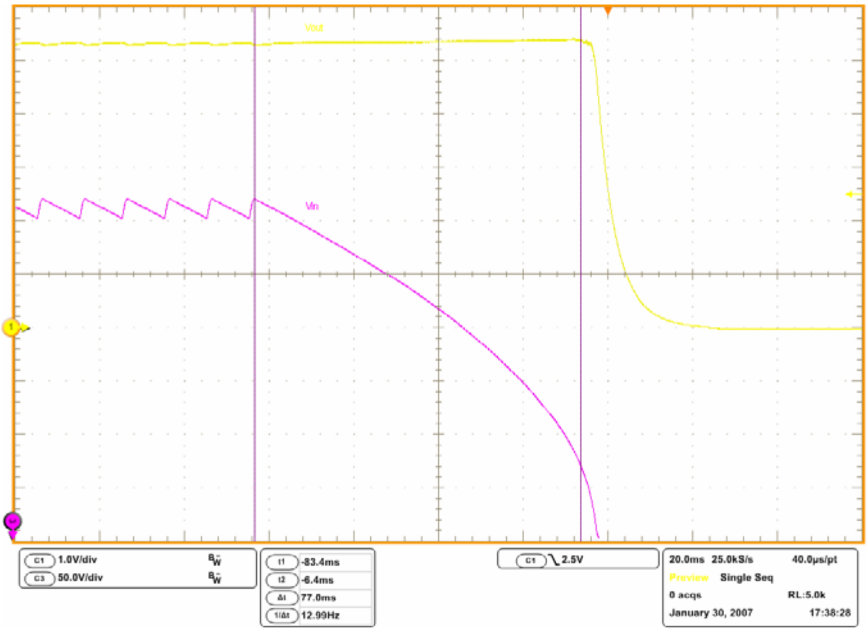
Figure 13. Power down at 115 V_{ac} - 60 Hz



CH1: output voltage (yellow)

CH3: rectified input voltage (purple)

Figure 14. Power down at 230 V_{ac} - 50 Hz



CH1: output voltage (yellow)

CH3: rectified input voltage (purple)

4 Conducted noise measurements (pre-compliance test)

Figure 15 and *Figure 16* show the conducted noise measurements performed at the two nominal voltages with peak detection and considering only the worst phase. The measurements have a good margin with respect to the limits (stated in EN55022 CLASS B specifications).

Figure 15. CE peak measure at 115 V_{ac} and full load

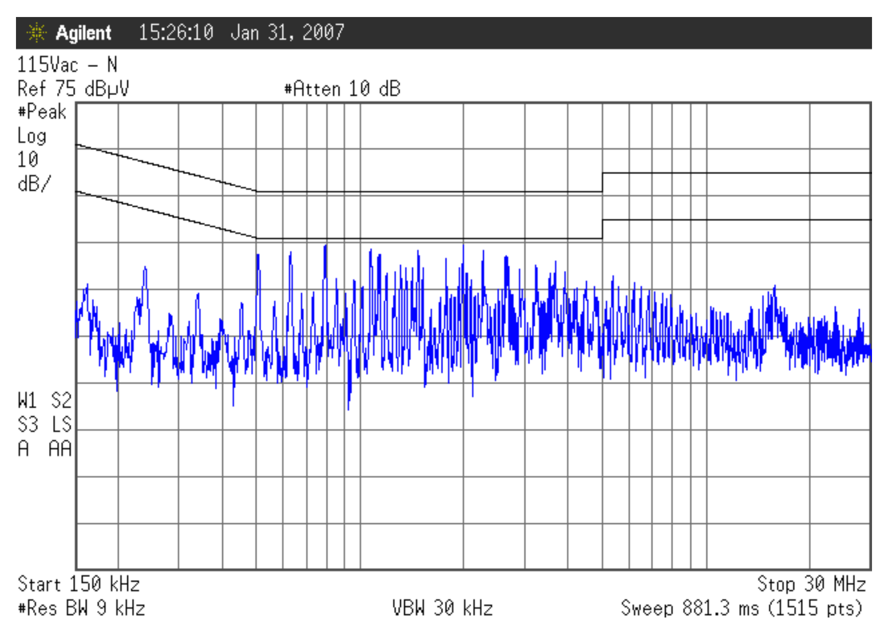
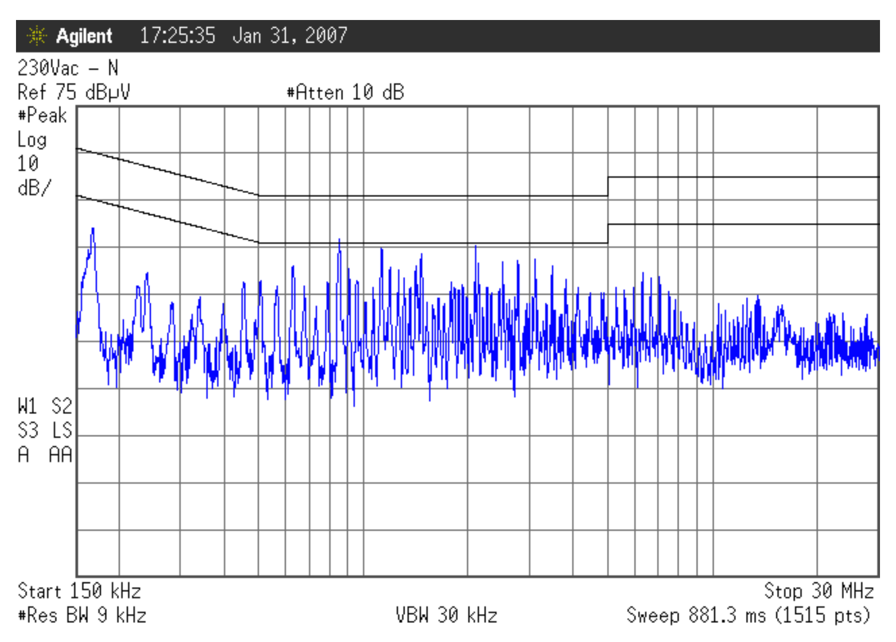


Figure 16. CE peak measure at 230 V_{ac} and full load



5 Thermal measurements

A thermal analysis of the board was performed using an IR camera. The results are shown in *Figure 17* and *Figure 18* for 115 V_{ac} and 230 V_{ac} mains input. Both images refer to full load condition (Iout = 600 mA).

T_{AMB} = 25 °C for both figures

Emissivity = 0.9 for all points

Figure 17. V_{in} = 115 V_{ac} - full load - bottom and top sides

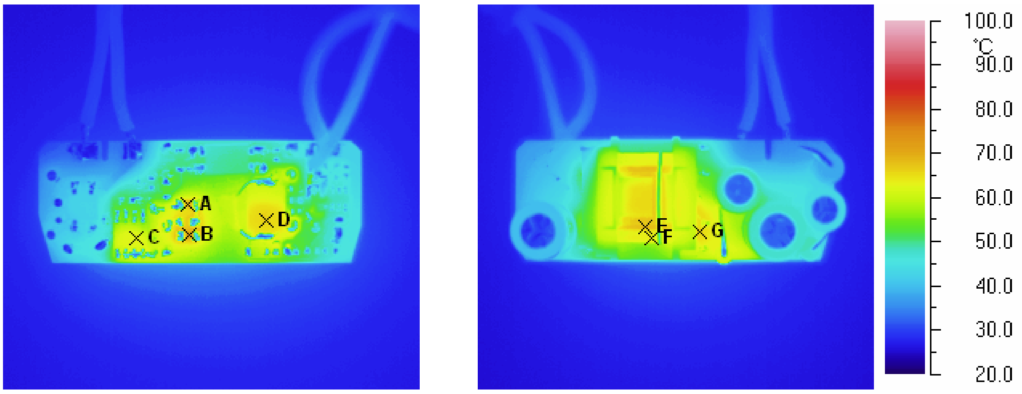


Table 5. Key component temperatures at 115 V_{ac} - 600 mA

Point	Temperature [°C]	Reference
A	69.2	R2 (clamp)
B	72.3	R1 (clamp)
C	63.0	IC2 (VIPer12A-E)
D	66.3	D4 (output diode)
E	68.3	TR1 (windings)
F	64.0	TR1 (ferrite)
G	66.2	Hot spot on PCB due to bottom side components

Figure 18. V_{in} = 230 V_{ac} - full load - bottom and top sides

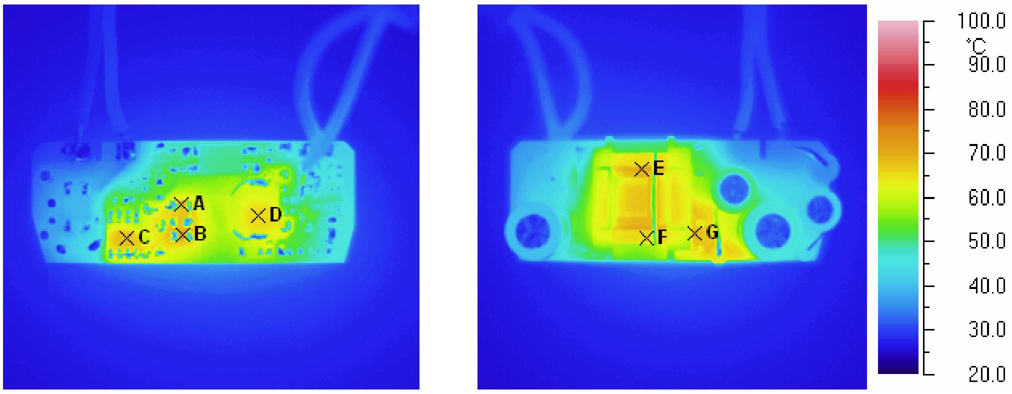


Table 6. Key component temperatures at 230 V_{ac} - 600 mA

Point	Temperature [°C]	Reference
A	70.4	R2 (clamp)
B	72.7	R1 (clamp)
C	67.9	IC2 (VIPer12A-E)
D	66.1	D4 (output diode)
E	70.4	TR1 (windings)
F	66.0	TR1 (ferrite)
G	68.5	Hot spot on PCB due to bottom side components

6 BOM

Table 7. EVALTSM1052 bill of material

Ref	Description	Size	Manufacturer
C1	Electr.cap. 2.2 µF 400 V 105ºC SEK	ø6x11 p2.5	TEAPO/YAGEO
C2	Electr.cap. 4.7 µF 400 V 105ºC SEK	ø8x11 p3.5	TEAPO/YAGEO
C3	Electr.cap. 33 µF 50 V 105ºC	ø5x11 p2.5	
C6	Electr.cap. 470 µF 16 V 105ºC SEK	ø8x11 p3.5	TEAPO/YAGEO
C4	Chip capacitor 1.5 nF/250 V X7R	0805	
C5	Chip capacitor 330 nF/16 V X7R	0603	
C7	Chip capacitor 22 nF/25 V X7R	0603	
C8	Chip capacitor 4.7 nF/25 V X7R	0603	
C9	Chip capacitor 1 uF/16 V X7R	0603	
C10	Chip capacitor 10 nF/50 V X7R	0603	
C11	Chip capacitor 1.8 nF/50 V X7R	0603	
D1	Single phase bridge S1ZB60	MBS	
D2	Diode UF108G	D041	PANJIT
D3 D5	DIODE 1N4148WS	SOD323	
D4	Diode STPS3L40S	SMC	STMicroelectronics
F1	Fuse res. 10 Ohm ±5% 2 W		
I1	Inductor 1 mH CECL-102K		COILS ELECTR.
IC1	Opto SFH617-A3 X007	SMT	SIEMENS
IC2	I.C. VIPer12AS-E	SO8	STMicroelectronics
IC3	I.C. TSM1052CLT	SOT23-6L	STMicroelectronics
R1	Chip resistor 330 K ±5%	0805	
R2	Chip resistor 680 Ohm ±5%	0805	
R3	Chip resistor 1 K ±5%	0603	
R4	Chip resistor 2.2 Ohm ±5%	0603	
R5	Chip resistor 100 Ohm ±5%	0603	
R6	Chip resistor 330 Ohm ±5%	0603	
R7 R9	Chip resistor 22 K ±1%	0603	
R8	Chip resistor 4.7 K ±5%	0603	
R10	Chip resistor 10 K ±1%	0603	
R11	Chip resistor 0.33 Ohm ±1% 200 ppm	1206	
R12	Chip resistor 2.2 K ±5%	0805	
R13	Chip resistor 220 K ±5%	0603	

Table 7. EVALTSM1052 bill of material (continued)

Ref	Description	Size	Manufacturer
R14	Chip resistor 22 K ±5%	0603	
R15	Chip resistor 0 Ohm	0603	
TR1	Transformer	EF12.6 LP	

7 PCB layout

Figure 19. THT components placing (top side)

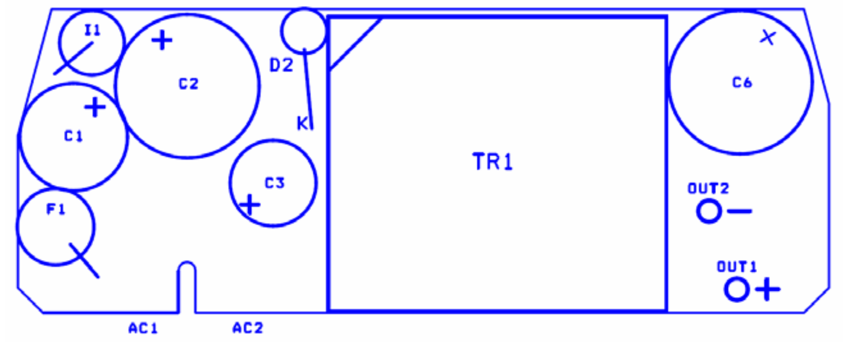
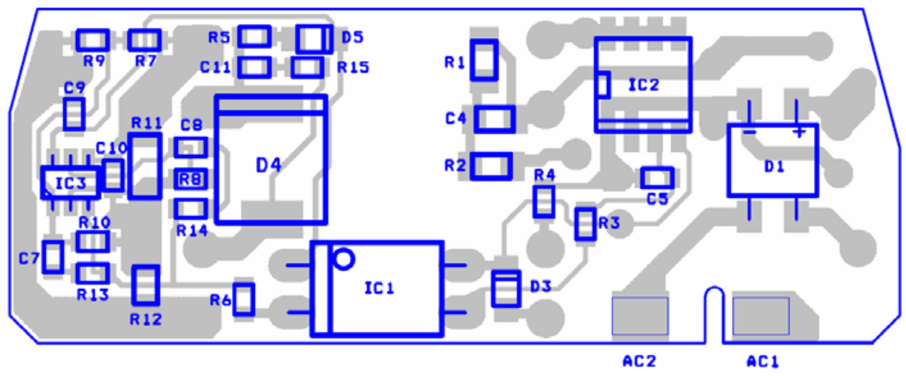


Figure 20. SMT components placing (bottom side) and copper tracks



8 Revision history

Table 8. Revision history

Date	Revision	Changes
04-Jul-2007	1	First issue

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