N-Channel 20-V (D-S) Fast Switching MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
20	0.0053 @ V_{GS} = 10 V	21.1	14
	0.0078 @ V_{GS} = 4.5 V	17.4	

FEATURES

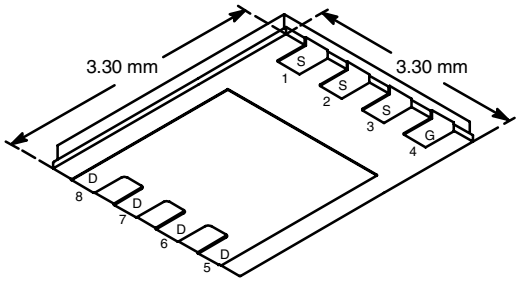
- TrenchFET® Gen II Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- PWM Optimized
- 100% R_g Tested

Pb-free
RoHS COMPLIANT

APPLICATIONS

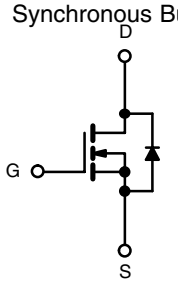
- Synchronous Rectification
- Synchronous Buck

PowerPAK 1212-8



Bottom View

Ordering Information: Si7110DN-T1—E3 (Lead (Pb)-Free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	20		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	21.1	13.5	A
	T_A = 70°C		16.9	10.8	
Pulsed Drain Current		I_{DM}	60		
Continuous Source Current (Diode Conduction)[a]		I_S	3.2	1.3	
Single Avalanche Current	L = 0.1 mH	I_{AS}	35		A
Single Avalanche Energy		E_{AS}	61		mJ
Maximum Power Dissipation[a]	T_A = 25°C	P_D	3.8	1.5	W
	T_A = 70°C		2.0	0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C
Soldering Recommendations (Peak Temperature)[b,c]			260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	24	33	°C/W
	Steady State		65	81	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.9	2.4	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.
b. See Solder Profile (http://www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

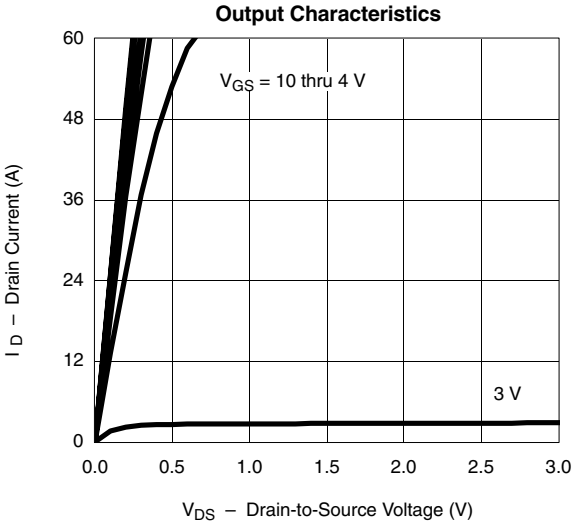
MOSFET SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

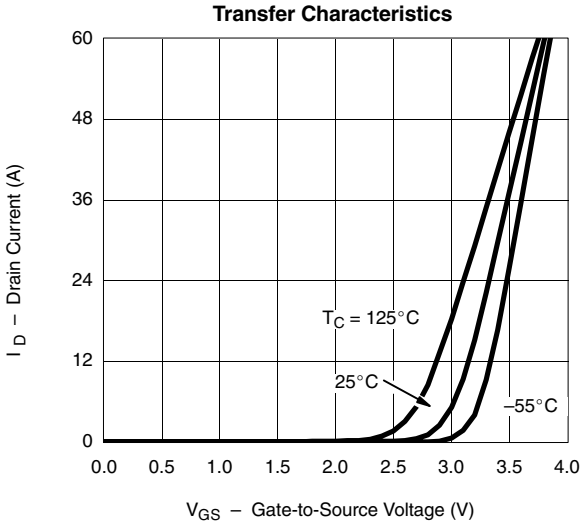
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μA	1.5		2.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20$ V, $V_{GS} = 0$ V			1	μA
		$V_{DS} = 20$ V, $V_{GS} = 0$ V, $T_J = 55$°C			5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	40			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 21.1$ A		0.0044	0.0053	Ω
		$V_{GS} = 4.5$ V, $I_D = 17.4$ A		0.0064	0.0078	
Forward Transconductance[a]	g_{fs}	$V_{DS} = 15$ V, $I_D = 21.1$ A		71		S
Diode Forward Voltage[a]	V_{SD}	$I_S = 3.2$ A, $V_{GS} = 0$ V		0.8	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 21.1$ A		14	21	nC
Gate-Source Charge	Q_{gs}			7		
Gate-Drain Charge	Q_{gd}			4.5		
Gate-Resistance	R_g	f = 1 MHz	0.7	1.4	2.1	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 10$ Ω $I_D \cong 1$ A, $V_{GEN} = 10$ V, $R_g = 6$ Ω		12	20	ns
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			36	55	
Fall Time	t_f			10	15	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 3.2$ A, di/dt = 100 A/μs		30	60	

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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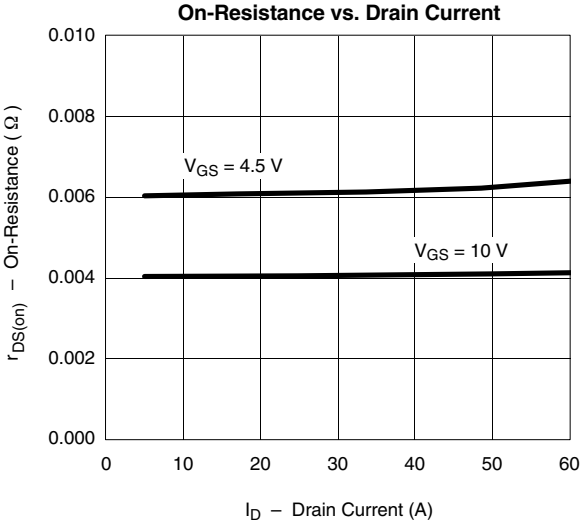

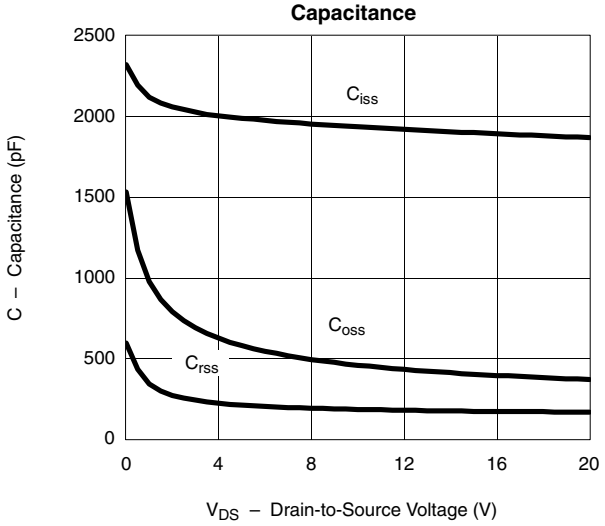

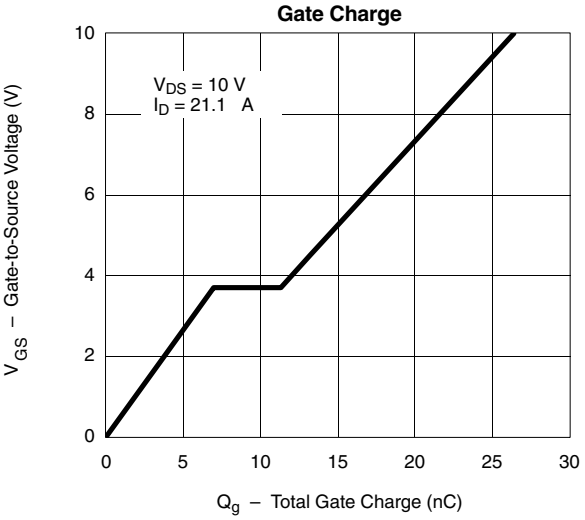

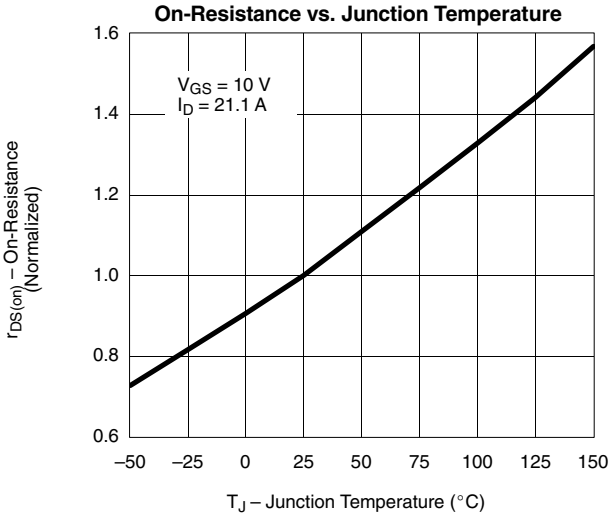

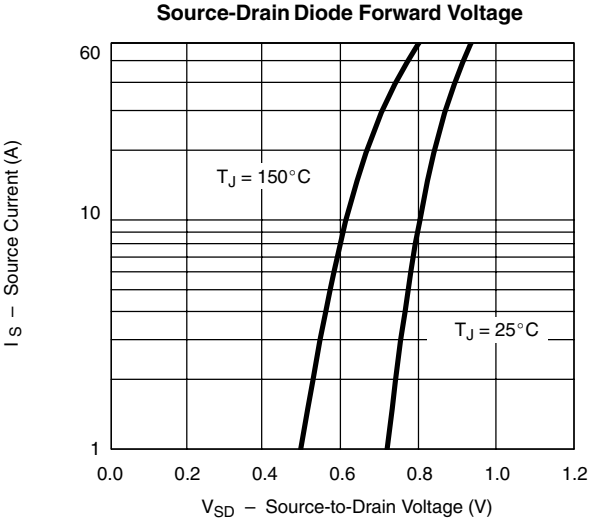

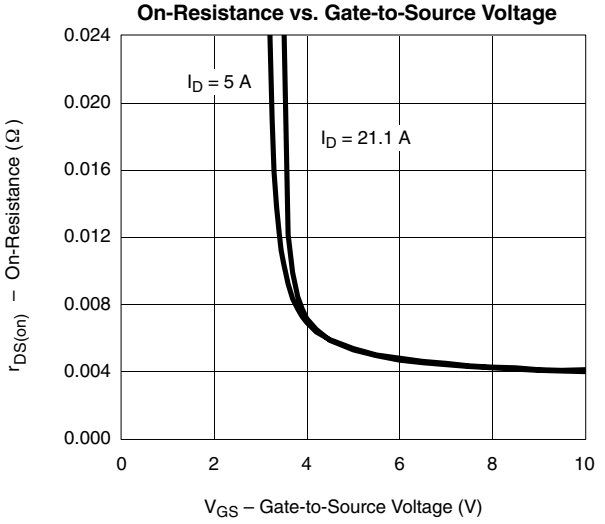

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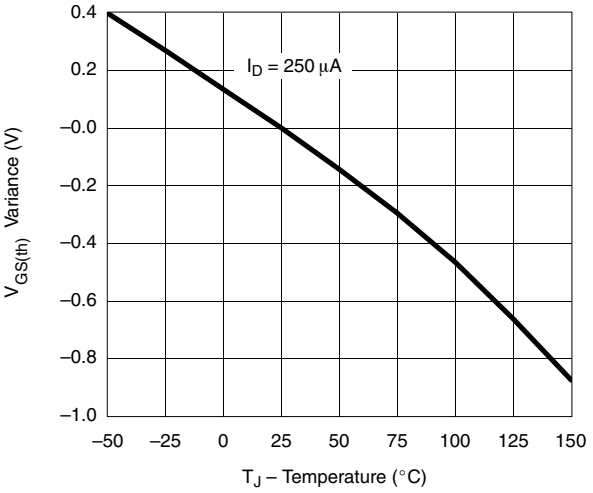
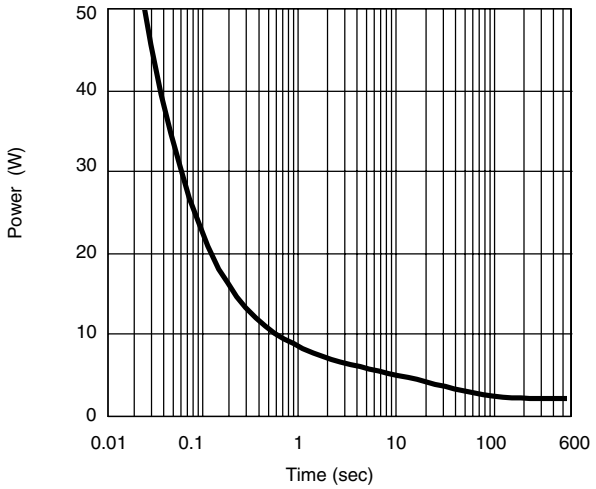
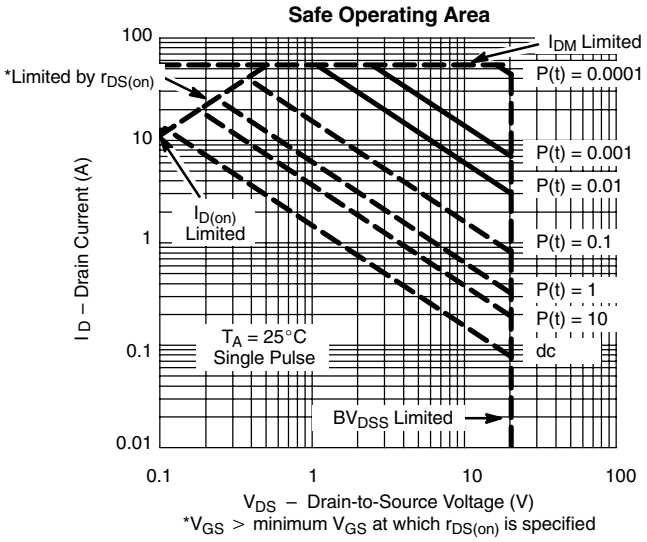
Threshold Voltage



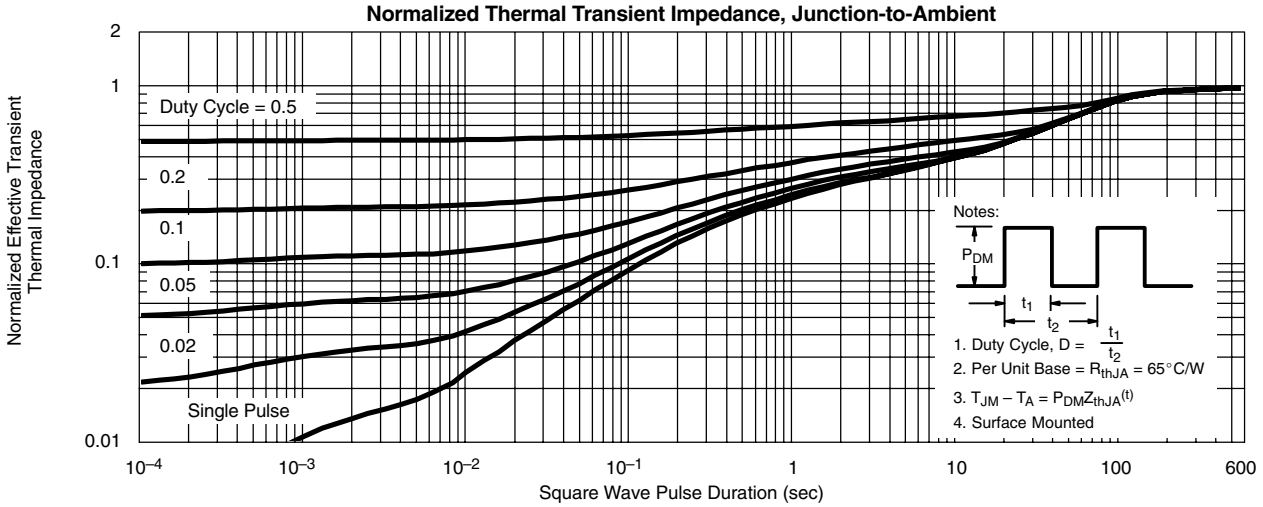
Single Pulse Power, Juncion-to-Ambient



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



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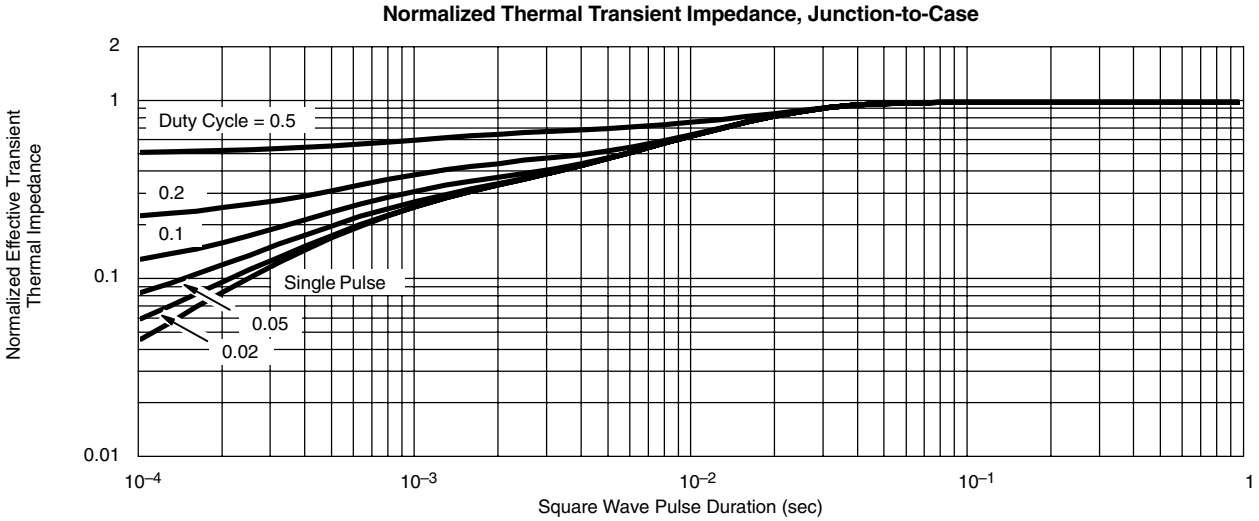

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