

SN54ALS564B, SN74ALS564B OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS164B – APRIL 1982 – REVISED JANUARY 1995

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Buffered Control Inputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N) and Ceramic (J) 300-mil DIPs, and Ceramic Flat (W) Packages

description

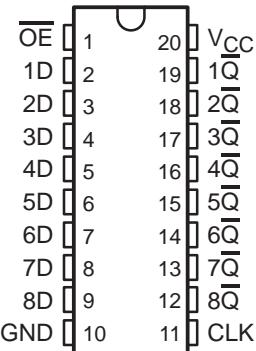
These octal D-type edge-triggered flip-flops feature inverting 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input.

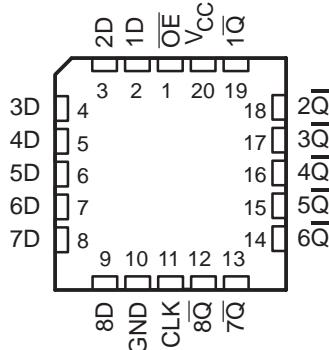
The output-enable (\overline{OE}) input does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS564B is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS564B is characterized for operation from 0°C to 70°C .

SN54ALS564B . . . J OR W PACKAGE
SN74ALS564B . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS564B . . . FK PACKAGE
(TOP VIEW)



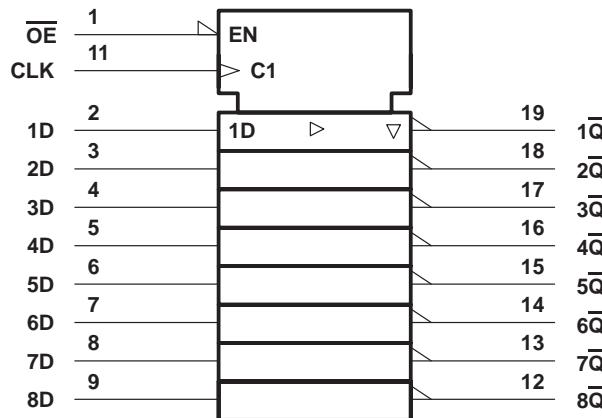
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	\overline{Q}
L	\uparrow	H	L
L	\uparrow	L	H
L	L	X	\overline{Q}_0
H	X	X	Z

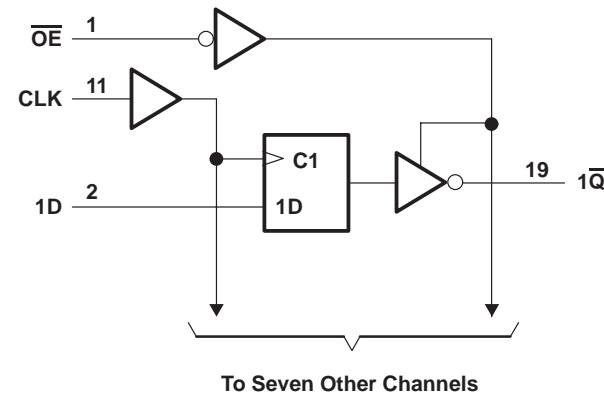
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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS564B			SN74ALS564B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-1			-2.6	mA
I _{OL}	Low-level output current			12			24	mA
f _{clock}	Clock frequency	0	22		0	30		MHz
t _w	Pulse duration, CLK high or low	25			14			ns
t _{su}	Setup time, data before CLK↑	15			15			ns
t _h	Hold time, data after CLK↑	4			0			ns
T _A	Operating free-air temperature	-55	125		0	70		°C

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WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS564B			SN74ALS564B			UNIT
		MIN	TYPT†	MAX	MIN	TYPT†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 \text{ V}$ $I_{OH} = -1 \text{ mA}$ $I_{OH} = -2.6 \text{ mA}$	2.4	3.3				2.4	
V_{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4
		$I_{OL} = 24 \text{ mA}$					0.35	0.5
I_{OZH}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.7 \text{ V}$			20			20	μA
I_{OZL}	$V_{CC} = 5.5 \text{ V}$, $V_O = 0.4 \text{ V}$			-20			-20	μA
I_I	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$			-0.2			-0.2	mA
I_O^{\ddagger}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-20	-112	-30	-112			mA
I_{CC}	$V_{CC} = 5.5 \text{ V}$	Outputs high		10	18		10	18
		Outputs low		15	24		15	24
		Outputs disabled		16	30		16	30

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

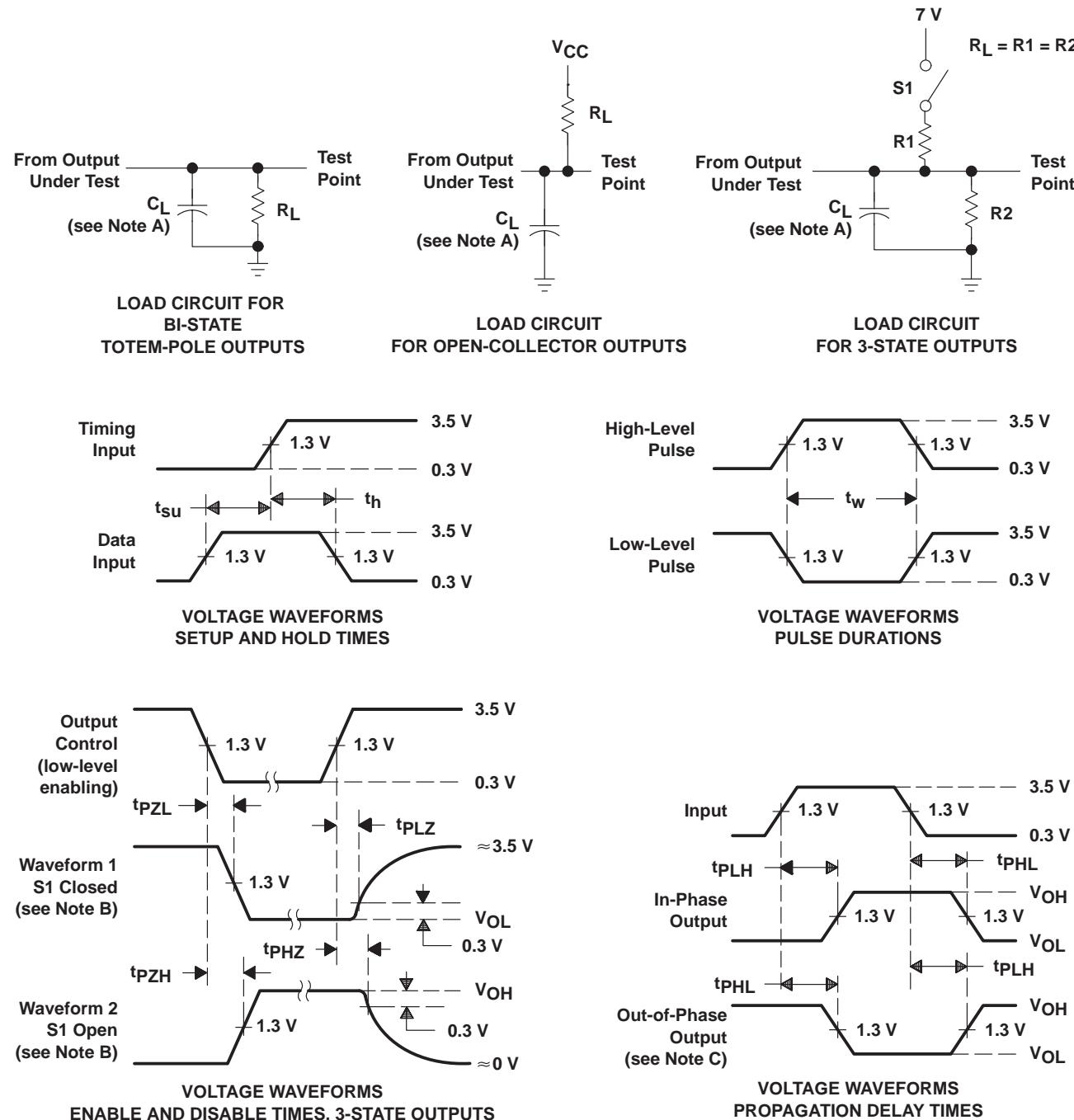
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R1 = 500 \Omega$, $R2 = 500 \Omega$, $T_A = \text{MIN to MAX}^{\$}$				UNIT	
			SN54ALS564B		SN74ALS564B			
			MIN	MAX	MIN	MAX		
f_{max}			22		30		MHz	
t_{PLH}	CLK	Any \bar{Q}	4	24	3	14	ns	
t_{PHL}			4	20	4	14		
t_{PZH}	\bar{OE}	Any \bar{Q}	4	24	3	18	ns	
t_{PZL}			3	23	4	18		
t_{PHZ}	\bar{OE}	Any \bar{Q}	2	14	1	10	ns	
t_{PLZ}			3	29	2	15		

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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**PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8872801RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8872801RA SNJ54ALS564BJ	Samples
SN74ALS564BDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS564B	Samples
SN74ALS564BN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS564BN	Samples
SN74ALS564BNSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS564B	Samples
SNJ54ALS564BJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8872801RA SNJ54ALS564BJ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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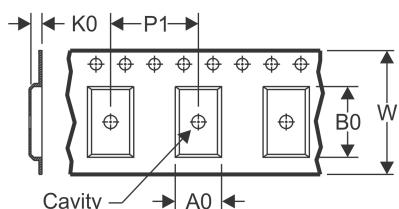
OTHER QUALIFIED VERSIONS OF SN54ALS564B, SN74ALS564B :

- Catalog: [SN74ALS564B](#)
- Military: [SN54ALS564B](#)

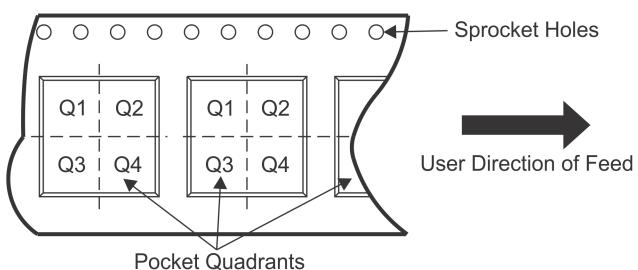
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

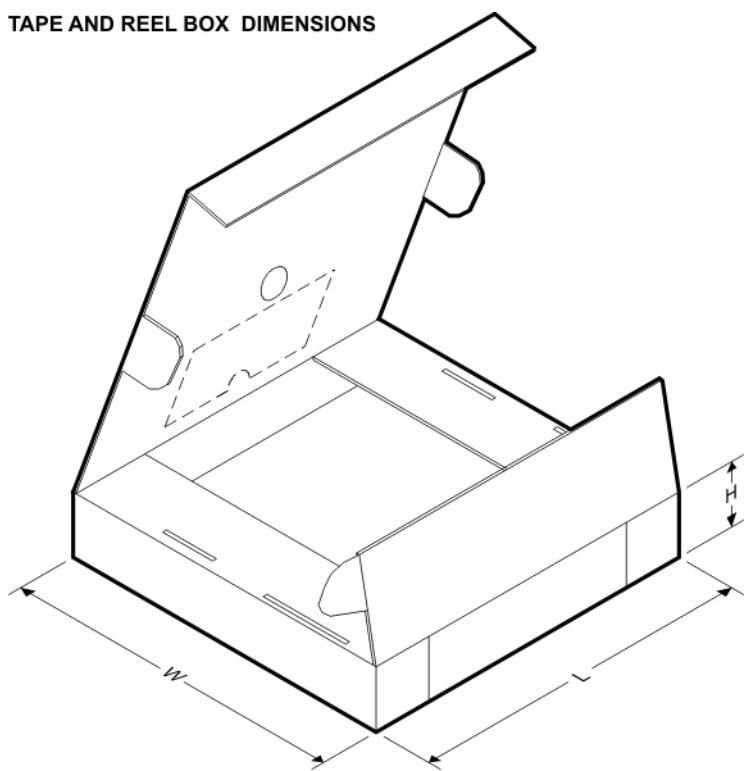
TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS564BNSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

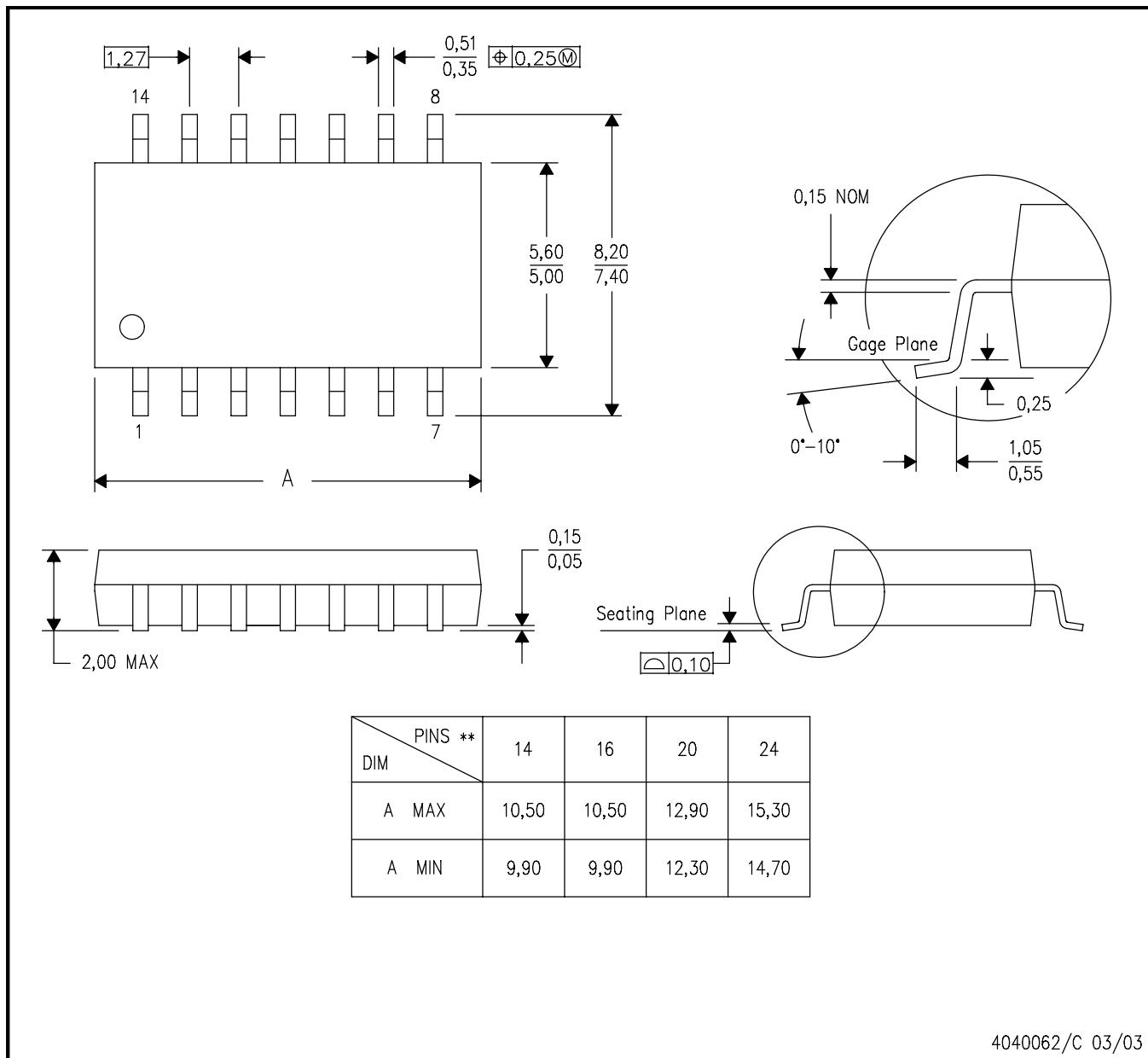
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS564BNSR	SO	NS	20	2000	367.0	367.0	45.0

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



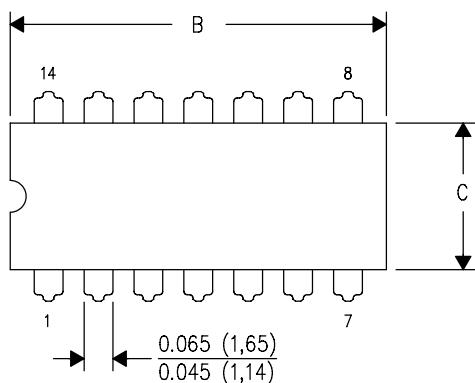
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

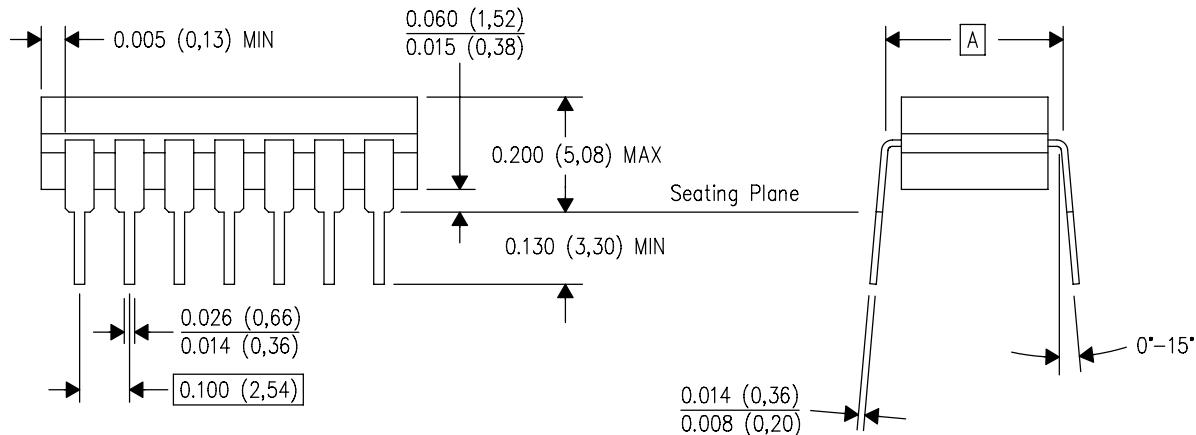
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



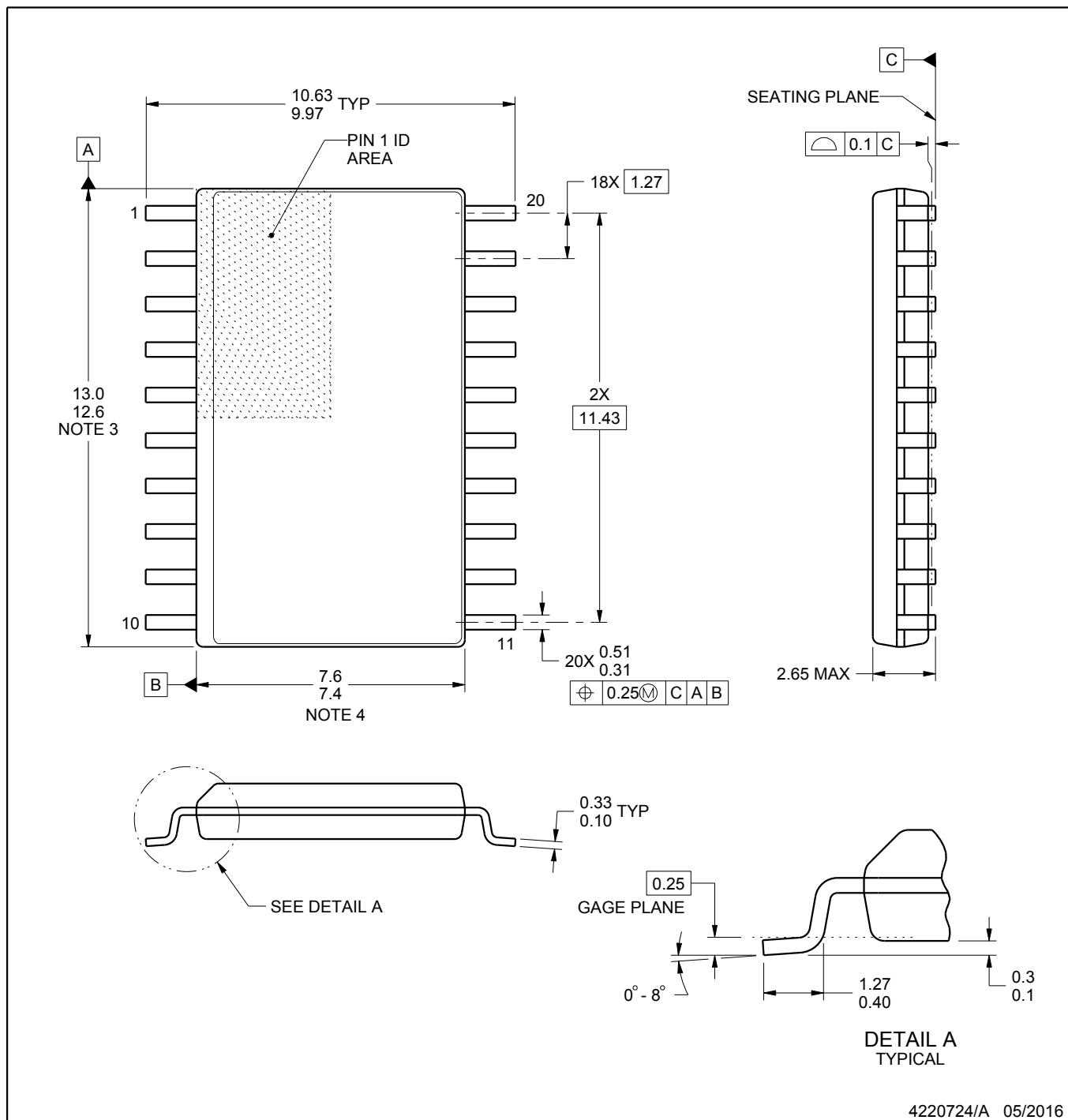


PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIC



NOTES:

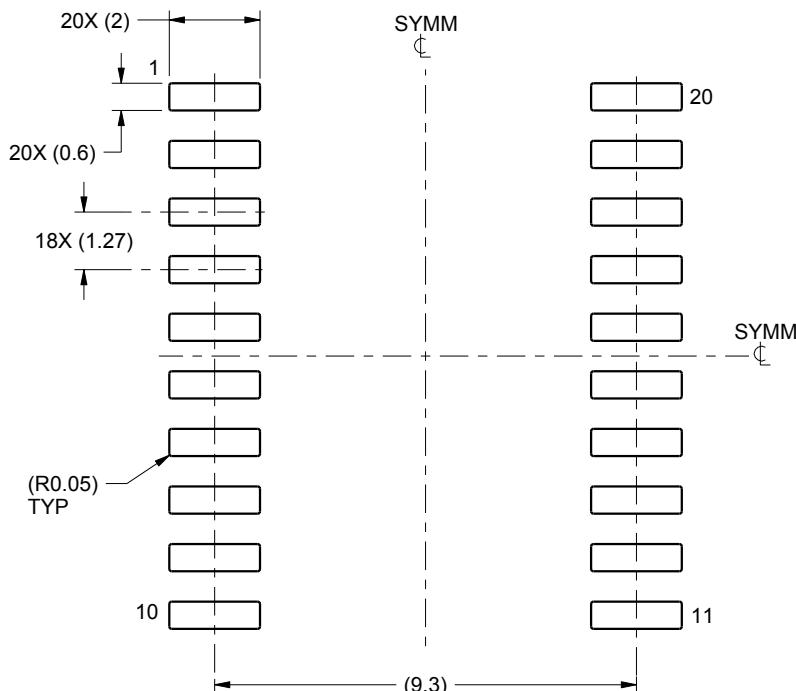
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

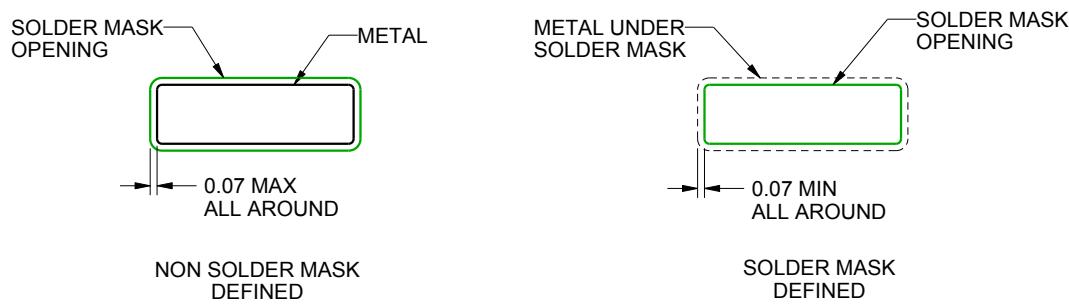
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

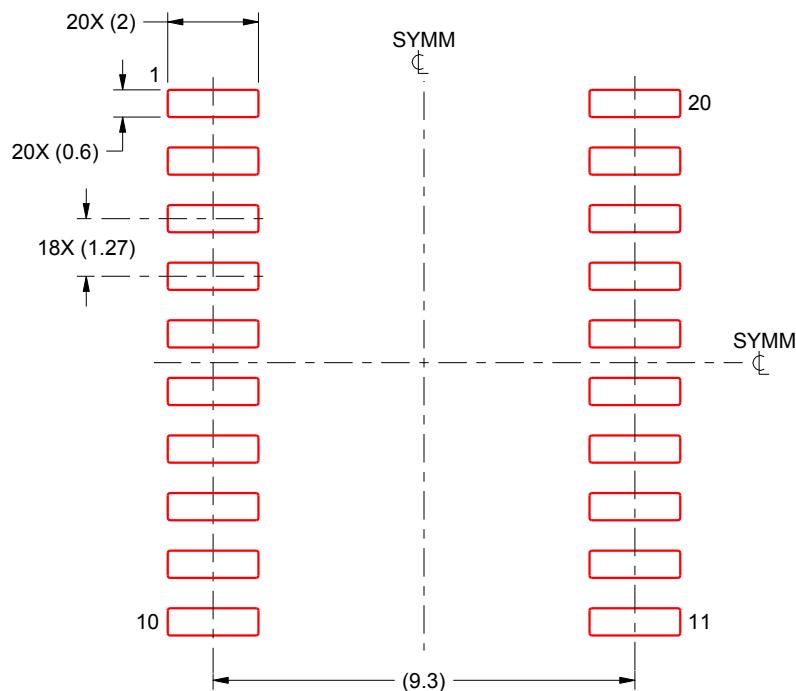
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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