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# FQP7N80C / FQPF7N80C

## N-Channel QFET® MOSFET

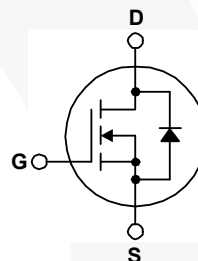
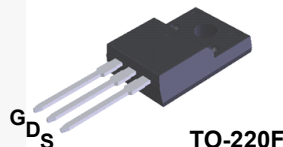
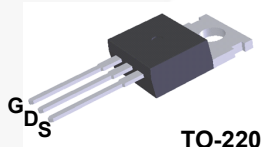
800 V, 6.6 A, 1.9 Ω

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- 6.6 A, 800 V,  $R_{DS(on)} = 1.9 \Omega$  (Max.) @  $V_{GS} = 10 V$ ,  $I_D = 3.3 A$
- Low Gate Charge (Typ. 27 nC)
- Low Crss (Typ. 10 pF)
- 100% Avalanche Tested



### Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	FQP7N80C	FQPF7N80C	Unit
$V_{DSS}$	Drain-Source Voltage	800		V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ C$ )	6.6	6.6 *	A
	- Continuous ( $T_C = 100^\circ C$ )	4.2	4.2 *	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	26.4	26.4 *	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$		V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	580		mJ
$I_{AR}$	Avalanche Current (Note 1)	6.6		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	16.7		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ C$ )	167	56	W
	- Derate above $25^\circ C$	1.33	0.44	W/ $^\circ C$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300		$^\circ C$

\* Drain current limited by maximum junction temperature.

### Thermal Characteristics

Symbol	Parameter	FQP7N80C	FQPF7N80C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.75	2.25	$^\circ C/W$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ, Max.	0.5	--	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	62.5	$^\circ C/W$

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP7N80C	FQP7N80C	TO-220	Tube	N/A	N/A	50 units
FQPF7N80C	FQPF7N80C	TO-220F	Tube	N/A	N/A	50 units

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	800	--	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.93	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	$\mu\text{A}$
		$V_{DS} = 640\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 3.3\text{ A}$	--	1.57	1.9	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 3.3\text{ A}$	--	5.5	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1290	1680	pF
$C_{oss}$	Output Capacitance		--	120	155	pF
$C_{rss}$	Reverse Transfer Capacitance		--	10	13	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 6.6\text{ A},$ $R_G = 25\ \Omega$	--	35	80	ns	
$t_r$	Turn-On Rise Time		--	100	210	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4)	--	50	110	ns
$t_f$	Turn-Off Fall Time		(Note 4)	--	60	130	ns
$Q_g$	Total Gate Charge	$V_{DS} = 640\text{ V}, I_D = 6.6\text{ A},$ $V_{GS} = 10\text{ V}$	--	27	35	nC	
$Q_{gs}$	Gate-Source Charge		(Note 4)	--	8.2	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4)	--	11	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	6.6	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	26.4	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 6.6\text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 6.6\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$	--	650	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	7.0	--	$\mu\text{C}$

#### Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2.  $L = 25\text{ mH}, I_{AS} = 6.6\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 8\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

## Typical Characteristics

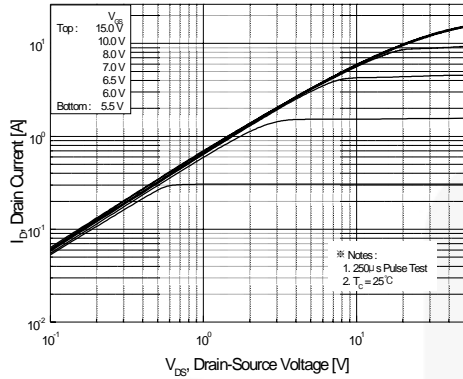


Figure 1. On-Region Characteristics

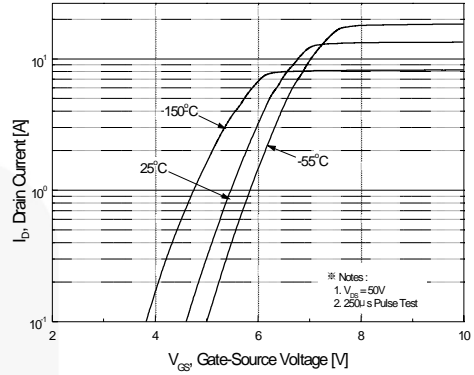


Figure 2. Transfer Characteristics

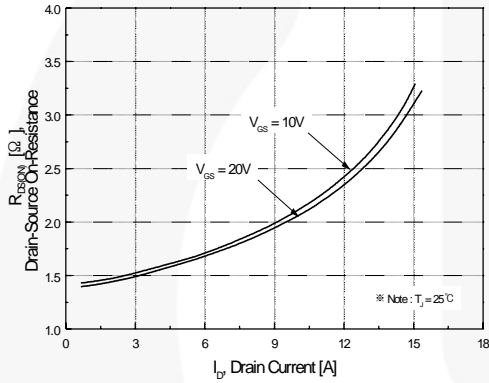


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

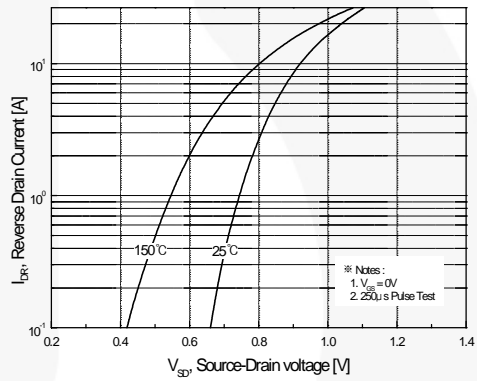


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

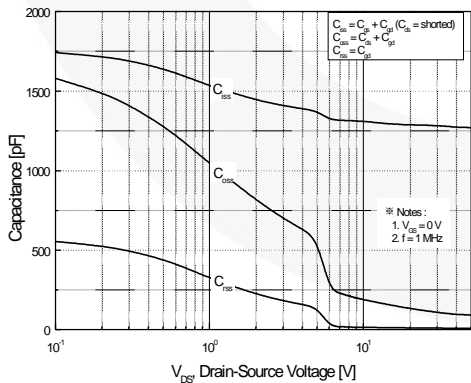


Figure 5. Capacitance Characteristics

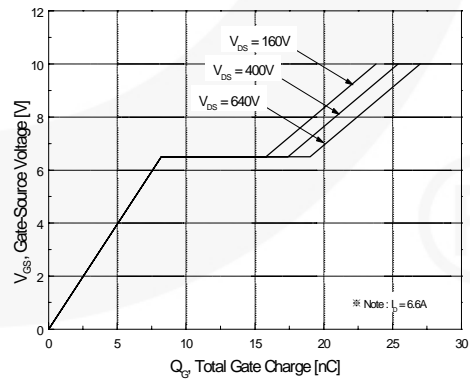
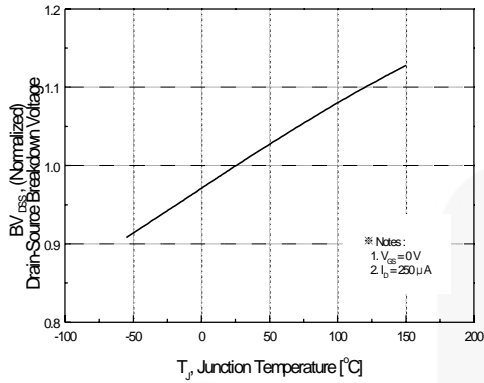
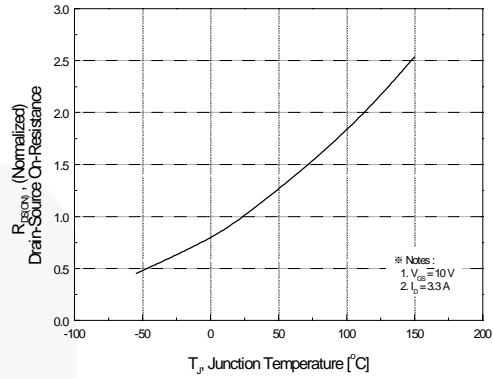


Figure 6. Gate Charge Characteristics

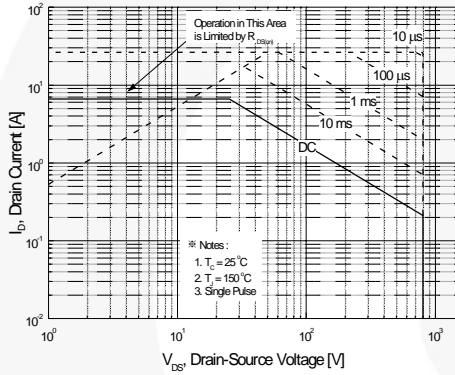
**Typical Characteristics** (Continued)



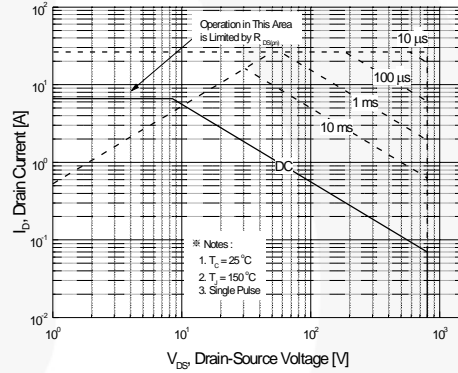
**Figure 7. Breakdown Voltage Variation vs Temperature**



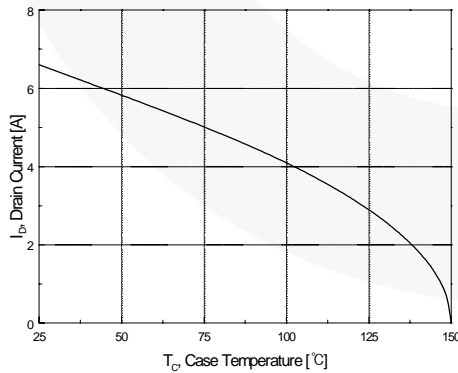
**Figure 8. On-Resistance Variation vs Temperature**



**Figure 9-1. Maximum Safe Operating Area for FQP7N80C**

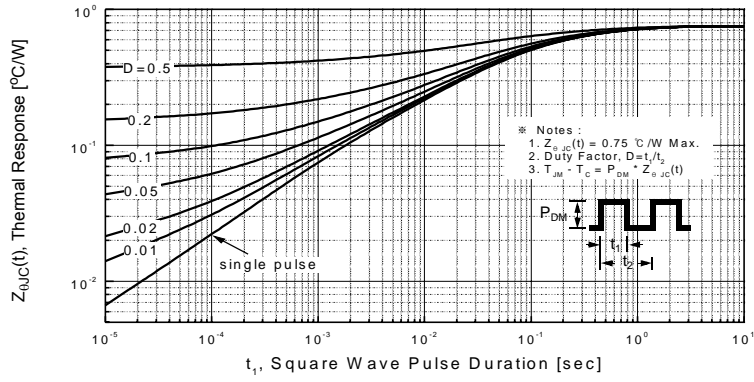


**Figure 9-2. Maximum Safe Operating Area for FQPF7N80C**

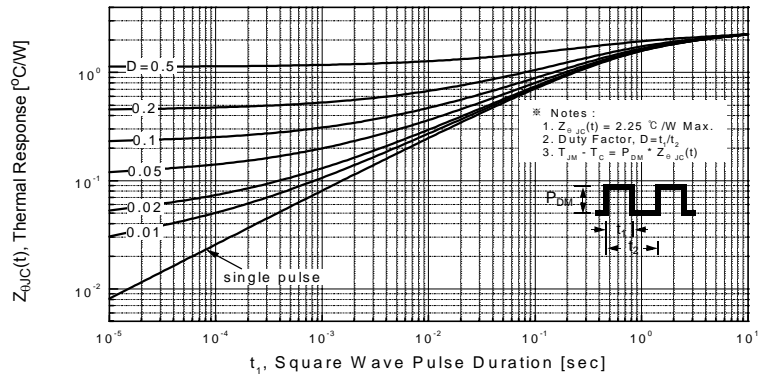


**Figure 10. Maximum Drain Current vs Case Temperature**

**Typical Characteristics** (Continued)



**Figure 11-1. Transient Thermal Response Curve for FQP7N80C**



**Figure 11-2. Transient Thermal Response Curve for FQPF7N80C**

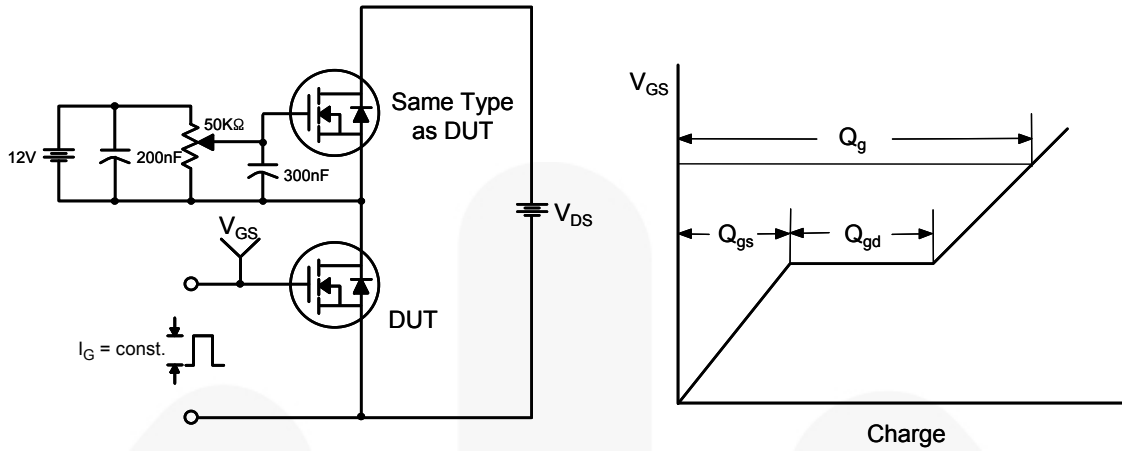


Figure 12. Gate Charge Test Circuit & Waveform

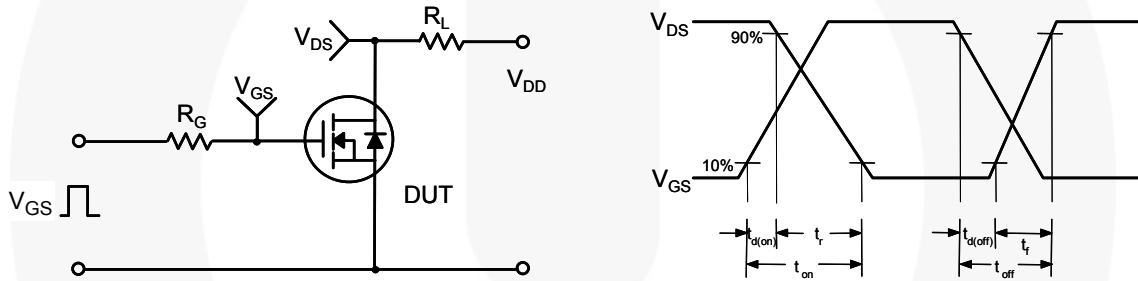


Figure 13. Resistive Switching Test Circuit & Waveforms

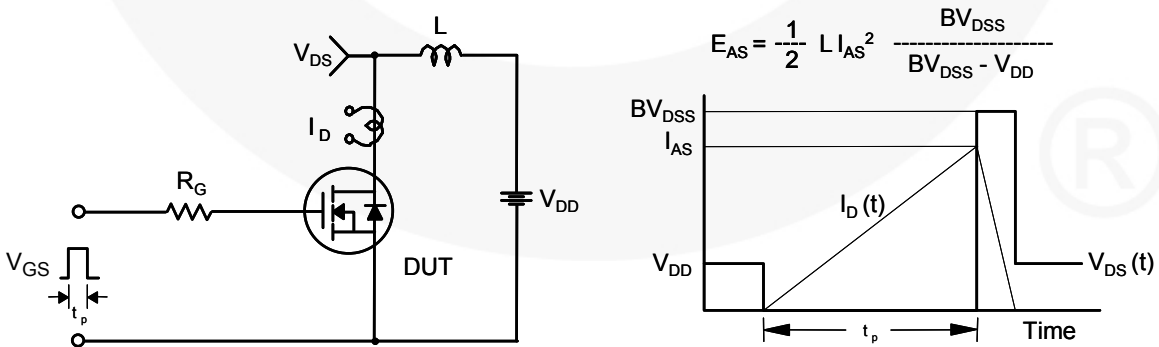


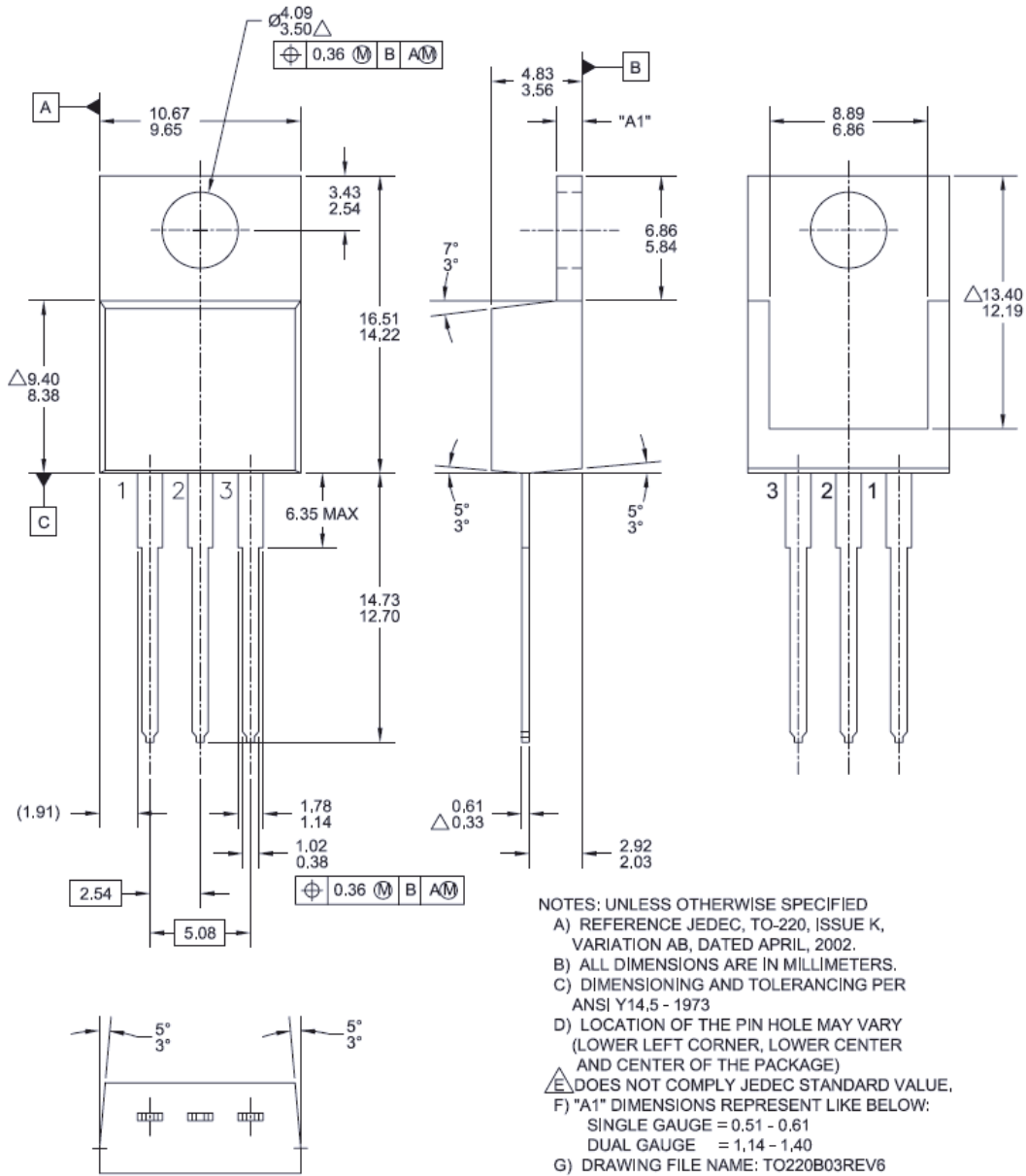
Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



**Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms**



## Mechanical Dimensions



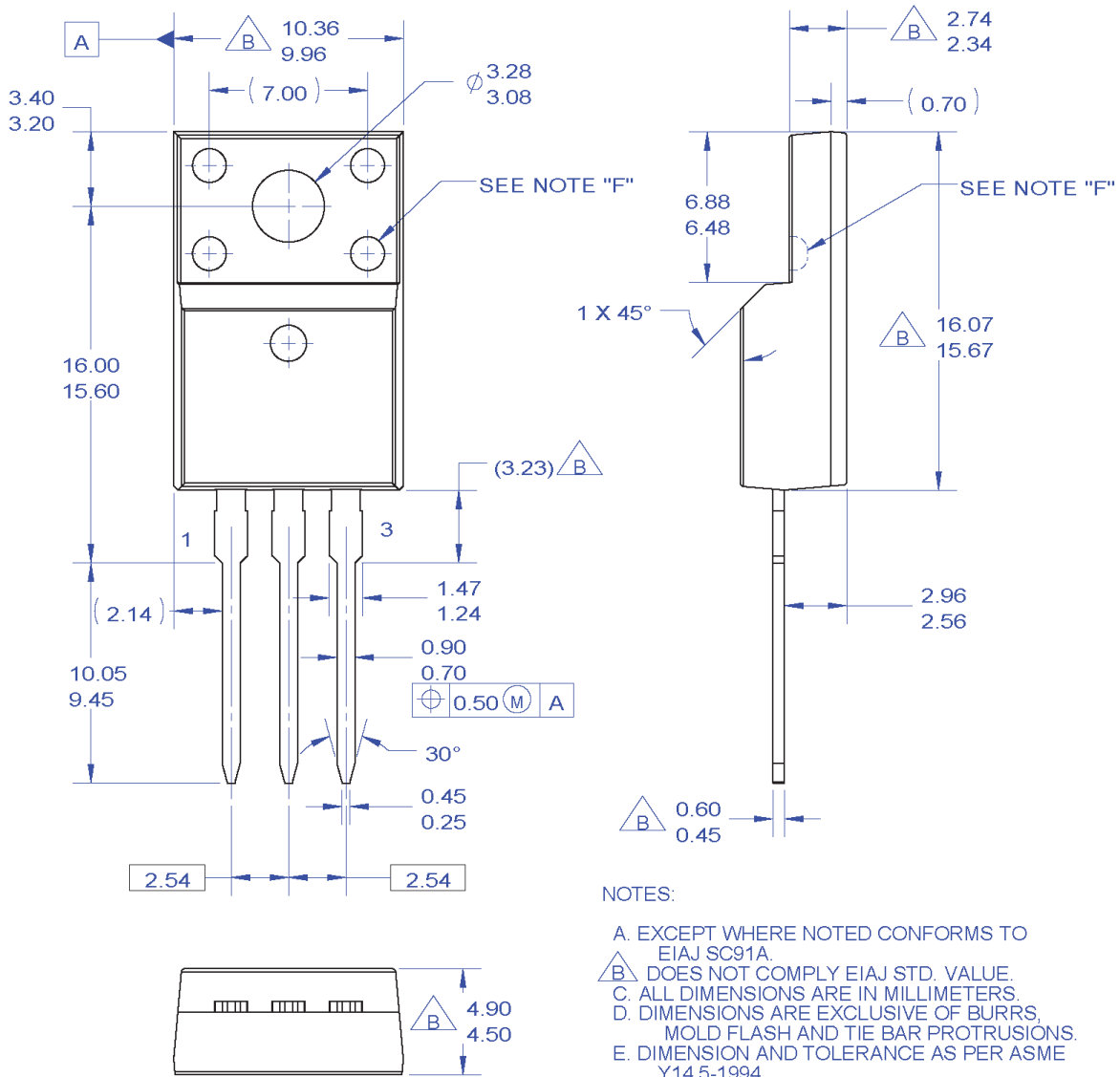
**Figure 16. TO-220, Molded, 3-Lead, Jedec Variation AB**

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## Mechanical Dimensions



### NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.  
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV3

**Figure 17. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead**

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