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FAIRCHILD SEMICONDUCTOR®

August 2005

FDN352AP
Single P-Channel, PowerTrench® MOSFET

Features

- –1.3 A, –30V $R_{DS(ON)}$ = 180 mΩ @ V_{GS} = –10V
  –1.1 A, –30V $R_{DS(ON)}$ = 300 mΩ @ V_{GS} = –4.5V
- High performance trench technology for extremely low $R_{DS(ON)}$.
- High power version of industry Standard SOT-23 package. Identical pin-out to SOT-23 with 30% higher power handling capability.

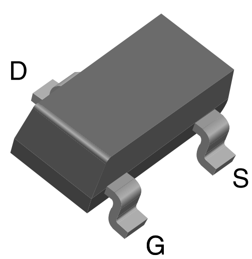
Applications

- Notebook computer power management

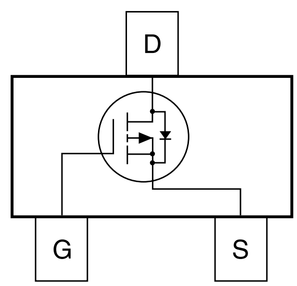
General Description

This P-Channel Logic Level MOSFET is produced using Fairchild Semiconductor advanced Power Trench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss is needed in a very small outline surface mount package.



SuperSOT™-3



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		–30	V
V_{GSS}	Gate-Source Voltage		±25	V
I_D	Drain Current – Continuous	(Note 1a)	–1.3	A
	– Pulsed		–10	
P_D	Power Dissipation for Single Operation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C
Thermal Characteristics				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
52AP	FDN352AP	7”	8mm	3000 units

Electrical Characteristics $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = –250$ µA	–30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = –250$ µA, Referenced to 25°C		–17		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = –24$ V, $V_{GS} = 0$ V			–1	µA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm 25$ V, $V_{DS} = 0$ V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = –250$ µA	–0.8	–2.0	–2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = –250$ µA, Referenced to 25°C		4		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = –10$ V, $I_D = –1.3$ A $V_{GS} = –4.5$ V, $I_D = –1.1$ A $V_{GS} = –4.5$ V, $I_D = –1.1$ A, $T_J = 125°C$		150 250 330	180 300 400	mΩ
g_{FS}	Forward Transconductance	$V_{DS} = –5$ V, $I_D = –0.9$ A		2.0		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = –15$ V, $V_{GS} = 0$ V, f = 1.0 MHz		150		pF
C_{oss}	Output Capacitance			40		pF
C_{rss}	Reverse Transfer Capacitance			20		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = –10$ V, $I_D = –1$ A, $V_{GS} = –10$ V, $R_{GEN} = 6\ \Omega$		4	8	ns
t_r	Turn–On Rise Time			15	28	ns
$t_{d(off)}$	Turn–Off Delay Time			10	18	ns
t_f	Turn–Off Fall Time			1	2	ns
Q_g	Total Gate Charge	$V_{DS} = –10V$, $I_D = –0.9$ A, $V_{GS} = –4.5$ V		1.4	1.9	nC
Q_{gs}	Gate–Source Charge			0.5		nC
Q_{gd}	Gate–Drain Charge			0.5		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–0.42	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = –0.42$ A (Note 2)		–0.8	–1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = –3.9$ A, $dI_F/dt = 100$ A/µs		17		ns
Q_{rr}	Diode Reverse Recovery Charge			7		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.
   (a) $R_{\theta JA} = 250°C/W$ when mounted on a 0.02 in^2 pad of 2oz. copper.
   (b) $R_{\theta JA} = 270°C/W$ when mounted on a 0.001 in^2 pad of 2oz. copper.
2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

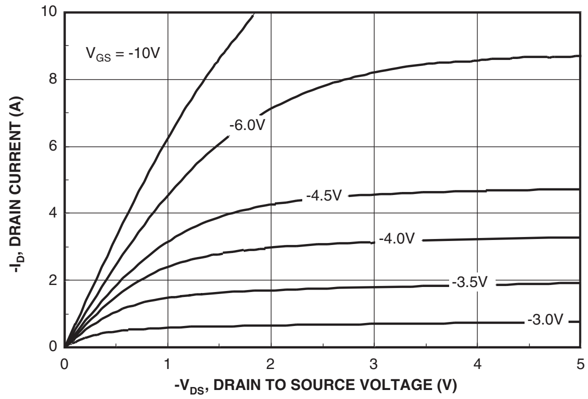


Figure 1. On-Region Characteristics.

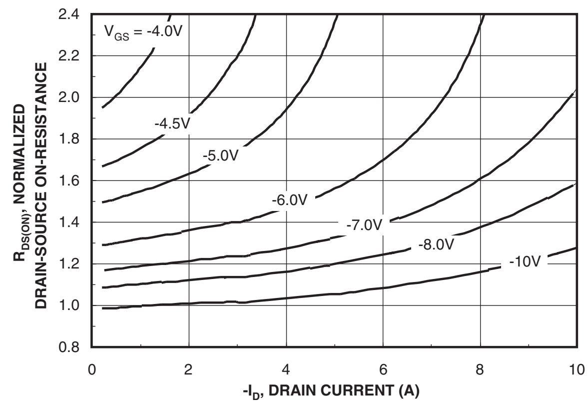


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

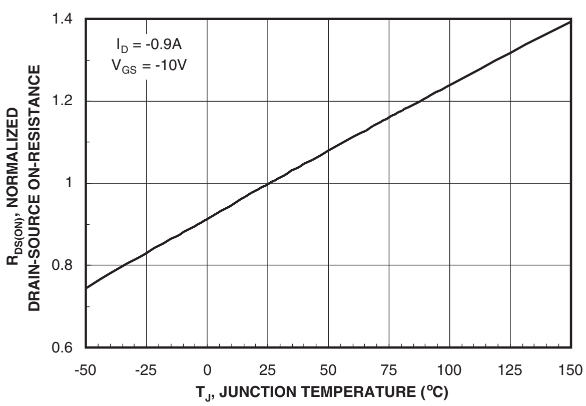


Figure 3. On-Resistance Variation with Temperature.

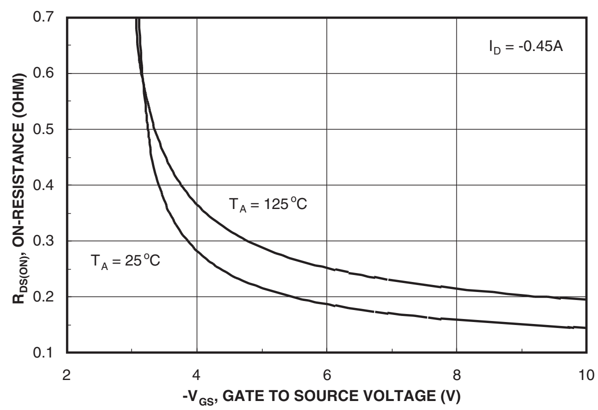


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

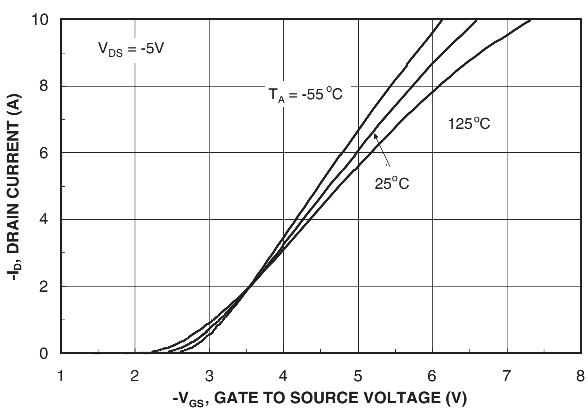


Figure 5. Transfer Characteristics.

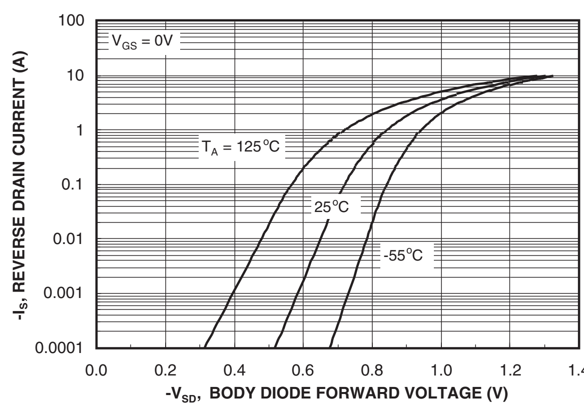


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

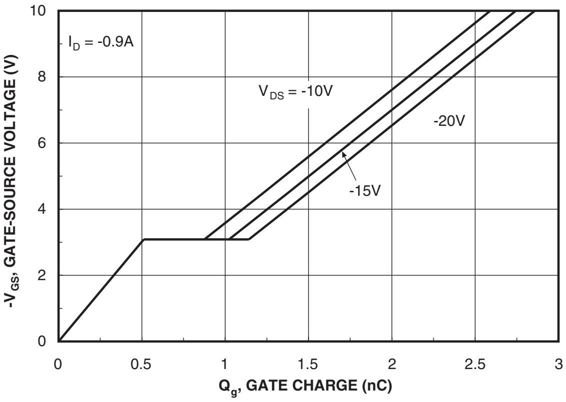


Figure 7. Gate Charge Characteristics.

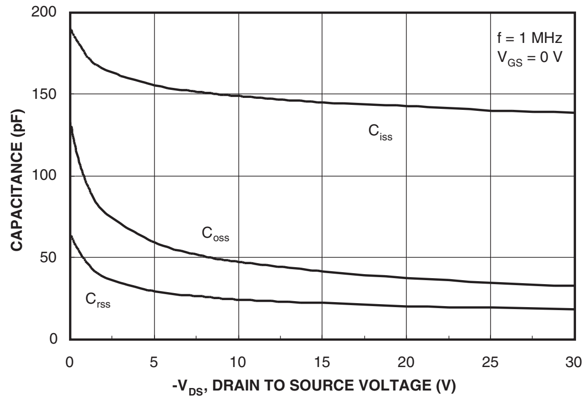


Figure 8. Capacitance Characteristics.

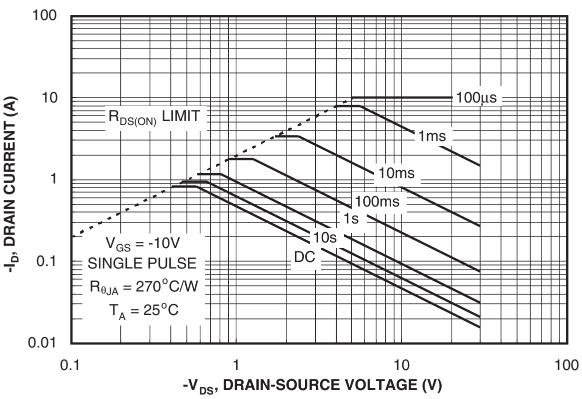


Figure 9. Maximum Safe Operating Area.

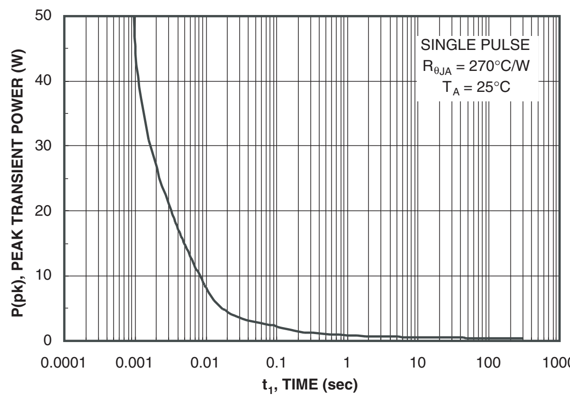


Figure 10. Single Pulse Maximum Power Dissipation.

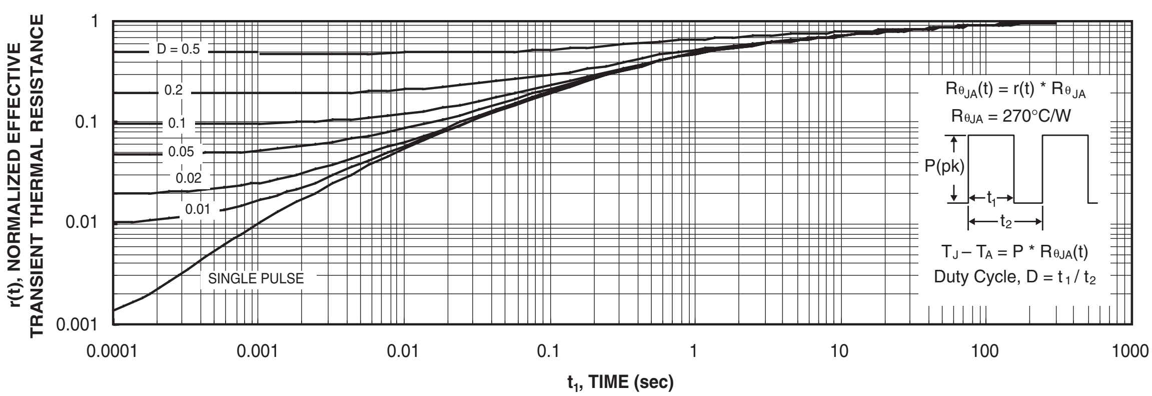


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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