AUTOSWITCHING POWER MUX

Check for Samples: TPS2112A, TPS2113A

FEATURES

- **Two-Input, One-Output Power Multiplexer with Low $r_{DS(on)}$ Switches:**
  - **84 mΩ Typ (TPS2113A)**
  - **120 mΩ Typ (TPS2112A)**
- **Reverse and Cross-Conduction Blocking**
- **Wide Operating Voltage: 2.8 V to 5.5 V**
- **Low Standby Current: 0.5 µA Typ**
- **Low Operating Current: 55 µA Typ**
- **Adjustable Current Limit**
- **Controlled Output Voltage Transition Time:**
  - **Limits Inrush Current**
  - **Minimizes Output Voltage Hold-Up Capacitance**
- **CMOS- and TTL-Compatible Control Inputs**
- **Auto-Switching Operating Mode**
- **Thermal Shutdown**
- **Available in TSSOP-8 and 3-mm × 3-mm SON-8 Packages**

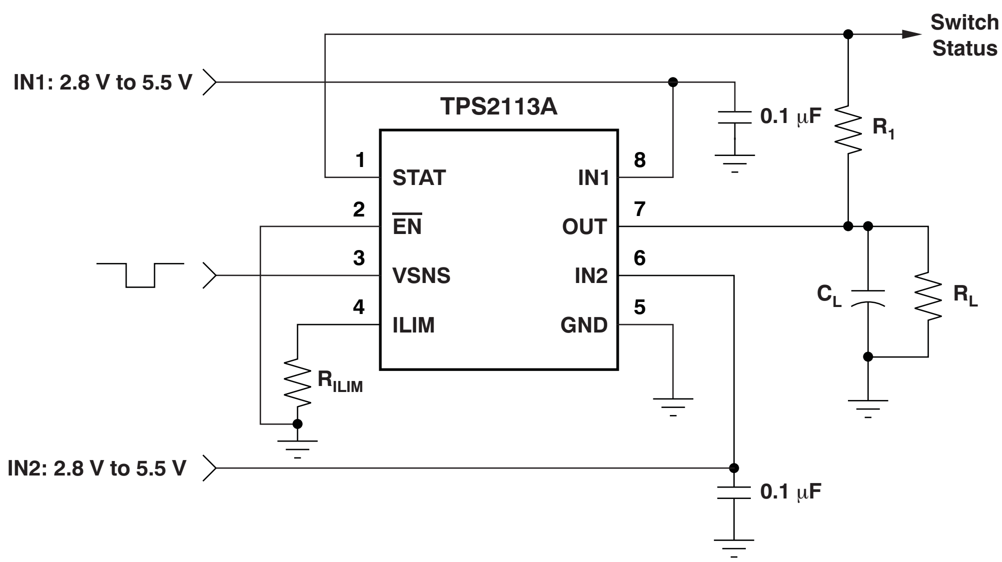
APPLICATIONS

- **PCs**
- **PDAs**
- **Digital Cameras**
- **Modems**
- **Cell Phones**
- **Digital Radios**
- **MP3 Players**

DESCRIPTION

The TPS211xA family of power multiplexers enables seamless transition between two power supplies (such as a battery and a wall adapter), each operating at 2.8 V to 5.5 V and delivering up to 2 A, depending on package. The TPS211xA family includes extensive protection circuitry, including user-programmable current limiting, thermal protection, inrush current control, seamless supply transition, cross-conduction blocking, and reverse-conduction blocking. These features greatly simplify designing power multiplexer applications.

TYPICAL APPLICATION



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS

FEATURE		TPS2110A	TPS2111A	TPS2112A	TPS2113A	TPS2114A	TPS2115A
Current Limit Adjustment Range		0.31 A to 0.75 A	0.63 A to 1.25 A	0.31 A to 0.75 A	0.63 A to 2 A	0.31 A to 0.75 A	0.63 A to 2 A
Switching Modes	Manual	Yes	Yes	No	No	Yes	Yes
	Automatic	Yes	Yes	Yes	Yes	Yes	Yes
Switch Status Output		No	No	Yes	Yes	Yes	Yes

DEVICE INFORMATION[1]

T_A	PACKAGE	I_{OUT} (A)	ORDERING NUMBER	PACKAGE MARKING
−40°C to +85°C	TSSOP-8 (PW)	0.75	TPS2112APW	2112A
		1.25	TPS2113APW	2113A
	SON-8 (DRB)	2	TPS2113ADRB	PTOI

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS[1]

Over recommended junction temperature range, unless otherwise noted.

		TPS2112A, TPS2113A	UNIT
Input voltage range at pins IN1, IN2, $\overline{EN}$, VSNS, ILIM[2]		−0.3 to 6	V
Output voltage range, $V_{O(OUT)}$, $V_{O(STAT)}$[2]		−0.3 to 6	V
Output sink current, $I_{O(STAT)}$		5	mA
Continuous output current, I_O	TPS2112APW	0.9	A
	TPS2113APW	1.5	A
	TPS2113ADRB, $T_J \le 105°C$	2.5	A
Continuous total power dissipation		See Dissipation Ratings table	
Junction temperature		Internally Limited	
ESD	Human body model (HBM)	2	kV
	Charged device model (CDM)	500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

DISSIPATION RATINGS

PACKAGE	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
TSSOP-8 (PW)	3.9 mW/°C	387 mW	213 mW	155 mW
SON-8 (DRB)[1]	25.0 mW/°C	2.50 mW	1.38 mW	1.0 W

(1) See TI application note SLMA002 for mounting recommendations.

RECOMMENDED OPERATING CONDITIONS

		TPS2112A, TPS2113A			
		MIN	NOM	MAX	UNIT
Input voltage at IN1, $V_{I(IN1)}$	$V_{I(IN2)} \geq 2.8$ V	1.5		5.5	V
	$V_{I(IN2)} < 2.8$ V	2.8		5.5	
Input voltage at IN2, $V_{I(IN2)}$	$V_{I(IN1)} \geq 2.8$ V	1.5		5.5	V
	$V_{I(IN1)} < 2.8$ V	2.8		5.5	
Input voltage: $V_{I(\overline{EN})}$, $V_{I(VSNS)}$		0		5.5	V
Nominal current limit adjustment range, $I_{O(OUT)}$ [(1)]	TPS2112APW	0.31		0.75	A
	TPS2113APW	0.63		1.25	
	TPS2113ADRB, $T_J \leq 105°C$	0.63		2	A
Operating virtual junction temperature, T_J		–40		125	°C

(1) Minimum recommended current limit is based on accuracy considerations.

ELECTRICAL CHARACTERISTICS: Power Switch

Over recommended operating junction temperature, R_{ILIM} = 400 Ω, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TPS2112A			TPS2113A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Drain-source on-state resistance (INx−OUT)	$r_{DS(on)}$ [(1)]	T_J = 25°C, I_L = 500 mA	$V_{I(IN1)} = V_{I(IN2)} = 5.0$ V		120	140		84	110	mΩ
			$V_{I(IN1)} = V_{I(IN2)} = 3.3$ V		120	140		84	110	
			$V_{I(IN1)} = V_{I(IN2)} = 2.8$ V		120	140		84	110	
		T_J = 125°C, I_L = 500 mA	$V_{I(IN1)} = V_{I(IN2)} = 5.0$ V			220			150	mΩ
			$V_{I(IN1)} = V_{I(IN2)} = 3.3$ V			220			150	
			$V_{I(IN1)} = V_{I(IN2)} = 2.8$ V			220			150	

(1) The TPS211xA can switch a voltage as low as 1.5 V as long as there is a minimum of 2.8 V at one of the input power pins. In this specific case, the lower supply voltage has no effect on the IN1 and IN2 switch on-resistances.

ELECTRICAL CHARACTERISTICS

Over recommended operating junction temperature, $I_{O(OUT)}$ = 0 A, and R_{ILIM} = 400 Ω, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TPS2112A, TPS2113A			UNIT
			MIN	TYP	MAX	
LOGIC INPUTS ($\overline{EN}$)						
High-level input voltage	V_{IH}		2			V
Low-level input voltage	V_{IL}				0.7	V
Input current		$\overline{EN}$ = High, sink current			1	µA
		$\overline{EN}$ = Low, source current	0.5	1.4	5	
SUPPLY AND LEAKAGE CURRENTS						
Supply current from IN1 (operating)		$V_{I(VSNS)}$ = 1.5 V, $\overline{EN}$ = Low (IN1 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V		55	90	µA
		$V_{I(VSNS)}$ = 1.5 V, $\overline{EN}$ = Low (IN1 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V,		1	12	
		$V_{I(VSNS)}$ = 0 V, $\overline{EN}$ = Low (IN2 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V			75	
		$V_{I(VSNS)}$ = 0 V, $\overline{EN}$ = Low (IN2 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V			1	
Supply current from IN2 (operating)		$V_{I(VSNS)}$ = 1.5 V, $\overline{EN}$ = Low (IN1 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V			1	µA
		$V_{I(VSNS)}$ = 1.5 V, $\overline{EN}$ = Low (IN1 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V			75	
		$V_{I(VSNS)}$ = 0 V, $\overline{EN}$ = Low (IN2 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V		1	12	
		$V_{I(VSNS)}$ = 0 V, $\overline{EN}$ = Low (IN2 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V		55	90	

ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating junction temperature, $I_{O(OUT)}$ = 0 A, and R_{ILIM} = 400 Ω, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TPS2112A, TPS2113A MIN	TYP	MAX	UNIT
SUPPLY AND LEAKAGE CURRENTS, *Continued*						
Quiescent current from IN1 (standby)		$\overline{EN}$ = High (inactive), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V		0.5	2	µA
		$\overline{EN}$ = High (inactive), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V			1	
Quiescent current from IN2 (standby)		$\overline{EN}$ = High (inactive), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V			1	µA
		$\overline{EN}$ = High (inactive), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V		0.5	2	
Forward leakage current from IN1 (measured from OUT to GND)		$\overline{EN}$ = High (inactive), $V_{I(IN1)}$ = 5.5 V, IN2 open, $V_{O(OUT)}$ = 0 V (shorted), T_J = 25°C		0.1	5	µA
Forward leakage current from IN2 (measured from OUT to GND)		$\overline{EN}$ = High (inactive), $V_{I(IN2)}$ = 5.5 V, IN1 open, $V_{O(OUT)}$ = 0 V (shorted), T_J = 25°C		0.1	5	µA
Reverse leakage current to INx (measured from INx to GND)		$\overline{EN}$ = High (inactive), $V_{I(INx)}$ = 0 V, $V_{O(OUT)}$ = 5.5 V, T_J = 25°C		0.3	5	µA
STAT OUTPUT						
Leakage current		$V_{O(STAT)}$ = 5.5 V		0.01	1	µA
Saturation voltage		$I_{I(STAT)}$ = 2 mA, IN1 switch is on		0.13	0.4	V
Deglitch time (falling edge only)				150		µs
CURRENT LIMIT CIRCUIT						
Current limit accuracy	TPS2112A	R_{ILIM} = 400 Ω	0.51	0.63	0.80	A
		R_{ILIM} = 700 Ω	0.30	0.36	0.50	
	TPS2113A	R_{ILIM} = 400 Ω	0.95	1.25	1.56	A
		R_{ILIM} = 700 Ω	0.47	0.71	0.99	
Current limit settling time	t_d	Time for short-circuit output current to settle within 10% of its steady state value.		1		ms
Input current at ILIM		$V_{I(ILIM)}$ = 0 V	–15		0	µA
VSNS COMPARATOR						
VSNS threshold voltage		$V_{I(VSNS)}$ ↑	0.78	0.80	0.82	V
		$V_{I(VSNS)}$ ↓	0.735	0.755	0.775	
VSNS comparator hysteresis			30		60	mV
Deglitch of VSNS comparator (both ↑ ↓)			90	150	220	µs
Input current		0 V ≤ $V_{I(VSNS)}$ ≤ 5.5 V	–1		1	µA
UVLO						
IN1 and IN2 UVLO		Falling edge	1.15	1.25		V
		Rising edge		1.30	1.35	
IN1 and IN2 UVLO hysteresis			30	57	65	mV
Internal V_{DD} UVLO (the higher of IN1 and IN2)		Falling edge	2.4	2.53		V
		Rising edge		2.58	2.8	
Internal V_{DD} UVLO hysteresis			30	50	75	mV
UVLO deglitch for IN1, IN2		Falling edge		110		µs

ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating junction temperature, $I_{O(OUT)}$ = 0 A, and R_{ILIM} = 400 Ω, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TPS2112A, TPS2113A MIN	TYP	MAX	UNIT
REVERSE CONDUCTION BLOCKING						
Minimum output-to-input voltage difference to block switching	$\Delta V_{O(I\_block)}$	$\overline{EN}$ = high, $V_{I(IN1)}$ = 3.3 V and $V_{I(IN2)}$ = $V_{I(VSNS)}$ = 0 V. Connect OUT to a 5-V supply through a series 1-kΩ resistor. Let $\overline{EN}$ = low. Slowly decrease the supply voltage until OUT connects to IN1.	80	100	120	mV
THERMAL SHUTDOWN						
Thermal shutdown threshold		TPS211xA is in current limit.	135			°C
Recovery from thermal shutdown		TPS211xA is in current limit.	125			°C
Hysteresis				10		°C
IN2−IN1 COMPARATORS						
Hysteresis of IN2−IN1 comparator			0.1		0.2	V
Deglitch of IN2−IN1 comparator (both ↑ ↓)			10	20	50	µs

SWITCHING CHARACTERISTICS

Over recommended operating junction temperature, $V_{I(IN1)}$ = $V_{I(IN2)}$ = 5.5 V, and R_{ILIM} = 400 Ω, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TPS2112A MIN	TYP	MAX	TPS2113A MIN	TYP	MAX	UNIT
t_R	Output rise time from an enable	$V_{I(IN1)}$ = $V_{I(IN2)}$ = 5 V, $V_{I(SNS)}$ = 1.5 V	T_J = 25°C, C_L = 1 µF, I_L = 500 mA; see Figure 1**(a)**.	0.5	1.0	1.5	1	1.8	3	ms
t_F	Output fall time from a disable	$V_{I(IN1)}$ = $V_{I(IN2)}$ = 5 V, $V_{I(SNS)}$ = 1.5 V	T_J = 25°C, C_L = 1 µF, I_L = 500 mA; see Figure 1**(a)**.	0.35	0.5	0.7	0.5	1	2	ms
t_T	Transition time	IN1 to IN2 transition, $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5 V, $V_{I(\overline{EN})}$ = 0 V	T_J = 125°C, C_L = 10 µF, I_L = 500 mA; measure transition time as 10% to 90% rise time or from 3.4 V to 4.8 V on $V_{O(OUT)}$. See Figure 1**(b)**.		40	60		40	60	µs
t_{PLH1}	Turn-on propagation delay from an enable	$V_{I(IN1)}$ = $VI_{(IN2)}$ = 5 V Measured from enable to 10% of $V_{O(OUT)}$, $V_{I(SNS)}$ = 1.5 V	T_J = 25°C, C_L = 10 µF, I_L = 500 mA; see Figure 1**(a)**.		0.5			1		ms
t_{PHL1}	Turn-off propagation delay from a disable	$V_{I(IN1)}$ = $VI_{(IN2)}$ = 5 V Measured from disable to 90% of $V_{O(OUT)}$, $V_{I(SNS)}$ = 1.5 V	T_J = 25°C, C_L = 10 µF, I_L = 500 mA; see Figure 1**(a)**.		3			5		ms
t_{PLH2}	Switch-over rising propagation delay	Logic 1 to Logic 0 transition on VSNS, $V_{I(IN1)}$ = 1.5 V, $V_{I(IN2)}$ = 5 V, $V_{I(\overline{EN})}$ = 0 V, Measured from VSNS to 10% of $V_{O(OUT)}$	T_J = 25°C, C_L = 10 µF, I_L = 500 mA; see Figure 1**(c)**.		40	100		40	100	µs
t_{PHL2}	Switch-over falling propagation delay	Logic 0 to Logic 1 transition on VSNS, $V_{I(IN1)}$ = 1.5 V, $V_{I(IN2)}$ = 5 V, $V_{I(\overline{EN})}$ = 0 V, Measured from VSNS to 90% of $V_{O(OUT)}$	T_J = 25°C, C_L = 10 µF, I_L = 500 mA; see Figure 1**(c)**.	2	3	10	2	5	10	ms

PARAMETER MEASUREMENT INFORMATION

TIMING WAVEFORMS

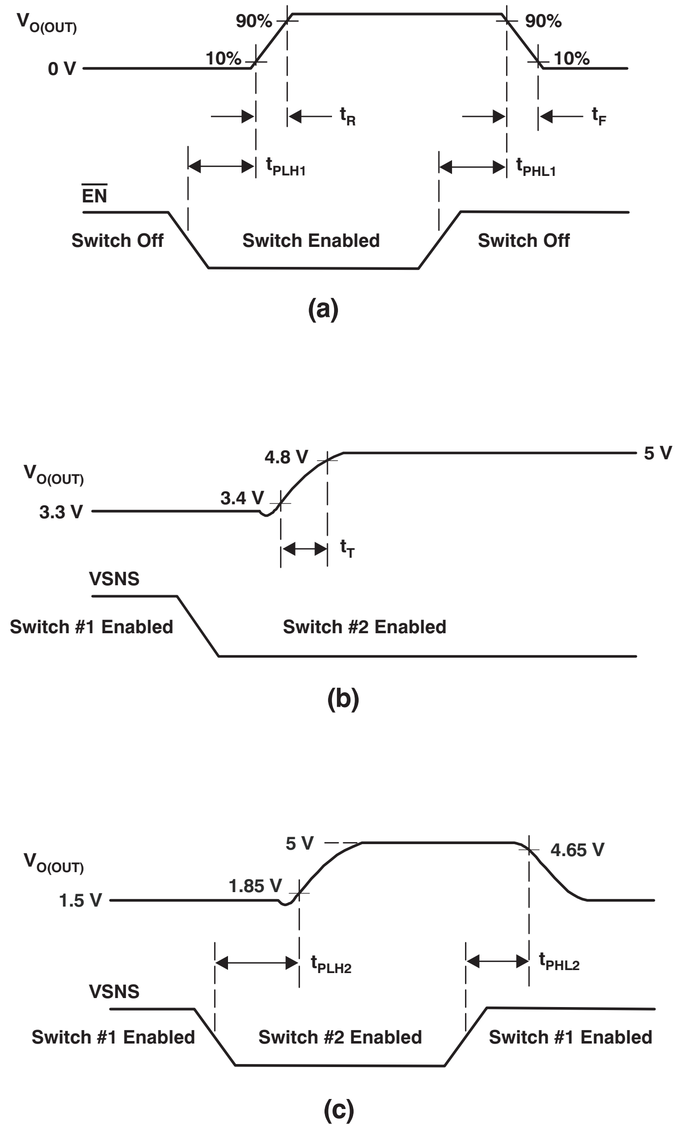


Figure 1. Propagation Delays and Transition Timing Waveforms

DEVICE INFORMATION

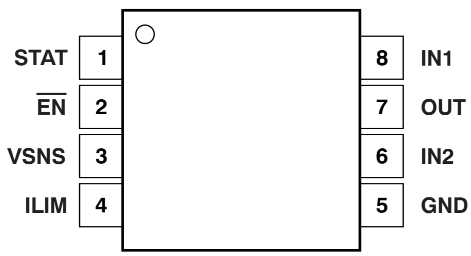
TRUTH TABLE

$\overline{EN}$	$V_{I(VSNS)}$ > 0.8 V (1)	$V_{I(IN2)} > V_{I(IN1)}$	STAT	OUT (2)
0	Yes	X	0	IN1
0	No	No	0	IN1
0	No	Yes	Hi-Z	IN2
1	X	X	0	Hi-Z

(1) X = Don't care.
(2) The undervoltage lockout circuit causes the output (OUT) to go Hi-Z if the selected power supply does not exceed the IN1/IN2 UVLO, or if neither of the supplies exceeds the internal V_{DD} UVLO.

PIN CONFIGURATIONS

PW PACKAGE
TSSOP-8
(TOP VIEW)



DRB PACKAGE
SON-8
(TOP VIEW)

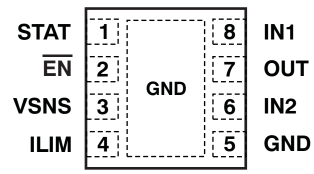
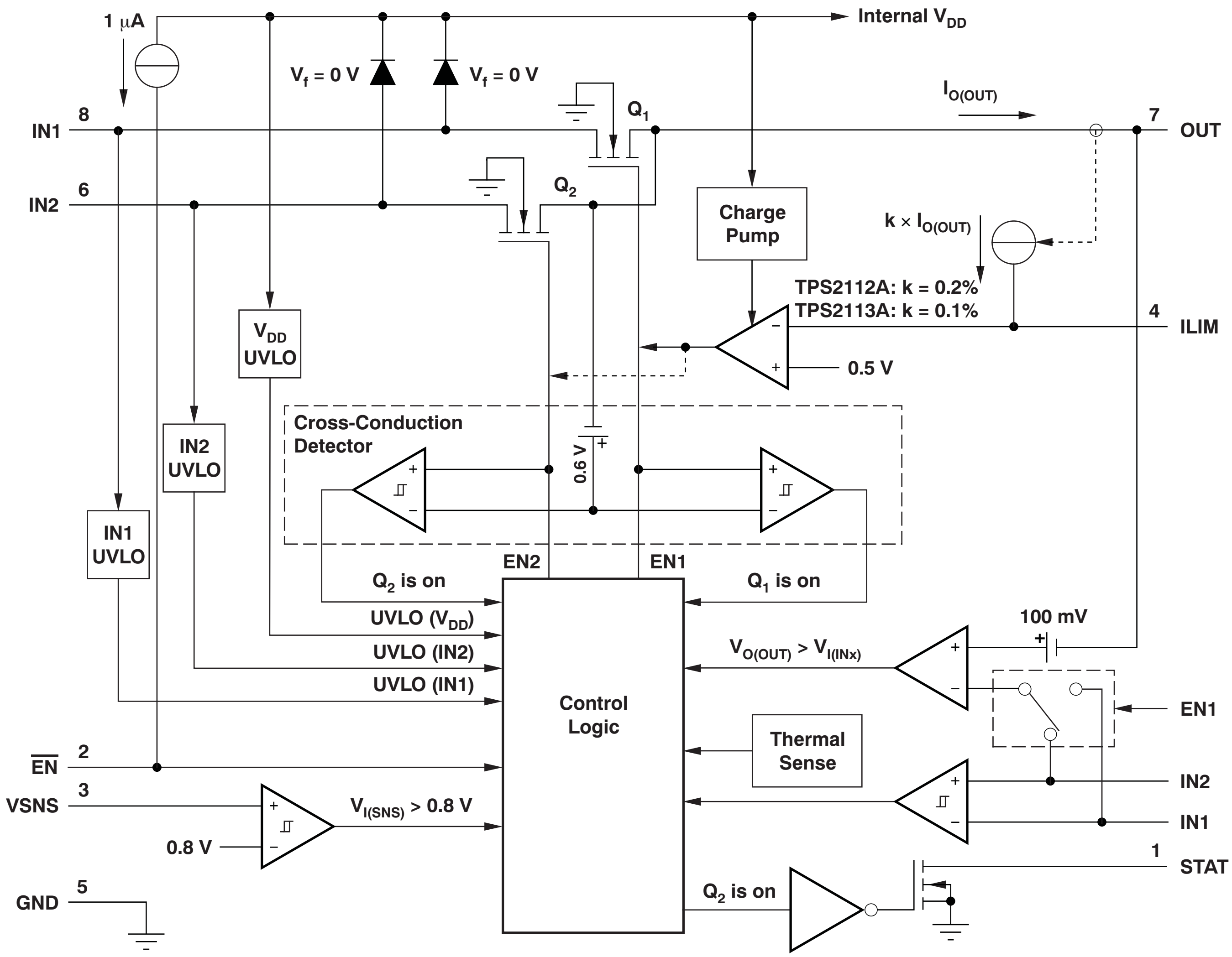


Table 1. TERMINAL FUNCTIONS

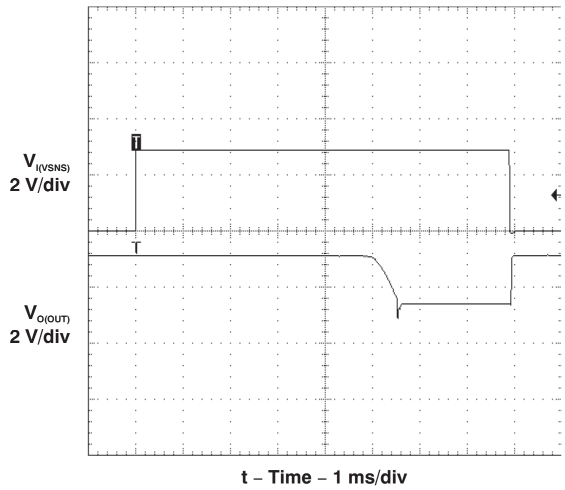
TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN}$	2	I	TTL- and CMOS-compatible input with a 1-μA pull-up. The Truth Table illustrates the functionality of $\overline{EN}$.
GND	5	Power	Ground
IN1	8	I	Primary power switch input. The IN1 switch can be enabled only if the IN1 supply is above the UVLO threshold and at least one supply exceeds the internal V_{DD} UVLO.
IN2	6	I	Secondary power switch input. The IN2 switch can be enabled only if the IN2 supply is above the UVLO threshold and at least one supply exceeds the internal V_{DD} UVLO.
ILIM	4	I	A resistor (R_{ILIM}) from ILIM to GND sets the current limit (I_L) to 250/R_{ILIM} and 500/R_{ILIM} for the TPS2112A and TPS2113A, respectively.
OUT	7	O	Power switch output
STAT	1	O	STAT is an open-drain output that is Hi-Z if the IN2 switch is ON. STAT pulls low if the IN1 switch is ON or if OUT is Hi-Z (that is, $\overline{EN}$ is equal to logic '0')
VSNS	3	I	An internal power FET connects OUT to IN1 if the VSNS voltage is greater than 0.8 V. Otherwise, the FET connects OUT to the higher of IN1 and IN2. The Truth Table illustrates the functionality of VSNS.
Pad	—	Power	**DRB package only.** Connect to GND. Must be connected to large copper area in order to meet stated package dissipation ratings.

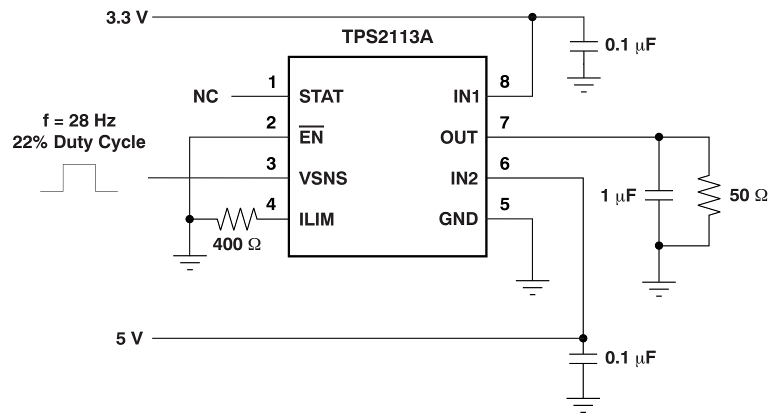
FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

OUTPUT SWITCHOVER RESPONSE

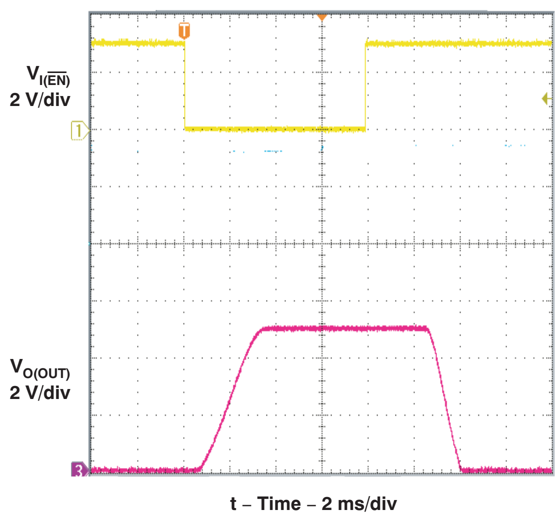


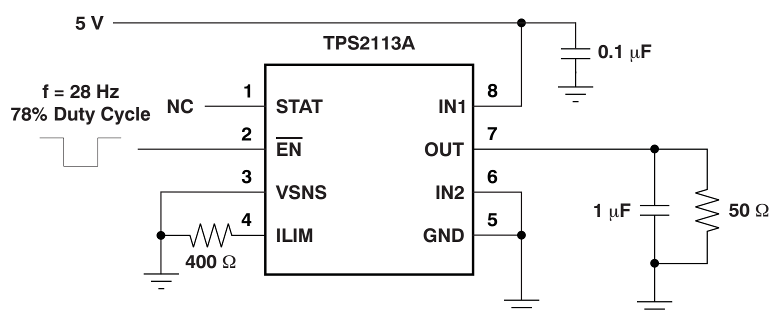


Output Switchover Response Test Circuit

Figure 2.

OUTPUT TURN-ON RESPONSE



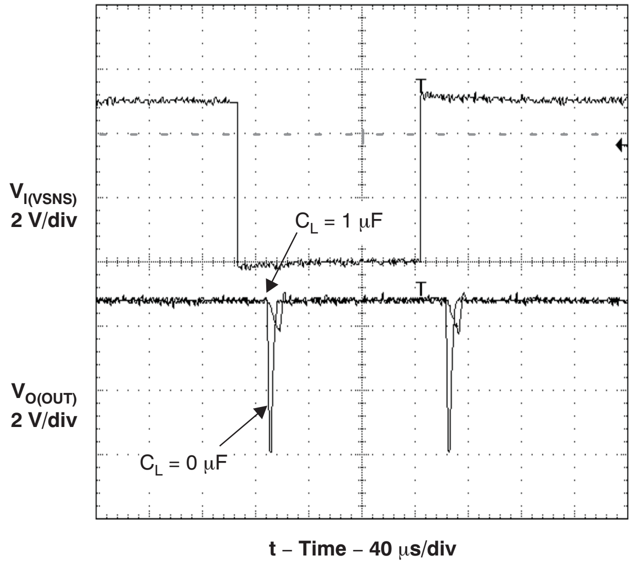


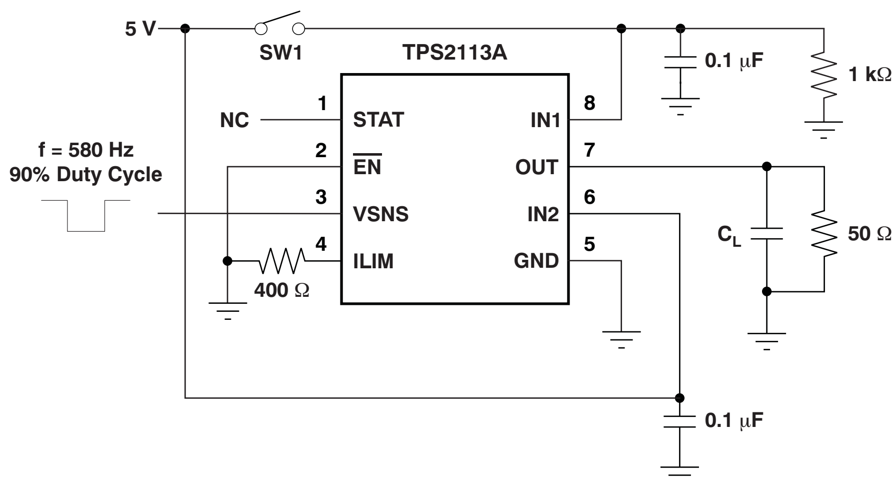
Output Turn-On Response Test Circuit

Figure 3.

TYPICAL CHARACTERISTICS (continued)

OUTPUT SWITCHOVER VOLTAGE DROOP





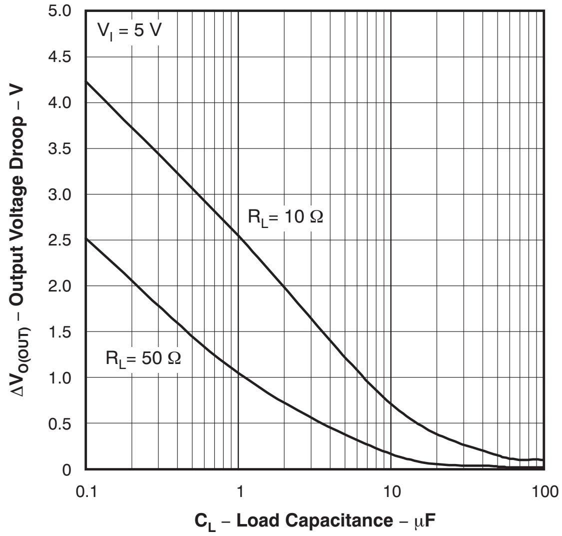
Output Switchover Voltage Droop Test Circuit

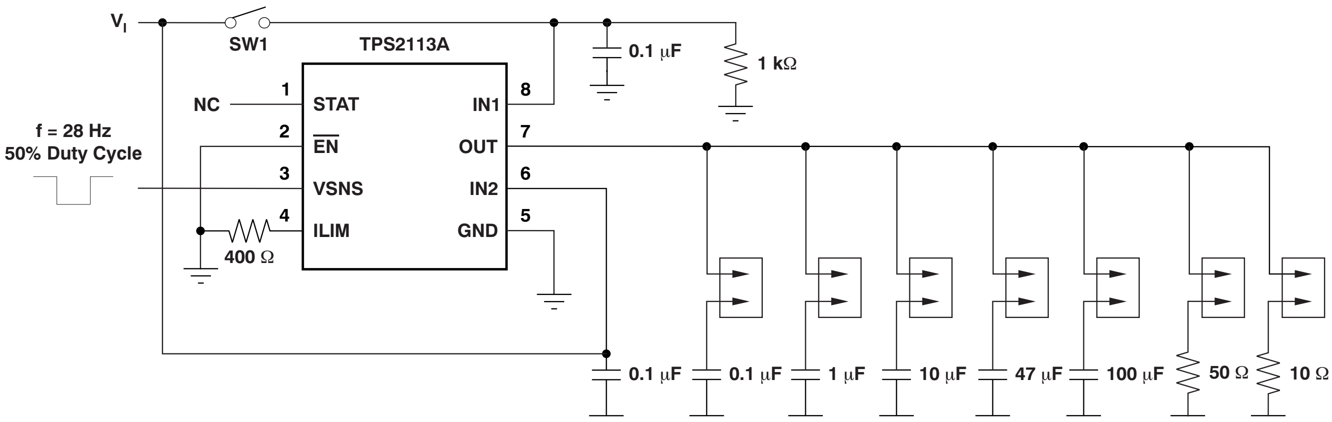
Figure 4.

Note: To initialize the TPS2113A for this test, set input VSNS equal to 0 V, turn on the 5-V supply, and then turn on switch SW1.

TYPICAL CHARACTERISTICS (continued)

OUTPUT SWITCHOVER VOLTAGE DROOP vs LOAD CAPACITANCE





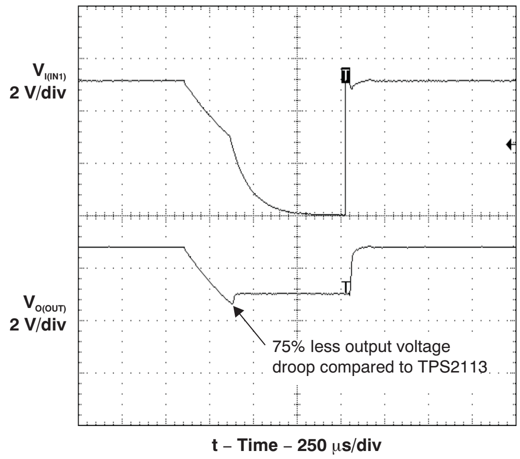
Output Switchover Voltage Droop Test Circuit

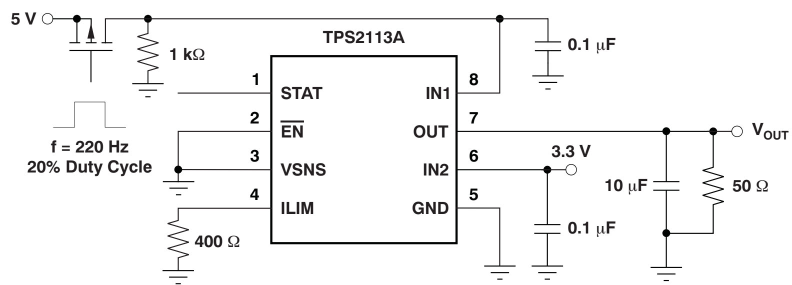
Figure 5.

Note: To initialize the TPS2113A for this test, set input VSNS equal to 0 V, turn on the V_I supply, and then turn on switch SW1.

TYPICAL CHARACTERISTICS (continued)

AUTO SWITCHOVER VOLTAGE DROOP



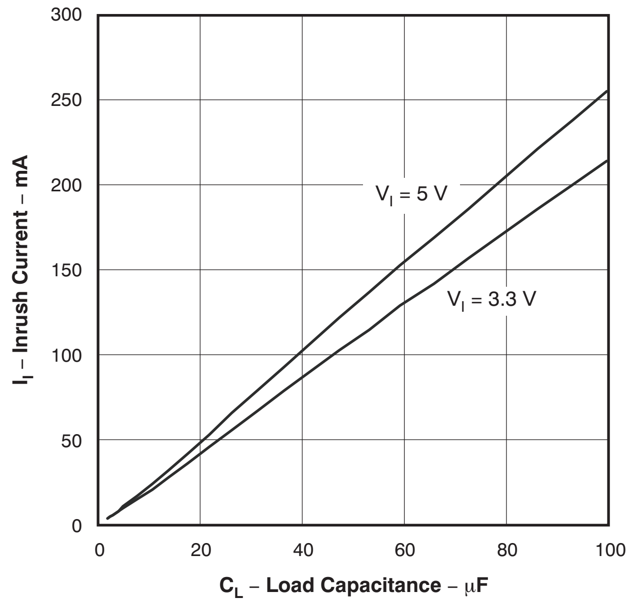


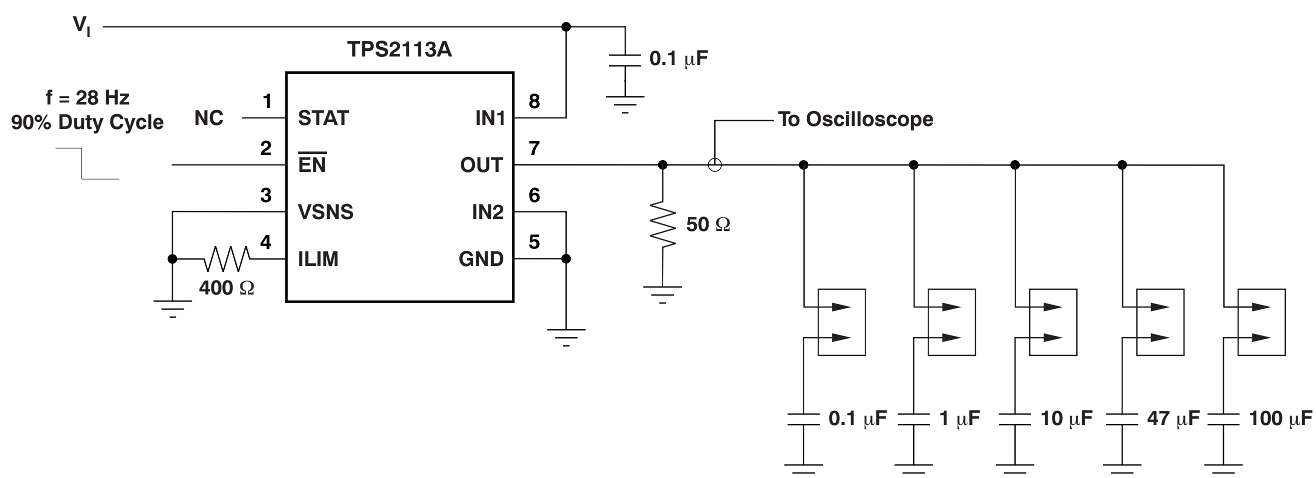
Auto Switchover Voltage Droop Test Circuit

Figure 6.

TYPICAL CHARACTERISTICS (continued)

**INRUSH CURRENT
vs
LOAD CAPACITANCE**





Output Capacitor Inrush Current Test Circuit

Figure 7.

TYPICAL CHARACTERISTICS (continued)

SWITCH ON-RESISTANCE vs JUNCTION TEMPERATURE

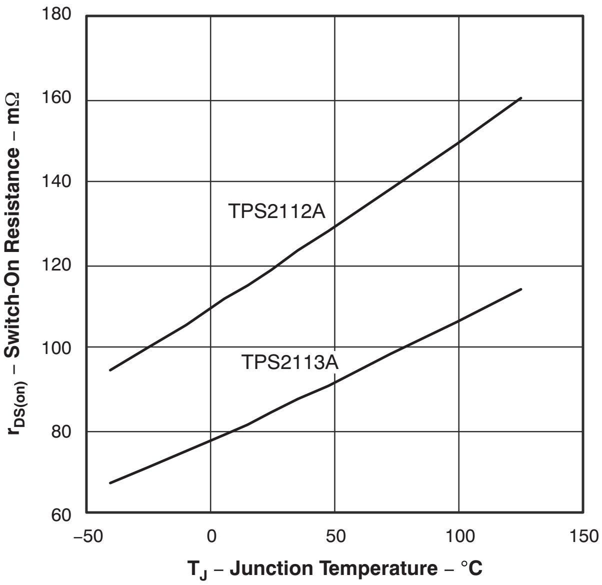


Figure 8.

SWITCH ON-RESISTANCE vs SUPPLY VOLTAGE

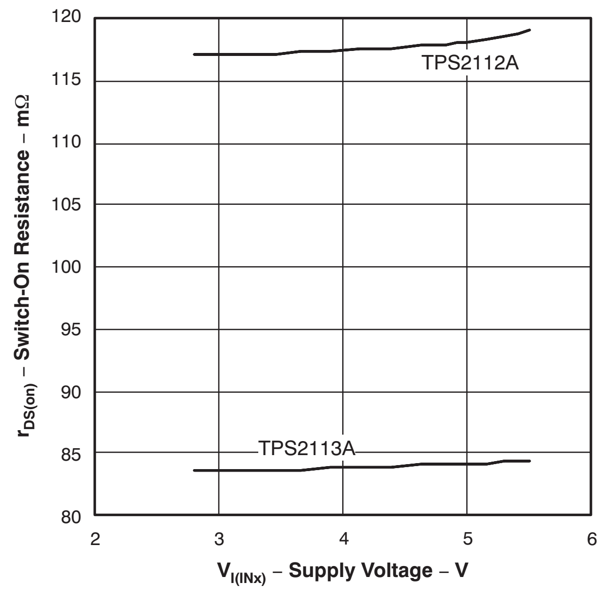


Figure 9.

IN1 SUPPLY CURRENT vs SUPPLY VOLTAGE

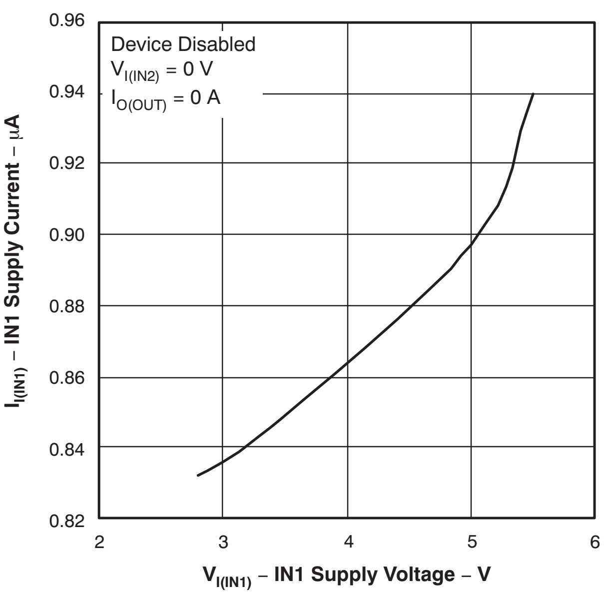


Figure 10.

IN1 SUPPLY CURRENT vs SUPPLY VOLTAGE

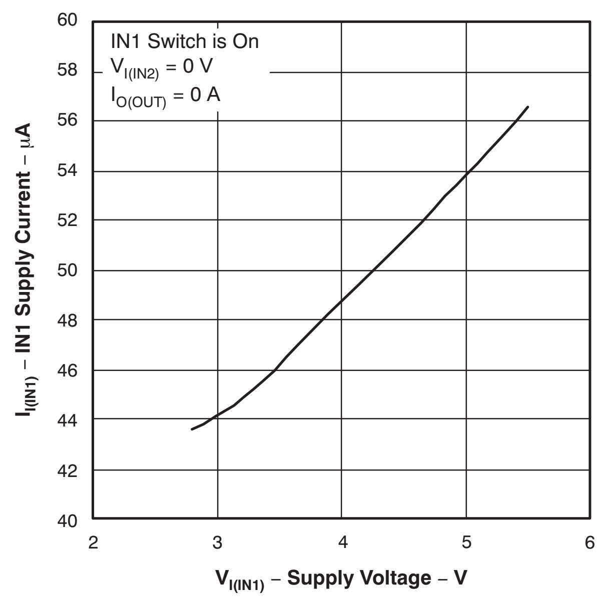


Figure 11.

TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT
vs
JUNCTION TEMPERATURE

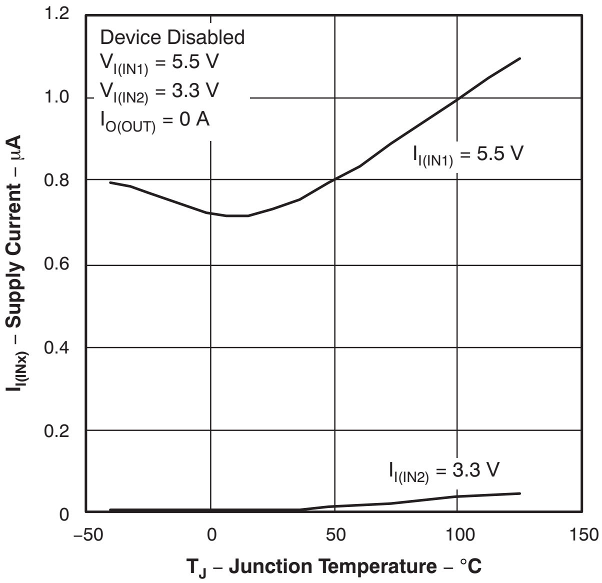


Figure 12.

SUPPLY CURRENT
vs
JUNCTION TEMPERATURE

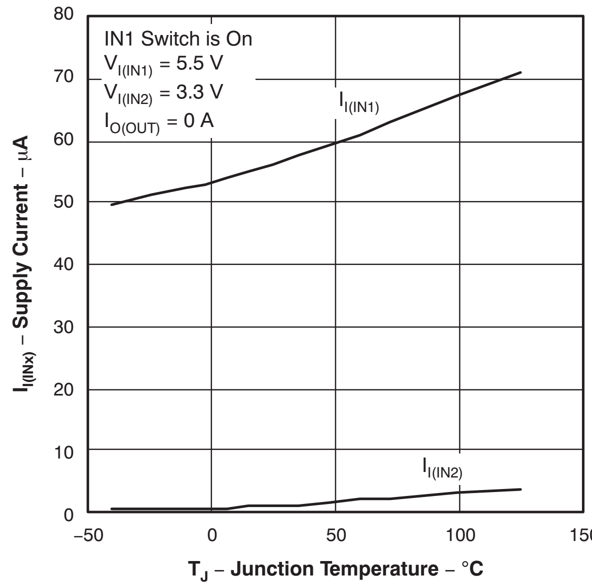


Figure 13.

APPLICATION INFORMATION

Some applications have two energy sources, one of which should be used in preference to another. Figure 14 shows a circuit that will connect IN1 to OUT until the voltage at IN1 falls below a user-specified value. Once the voltage on IN1 falls below this value, the TPS2112A/3A will select the higher of the two supplies. This usually means that the TPS2112A/3A will swap to IN2.

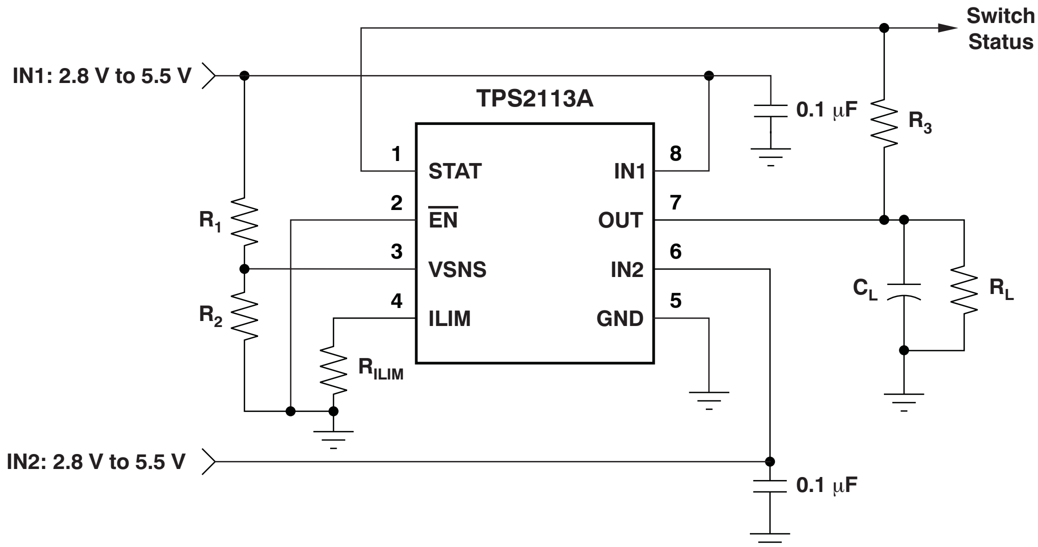


Figure 14. Auto-Selecting for a Dual Power-Supply Application

In Figure 15, the multiplexer selects between two power supplies based upon the VSNS logic signal. OUT connects to IN1 if VSNS is logic '1'; otherwise, OUT connects to IN2 if V_{IN2} is greater than V_{IN1}. The logic thresholds for the VSNS terminal are compatible with both TTL and CMOS logic.

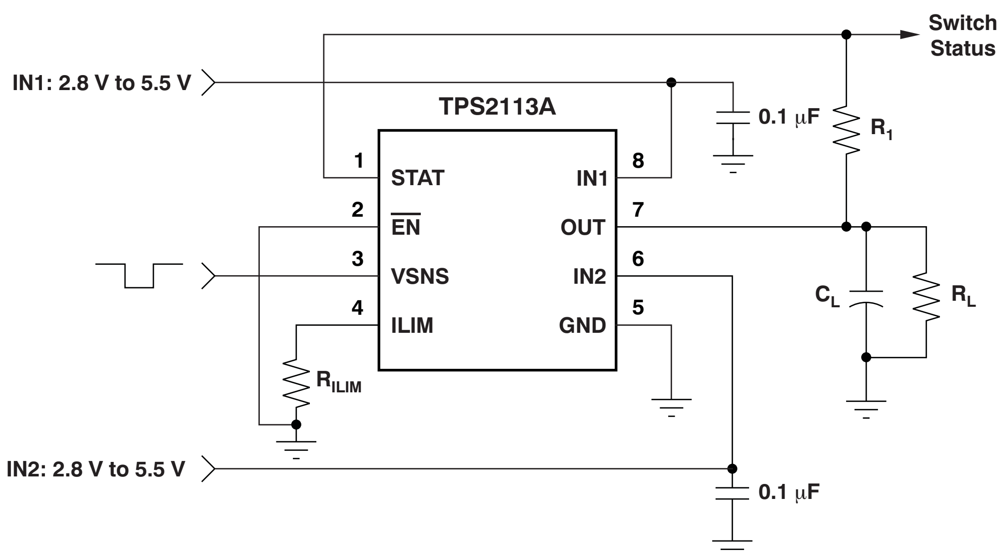


Figure 15. Manually Switching Power Sources

DETAILED DESCRIPTION

AUTO-SWITCHING MODE

The TPS2112A/3A only supports the auto-switching mode. In this mode, OUT connects to IN1 if $V_{I(VSNS)}$ is greater than 0.8 V, otherwise OUT connects to the higher of IN1 and IN2.

The VSNS terminal includes hysteresis equal to 3.75% to 7.5% of the threshold selected for transition from the primary supply to the higher of the two supplies. This hysteresis helps avoid repeated switching from one supply to the other due to resistive drops.

N-CHANNEL MOSFETs

Two internal high-side power MOSFETs implement a single-pole double-throw (SPDT) switch. Digital logic selects the IN1 switch, IN2 switch, or no switch (Hi-Z state). The MOSFETs have no parallel diodes so output-to-input current cannot flow when the FET is off. An integrated comparator prevents turn-on of a FET switch if the output voltage is greater than the input voltage.

CROSS-CONDUCTION BLOCKING

The switching circuitry ensures that both power switches will never conduct at the same time. A comparator monitors the gate-to-source voltage of each power FET and allows a FET to turn on only if the gate-to-source voltage of the other FET is below the turn-on threshold voltage.

REVERSE-CONDUCTION BLOCKING

When the TPS211xA switches from a higher-voltage supply to a lower-voltage supply, current can potentially flow back from the load capacitor into the lower-voltage supply. To minimize such reverse conduction, the TPS211xA will not connect a supply to the output until the output voltage has fallen to within 100 mV of the supply voltage. Once a supply has been connected to the output, it will remain connected regardless of output voltage.

CHARGE PUMP

The higher of supplies IN1 and IN2 powers the internal charge pump. The charge pump provides power to the current limit amplifier and allows the output FET gate voltage to be higher than the IN1 and IN2 supply voltages. A gate voltage that is higher than the source voltage is necessary to turn on the N-channel FET.

CURRENT LIMITING

A resistor R_{ILIM} from ILIM to GND sets the current limit to $250/R_{ILIM}$ and $500/R_{ILIM}$ for the TPS2112A and TPS2113A, respectively. Setting resistor R_{ILIM} equal to zero is not recommended as that disables current limiting.

OUTPUT VOLTAGE SLEW-RATE CONTROL

The TPS2112A/3A slews the output voltage at a slow rate when OUT switches to IN1 or IN2 from the Hi-Z state (see the Truth Table). A slow slew rate limits the inrush current into the load capacitor. High inrush currents can glitch the voltage bus and cause a system to hang up or reset. It can also cause reliability issues—like pit the connector power contacts, when hot-plugging a load such as a PCI card. The TPS2112A/3A slews the output voltage at a much faster rate when OUT switches between IN1 and IN2. The fast rate minimizes the output voltage droop and reduces the output voltage hold-up capacitance requirement.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2010) to Revision C **Page**

- Changed description of power supplies in *Description* section ... 1
- Changed *Current Limit Adjustment Range* parameter TPS2113A and TPS2115A specifications in Available Options table ... 2
- Added I_{OUT} column to Device Information table, changed table name ... 2
- Changed *Continuous output current* parameter in Absolute Maximum Ratings table ... 2
- Changed *Current limit adjustment range* parameter in Recommended Operating Conditions table ... 3
- Added footnote 1 to Recommended Operating Conditions table ... 3
- Changed second paragraph in *Application Information* section ... 16

Changes from Revision A (February, 2006) to Revision B **Page**

- Updated document to current format ... 1
- Deleted package information from *Available Options* table ... 2
- Revised *Ordering Information* table ... 2
- Deleted *storage temperature*, *operating virtual junction temperature range,* and *lead temperature* specifications from, added *electrostatic discharge* and *junction temperature* specifications to Absolute Maximum Ratings table; deleted *ESD Protection* table ... 2
- Added DRB package information and footnote to *Dissipation Ratings* table ... 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2112APW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2112A	Samples
TPS2112APWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2112A	Samples
TPS2113ADRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PTOI	Samples
TPS2113ADRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PTOI	Samples
TPS2113APW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2113A	Samples
TPS2113APWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2113A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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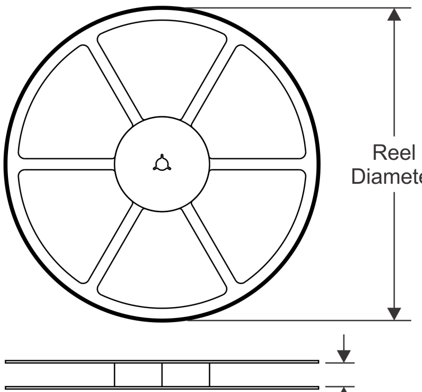
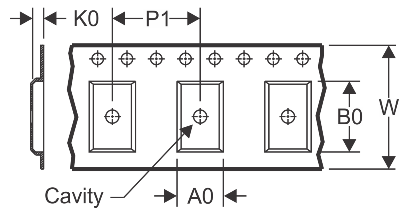
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

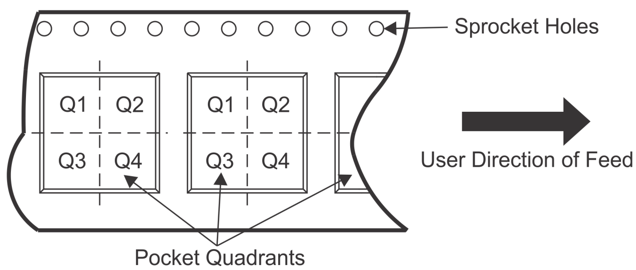


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

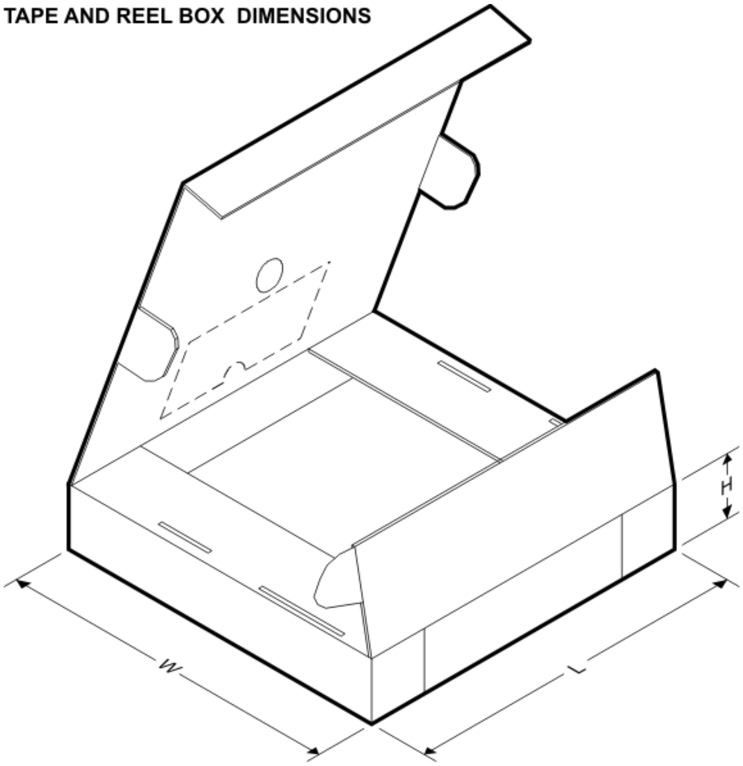
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2113ADRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2113ADRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

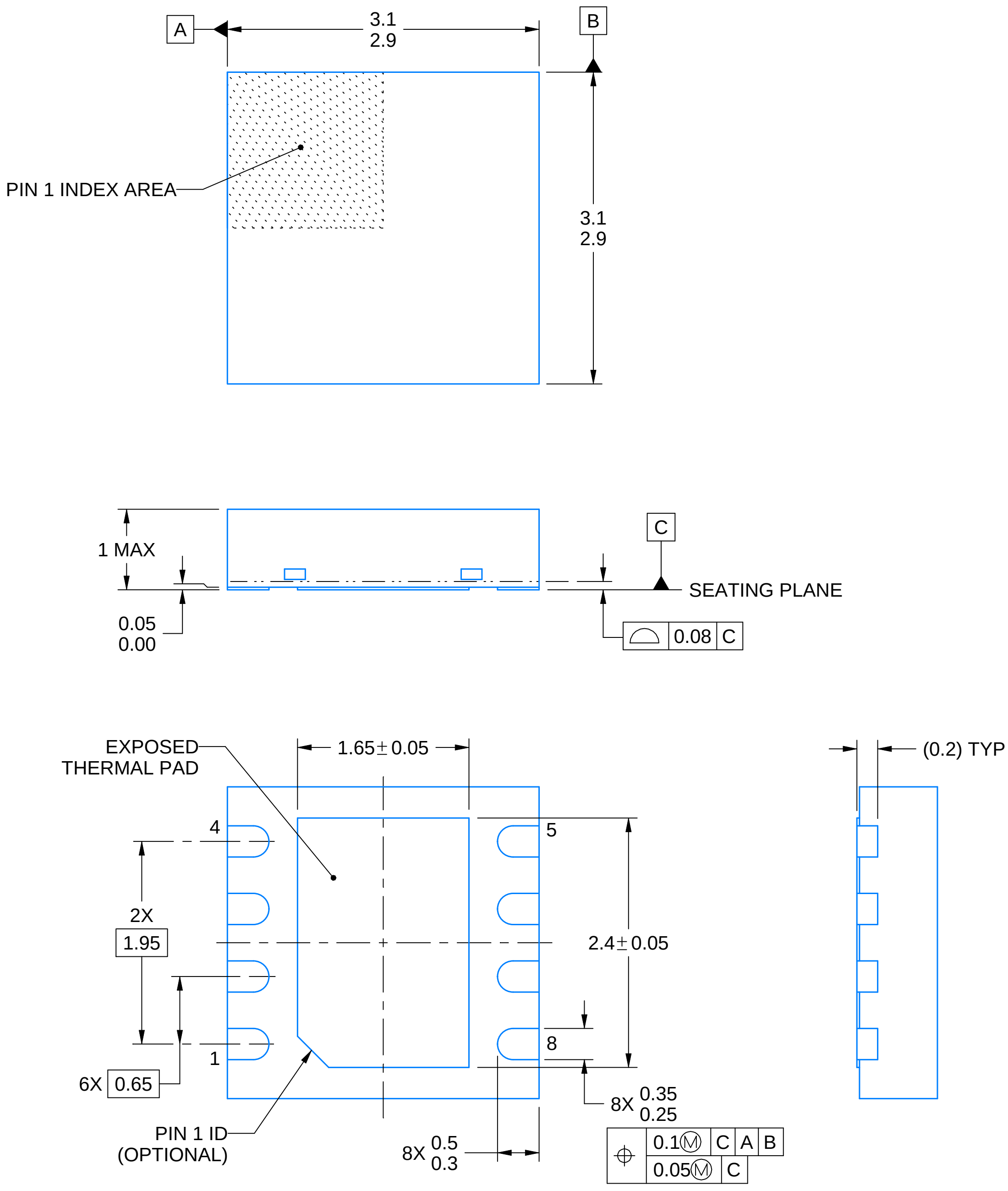
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2113ADRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS2113ADRBT	SON	DRB	8	250	210.0	185.0	35.0

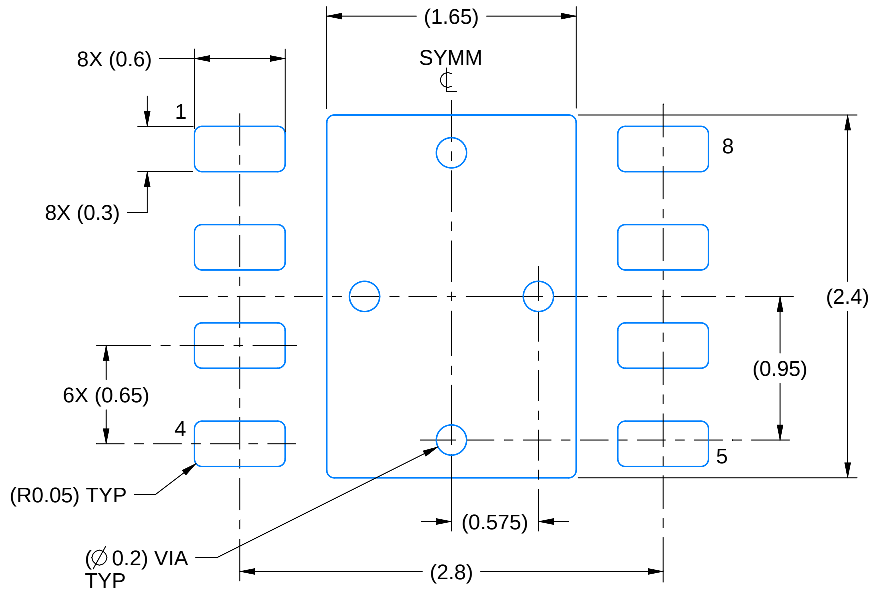
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



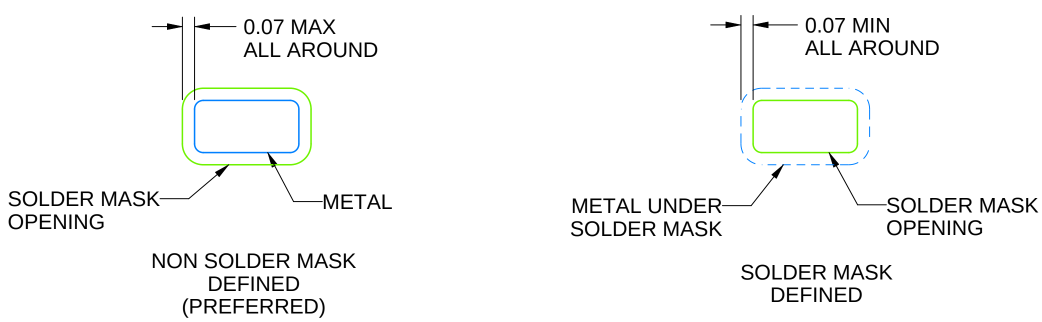
4218876/A 12/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

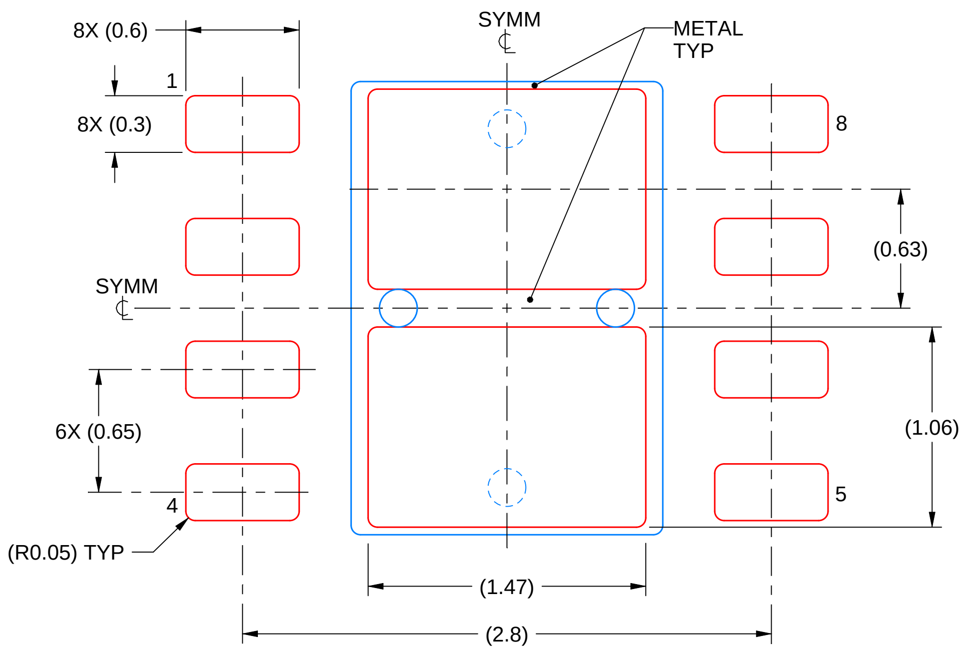


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



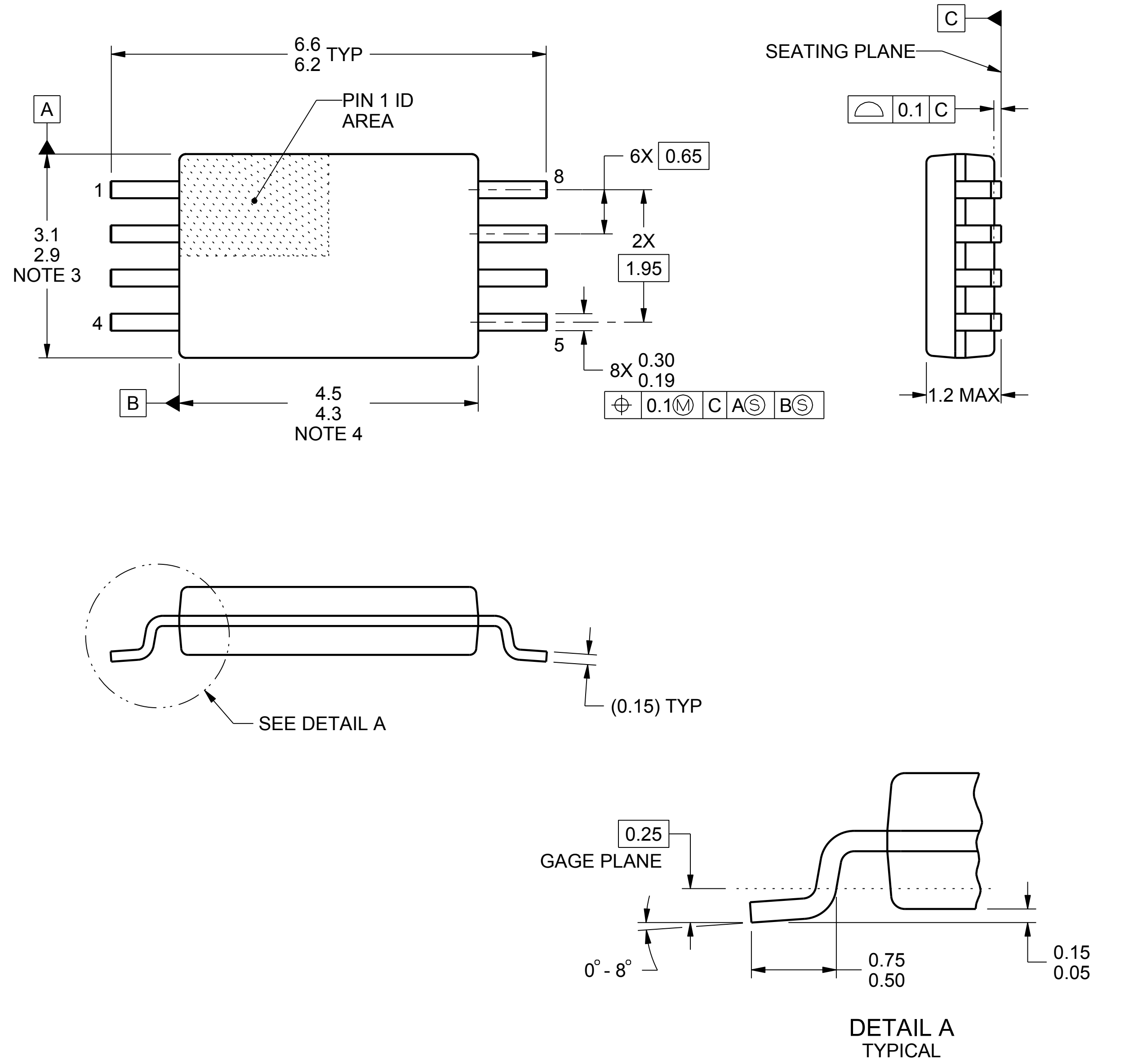
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

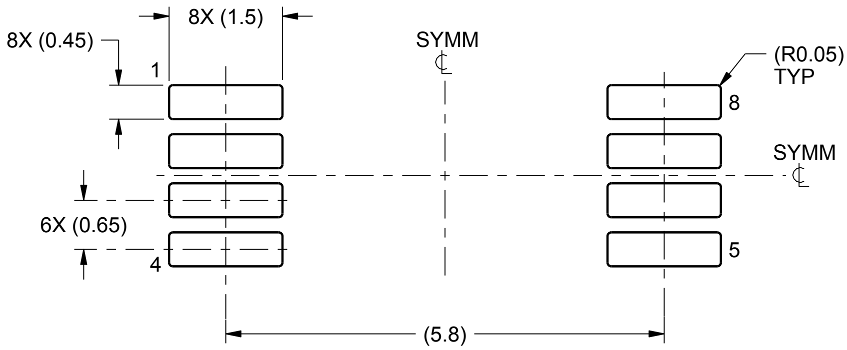
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



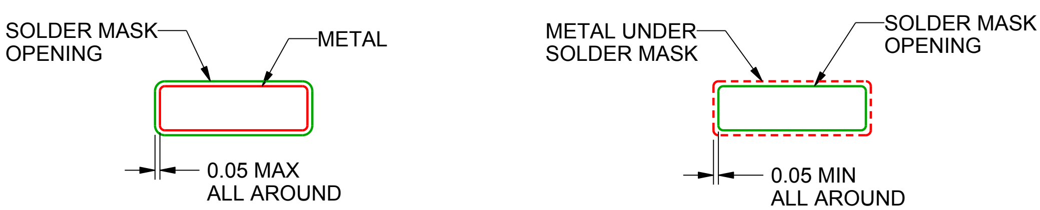
4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

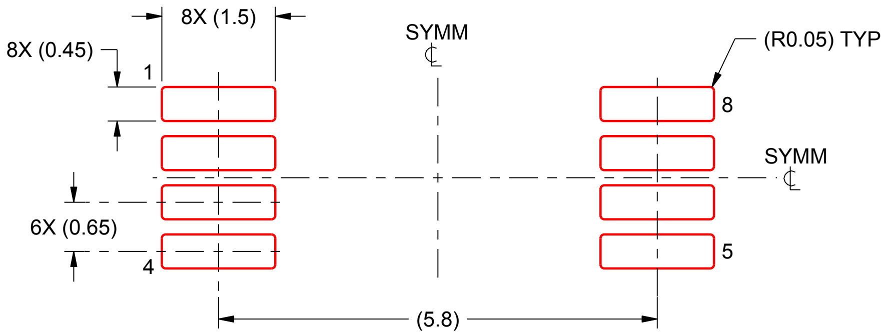
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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