PSMN3R5-30YL

N-channel 30 V 3.5 mΩ logic level MOSFET in LFPAK

3 August 2018 Product data sheet

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in industrial and communications applications.

2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

3. Applications

- Class-D amplifiers
- DC-to-DC converters
- Motor control
- Server power supplies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	30	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	100	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	74	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A; T_j = 25 °C		-	2.43	3.5	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 10 A; V_{DS} = 12 V; V_{GS} = 4.5 V; Fig. 14; Fig. 15		-	5	-	nC
$Q_{G(tot)}$	total gate charge			-	19	-	nC
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 100 A; V_{sup} ≤ 30 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped		-	-	54	mJ

[1] Continuous current is limited by package.

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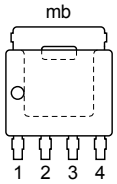
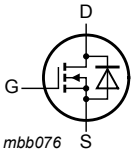
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK56; Power-SO8 (SOT669)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R5-30YL	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN3R5-30YL	3R530

8. Limiting values

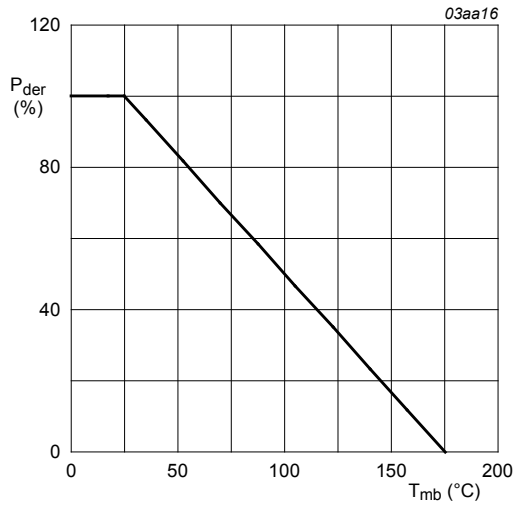
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	30	V
V_{DSM}	peak drain-source voltage	t_p ≤ 25 ns; f ≤ 500 kHz; $E_{DS(AL)}$ ≤ 180 nJ; pulsed		-	35	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	30	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	74	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2	[1]	-	86	A
		V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	100	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	447	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[1]	-	100	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	447	A
Avalanche ruggedness						

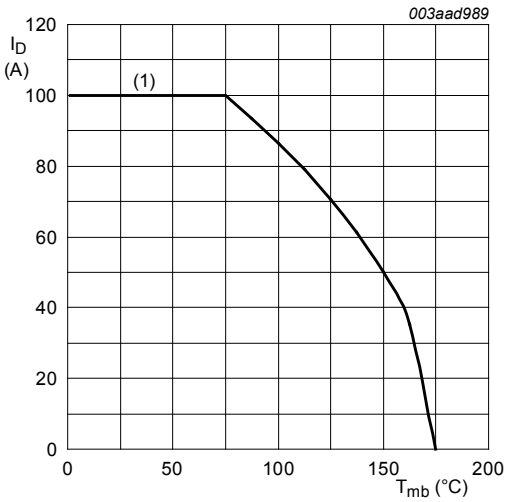
Symbol	Parameter	Conditions		Min	Max	Unit
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 100 A; $V_{sup} \leq$ 30 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped		-	54	mJ

[1] Continuous current is limited by package.



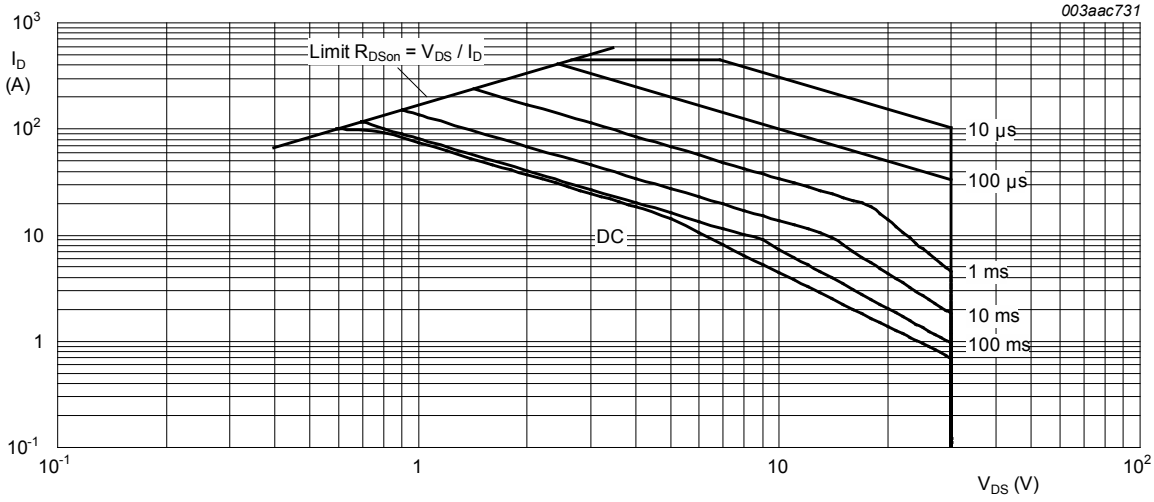
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 10$ V; (1) Capped at 100 A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature



$T_{mb} = 25$ °C; I_{DM} is single pulse

(1) Capped at 100 A due to package.

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	0.6	1.68	K/W

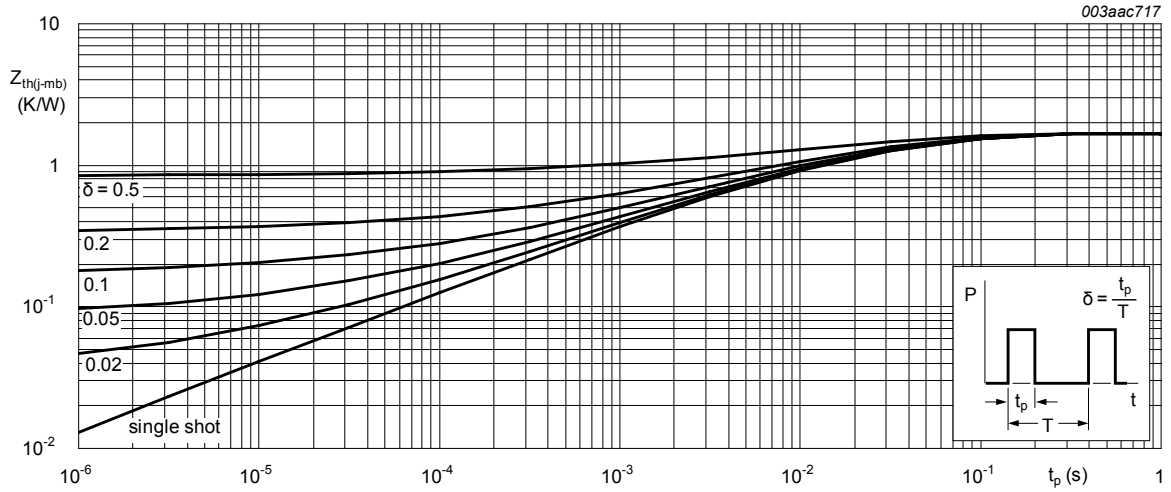


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

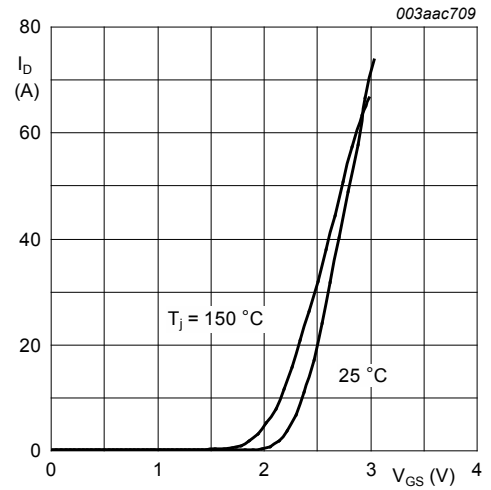
10. Characteristics

Table 7. Characteristics

Tested to JEDEC standards where applicable.

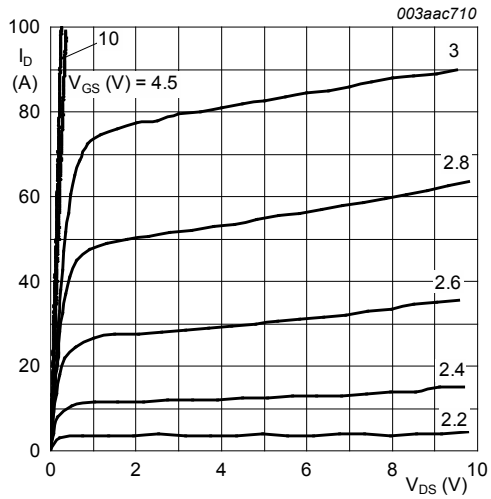
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		30	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 11; Fig. 12		1.3	1.7	2.15	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 150 °C; Fig. 12		0.65	-	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 12		-	-	2.45	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 °C		-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 15 A; T_j = 25 °C		-	3.37	4.61	mΩ
		V_{GS} = 10 V; I_D = 15 A; T_j = 150 °C; Fig. 13		-	-	6	mΩ
		V_{GS} = 10 V; I_D = 15 A; T_j = 25 °C		-	2.43	3.5	mΩ
R_G	gate resistance	f = 1 MHz		-	0.53	1.5	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 12 V; V_{GS} = 4.5 V; Fig. 14; Fig. 15		-	19	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	37	-	nC
		I_D = 10 A; V_{DS} = 12 V; V_{GS} = 10 V; Fig. 14; Fig. 15		-	41	-	nC
Q_{GS}	gate-source charge	I_D = 10 A; V_{DS} = 12 V; V_{GS} = 4.5 V; Fig. 14; Fig. 15		-	6	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	4	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	2	-	nC
Q_{GD}	gate-drain charge			-	5	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	V_{DS} = 12 V; Fig. 14; Fig. 15		-	2.4	-	V
C_{iss}	input capacitance	V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16		-	2458	3441	pF
C_{oss}	output capacitance			-	532	718	pF
C_{rss}	reverse transfer capacitance			-	252	353	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 12 V; R_L = 0.5 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 4.7 Ω		-	33	-	ns
t_r	rise time			-	50	-	ns
$t_{d(off)}$	turn-off delay time			-	45	-	ns
t_f	fall time			-	18	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17		-	0.82	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V		-	37	-	ns
Q_r	recovered charge			-	31	-	nC



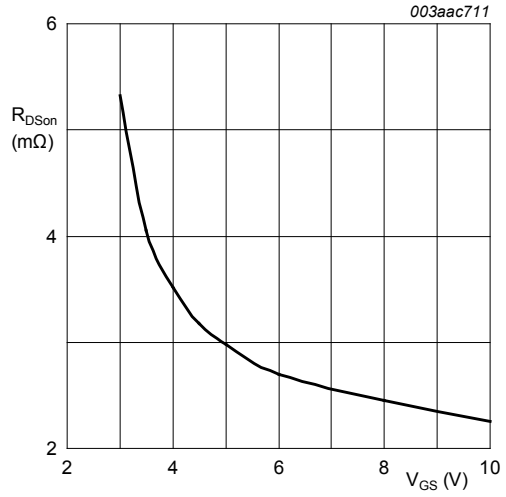
$V_{DS} = 10\ V$

Fig. 5. Transfer characteristics: drain current as a function of gate-source voltage; typical values



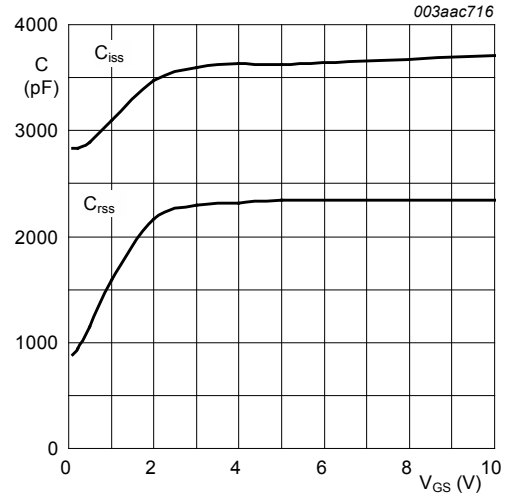
$T_j = 25\ °C; t_p = 300\ \mu s$

Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values



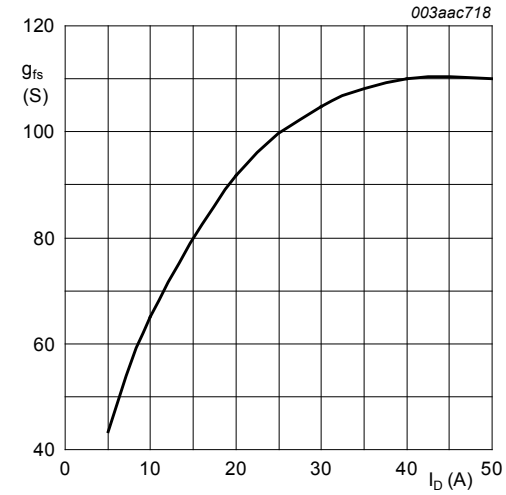
$T_j = 25\ °C; I_D = 15\ A$

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



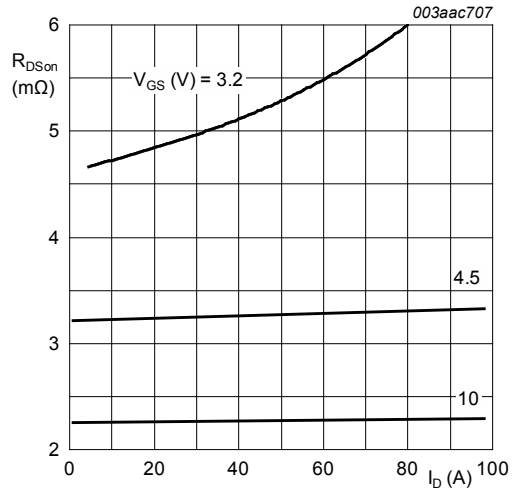
$V_{DS} = 0\ V; f = 1\ MHz$

Fig. 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



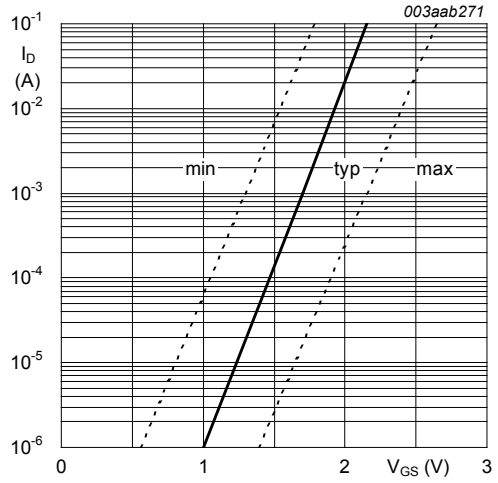
$T_j = 25\ °C; V_{DS} = 15\ V$

Fig. 9. Forward transconductance as a function of drain current; typical values



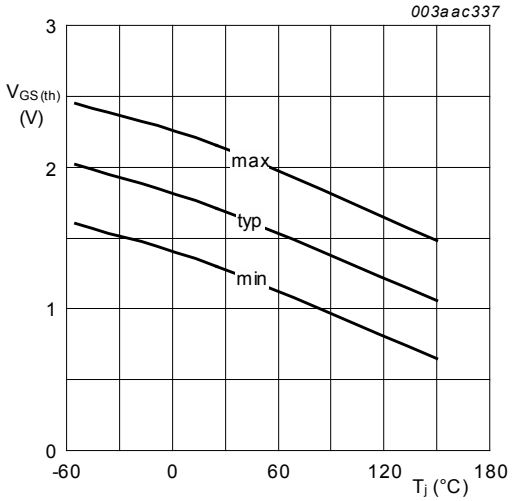
$T_j = 25\ °C; t_p = 300\ \mu s$

Fig. 10. Drain-source on-state resistance as a function of drain current; typical values



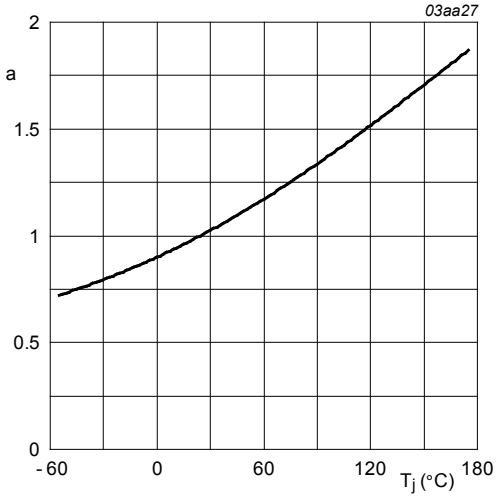
$T_j = 25\ °C; V_{DS} = 5\ V$

Fig. 11. Sub-threshold drain current as a function of gate-source voltage



$I_D = 1\,mA; V_{DS} = V_{GS}$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

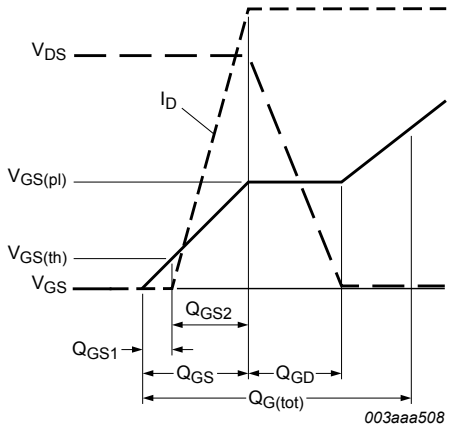
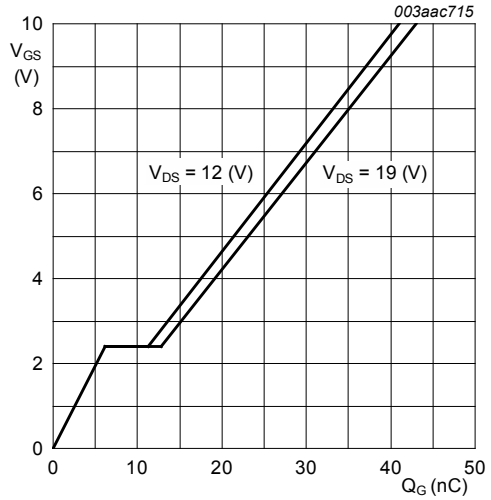
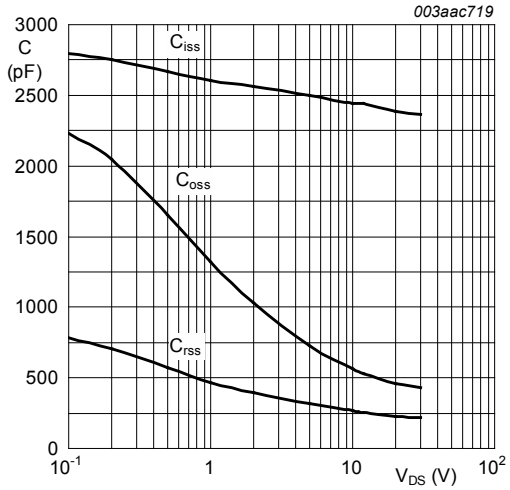


Fig. 14. Gate charge waveform definitions



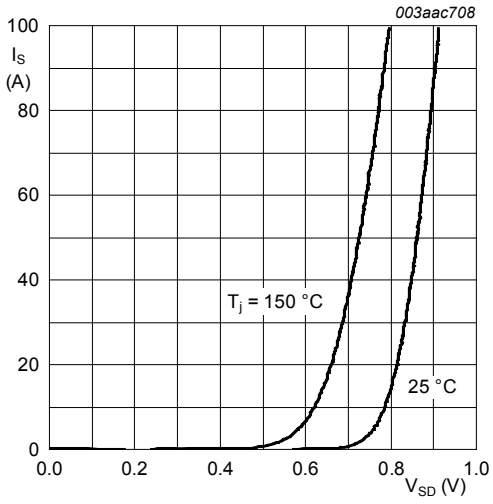
$T_j = 25\ °C; I_D = 10\ A$

Fig. 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\ V; f = 1\ MHz$

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

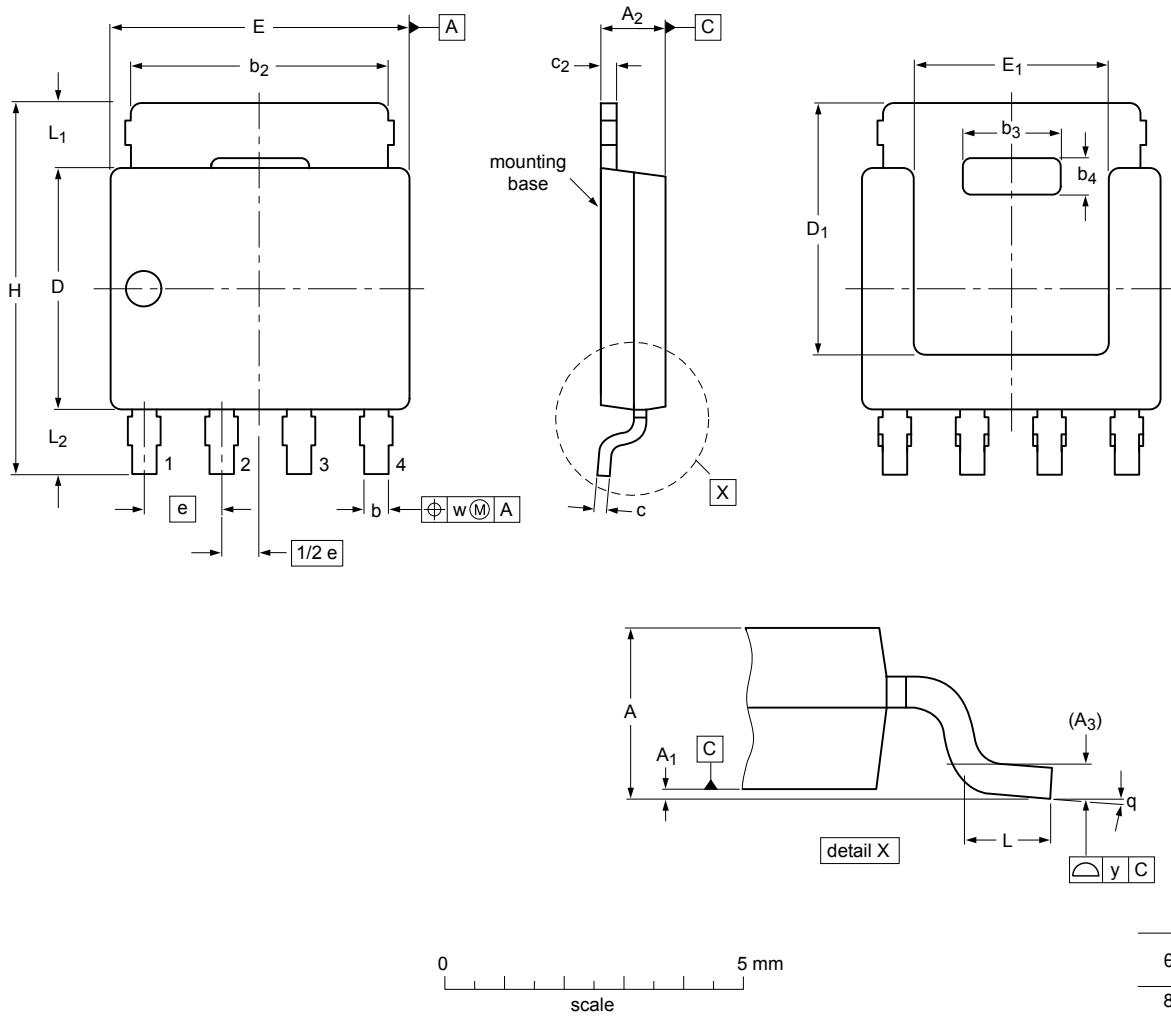


$V_{GS} = 0\ V$

Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads **SOT669**



θ
8°
0°

Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	$D^{(1)}$	$D_1{}^{(1)}$	$E^{(1)}$	$E_1{}^{(1)}$	e	H	L	L_1	L_2	w	y
mm	max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3		
	nom				0.25											1.27					0.25	0.1
	min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~11-03-25~~ 13-02-27

Fig. 18. Package outline LFPAK56; Power-SO8 (SOT669)

12. Soldering

Footprint information for reflow soldering **SOT669**

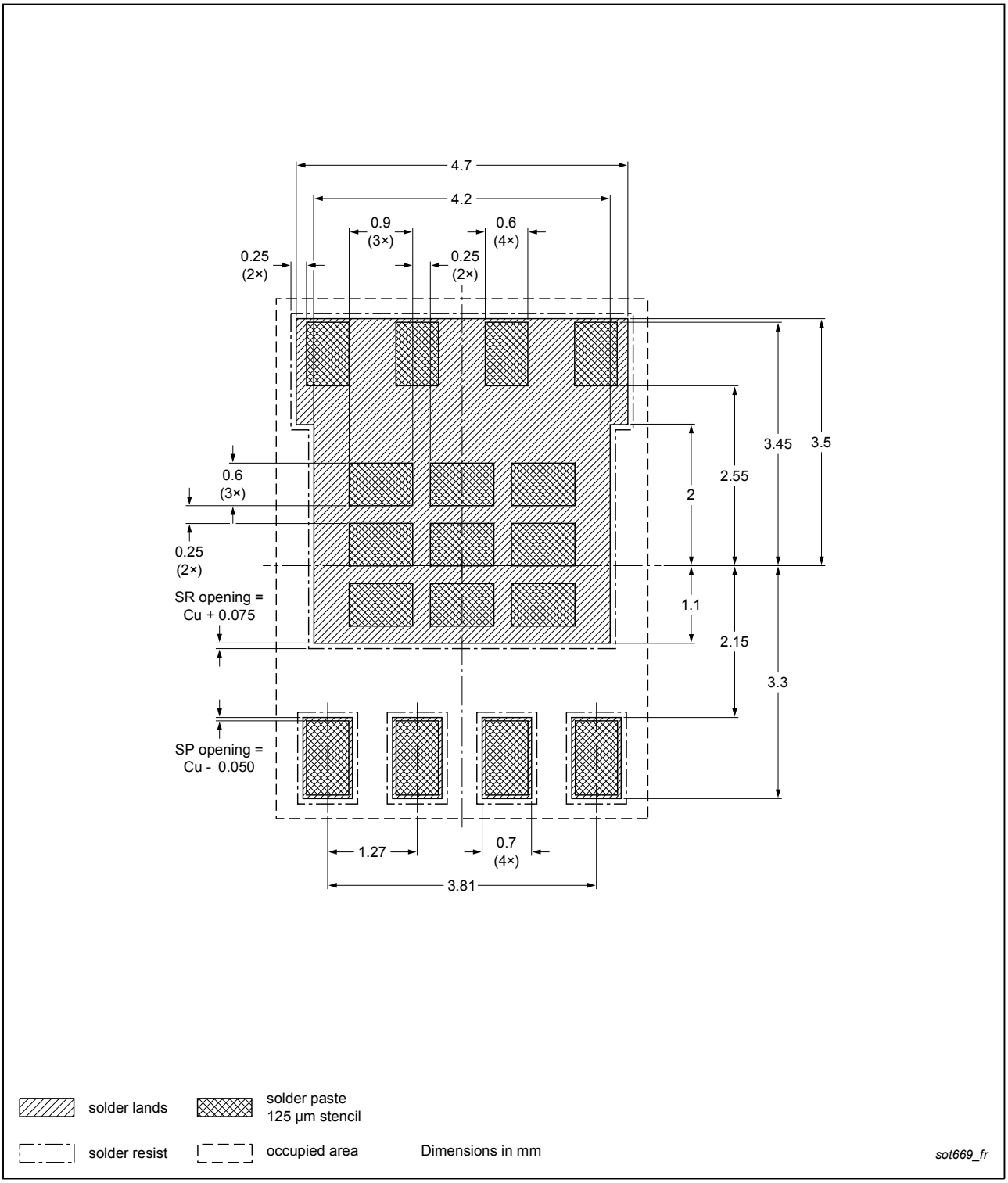


Fig. 19. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)

Wave soldering footprint information for LFPAK56 package **SOT669**

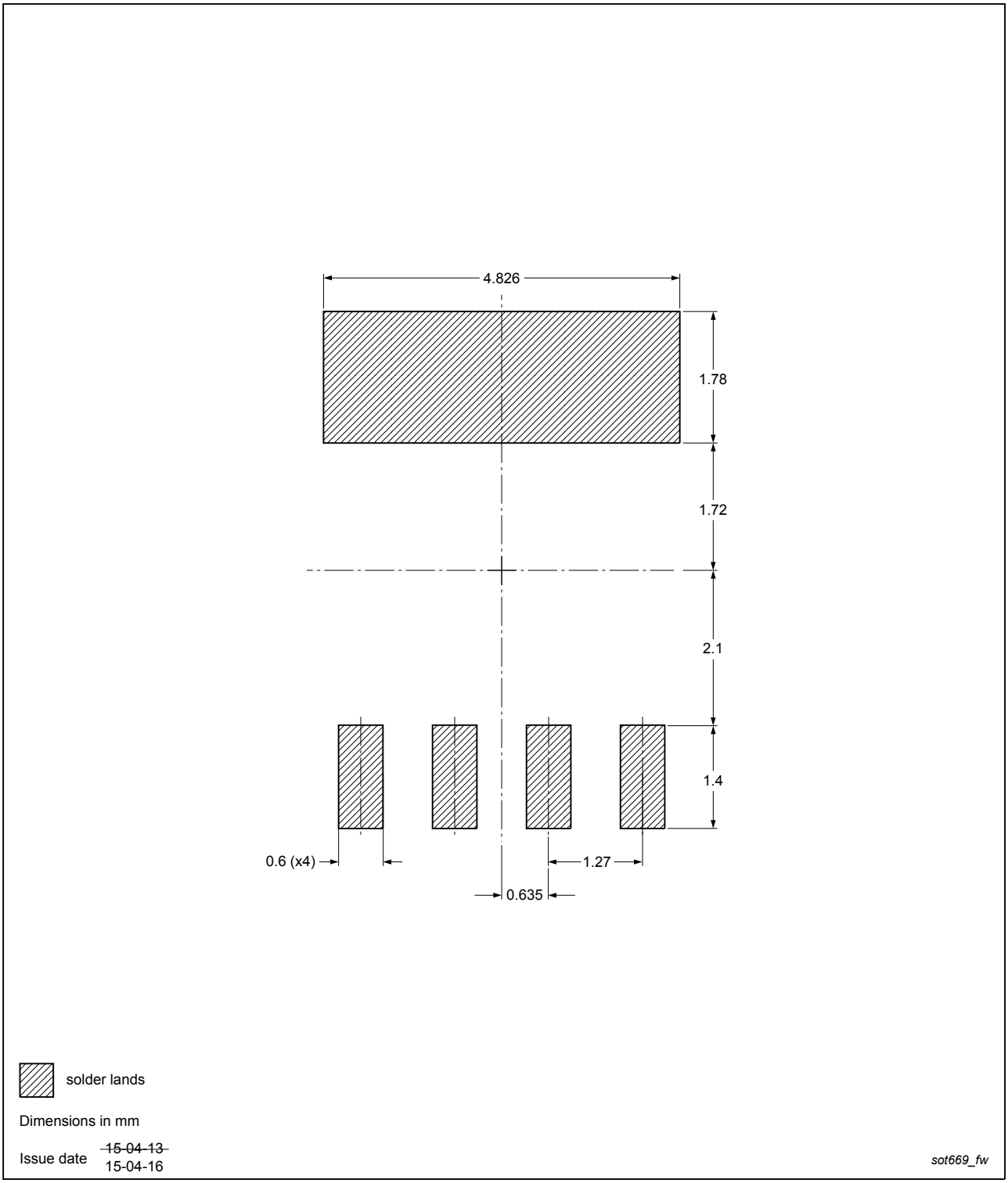


Fig. 20. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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