MC100EPT21

3.3V Differential LVPECL/LVDS/CML to LVTTL/LVCMOS Translator

The MC100EPT21 is a Differential LVPECL/LVDS/CML to LVTTL/LVCMOS translator. Because LVPECL (Positive ECL), LVDS, and positive CML input levels and LVTTL/LVCMOS output levels are used, only +3.3 V and ground are required. The small outline 8−lead SOIC package makes the EPT21 ideal for applications which require the translation of a clock or data signal.

The V_{BB} output allows this EPT21 to be cap coupled in either single−ended or differential input mode. When single−ended cap coupled, V_{BB} output is tied to the $\overline{D}$ input and D is driven for a non−inverting buffer, or V_{BB} output is tied to the D input and $\overline{D}$ is driven for an inverting buffer. When cap coupled differentially, V_{BB} output is connected through a resistor to each input pin. If used, the V_{BB} pin should be bypassed to V_{CC} via a 0.01 μF capacitor. For additional information see AND8020/D. For a single−ended direct connection use an external voltage reference source such as a resistor divider. Do not use V_{BB} for a single−ended direct connection or port to another device.

Features

- 1.4 ns Typical Propagation Delay
- Maximum Frequency > 275 MHz Typical
- LVPECL/LVDS/CML Inputs, LVTTL/LVCMOS Outputs
- 24 mA TTL outputs
- Operating Range: V_{CC} = 3.0 V to 3.6 V with GND = 0 V
- The 100 Series Contains Temperature Compensation
- V_{BB} Output
- These Devices are Pb−Free and are RoHS Compliant

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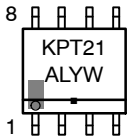
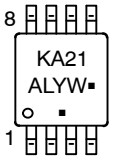
MARKING DIAGRAMS*

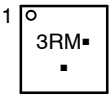
SO−8
D SUFFIX
CASE 751



TSSOP−8
DT SUFFIX
CASE 948R



DFN8
MN SUFFIX
CASE 506AA



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

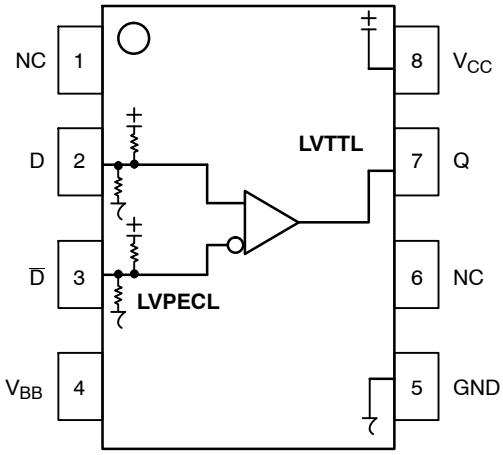


Figure 1. Logic Diagram and 8−Lead Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
Q	LVTTL/LVCMOS Output
D*, $\overline{D}$*	Differential LVPECL/LVDS/CML Input
V_{CC}	Positive Supply
V_{BB}	Output Reference Voltage
GND	Ground
NC	No Connect
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

* Pin will default to 1/2 of V_{CC} when left open.

Table 2. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor	D	50 kΩ
Internal Input Pulldown Resistor	$\overline{D}$	50 kΩ
Internal Input Pullup Resistor	D, $\overline{D}$	50 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 1.5 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	SOIC−8 TSSOP−8 DFN8	 Level 1 Level 3 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		81 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Power Supply	GND = 0 V		3.8	V
V_{IN}	PECL Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	0 to 3.8	V
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SO−8 SO−8	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	SO−8	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	TSSOP−8 TSSOP−8	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	TSSOP−8	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W °C/W
T_{sol}	Wave Solder Pb Pb−Free	< 2 to 3 sec @ 248°C <2 to 3 sec @ 260°C		265 265	°C
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board − 2S2P (2 signal, 2 power)

Table 4. PECL INPUT DC CHARACTERISTICS V_{CC} = 3.3 V, GND = 0.0 V (Note 3)

		−40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage (Single−Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single−Ended)	1355		1675	1355		1675	1355		1675	mV
V_{BB}	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	−150			−150			−150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input parameters vary 1:1 with V_{CC}.
4. V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 5. LVTTL/LVCMOS OUTPUT DC CHARACTERISTICS V_{CC} = 3.3 V, GND = 0.0 V, T_A = −40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.0 mA	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA			0.5	V
I_{CCH}	Power Supply Current	Outputs set to HIGH	5	17	25	mA
I_{CCL}	Power Supply Current	Outputs set to LOW	8	21	30	mA
I_{OS}	Output Short Circuit Current		−130		−80	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. AC CHARACTERISTICS V_{CC} = 3.0 V to 3.6 V, GND = 0.0 V (Note 5)

		−40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Frequency (Figure 2)	275	350		275	350		275	350		MHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	800 1200	1400 1400	2050 1800	800 1200	1400 1400	2250 1800	900 1100	1600 1300	2950 1900	ps
t_{SKEW}	Duty Cycle Skew (Note 6)	45	50	55	45	50	55	45	50	55	%
t_{SKPP}	Part−to−Part Skew (Note 6)			500			500			500	ps
t_{JITTER}	Random Clock Jitter (RMS)		3.5	5		3.5	5		3.5	5	ps
V_{PP}	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times (0.8V − 2.0V) Q, $\overline{Q}$	250	600	900	250	600	900	250	600	900	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Measured with a 750 mV 50% duty−cycle clock source. R_L = 500 Ω to GND and C_L = 20 pF to GND. Refer to FIgure 3.
6. Skews are measured between outputs under identical transitions. Duty cycle skew is measured between differential outputs using the deviations of the sum Tpw− and Tpw+.

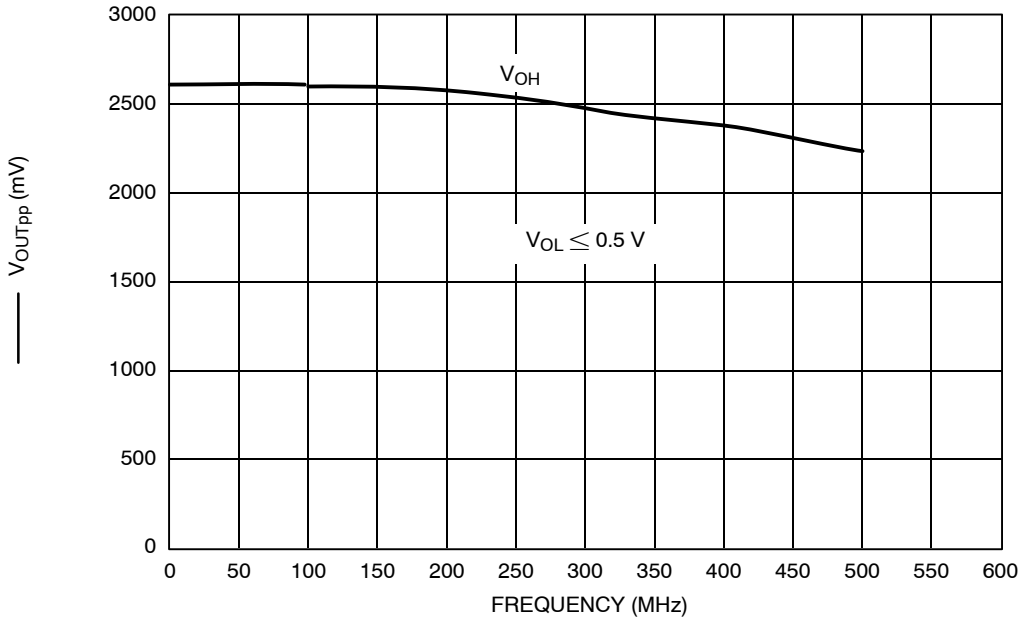


Figure 2. F_{max}

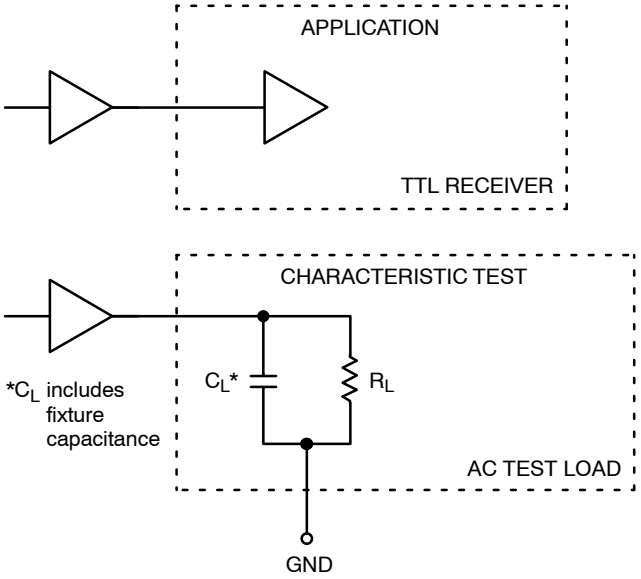


Figure 3. TTL Output Loading Used For Device Evaluation

ORDERING INFORMATION

Device	Package	Shipping†
MC100EPT21DG	SOIC−8 (Pb−Free)	98 Units / Rail
MC100EPT21DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC100EPT21DTG	TSSOP−8 (Pb−Free)	100 Units / Rail
MC100EPT21DTR2G	TSSOP−8 (Pb−Free)	2500 / Tape & Reel
MC100EPT21MNR4G	DFN8 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

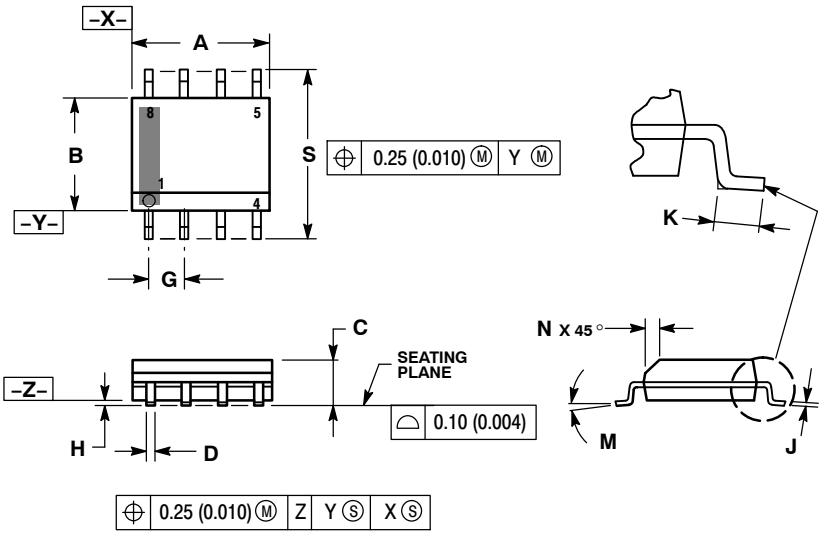
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

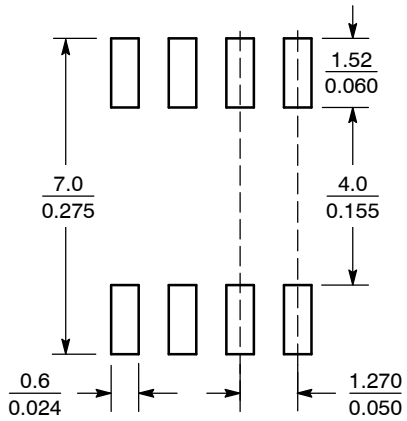
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

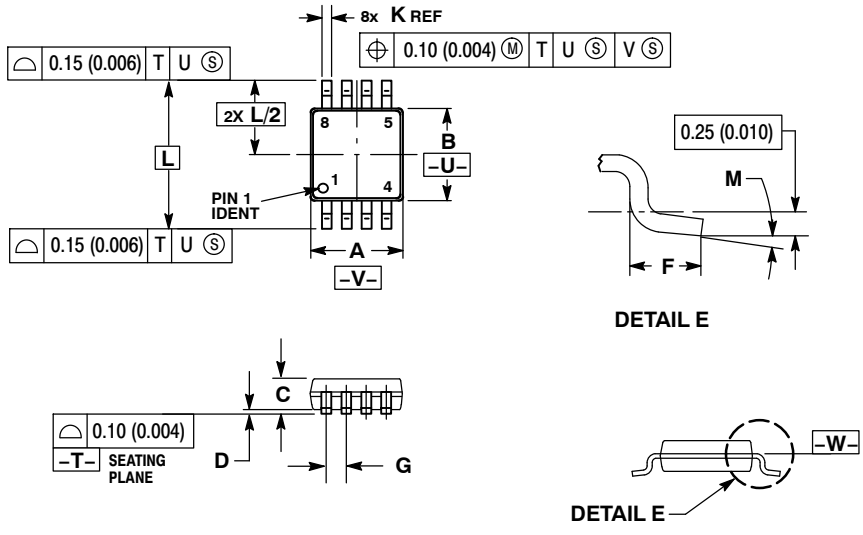


SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP−8
DT SUFFIX
CASE 948R−02
ISSUE A

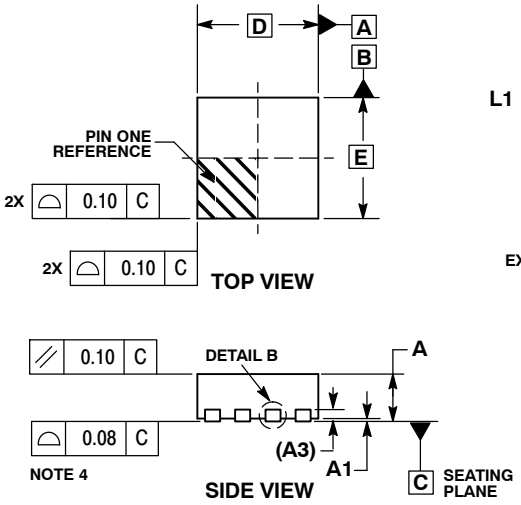


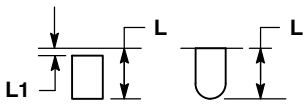
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

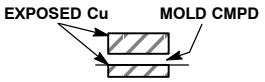
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

PACKAGE DIMENSIONS

DFN8 2x2, 0.5P
CASE 506AA
ISSUE E

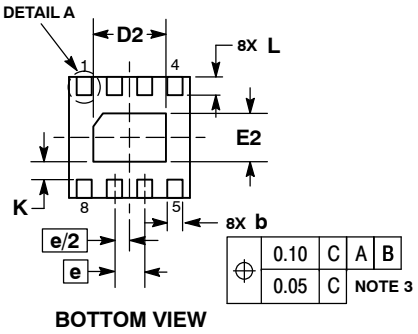




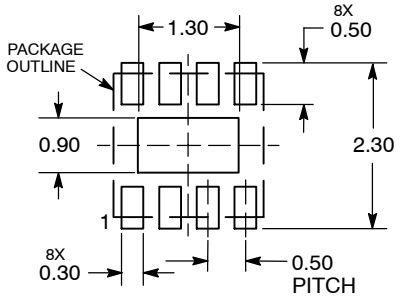


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.30 REF	
L	0.25	0.35
L1	---	0.10



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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