

IR2304(S) & (PbF)

HALF-BRIDGE DRIVER

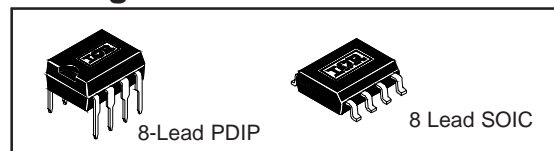
Product Summary

V _{OFFSET}	600V max.
I _{O+/-} (min)	60 mA/130 mA
V _{OUT}	10 - 20V
Delay Matching	50 ns
Internal deadtime	100 ns
ton/off (typ.)	220/220 ns

Features

- Floating channel designed for bootstrap operation to +600V. Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 10 to 20V
- Under voltage lockout for both channels
- 3.3V, 5V, and 15V input logic input compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Lower di/dt gate driver for better noise immunity
- Internal 100ns dead-time
- Output in phase with input
- Available in Lead-Free

Package

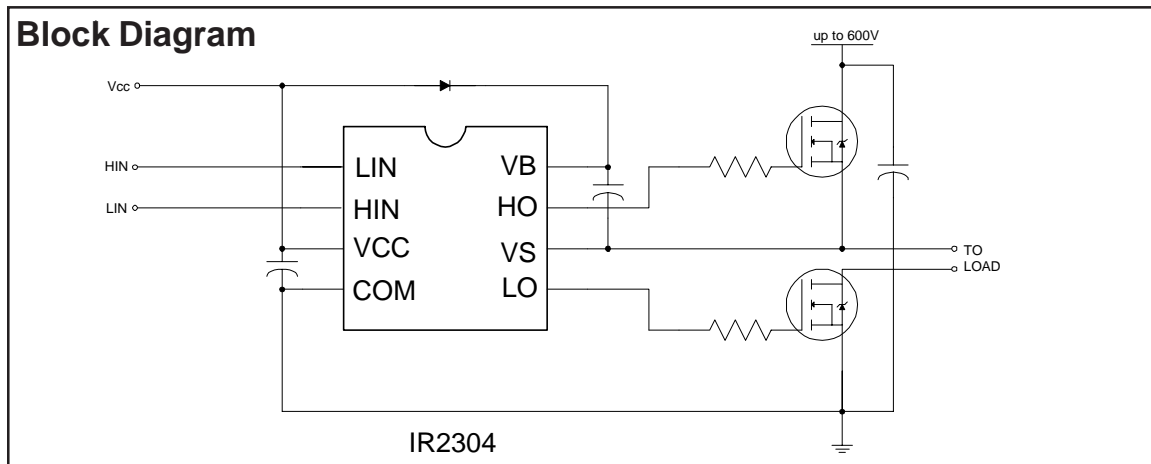


Description

The IR2304(S) are a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

2106/2301/2108/2109/2302/2304 Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Dead-Time	Ground Pins
2106/2301	HIN/LIN	no	none	COM
21064				VSS/COM
2108	HIN/LIN	yes	Internal 540ns Programmable 0.54-5µs	COM
21084				VSS/COM
2109/2302	IN/SD	yes	Internal 540ns Programmable 0.54-5µs	COM
21094				VSS/COM
2304	HIN/LIN	yes	Internal 100ns	COM



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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _S	High side offset voltage	V _B - 25	V _B + 0.3	V	
V _B	High side floating supply voltage	-0.3	625		
V _{HO}	High side floating output voltage HO	V _S - 0.3	V _B + 0.3		
V _{CC}	Low side and logic fixed supply voltage	-0.3	25		
V _{LO}	Low side output voltage LO	-0.3	V _{CC} + 0.3		
V _{IN}	Logic input voltage (HIN, LIN)	-0.3	V _{CC} + 0.3		
Com	Logic ground	V _{CC} -25	V _{CC} + 0.3		
dV _S /dt	Allowable offset voltage SLEW RATE	—	50	V/ns	
P _D	Package power dissipation @ T _A ≤ +25°C	8-Lead SOIC	—	0.625	W
		8-Lead PDIP	—	1.0	
R _{thJA}	Thermal resistance, junction to ambient	8-Lead SOIC	—	200	°C/W
		8-Lead PDIP	—	125	
T _J	Junction temperature	—	150	°C	
T _S	Storage temperature	-50	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply voltage	V _S + 10	V _S + 20	V
V _S	High side floating supply offset voltage	Note 1	600	
V _{HO}	High side (HO) output voltage	V _S	V _B	
V _{LO}	Low side (LO) output voltage	COM	V _{CC}	
V _{IN}	Logic input voltage (HIN, LIN)	COM	V _{CC}	
V _{CC}	Low side supply voltage	10	20	
T _A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of COM -5 to COM +600V. Logic state held for V_S of COM -5V to COM -V_{BS}.

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V and $T_A = 25^\circ\text{C}$ unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and V_S is applicable to HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9		
V_{CCUVH} V_{BSUVH}	V_{CC} supply undervoltage lockout hysteresis	0.3	0.7	—		
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600\text{V}$
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		$V_{IN} = 0\text{V}$ or 5V
I_{QCC}	Quiescent V_{CC} supply current	50	120	240		$V_{IN} = 0\text{V}$ or 5V
V_{IH}	Logic "1" input voltage	2.3	—	—	V	
V_{IL}	Logic "0" input voltage	—	—	0.8		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	—	2.8		$I_O = 20\text{mA}$
V_{OL}	Low level output voltage, V_O	—	—	1.2		
I_{IN+}	Logic "1" input bias current	—	5	40	μA	$V_{IN} = 5\text{V}$
I_{IN-}	Logic "0" input bias current	—	1.0	2.0		$V_{IN} = 0\text{V}$
I_{O+}	Output high short circuit pulse current	60	—	—	mA	$V_O = 0\text{V}$
I_{O-}	Output low short circuit pulsed current	130	—	—		$PW \leq 10 \mu\text{s}$

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, $V_S = \text{COM}$, $C_L = 1000 \text{ pF}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	120	220	320	ns	$V_S = 0\text{V}$
t_{off}	Turn-off propagation delay	130	220	330		$V_S = 0\text{V}$ or 600V
t_r	Turn-on rise time	60	200	300		
t_f	Turn-off fall time	20	100	170		
DT	Dead time	80	100	190		
MT	Delay matching, HS & LS turn-on/off	—	—	50		

Lead Assignments

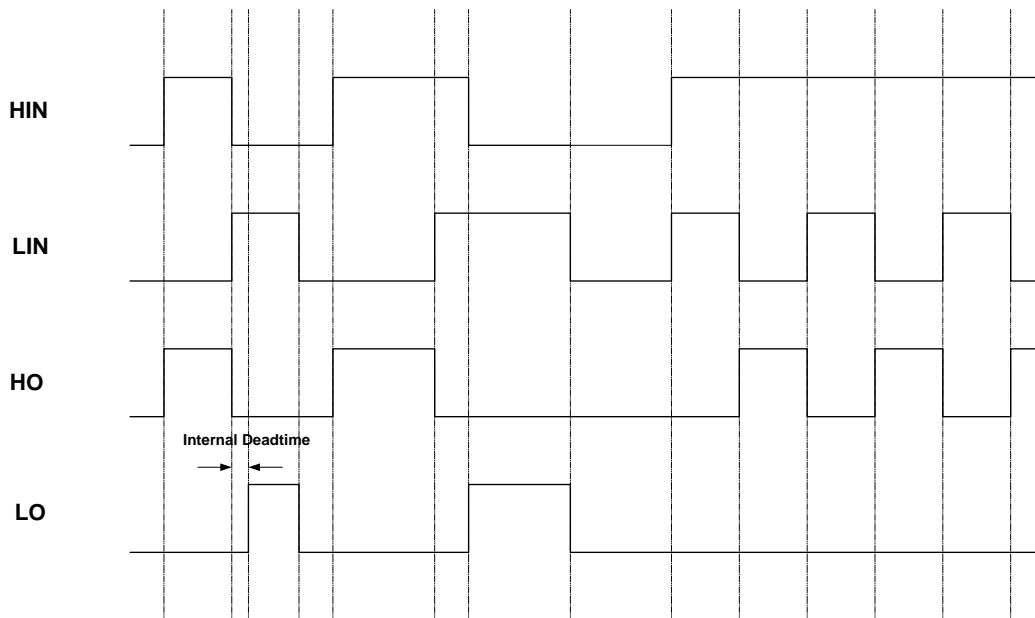
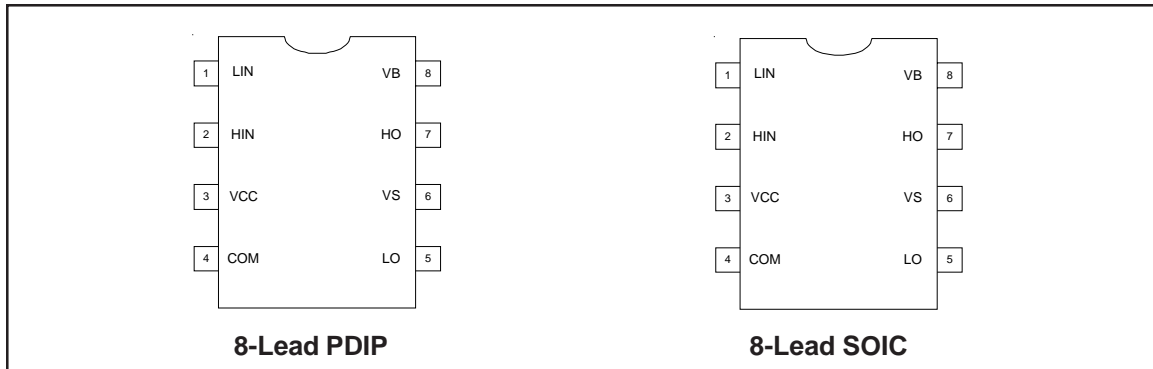


Figure 1. Input/Output Functionality Diagram

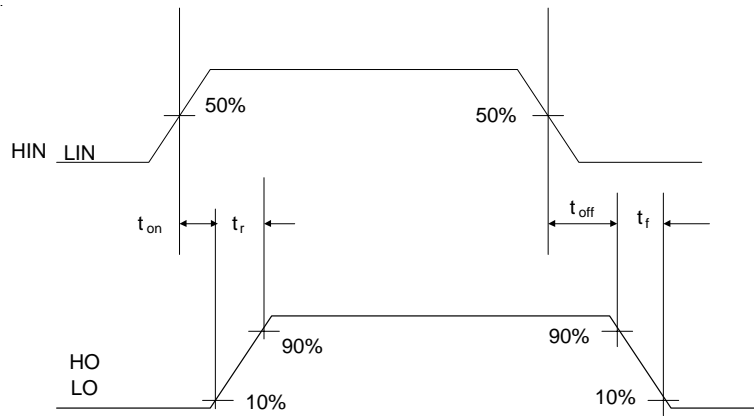


Figure 2. Switching Time Waveforms

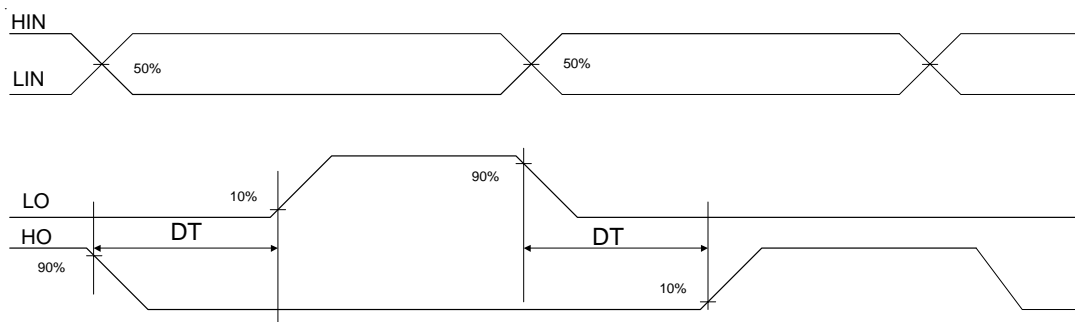
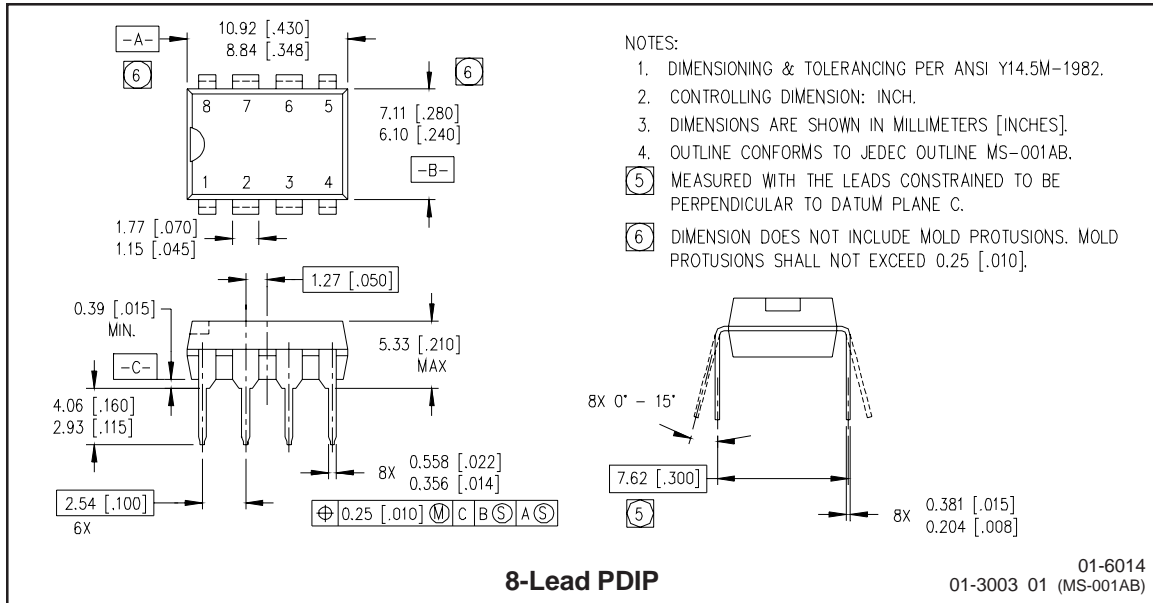
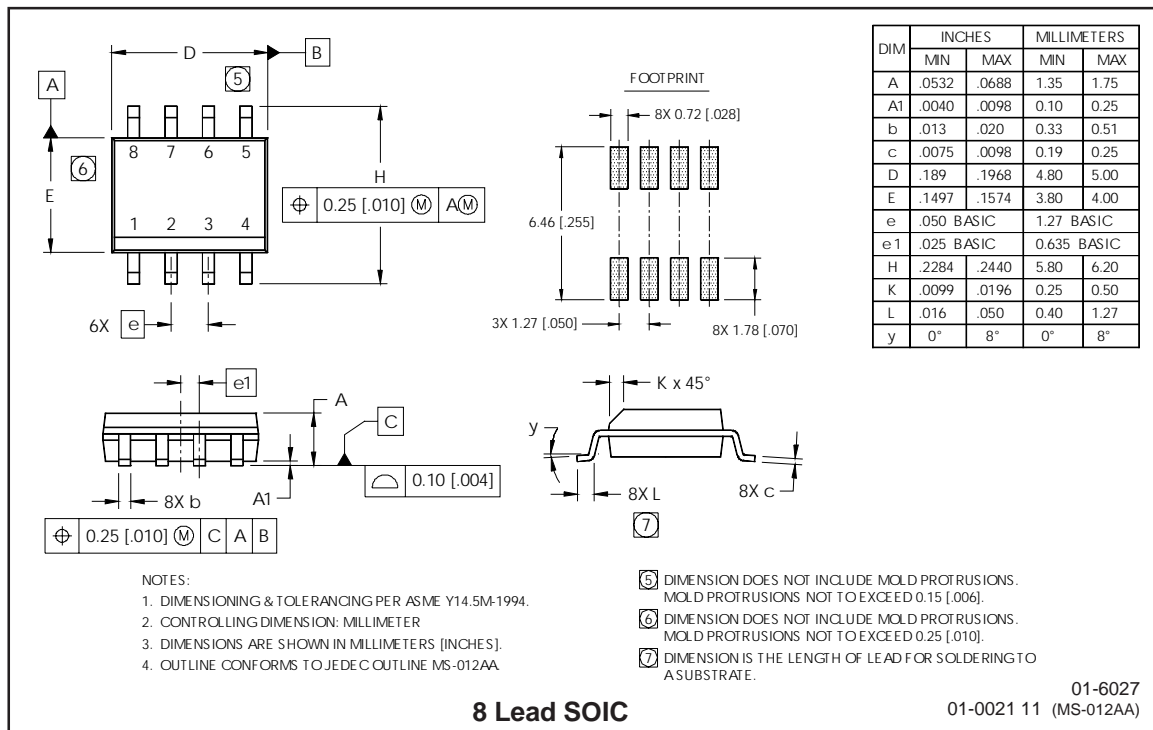


Figure 3. Internal Deadtime Timing

Case outlines



- NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
 - ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
 - ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

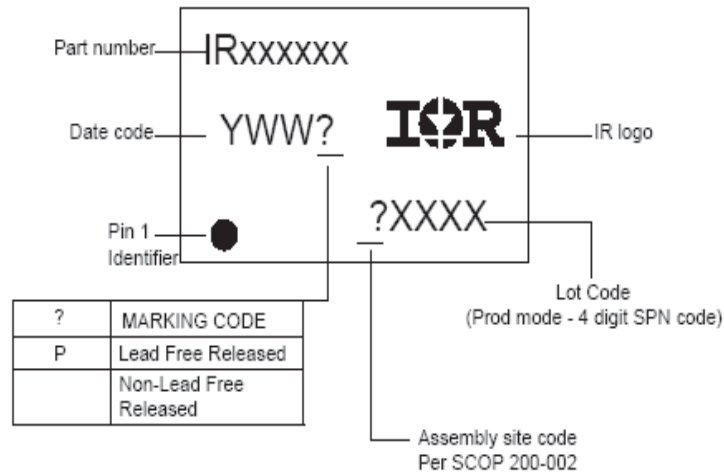


- NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
 2. CONTROLLING DIMENSION: MILLIMETER
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
 - ⑤ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS NOT TO EXCEED 0.15 [.006].
 - ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS NOT TO EXCEED 0.25 [.010].
 - ⑦ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

IR2304(S)&(PbF)

International
IR Rectifier

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

8-Lead PDIP IR2304 order IR2304
8-Lead SOIC IR2304S order IR2304S

Lead-Free Part

8-Lead PDIP IR2304 order IR2304PbF
8-Lead SOIC IR2304S order IR2304SPbF

International
IR Rectifier

This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web Site.
Data and specifications subject to change without notice.

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