18-Mbit DDR II+ SRAM Two-Word Burst Architecture (2.5 Cycle Read Latency)

Features

- 18-Mbit density (2 M × 8, 2 M × 9, 1 M × 18, 512 K × 36)
- 550 MHz clock for high bandwidth
- 2-word burst for reducing address bus frequency
- Double data rate (DDR) interfaces
  (data transferred at 1100 MHz) at 550 MHz
- Available in 2.5 clock cycle latency
- Two input clocks (K and $\overline{K}$) for precise DDR timing
  - SRAM uses rising edges only
- Echo clocks (CQ and $\overline{CQ}$) simplify data capture in high-speed systems
- Data valid pin (QVLD) to indicate valid data on the output
- Synchronous internally self-timed writes
- DDR II+ operates with 2.5 cycle read latency when $\overline{DOFF}$ is asserted HIGH
- Operates similar to DDR I device with 1 cycle read latency when $\overline{DOFF}$ is asserted LOW
- Core V_{DD} = 1.8 V ± 0.1 V; I/O V_{DDQ} = 1.4 V to V_{DD}[1]
  - Supports both 1.5 V and 1.8 V I/O supply
- HSTL inputs and variable drive HSTL output buffers
- Available in 165-Ball FBGA package (13 × 15 × 1.4 mm)
- Offered in both Pb-free and non Pb-free packages
- JTAG 1149.1 compatible test access port
- Phase-locked loop (PLL) for accurate data placement

Configurations

With Read cycle latency of 2.5 cycles:

CY7C11661KV18 – 2 M × 8

CY7C11771KV18 – 2 M × 9

CY7C11681KV18 – 1 M × 18

CY7C11701KV18 – 512 K × 36

Functional Description

The CY7C11661KV18, CY7C11771KV18, CY7C11681KV18, and CY7C11701KV18 are 1.8 V Synchronous Pipelined SRAMs equipped with DDR II+ architecture. The DDR II+ consists of an SRAM core with advanced synchronous peripheral circuitry. Addresses for read and write are latched on alternate rising edges of the input (K) clock. Write data is registered on the rising edges of both K and $\overline{K}$. Read data is driven on the rising edges of K and $\overline{K}$. Each address location is associated with two 8-bit words (CY7C11661KV18), 9-bit words (CY7C11771KV18), 18-bit words (CY7C11681KV18), or 36-bit words (CY7C11701KV18) that burst sequentially into or out of the device.

Asynchronous inputs include an output impedance matching input (ZQ). Synchronous data outputs (Q, sharing the same physical pins as the data inputs D) are tightly matched to the two output echo clocks CQ/$\overline{CQ}$, eliminating the need for separately capturing data from each individual DDR SRAM in the system design.

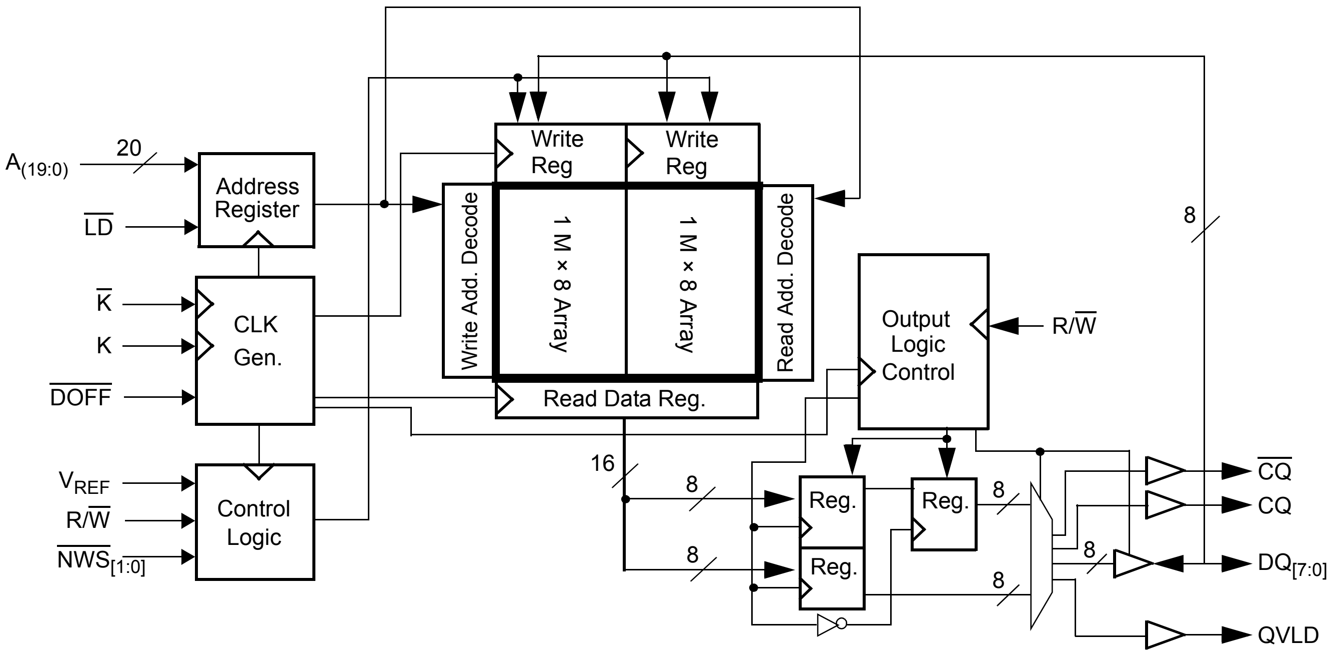
All synchronous inputs pass through input registers controlled by the K or $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the K or $\overline{K}$ input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

Table 1. Selection Guide

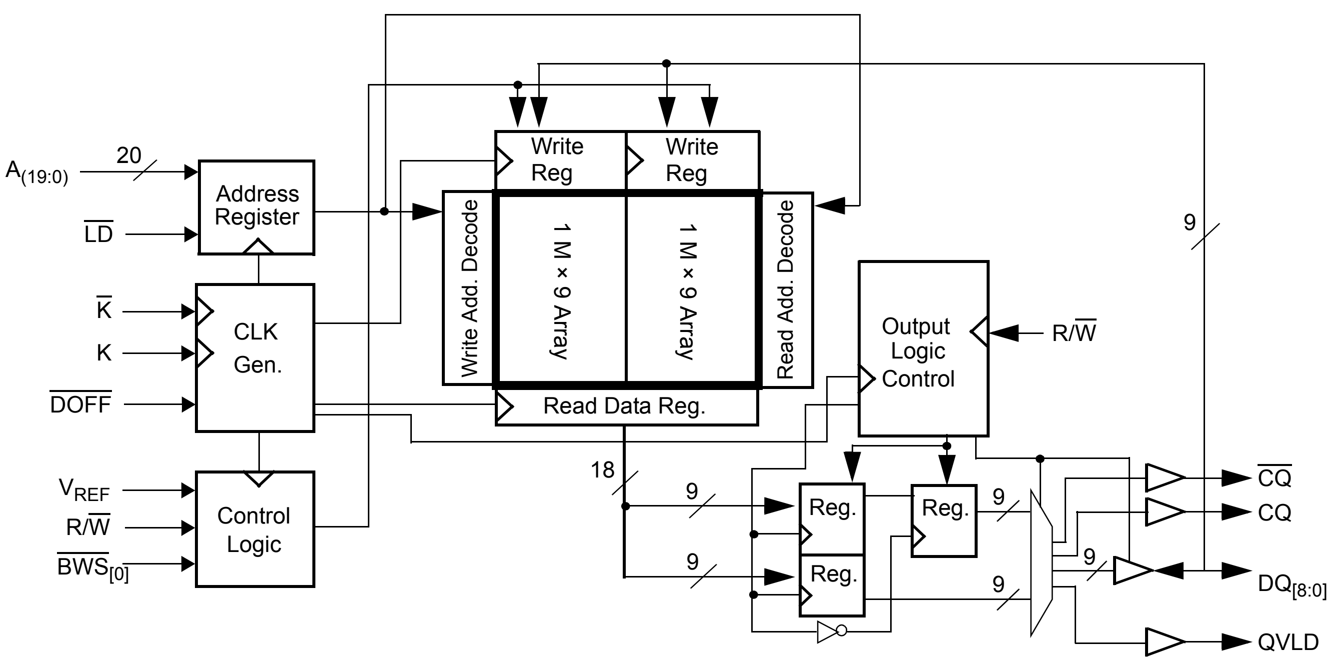
Description		550 MHz	500 MHz	450 MHz	400 MHz	Unit
Maximum operating frequency		550	500	450	400	MHz
Maximum operating current	x8	740	690	630	580	mA
	x9	740	690	630	580	
	x18	760	700	650	590	
	x36	970	890	820	750	

Note
1. The Cypress QDR II+ devices surpass the QDR consortium specification and can support V_{DDQ} = 1.4 V to V_{DD}.

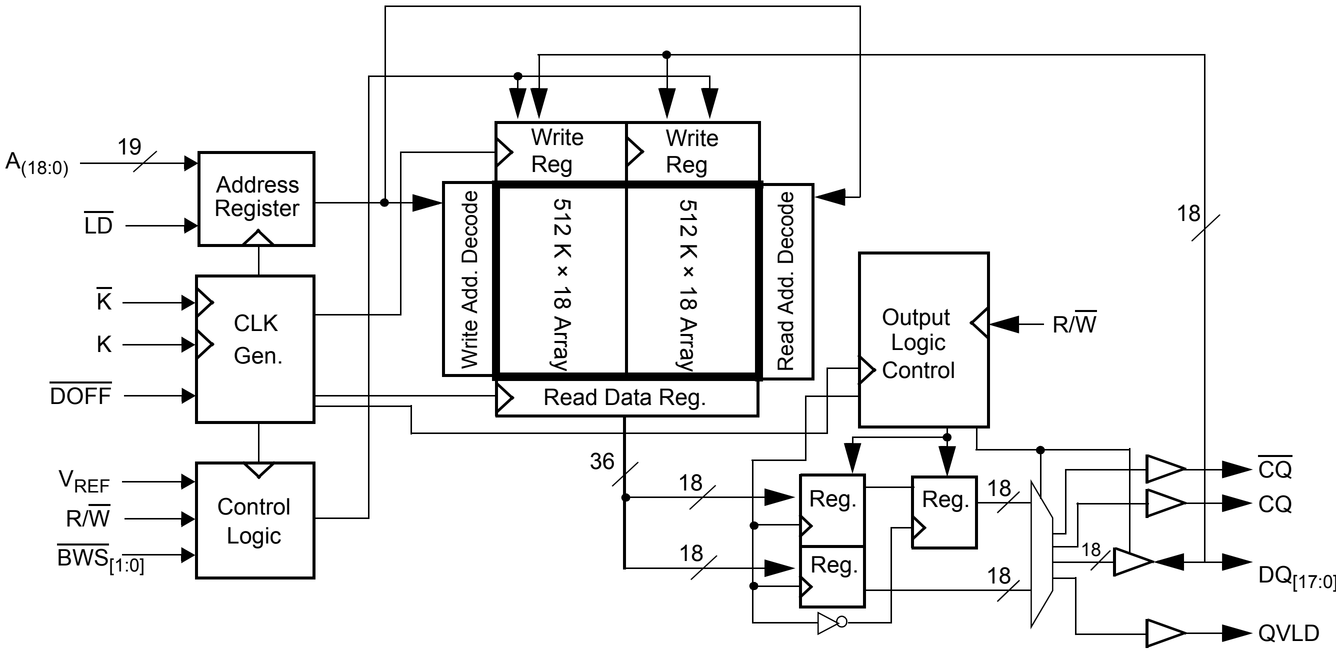
Logic Block Diagram (CY7C11661KV18)



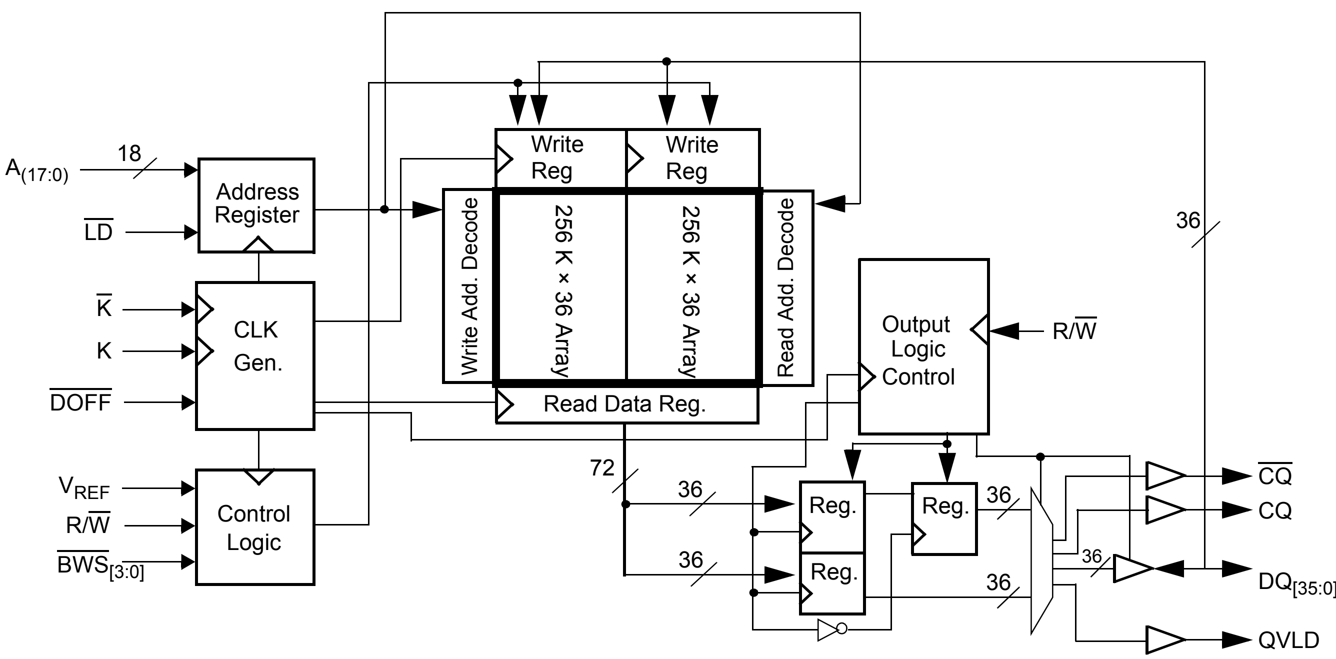
Logic Block Diagram (CY7C11771KV18)



Logic Block Diagram (CY7C11681KV18)



Logic Block Diagram (CY7C11701KV18)



Contents

Functional Overview

The CY7C11661KV18, CY7C11771KV18, CY7C11681KV18, and CY7C11701KV18 are synchronous pipelined Burst SRAMs equipped with a DDR interface, which operates with a read latency of two and half cycles when $\overline{\text{DOFF}}$ pin is tied HIGH. When $\overline{\text{DOFF}}$ pin is set LOW or connected to V_{SS}, the device behaves in DDR I mode with a read latency of one clock cycle.

Accesses are initiated on the rising edge of the positive input clock (K). All synchronous input and output timing are referenced from the rising edge of the input clocks (K and $\overline{\text{K}}$).

All synchronous data inputs ($D_{[x:0]}$) pass through input registers controlled by the rising edge of the input clocks (K and $\overline{\text{K}}$). All synchronous data outputs ($Q_{[x:0]}$) pass through output registers controlled by the rising edge of the input clocks (K and $\overline{\text{K}}$).

All synchronous control (R/$\overline{\text{W}}$, $\overline{\text{LD}}$, $\overline{\text{NWS}}_{[X:0]}$, $\overline{\text{BWS}}_{[X:0]}$) inputs pass through input registers controlled by the rising edge of the input clock (K).

CY7C11681KV18 is described in the following sections. The same basic descriptions apply to CY7C11661KV18, CY7C11771KV18, and CY7C11701KV18.

Read Operations

The CY7C11681KV18 is organized internally as two arrays of 512 K × 18. Accesses are completed in a burst of two sequential 18-bit data words. Read operations are initiated by asserting R/$\overline{\text{W}}$ HIGH and $\overline{\text{LD}}$ LOW at the rising edge of the positive input clock (K). The address presented to the address inputs is stored in the read address register. Following the next two $\overline{\text{K}}$ clock rise, the corresponding 18-bit word of data from this address location is driven onto the $Q_{[17:0]}$ using $\overline{\text{K}}$ as the output timing reference. On the subsequent rising edge of K, the next 18-bit data word is driven onto the $Q_{[17:0]}$. The requested data is valid 0.45 ns from the rising edge of the input clock (K and $\overline{\text{K}}$). To maintain the internal logic, each read access must be allowed to complete. Read accesses can be initiated on every rising edge of the positive input clock (K).

When read access is deselected, the CY7C11681KV18 first completes the pending read transactions. Synchronous internal circuitry automatically tristates the output following the next rising edge of the negative input clock ($\overline{\text{K}}$). This enables a transition between devices without the insertion of wait states in a depth expanded memory.

Write Operations

Write operations are initiated by asserting R/$\overline{\text{W}}$ LOW and $\overline{\text{LD}}$ LOW at the rising edge of the positive input clock (K). The address presented to address inputs is stored in the write address register. On the following K clock rise, the data presented to $D_{[17:0]}$ is latched and stored into the 18-bit write data register, provided $\overline{\text{BWS}}_{[1:0]}$ are both asserted active. On the subsequent rising edge of the negative input clock ($\overline{\text{K}}$) the information presented to $D_{[17:0]}$ is also stored into the write data register, provided $\overline{\text{BWS}}_{[1:0]}$ are both asserted active. The 36 bits of data are then written into the memory array at the specified location. Write accesses can be initiated on every rising edge of the positive input clock (K). Doing so pipelines the data flow such that 18 bits of data can be transferred into the device on every rising edge of the input clocks (K and $\overline{\text{K}}$).

When the write access is deselected, the device ignores all inputs after the pending write operations have been completed.

Byte Write Operations

Byte write operations are supported by the CY7C11681KV18. A write operation is initiated as described in the Write Operations section. The bytes that are written are determined by $\overline{\text{BWS}}_0$ and $\overline{\text{BWS}}_1$, which are sampled with each set of 18-bit data words. Asserting the appropriate Byte Write Select input during the data portion of a write latches the data being presented and writes it into the device. Deasserting the Byte Write Select input during the data portion of a write enables the data stored in the device for that byte to remain unaltered. This feature can be used to simplify read, modify, or write operations to a byte write operation.

DDR Operation

The CY7C11681KV18 enables high performance operation through high clock frequencies (achieved through pipelining) and DDR mode of operation. The CY7C11681KV18 requires two No Operation (NOP) cycle during transition from a read to a write cycle. At higher frequencies, some applications require third NOP cycle to avoid contention.

If a read occurs after a write cycle, address and data for the write are stored in registers. The write information is stored because the SRAM cannot perform the last word write to the array without conflicting with the read. The data stays in this register until the next write cycle occurs. On the first write cycle after the read(s), the stored data from the earlier write is written into the SRAM array. This is called a Posted write.

If a read is performed on the same address on which a write is performed in the previous cycle, the SRAM reads out the most current data. The SRAM does this by bypassing the memory array and reading the data from the registers.

Depth Expansion

Depth expansion requires replicating the $\overline{\text{LD}}$ control signal for each bank. All other control signals can be common between banks as appropriate.

Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to allow the SRAM to adjust its output driver impedance. The value of RQ must be 5x the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of ±15% is between 175 Ω and 350 Ω, with V_{DDQ} = 1.5 V. The output impedance is adjusted every 1024 cycles upon power-up to account for drifts in supply voltage and temperature.

Echo Clocks

Echo clocks are provided on the DDR II+ to simplify data capture on high speed systems. Two echo clocks are generated by the DDR II+. CQ is referenced with respect to K and $\overline{\text{CQ}}$ is referenced with respect to $\overline{\text{K}}$. These are free-running clocks and are synchronized to the input clock of the DDR II+. The timing for the echo clocks is shown in the Switching Characteristics on page 20.

Valid Data Indicator (QVLD)

QVLD is provided on the DDR II+ to simplify data capture on high speed systems. The QVLD is generated by the DDR II+ device along with data output. This signal is also edge aligned with the echo clock and follows the timing of any data pin. This signal is asserted half a cycle before valid data arrives.

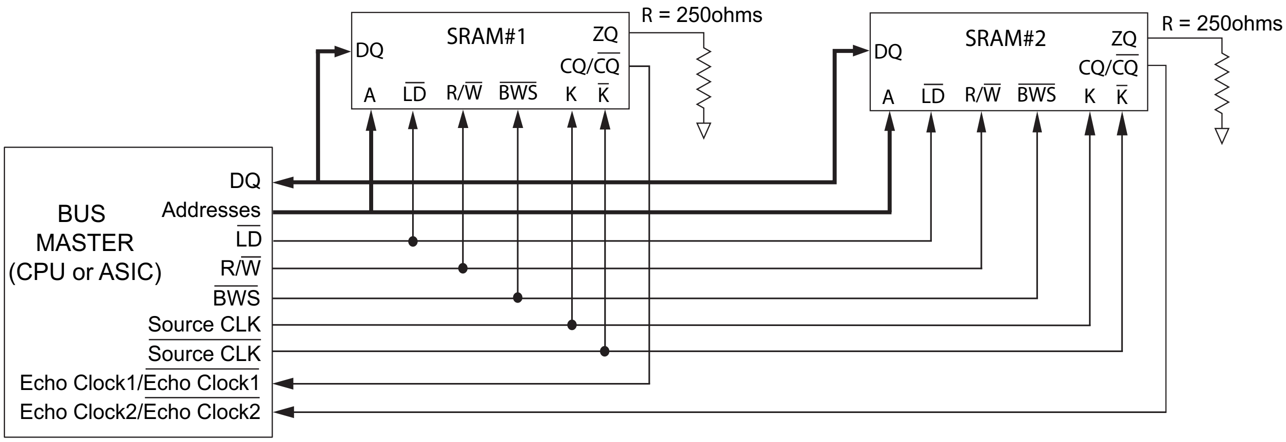
PLL

These chips use a PLL that is designed to function between 120 MHz and the specified maximum clock frequency. During power-up, when the DOFF is tied HIGH, the PLL is locked after 20 µs of stable clock. The PLL can also be reset by slowing or stopping the input clocks K and K for a minimum of 30 ns. However, it is not necessary to reset the PLL to lock to the desired frequency. The PLL automatically locks 20 µs after a stable clock is presented. The PLL may be disabled by applying ground to the DOFF pin. When the PLL is turned off, the device behaves in DDR I mode (with one cycle latency and a longer access time). For information, refer to the application note, *PLL Considerations in QDRII/DDRII/QDRII+/DDRII+*.

Application Example

Figure 1 shows two DDR II+ used in an application.

Figure 1. Application Example



Truth Table

The truth table for the CY7C11661KV18, CY7C11771KV18, CY7C11681KV18, and CY7C11701KV18 follows.[2, 3, 4, 5, 6, 7]

Operation	K	$\overline{LD}$	R/$\overline{W}$	DQ	DQ
Write cycle: Load address; wait one cycle; input write data on consecutive K and $\overline{K}$ rising edges.	L-H	L	L	D(A) at K(t + 1) ↑	D(A+1) at $\overline{K}$(t + 1) ↑
Read cycle: (2.5 cycle latency) Load address; wait two and half cycles; read data on consecutive $\overline{K}$ and K rising edges.	L-H	L	H	Q(A) at $\overline{K}$(t + 2)↑	Q(A+1) at K(t + 3) ↑
NOP: No operation	L-H	H	X	High Z	High Z
Standby: clock stopped	Stopped	X	X	Previous state	Previous state

Write Cycle Description – CY7C11661KV18 and CY7C11681KV18

The write cycle description table for CY7C11661KV18 and CY7C11681KV18 follows.[2, 8]

$\overline{BWS_0}$/ $\overline{NWS_0}$	$\overline{BWS_1}$/ $\overline{NWS_1}$	K	$\overline{K}$	Comments
L	L	L–H	–	During the data portion of a write sequence: CY7C11661KV18 – both nibbles ($D_{[7:0]}$) are written into the device. CY7C11681KV18 – both bytes ($D_{[17:0]}$) are written into the device.
L	L	–	L-H	During the data portion of a write sequence: CY7C11661KV18 – both nibbles ($D_{[7:0]}$) are written into the device. CY7C11681KV18 – both bytes ($D_{[17:0]}$) are written into the device.
L	H	L–H	–	During the data portion of a write sequence: CY7C11661KV18 – only the lower nibble ($D_{[3:0]}$) is written into the device, $D_{[7:4]}$ remains unaltered. CY7C11681KV18 – only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
L	H	–	L–H	During the data portion of a write sequence: CY7C11661KV18 – only the lower nibble ($D_{[3:0]}$) is written into the device, $D_{[7:4]}$ remains unaltered. CY7C11681KV18 – only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
H	L	L–H	–	During the data portion of a write sequence: CY7C11661KV18 – only the upper nibble ($D_{[7:4]}$) is written into the device, $D_{[3:0]}$ remains unaltered. CY7C11681KV18 – only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	L	–	L–H	During the data portion of a write sequence: CY7C11661KV18 – only the upper nibble ($D_{[7:4]}$) is written into the device, $D_{[3:0]}$ remains unaltered. CY7C11681KV18 – only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	H	L–H	–	No data is written into the devices during this portion of a write operation.
H	H	–	L–H	No data is written into the devices during this portion of a write operation.

Notes

2. X = "Do not Care," H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.
3. Device powers up deselected with the outputs in a tristate condition.
4. "A" represents address location latched by the devices when transaction was initiated. A + 1 represents the address sequence in the burst.
5. "t" represents the cycle at which a read/write operation is started. t + 1 and t + 2 are the first and second clock cycles succeeding the "t" clock cycle.
6. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on K and $\overline{K}$ rising edges as well.
7. Ensure that when clock is stopped K = $\overline{K}$ and C = $\overline{C}$ = HIGH. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
8. Is based on a write cycle that was initiated in accordance with the Write Cycle Description – CY7C11661KV18 and CY7C11681KV18 table. $\overline{NWS_0}$, $\overline{NWS_1}$, $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

Write Cycle Descriptions – CY7C11771KV18

The write cycle description table for CY7C11771KV18 follows. [2, 8]

$\overline{BWS_0}$	K	$\overline{K}$	Comments
L	L–H	–	During the data portion of a write sequence, the single byte ($D_{[8:0]}$) is written into the device.
L	–	L–H	During the data portion of a write sequence, the single byte ($D_{[8:0]}$) is written into the device.
H	L–H	–	No data is written into the device during this portion of a write operation.
H	–	L–H	No data is written into the device during this portion of a write operation.

Write Cycle Descriptions – CY7C11701KV18

The write cycle description table for CY7C11701KV18 follows.[2, 8]

$\overline{BWS_0}$	$\overline{BWS_1}$	$\overline{BWS_2}$	$\overline{BWS_3}$	K	$\overline{K}$	Comments
L	L	L	L	L–H	–	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	L	L	L	–	L–H	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	H	H	H	L–H	–	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
L	H	H	H	–	L–H	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
H	L	H	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	L	H	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	H	L	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	L	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	H	L	L–H	–	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	L	–	L–H	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	H	L–H	–	No data is written into the device during this portion of a write operation.
H	H	H	H	–	L–H	No data is written into the device during this portion of a write operation.

IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan Test Access Port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard #1149.1-2001. The TAP operates using JEDEC standard 1.8V I/O logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to V_{DD} through a pull-up resistor. TDO must be left unconnected. Upon power-up, the device comes up in a reset state, which does not interfere with the operation of the device.

Test Access Port—Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information about loading the instruction register, see the TAP Controller State Diagram on page 11. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The output is active, depending upon the current state of the TAP state machine (see Instruction Codes on page 14). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This Reset does not affect the operation of the SRAM and can be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high z state.

TAP Registers

Registers are connected between the TDI and TDO pins to scan the data in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins, as shown in TAP Controller Block Diagram on page 12. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This enables shifting of data through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the SRAM. Several No Connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the input and output ring.

The Boundary Scan Order on page 15 shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Identification Register Definitions on page 14.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in Instruction Codes on page 14. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in this section in detail.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

IDCODE

The IDCODE instruction loads a vendor-specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO pins and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register at power-up or whenever the TAP controller is supplied a Test-Logic-Reset state.

SAMPLE Z

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a high z state until the next command is supplied during the Update IR state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required, that is, while the data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the Shift-DR controller state.

EXTEST OUTPUT BUS TRISTATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tristate mode.

The boundary scan register has a special bit located at bit #108. When this scan cell, called the “extest output bus tristate,” is latched into the preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a high z condition.

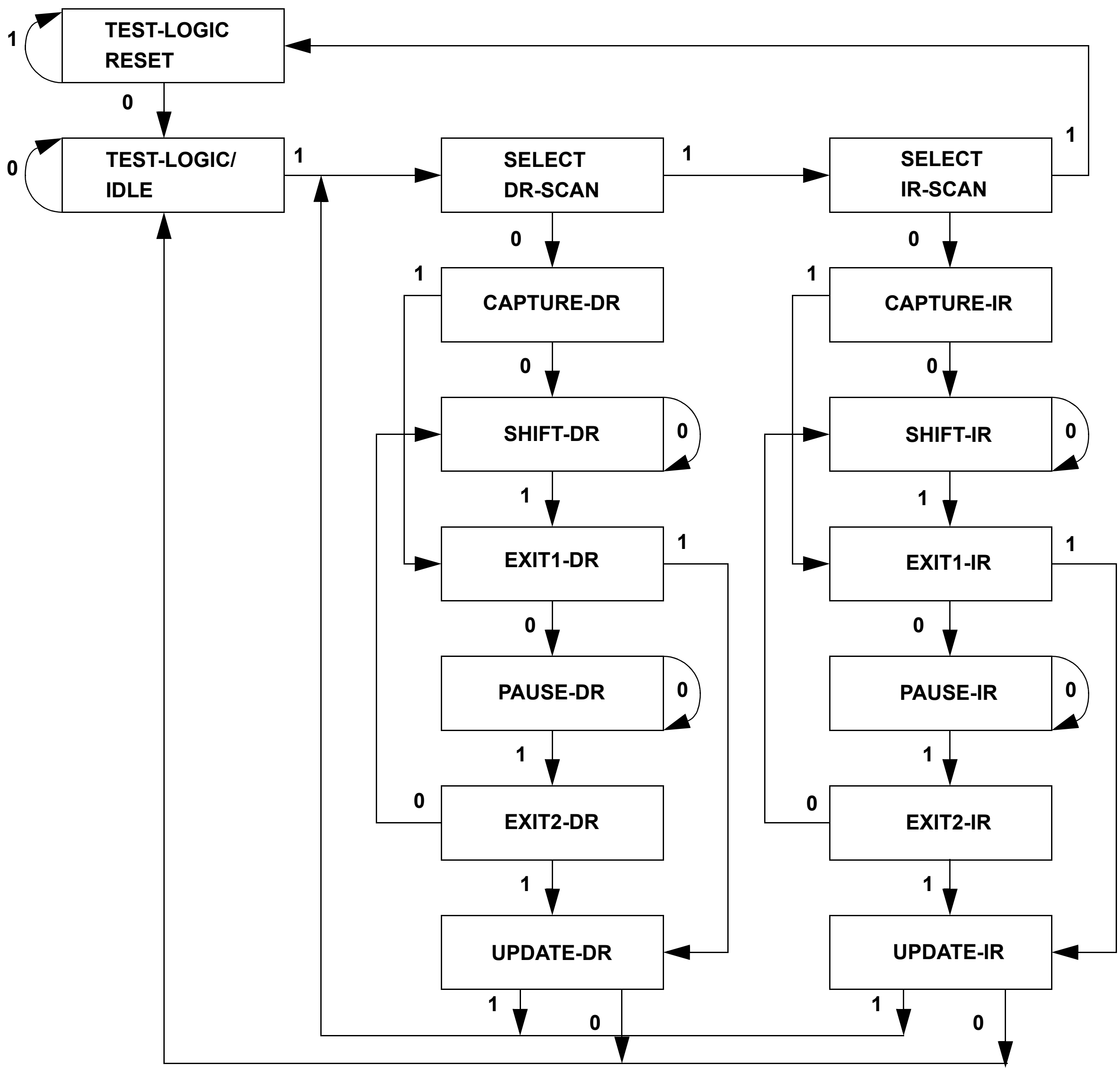
This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the Test-Logic-Reset state.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

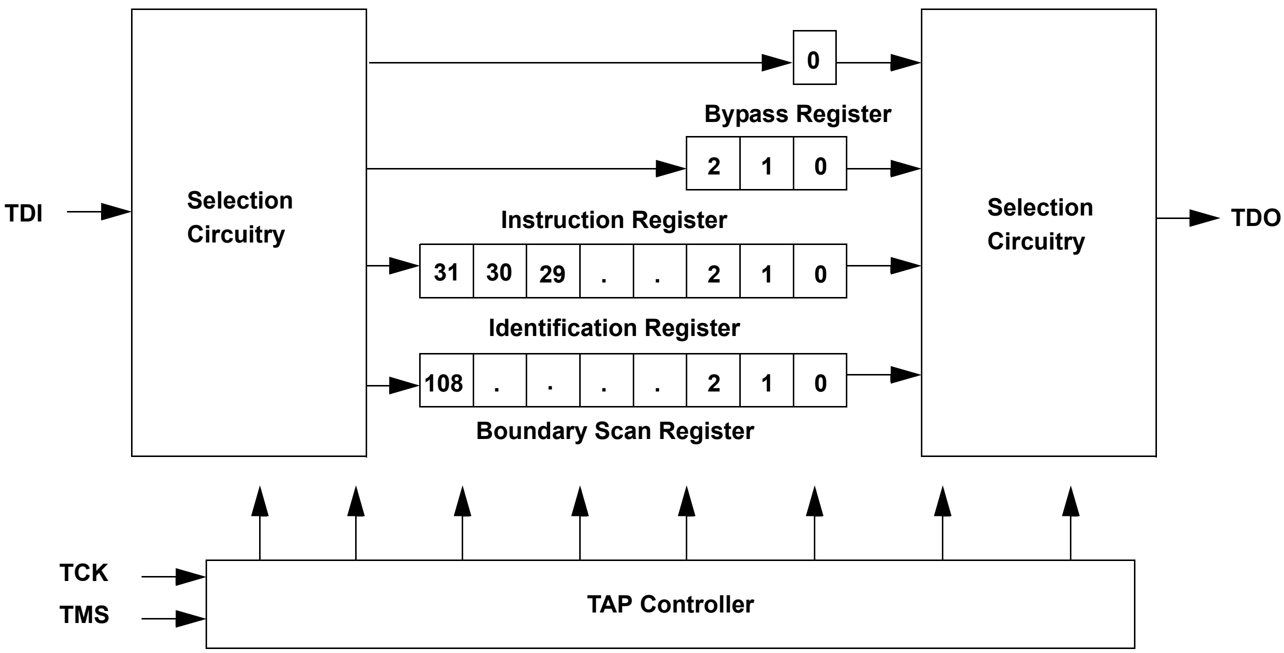
The state diagram for the TAP controller follows.[9]

Figure 2. TAP Controller State Diagram



Note
9. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

Figure 3. TAP Controller Block Diagram



TAP Electrical Characteristics

Over the Operating Range[10, 11, 12]

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH1}	Output HIGH voltage	$I_{OH} = -2.0$ mA	1.4		V
V_{OH2}	Output HIGH voltage	$I_{OH} = -100$ µA	1.6		V
V_{OL1}	Output LOW voltage	$I_{OL} = 2.0$ mA		0.4	V
V_{OL2}	Output LOW voltage	$I_{OL} = 100$ µA		0.2	V
V_{IH}	Input HIGH voltage		0.65 V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage		–0.3	0.35 V_{DD}	V
I_X	Input and output load current	GND ≤ V_I ≤ V_{DD}	–5	5	µA

Notes
10. These characteristics pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in the DC Electrical Characteristics Table.
11. Overshoot: $V_{IH}(AC) < V_{DDQ} + 0.3$ V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) > -0.3$ V (Pulse width less than $t_{CYC}/2$).
12. All voltage referenced to ground.

TAP AC Switching Characteristics

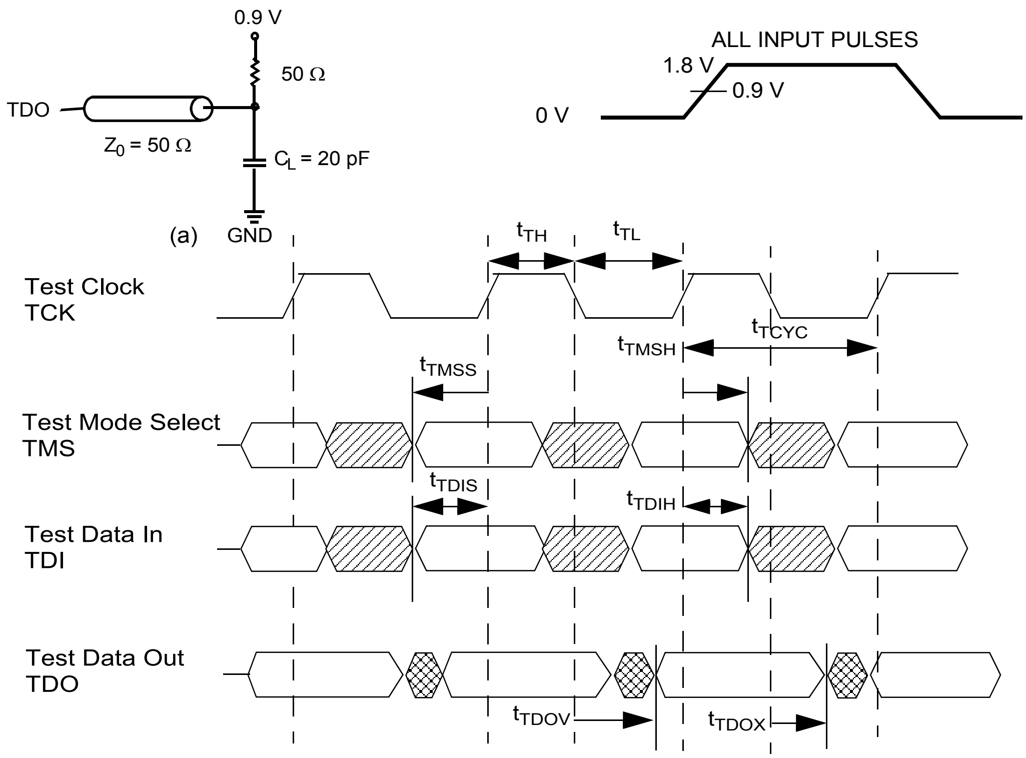
Over the operating range[13, 14]

Parameter	Description	Min	Max	Unit
t_{TCYC}	TCK clock cycle time	50	–	ns
t_{TF}	TCK clock frequency	–	20	MHz
t_{TH}	TCK clock HIGH	20	–	ns
t_{TL}	TCK clock LOW	20	–	ns
Setup Times				
t_{TMSS}	TMS setup to TCK clock rise	5	–	ns
t_{TDIS}	TDI setup to TCK clock rise	5	–	ns
t_{CS}	Capture setup to TCK rise	5	–	ns
Hold Times				
t_{TMSH}	TMS hold after TCK clock rise	5	–	ns
t_{TDIH}	TDI hold after clock rise	5	–	ns
t_{CH}	Capture hold after clock rise	5	–	ns
Output Times				
t_{TDOV}	TCK clock LOW to TDO valid	–	10	ns
t_{TDOX}	TCK clock LOW to TDO invalid	0	–	ns

TAP Timing and Test Conditions

Figure 4 shows the TAP timing and test conditions.[14]

Figure 4. TAP Timing and Test Conditions



Notes
13. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
14. Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

Table 2. Identification Register Definitions

Instruction Field	Value				Description
	CY7C11661KV18	CY7C11771KV18	CY7C11681KV18	CY7C11701KV18	
Revision Number (31:29)	000	000	000	000	Version number.
Cypress Device ID (28:12)	11010111000000100	11010111000001100	11010111000010100	11010111000100100	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	00000110100	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	1	1	1	Indicates the presence of an ID register.

Table 3. Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	109

Table 4. Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input and output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the input and output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the input and output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Table 5. Boundary Scan Order

Bit #	Bump ID
0	6R
1	6P
2	6N
3	7P
4	7N
5	7R
6	8R
7	8P
8	9R
9	11P
10	10P
11	10N
12	9P
13	10M
14	11N
15	9M
16	9N
17	11L
18	11M
19	9L
20	10L
21	11K
22	10K
23	9J
24	9K
25	10J
26	11J
27	11H
28	10G
29	9G
30	11F
31	11G
32	9F
33	10F
34	11E
35	10E
36	10D
37	9E
38	10C
39	11D
40	9C
41	9D
42	11B
43	11C
44	9B
45	10B
46	11A
47	10A
48	9A
49	8B
50	7C
51	6C
52	8A
53	7A
54	7B
55	6B
56	6A
57	5B
58	5A
59	4A
60	5C
61	4B
62	3A
63	2A
64	1A
65	2B
66	3B
67	1C
68	1B
69	3D
70	3C
71	1D
72	2C
73	3E
74	2D
75	2E
76	1E
77	2F
78	3F
79	1G
80	1F
81	3G
82	2G
83	1H
84	1J
85	2J
86	3K
87	3J
88	2K
89	1K
90	2L
91	3L
92	1M
93	1L
94	3N
95	3M
96	1N
97	2M
98	3P
99	2N
100	2P
101	1P
102	3R
103	4R
104	4P
105	5P
106	5N
107	5R
108	Internal

Power-up Sequence in DDR II+ SRAM

DDR II+ SRAMs must be powered-up and initialized in a predefined manner to prevent undefined operations.

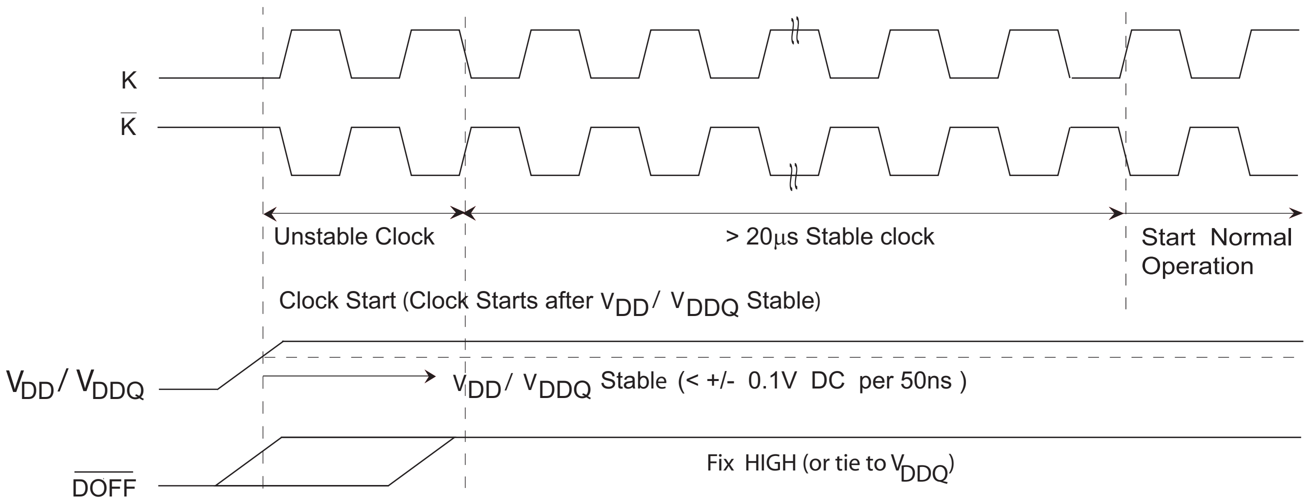
Power-up Sequence

- Apply power and drive $\overline{DOFF}$ either HIGH or LOW (All other inputs can be HIGH or LOW).
  - ❐ Apply V_{DD} before V_{DDQ}.
  - ❐ Apply V_{DDQ} before V_{REF} or at the same time as V_{REF}.
  - ❐ Drive $\overline{DOFF}$ HIGH.
- Provide stable $\overline{DOFF}$ (HIGH), power and clock (K, $\overline{K}$) for 20 μs to lock the PLL.

PLL Constraints

- PLL uses K clock as its synchronizing input. The input must have low phase jitter, which is specified as $t_{KC\ Var}$.
- The PLL functions at frequencies down to 120 MHz.
- If the input clock is unstable and the PLL is enabled, then the PLL may lock onto an incorrect frequency, causing unstable SRAM behavior. To avoid this, provide 20 μs of stable clock to relock to the desired clock frequency.

Figure 5. Power-up Waveforms



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power applied . –55 °C to +125 °C

Supply voltage on V_{DD} relative to GND ....–0.5 V to +2.9 V

Supply voltage on V_{DDQ} relative to GND....... –0.5 V to $+V_{DD}$

DC applied to outputs in high z..........–0.5 V to V_{DDQ} + 0.3 V

DC input voltage[11] ....–0.5 V to V_{DD} + 0.3 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage (MIL-STD-883, M 3015)... > 2001 V

Latch-up current .... > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}[15]	V_{DDQ}[15]
Commercial	0 °C to +70 °C	1.8 ± 0.1 V	1.4 V to V_{DD}
Industrial	–40 °C to +85 °C		

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical single-bit upsets	25 °C	197	216	FIT/Mb
LMBU	Logical multi-bit upsets	25 °C	0	0.01	FIT/Mb
SEL	Single event latch-up	85 °C	0	0.1	FIT/Dev

* *No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note AN54908 “Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates”

Electrical Characteristics

DC Electrical Characteristics

Over the Operating Range[12]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{DD}	Power supply voltage		1.7	1.8	1.9	V
V_{DDQ}	I/O supply voltage		1.4	1.5	V_{DD}	V
V_{OH}	Output HIGH voltage	Note 16	$V_{DDQ}/2 - 0.12$	–	$V_{DDQ}/2 + 0.12$	V
V_{OL}	Output LOW voltage	Note 17	$V_{DDQ}/2 - 0.12$	–	$V_{DDQ}/2 + 0.12$	V
$V_{OH(LOW)}$	Output HIGH voltage	I_{OH} = –0.1 mA, nominal impedance	$V_{DDQ} - 0.2$	–	V_{DDQ}	V
$V_{OL(LOW)}$	Output LOW voltage	I_{OL} = 0.1 mA, nominal impedance	V_{SS}	–	0.2	V
V_{IH}	Input HIGH voltage		$V_{REF} + 0.1$	–	$V_{DDQ} + 0.15$	V
V_{IL}	Input LOW voltage		–0.15	–	$V_{REF} - 0.1$	V
I_X	Input leakage current	$GND \le V_I \le V_{DDQ}$	–2	–	2	μA
I_{OZ}	Output leakage current	$GND \le V_I \le V_{DDQ}$, output disabled	–2	–	2	μA
V_{REF}	Input reference voltage[18]	Typical value = 0.75 V	0.68	0.75	0.95	V

Notes

15. Power-up: Assumes a linear ramp from 0 V to V_{DD}(min) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.
16. Outputs are impedance controlled. $I_{OH} = -(V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω ≤ RQ ≤ 350 Ω.
17. Outputs are impedance controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω ≤ RQ ≤ 350 Ω.
18. V_{REF}(min) = 0.68 V or 0.46 V_{DDQ}, whichever is larger, V_{REF}(max) = 0.95 V or 0.54 V_{DDQ}, whichever is smaller.

DC Electrical Characteristics (continued)

Over the Operating Range[12]

Parameter	Description	Test Conditions			Min	Typ	Max	Unit
I_{DD}[19]	V_{DD} operating supply	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	550 MHz	(x8)	–	–	740	mA
				(x9)	–	–	740	
				(x18)	–	–	760	
				(x36)	–	–	970	
			500 MHz	(x8)	–	–	690	mA
				(x9)	–	–	690	
				(x18)	–	–	700	
				(x36)	–	–	890	
			450 MHz	(x8)	–	–	630	mA
				(x9)	–	–	630	
				(x18)	–	–	650	
				(x36)	–	–	820	
			400 MHz	(x8)	–	–	580	mA
				(x9)	–	–	580	
				(x18)	–	–	590	
				(x36)	–	–	750	
I_{SB1}	Automatic power-down current	Max V_{DD}, both ports deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ f = f_{MAX} = 1/t_{CYC}, inputs static	550 MHz	(x8)	–	–	380	mA
				(x9)	–	–	380	
				(x18)	–	–	380	
				(x36)	–	–	380	
			500 MHz	(x8)	–	–	360	mA
				(x9)	–	–	360	
				(x18)	–	–	360	
				(x36)	–	–	360	
			450 MHz	(x8)	–	–	340	mA
				(x9)	–	–	340	
				(x18)	–	–	340	
				(x36)	–	–	340	
			400 MHz	(x8)	–	–	320	mA
				(x9)	–	–	320	
				(x18)	–	–	320	
				(x36)	–	–	320	

Note
19. The operation current is calculated with 50% read cycle and 50% write cycle.

AC Electrical Characteristics

Over the operating range[11]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH voltage		V_{REF} + 0.2	–	V_{DDQ} + 0.24	V
V_{IL}	Input LOW voltage		–0.24	–	V_{REF} – 0.2	V

Capacitance

Tested initially and after any design or process change that may affect these parameters.

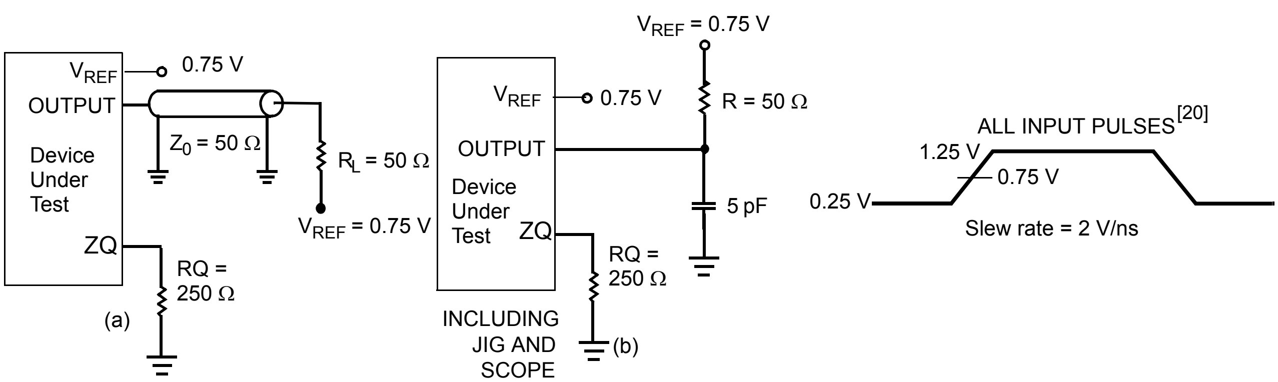
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 1.8 V, V_{DDQ} = 1.5 V	4	pF
C_O	Output capacitance		4	pF

Thermal Resistance

Tested initially and after any design or process change that may affect these parameters.

Parameter	Description	Test Conditions	165-FBGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	13.7	°C/W
Θ_{JC}	Thermal resistance (junction to case)		3.73	°C/W

Figure 6. AC Test Loads and Waveforms



Note

20. Unless otherwise noted, test conditions assume signal transition time of 2 V/ns, timing reference levels of 0.75 V, V_{REF} = 0.75 V, RQ = 250 Ω, V_{DDQ} = 1.5 V, input pulse levels of 0.25 V to 1.25 V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (a) of AC Test Loads and Waveforms.

Switching Characteristics

Over the operating range[20, 21]

Cypress Parameter	Consortium Parameter	Description	550 MHz		500 MHz		450 MHz		400 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{POWER}		V_{DD}(typical) to the first access[22]	1	–	1	–	1	–	1	–	ms
t_{CYC}	t_{KHKH}	K clock cycle time	1.81	8.4	2.0	8.4	2.2	8.4	2.5	8.4	ns
t_{KH}	t_{KHKL}	Input clock (K/$\overline{K}$) HIGH	0.4	–	0.4	–	0.4	–	0.4	–	ns
t_{KL}	t_{KLKH}	Input clock (K/$\overline{K}$) LOW	0.4	–	0.4	–	0.4	–	0.4	–	ns
$t_{KH\overline{K}H}$	$t_{KH\overline{K}H}$	K clock rise to $\overline{K}$ clock rise (rising edge to rising edge)	0.77	–	0.85	–	0.94	–	1.06	–	ns
Setup Times											
t_{SA}	t_{AVKH}	Address setup to K clock rise	0.23	–	0.25	–	0.275	–	0.4	–	ns
t_{SC}	t_{IVKH}	Control setup to K clock rise ($\overline{LD}$, R/$\overline{W}$)	0.23	–	0.25	–	0.275	–	0.4	–	ns
t_{SCDDR}	t_{IVKH}	Double data rate control setup to clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.18	–	0.20	–	0.22	–	0.28	–	ns
t_{SD}	t_{DVKH}	$D_{[X:0]}$ setup to clock (K/$\overline{K}$) rise	0.18	–	0.20	–	0.22	–	0.28	–	ns
Hold Times											
t_{HA}	t_{KHAX}	Address hold after K clock rise	0.23	–	0.25	–	0.275	–	0.4	–	ns
t_{HC}	t_{KHIX}	Control hold after K clock rise ($\overline{LD}$, R/$\overline{W}$)	0.23	–	0.25	–	0.275	–	0.4	–	ns
t_{HCDDR}	t_{KHIX}	Double data rate control hold after clock (K/$\overline{K}$) rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.18	–	0.20	–	0.22	–	0.28	–	ns
t_{HD}	t_{KHDX}	$D_{[X:0]}$ hold after clock (K/K) rise	0.18	–	0.20	–	0.22	–	0.28	–	ns
Output Times											
t_{CO}	t_{CHQV}	K/$\overline{K}$ clock rise to data valid	–	0.45	–	0.45	–	0.45	–	0.45	ns
t_{DOH}	t_{CHQX}	Data output hold after output K/$\overline{K}$ clock rise (active to active)	–0.45	–	–0.45	–	–0.45	–	–0.45	–	ns
t_{CCQO}	t_{CHCQV}	K/$\overline{K}$ clock rise to echo clock valid	–	0.45	–	0.45	–	0.45	–	0.45	ns
t_{CQOH}	t_{CHCQX}	Echo clock hold after K/$\overline{K}$ Clock rise	–0.45	–	–0.45	–	–0.45	–	–0.45	–	ns
t_{CQD}	t_{CQHQV}	Echo clock high to data valid	–	0.15	–	0.15	–	0.15	–	0.20	ns
t_{CQDOH}	t_{CQHQX}	Echo clock high to data invalid	–0.15	–	–0.15	–	–0.15	–	–0.20	–	ns
t_{CQH}	t_{CQHCQL}	Output clock (CQ/$\overline{CQ}$) HIGH[23]	0.655	–	0.75	–	0.85	–	1.00	–	ns
$t_{CQH\overline{CQ}H}$	$t_{CQH\overline{CQ}H}$	CQ clock rise to $\overline{CQ}$ clock rise (rising edge to rising edge)[23]	0.655	–	0.75	–	0.85	–	1.00	–	ns
t_{CHZ}	t_{CHQZ}	Clock (K/$\overline{K}$) rise to high Z (active to high z) [24, 25]	–	0.45	–	0.45	–	0.45	–	0.45	ns
t_{CLZ}	t_{CHQX1}	Clock (K/$\overline{K}$) rise to low Z[24, 25]	–0.45	–	–0.45	–	–0.45	–	–0.45	–	ns
t_{QVLD}	$t_{CQHQVLD}$	Echo clock high to QVLD valid[26]	–0.15	0.15	–0.15	0.15	–0.15	0.15	–0.20	0.20	ns
PLL Timing											
$t_{KC\ Var}$	$t_{KC\ Var}$	Clock phase jitter	–	0.15	–	0.15	–	0.15	–	0.20	ns
$t_{KC\ lock}$	$t_{KC\ lock}$	PLL lock time (K)	20	–	20	–	20	–	20	–	μs
$t_{KC\ Reset}$	$t_{KC\ Reset}$	K static to PLL reset[27]	30	–	30	–	30	–	30	–	ns

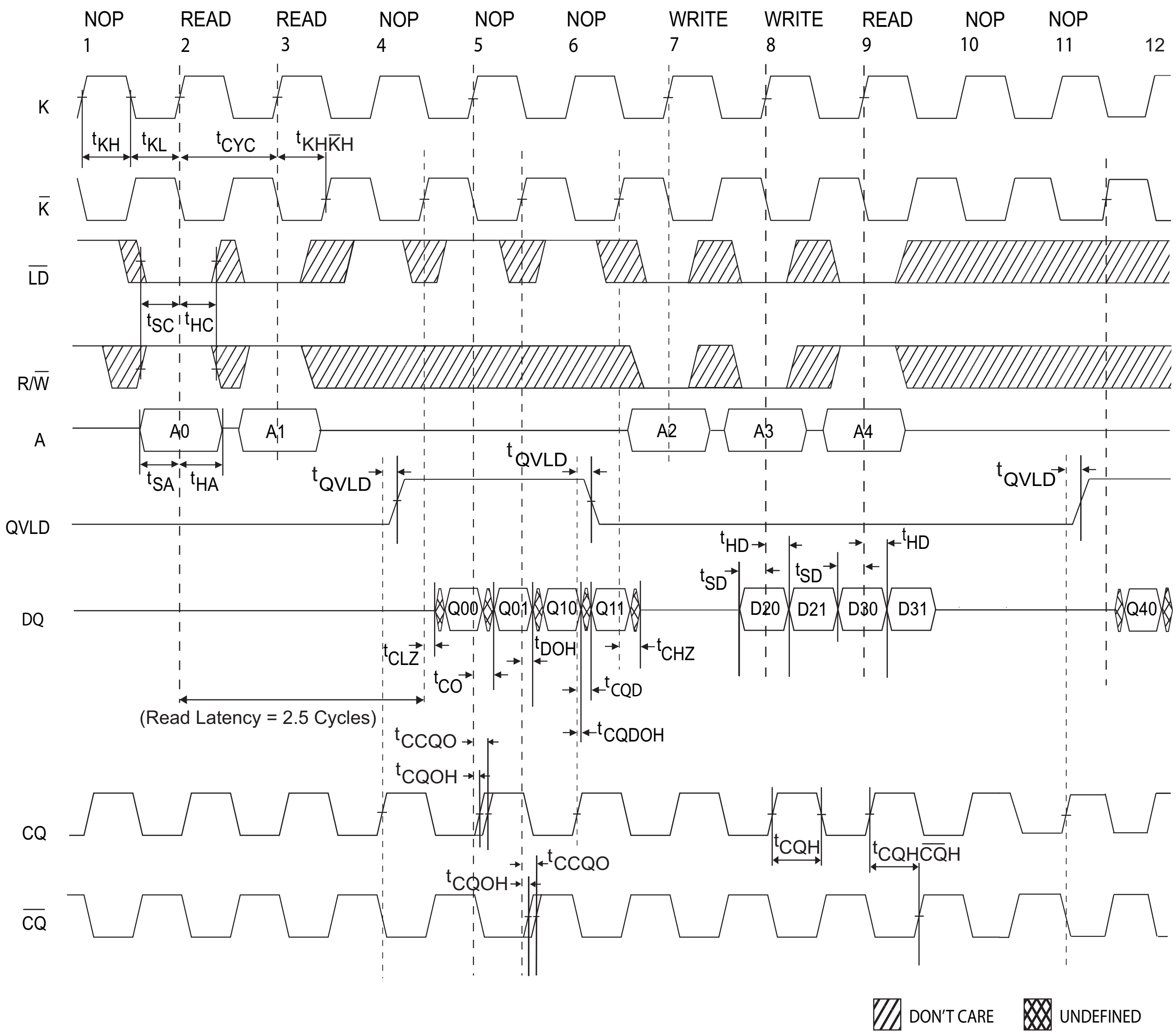
Notes

21. When a part with a maximum frequency above 400 MHz is operating at a lower clock frequency, it requires the input timings of the frequency range in which it is being operated and outputs data with the output timings of that frequency range.
22. This part has an internal voltage regulator; t_{POWER} is the time that the power is supplied above V_{DD} min initially before a read or write operation can be initiated.
23. These parameters are extrapolated from the input timing parameters (t_{CYC}/2 – 250 ps, where 250 ps is the internal jitter). These parameters are only guaranteed by design and are not tested in production.
24. t_{CHZ}, t_{CLZ} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads and Waveforms. Transition is measured ±100 mV from steady-state voltage.
25. At any voltage and temperature t_{CHZ} is less than t_{CLZ} and t_{CHZ} less than t_{CO}.
26. t_{QVLD} specification is applicable for both rising and falling edges of QVLD signal.
27. Hold to >V_{IH} or <V_{IL}.

Switching Waveforms

Read/Write/Deselect Sequence[28, 29, 30]

Figure 7. Waveform for 2.5 Cycle Read Latency



Notes

28. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, that is, A0 + 1.
29. Outputs are disabled (high z) one clock cycle after a NOP.
30. In this example, if address A4 = A3, then data Q40 = D30 and Q41 = D31. Write data is forwarded immediately as read results. This note applies to the whole diagram.

Ordering Information

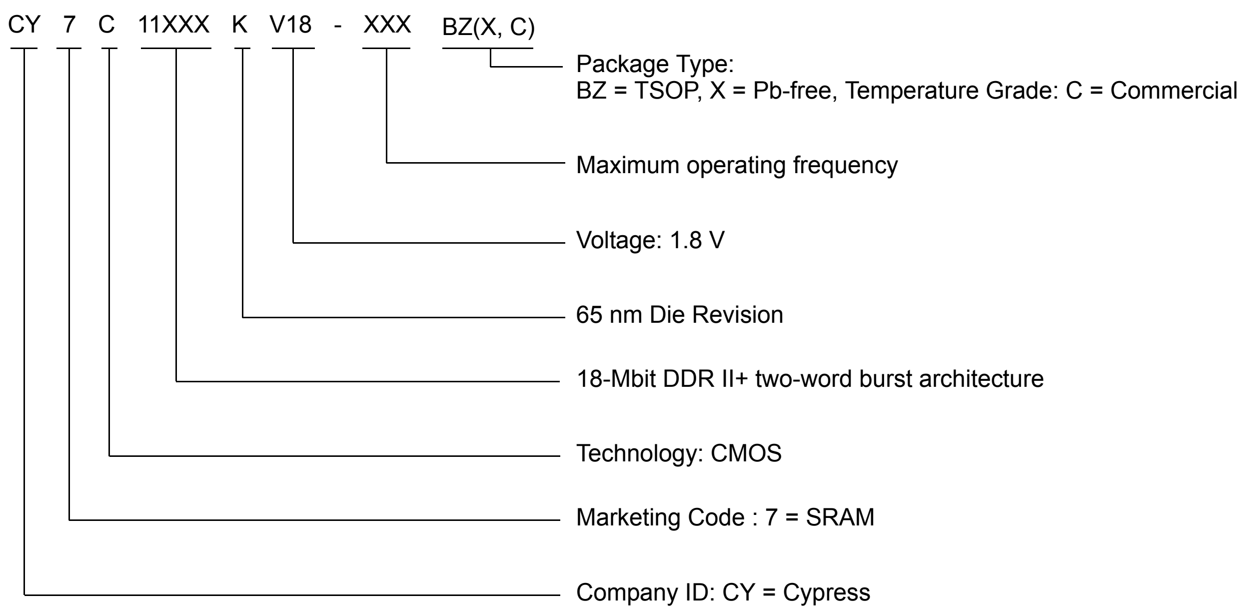
Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available.

For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative. Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

Table 6. Ordering Information

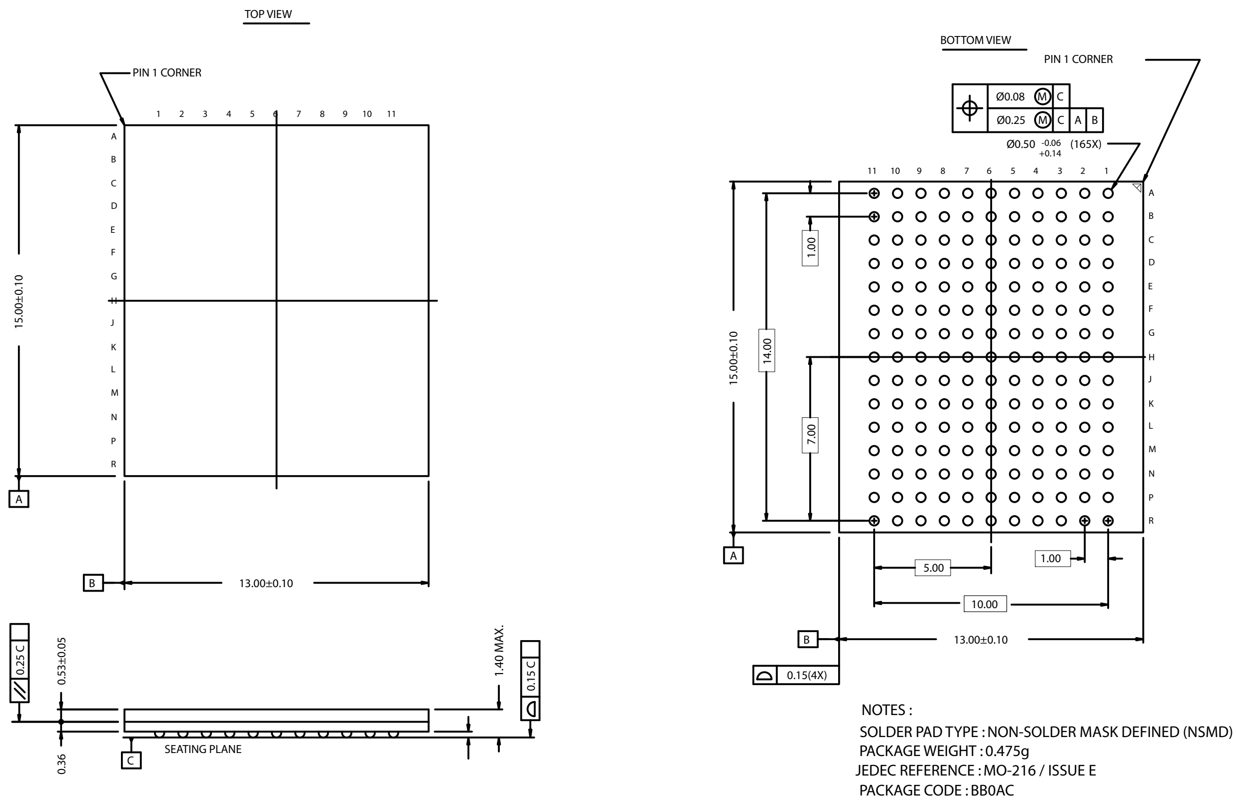
Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
450	CY7C11681KV18-450BZC	51-85180	165-Ball FBGA (13 × 15 × 1.4 mm)	Commercial
	CY7C11681KV18-450BZXC		165-Ball FBGA (13 × 15 × 1.4 mm) Pb-free	
	CY7C11701KV18-450BZXC		165-Ball FBGA (13 × 15 × 1.4 mm) Pb-free	
400	CY7C11681KV18-400BZC	51-85180	165-Ball FBGA (13 × 15 × 1.4 mm)	Commercial
	CY7C11701KV18-400BZXC		165-Ball FBGA (13 × 15 × 1.4 mm) Pb-free	
	CY7C11681KV18-400BZXC			

Ordering Code Definitions



Package Diagram

Figure 8. 165-Ball FBGA (13 × 15 × 1.4 mm), 51-85180



51-85180 *C

Acronyms

Acronym	Description
DDR	double data rate
FBGA	fine-pitch ball grid array
HSTL	high speed transceiver logic
JEDEC	joint electron device engineering council
JTAG	joint test action group
LMBU	logical multiple-bit upset
LSBU	logical single-bit upset
PLL	phase-locked loop
QDR	quad data rate
SEL	single event latch-up
TAP	test access port
TCK	test clock
TDI	test data in
TDO	test data out
TMS	test mode select

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	micro amperes
mA	milliamperes
ns	nano seconds
Ω	ohms
pF	pico Farad
V	volts
W	watts

Document History Page

Document Title: CY7C11661KV18/CY7C11771KV18/CY7C11681KV18/CY7C11701KV18, 18-Mbit DDR II+ SRAM Two-Word Burst Architecture (2.5 Cycle Read Latency) Document Number: 001-53199				
Revision	**ECN**	**Orig of Change**	**Submission Date**	**Description of Change**
**	2702744	VKN/PYRS	05/06/09	New datasheet
*A	2747707	VKN/AESA	08/03/2009	Converted from preliminary to final For 550 MHz, 500 MHz, and 450 MHz bins, changed t_{CO}, t_{CCQO}, t_{CHZ} to 450 ps and t_{DOH}, t_{CQOH}, t_{CLZ} to –450 ps Included Soft Error Immunity Data Modified Ordering Information table by including parts that are available and modified the disclaimer for the Ordering information
*B	2761928	AJU	09/10/2009	Post to external web
*C	2767155	VKN	09/23/2009	Changed Input Capacitance (C_{IN}) from 2 pF to 4 pF Changed Output Capacitance (C_O) from 3 pF to 4 pF Modified Ordering code disclaimer
*D	2785104	VKN	10/16/2009	Updated Ordering information table
*E	2855911	VKN	01/18/2010	Included “CY7C11701KV18-400BZXC” part in the Ordering information table Updated package outline diagram Added Contents.
*F	2896003	NJY	03/19/2010	Removed inactive parts from Ordering Information. Updated package diagram. Updated links in Sales, Solutions, and Legal Information.
*G	2950522	CS/NJY	08/16/10	Added partnumber CY7C11701KV18-450BZXC and CY7C11701KV18-400BZXC to the ordering information table. Template update. Added ordering code definitions, acronyms, and units of measure.
*H	3056557	NJY	10/12/2010	Added new CY7C11681KV18-400BZXC part number to the Ordering Information table.

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