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SN54ABT16244, SN74ABT16244A
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS
SCBS073H−SEPTEMBER 1991−REVISED AUGUST 2005

FEATURES

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JESD 70**
- **Typical V_{OLP} (Output Ground Bounce) <1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**
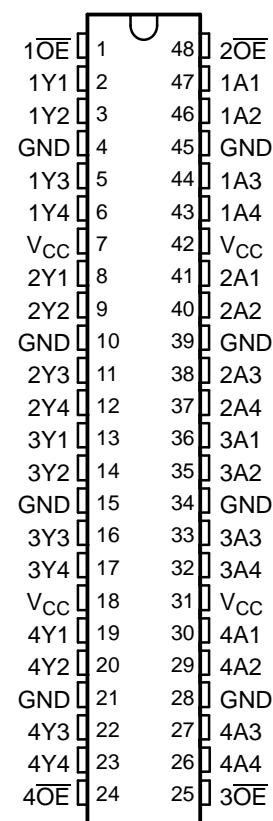
DESCRIPTION

The SN54ABT16244 and SN74ABT16244A are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

SN54ABT16244 . . . WD PACKAGE
SN74ABT16244A . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	48	2$\overline{OE}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V_{CC}	18	31	V_{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4$\overline{OE}$	24	25	3$\overline{OE}$

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16244A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(EACH BUFFER)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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LOGIC SYMBOL[1]

1OE̅	1	EN1
2OE̅	48	EN2
3OE̅	25	EN3
4OE̅	24	EN4

1A1	47	1 1 ▽	2	1Y1
1A2	46		3	1Y2
1A3	44		5	1Y3
1A4	43		6	1Y4
2A1	41	1 2 ▽	8	2Y1
2A2	40		9	2Y2
2A3	38		11	2Y3
2A4	37		12	2Y4
3A1	36	1 3 ▽	13	3Y1
3A2	35		14	3Y2
3A3	33		16	3Y3
3A4	32		17	3Y4
4A1	30	1 4 ▽	19	4Y1
4A2	29		20	4Y2
4A3	27		22	4Y3
4A4	26		23	4Y4
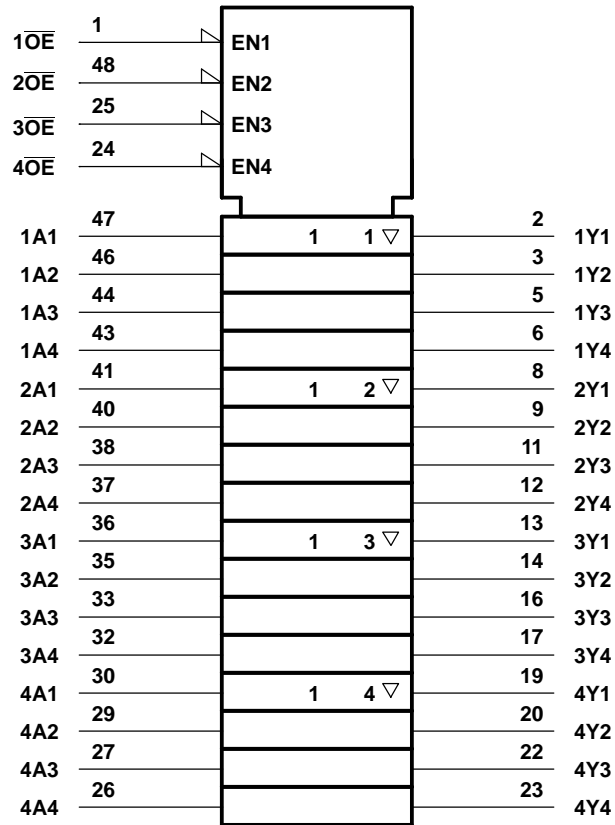
(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and
    IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)
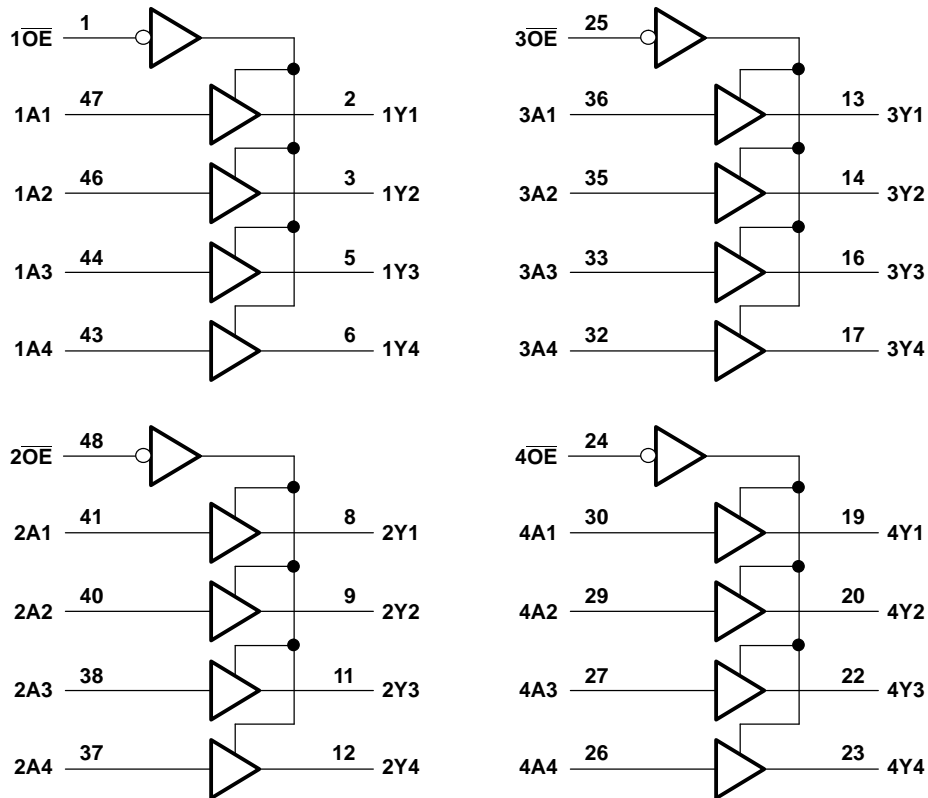
Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I	Input voltage range[2]		−0.5	7	V
V_O	Voltage range applied to any output in the high or power-off state		−0.5	5.5	V
I_O	Current into any output in the low state	SN54ABT16244		96	mA
		SN74ABT16244A		128	
I_{IK}	Input clamp current	$V_I < 0$		−18	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
θ_{JA}	Package thermal impedance[3]	DGG package		89	°C/W
		DGV package		93	
		DL package		94	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD 51.

Recommended Operating Conditions[1]

			SN54ABT16244 MIN	SN54ABT16244 MAX	SN74ABT16244A MIN	SN74ABT16244A MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C[1] MIN	T_A = 25°C[1] TYP[2]	T_A = 25°C[1] MAX	SN54ABT16244 MIN	SN54ABT16244 MAX	SN74ABT16244A MIN	SN74ABT16244A MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA	3			3		3		
	V_{CC} = 4.5 V	I_{OH} = −24 mA	2			2				
		I_{OH} = −32 mA	2[3]					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55		0.55			V
		I_{OL} = 64 mA			0.55[3]				0.55	
V_{hys}				100						mV
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			10[4]		10		10[4]	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−10[4]		−10		−10[4]	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 5.5 V			±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O [5]	V_{CC} = 5.5 V,	V_O = 2.5 V	−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			3		2		3	mA
		Outputs low			32		32		32	
		Outputs disabled			3		2		3	
ΔI_{CC} [6]	Data inputs: V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			0.05		1.5		0.05	mA
		Outputs disabled			0.05		1		0.05	
	Control inputs: V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				0.05		1.5		0.05	
C_i	V_I = 2.5 V or 0.5 V			3						pF
C_o	V_O = 2.5 V or 0.5 V			6						pF

(1) Characteristics for T_A = 25°C apply to the SN74ABT16244A only.
(2) All typical values are at V_{CC} = 5 V.
(3) On products compliant to MIL-PRF-38535, this parameter does not apply.
(4) This data-sheet limit may vary among suppliers.
(5) Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
(6) This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCBS073H−SEPTEMBER 1991−REVISED AUGUST 2005

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF
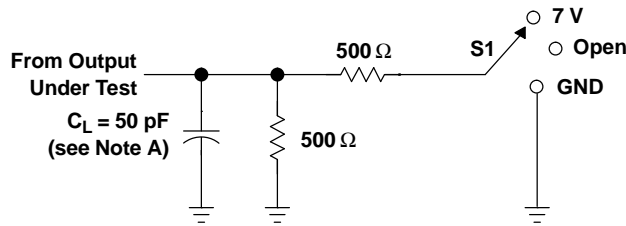(unless otherwise noted) (see Figure 1)

| PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16244					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A	Y	0.7	2.3	3.2	0.7	3.6	ns
t_{PHL}			0.5	2.6	3.7	0.5	4.2	
t_{PZH}	$\overline{OE}$	Y	0.7	3	4	0.7	4.9	ns
t_{PZL}			0.9	3.2	5.5	0.9	6.5	
t_{PHZ}	$\overline{OE}$	Y	1.7	3.6	5	1.7	6	ns
t_{PLZ}			1.5	2.9	4.7	1.5	5.7	

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF
(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16244A					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1	2.3	3.2	1	3.5	ns
t_{PHL}			1	2.6	3.7	1	4.1	
t_{PZH}	$\overline{OE}$	Y	1	3	3.8	1	4.8	ns
t_{PZL}			1	3.2	4	1	4.8	
t_{PHZ}	$\overline{OE}$	Y	1	3.6	4.4	1	4.8	ns
t_{PLZ}			1	2.9	3.7	1	4.1	

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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT
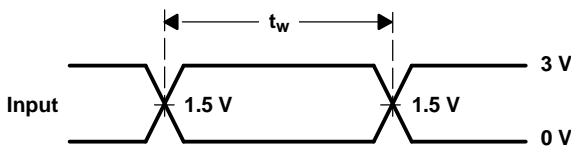
VOLTAGE WAVEFORMS
PULSE DURATION
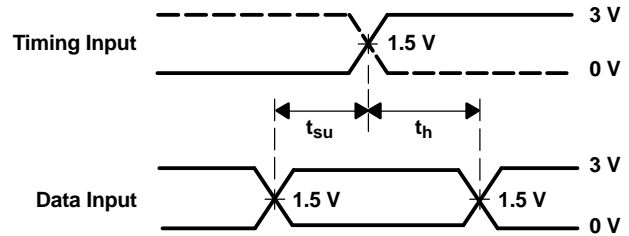
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
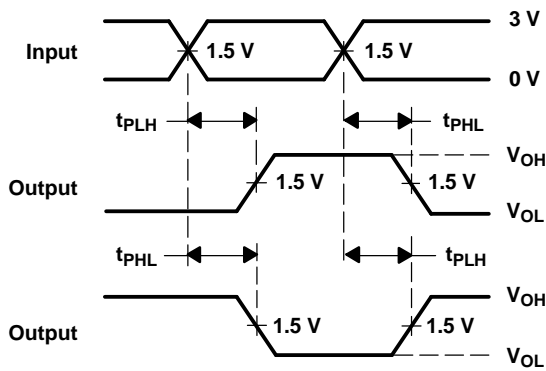
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
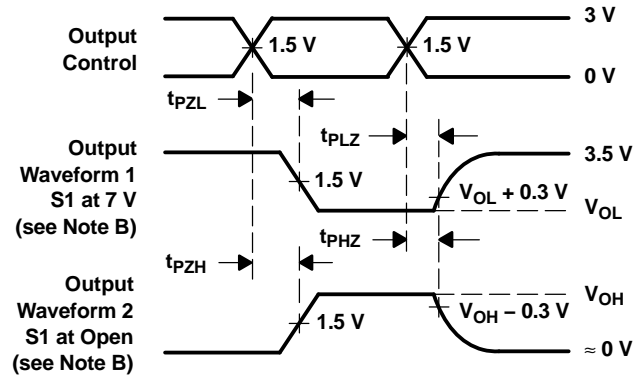
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
         Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
      C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
      D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9317401MXA	ACTIVE	CFP	WD	48	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9317401MX A SNJ54ABT16244W D	Samples
SN74ABT16244ADGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16244A	Samples
SN74ABT16244ADGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AH244A	Samples
SN74ABT16244ADL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16244A	Samples
SN74ABT16244ADLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16244A	Samples
SN74ABT16244ADLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16244A	Samples
SN74ABT16244ADLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16244A	Samples
SNJ54ABT16244WD	ACTIVE	CFP	WD	48	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9317401MX A SNJ54ABT16244W D	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

Q1	Q2	Q1	Q2
Q3	Q4	Q3	Q4

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16244ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ABT16244ADGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74ABT16244ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16244ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ABT16244ADGVR	TVSOP	DGV	48	2000	367.0	367.0	38.0
SN74ABT16244ADLR	SSOP	DL	48	1000	367.0	367.0	55.0

WD (R-GDFP-F**)   CERAMIC DUAL FLATPACK

48 LEADS SHOWN

NO. OF LEADS**	48	56
A MAX	0.640 (16,26)	0.740 (18,80)
A MIN	0.610 (15,49)	0.710 (18,03)

4040176 / D 10/97

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. This package can be hermetically sealed with a ceramic lid using glass frit.
          D. Index point is provided on cap for terminal identification only
          E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
                                          GDFP1-F56 and JEDEC MO-146AB

DL (R−PDSO−G48)   PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

0.0135 (0,343)
0.008 (0,203)

⊕ 0.005 (0,13) Ⓜ

48   25

0.420 (10,67)
0.395 (10,03)

0.299 (7,59)
0.291 (7,39)

0.010 (0,25)
0.005 (0,13)

Gage Plane

0.010 (0,25)

0°−8°

0.040 (1,02)
0.020 (0,51)

1   24

0.630 (16,00)
0.620 (15,75)

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

4040048−3/F   05/13

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MO−118

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DGV (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

0,40

$\dfrac{0,23}{0,13}$ ⊕   0,07 Ⓜ

24   13

4,50 / 4,30   6,60 / 6,20

1   12

A

0,16 NOM

Gage Plane

0°−8°

0,25

0,75 / 0,50

1,20 MAX

$\dfrac{0,15}{0,05}$

Seating Plane

⌒ 0,08

DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DGG (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold protrusion not to exceed 0,15.
   D. Falls within JEDEC MO-153

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