

Medium Power Phase Control Thyristors (Power Modules), 50 A, 70 A, 90 A



D-55 (T-module)

FEATURES

- Electrically isolated base plate
- Types up to 1200 V_{RRM}
- 3500 V_{RMS} isolating voltage
- Simplified mechanical designs, rapid assembly
- High surge capability
- Large creepage distances
- UL E78996 approved 
- Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

PRIMARY CHARACTERISTICS

Package	D-55 (T-module)
Circuit configuration	Single SCR
I _{T(AV)}	50 A, 70 A, 90 A
V _{DRM} /V _{RRM}	100 V, 1200 V
V _{TM}	1.55 V
I _{GT}	120 mA
T _J	-40 °C to +125 °C
Type	Modules - thyristor, standard

DESCRIPTION

These series of T-modules are intended for general purpose applications such as battery chargers, welders and plating equipment, regulated power supplies and temperature and speed control circuits. The semiconductors are electrically isolated from the metal base, allowing common heatsinks and compact assemblies to be built.

MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES T50RIA	VALUES T70RIA	VALUES T90RIA	UNITS
I _{T(AV)}	70 °C	50	70	90	A
I _{T(RMS)}		80	110	141	A
I _{TSM}	50 Hz	1310	1660	1780	A
	60 Hz	1370	1740	1870	
I ² t	50 Hz	8550	13 860	15 900	A ² s
	60 Hz	7800	12 650	14 500	
I ² √t		85 500	138 500	159 100	A ² √s
V _{RRM}	Range	100 to 1200	100 to 1200	100 to 1200	V
T _J		-40 to +125			°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V _{RRM} /V _{DRM} , MAXIMUM REPETITIVE PEAK REVERSE AND PEAK OFF-STATE VOLTAGE V	V _{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I _{RRM} /I _{DRM} MAXIMUM AT T _J = 25 °C μA
VS-T50RIA VS-T70RIA VS-T90RIA	10	100	150	100
	20	200	300	
	40	400	500	
	60	600	700	
	80	800	900	
	100	1000	1100	
	120	1200	1300	



ON-STATE CONDUCTION								
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES T50RIA	VALUES T70RIA	VALUES T90RIA	UNITS
Maximum average on-state current at case temperature	I _{T(AV)}	180° conduction, half sine wave			50	70	90	A
					70	70	70	°C
Maximum RMS on-state current	I _{T(RMS)}				80	110	141	A
Maximum peak, one-cycle on-state, non-repetitive surge current	I _{TSM}	t = 10 ms	No voltage reapplied	Sine half wave, initial T _J = T _J maximum	1310	1660	1780	A
		t = 8.3 ms			1370	1740	1870	
		t = 10 ms	100 % V _{RRM} reapplied		1100	1400	1500	
		t = 8.3 ms			1150	1460	1570	
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reapplied		8550	13 860	15 900	A ² s
		t = 8.3 ms			7800	12 650	14 500	
		t = 10 ms	100 % V _{RRM} reapplied		6050	9800	11 250	
		t = 8.3 ms			5520	8950	10 270	
Maximum I ² √t for fusing	I ² √t	t = 0.1 to 10 ms, no voltage reapplied			85 500	138 500	159 100	A ² √s
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % × π × I _{T(AV)} < I < π × I _{T(AV)}), T _J maximum			0.97	0.77	0.78	V
High level value of threshold voltage	V _{T(TO)2}	(I > π × I _{T(AV)}), T _J maximum			1.13	0.88	0.88	
Low level value of on-state slope resistance	r _{t1}	(16.7 % × π × I _{T(AV)} < I < π × I _{T(AV)}), T _J maximum			4.1	3.6	2.9	mΩ
High level value of on-state slope resistance	r _{t2}	(I > π × I _{T(AV)}), T _J maximum			3.3	3.2	2.6	
Maximum on-state voltage drop	V _{TM}	I _{TM} = π × I _{T(AV)} , T _J = 25 °C, t _p = 400 μs square Average power = V _{T(TO)} × I _{T(AV)} + r _f × (I _{T(RMS)}) ²			1.60	1.55	1.55	V
Maximum forward voltage drop	V _{FM}	I _{TM} = π × I _{T(AV)} , T _J = 25 °C, t _p = 400 μs square Average power = V _{T(TO)} × I _{T(AV)} + r _f × (I _{T(RMS)}) ²			1.60	1.55	1.55	V
Maximum holding current	I _H	Anode supply = 6 V, initial I _T = 30 A, T _J = 25 °C			200	200	200	mA
Maximum latching current	I _L	Anode supply = 6 V, resistive load = 10 Ω Gate pulse: 10 V, 100 μs, T _J = 25 °C			400	400	400	

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Typical turn-on time	t_{gd}	$T_J = 25^\circ\text{C}$, $V_d = 50\%$ V_{DRM} , $I_{TM} = 50$ A $I_g = 500$ mA, $t_r \leq 0.5$, $t_p \geq 6 \mu\text{s}$	0.9	μs
Typical reverse recovery time	t_{rr}	$T_J = 125^\circ\text{C}$, $I_{TM} = 50$ A, $t_p = 300 \mu\text{s}$, $dI/dt = 10$ A/μs	3	
Typical turn-off time	t_q	$T_J = T_J$ maximum, $I_{TM} = 50$ A, $t_p = 300 \mu\text{s}$, $dI/dt = 15$ A/μs, $V_R = 100$ V, linear to 80 % V_{DRM}	110	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = T_J$ maximum	15	mA
RMS isolation voltage	V_{ISOL}	50 Hz, circuit to base, all terminals shorted, $T_J = 25^\circ\text{C}$, $t = 1$ s	3500	V
Critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 80 % rated V_{DRM} ⁽¹⁾	500	V/μs

Note

⁽¹⁾ Available with $dV/dt = 1000$ V/μs, to complete code add S90 i.e. T90RIA80S90



TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES T50RIA	VALUES T70RIA	VALUES T90RIA	UNIT S
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10	12	12	W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, $f = 50$ Hz	2.5	3	3	
Maximum peak gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	2.5	3	3	A
Maximum peak negative gate voltage	$-V_{GT}$		10	10	10	V
Maximum required DC gate voltage to trigger	V_{GT}	$T_J = -40$ °C	4.0	4.0	4.0	V
		$T_J = 25$ °C	2.5	2.5	2.5	
		$T_J = T_J$ maximum	1.5	1.5	1.5	
Maximum required DC gate current to trigger	I_{GT}	$T_J = -40$ °C	250	270	270	mA
		$T_J = 25$ °C	100	120	120	
		$T_J = T_J$ maximum	50	60	60	
Maximum gate voltage that will not trigger	V_{GD}	$T_J = T_J$ maximum, rated V_{DRM} applied	0.2	0.2	0.2	V
Maximum gate current that will not trigger	I_{GD}		5.0	6.0	6.0	mA
Maximum rate of rise of turned-on current	di/dt	$V_D = 0.67$ rated V_{DRM} , $I_{TM} = 2 \times$ rated di/dt $I_g = 400$ mA for T50RIA and $I_g = 500$ mA for T70RIA/T90RIA; $t_r < 0.5$ μ s, $t_p \geq 6$ μ s For repetitive value use 40 % non-repetitive per JEDEC® STD. RS397, 5.2.2.6	200	200	200	A/ μ s
			180	180	180	
			160	160	160	
			150	150	150	

THERMAL AND MECHANICAL SPECIFICATIONS							
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES T50RIA	VALUES T70RIA	VALUES T90RIA	UNITS
Maximum junction operating temperature range	T _J			-40 to +125			°C
Maximum storage temperature range	T _{Stg}			-40 to +150			
Maximum thermal resistance, junction to case per junction	R _{thJC}	DC operation		0.65	0.50	0.38	K/W
Maximum thermal resistance, case to heatsink	R _{thCS}	Mounting surface, smooth, flat and greased		0.2			
Mounting torque, ± 10 % to heatsink terminals		Non-lubricated threads	M3.5 mounting screws ⁽¹⁾	1.3 ± 10 %			Nm
			M5 screw terminals	3 ± 10 %			
Approximate weight				54			g
Case style				D-55 (T-module)			

Note

- ⁽¹⁾ A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound

ΔR CONDUCTION PER JUNCTION											
DEVICES	SINUSOIDAL CONDUCTION AT T _J MAXIMUM					RECTANGULAR CONDUCTION AT T _J MAXIMUM					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
T50RIA	0.08	0.10	0.13	0.19	0.31	0.06	0.10	0.14	0.20	0.32	K/W
T70RIA	0.07	0.08	0.10	0.14	0.24	0.05	0.08	0.11	0.15	0.24	
T90RIA	0.05	0.06	0.08	0.12	0.20	0.04	0.06	0.09	0.12	0.20	

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

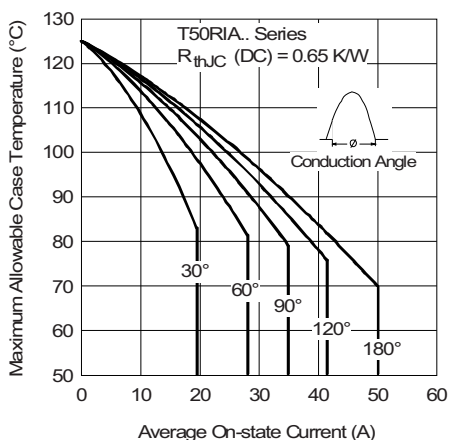


Fig. 1 - Current Ratings Characteristics

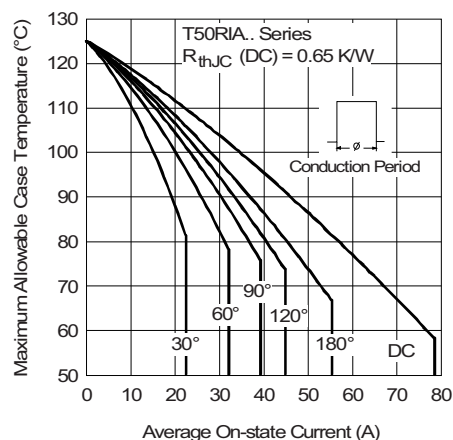


Fig. 2 - Current Ratings Characteristics

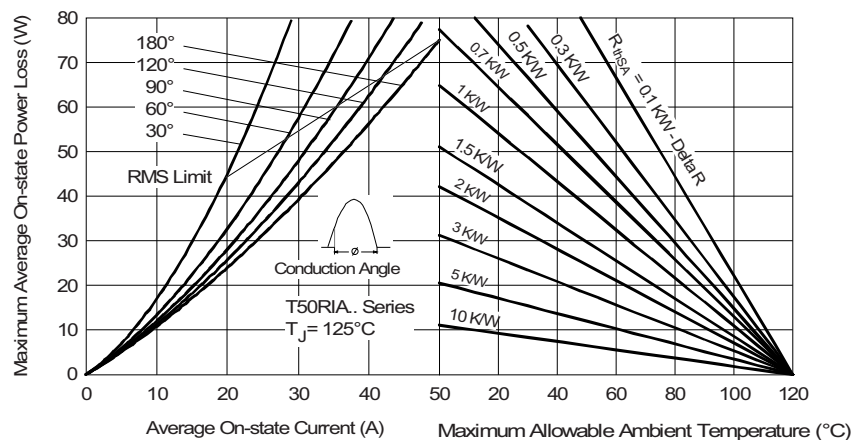


Fig. 3 - On-State Power Loss Characteristics

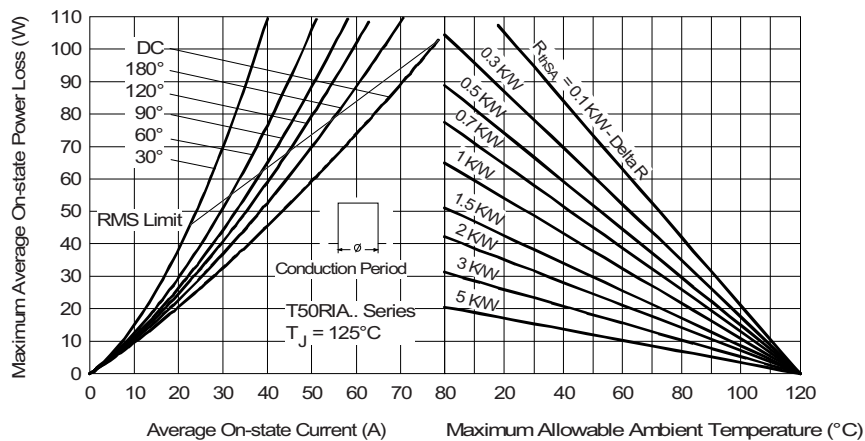


Fig. 4 - On-State Power Loss Characteristics

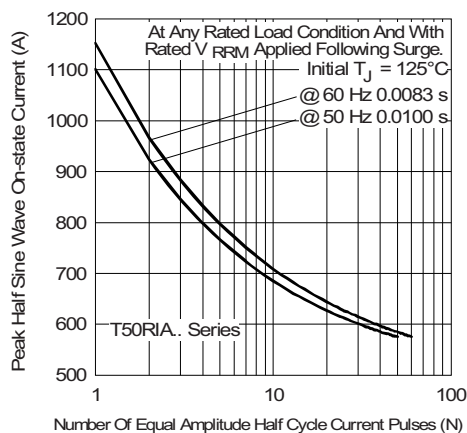


Fig. 5 - Maximum Non-Repetitive Surge Current

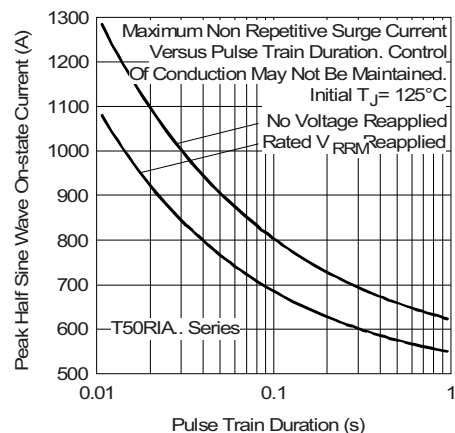


Fig. 6 - Maximum Non-Repetitive Surge Current

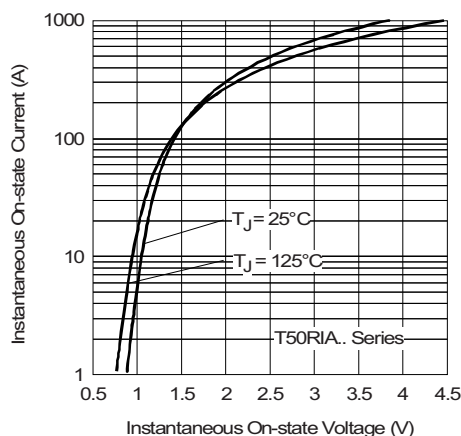


Fig. 7 - On-State Voltage Drop Characteristics

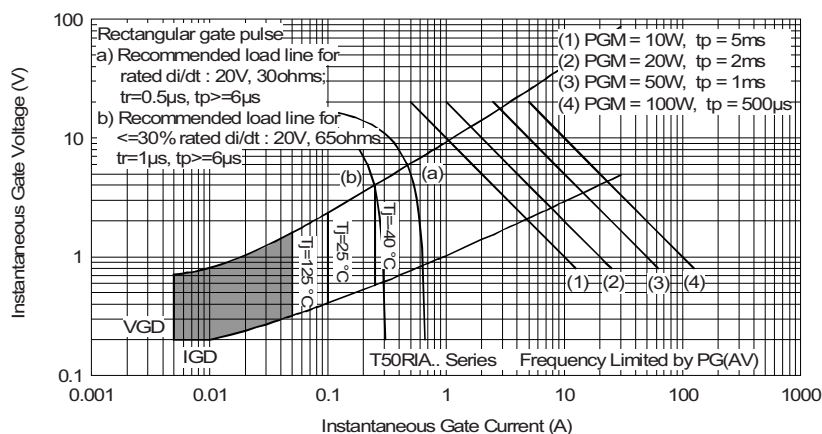


Fig. 8 - Gate Characteristics

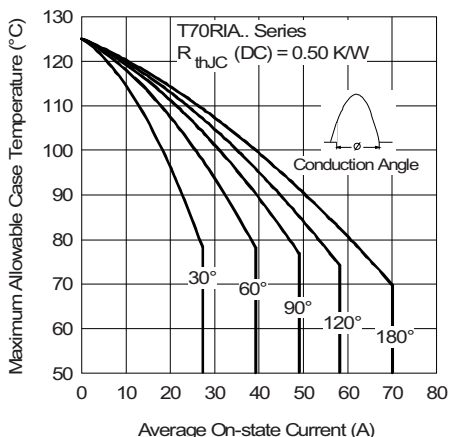


Fig. 9 - Current Ratings Characteristics

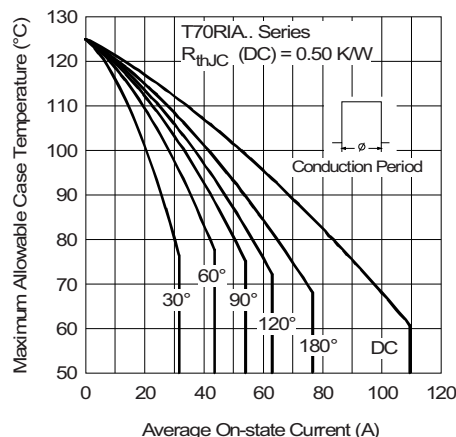


Fig. 10 - Current Ratings Characteristics

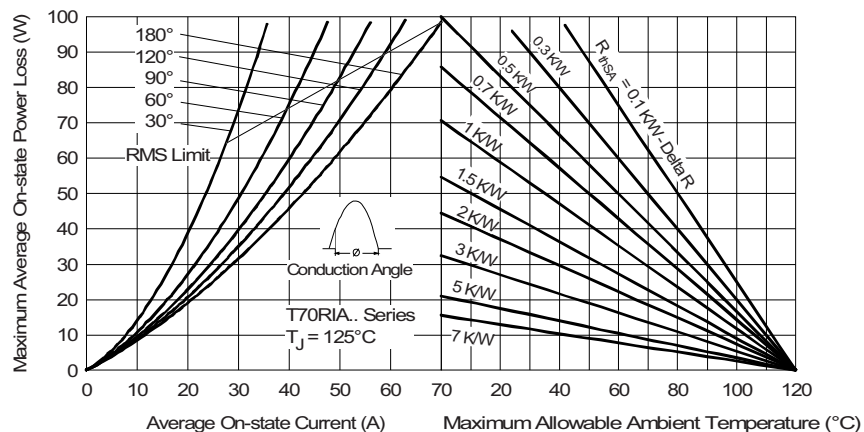


Fig. 11 - On-State Power Loss Characteristics

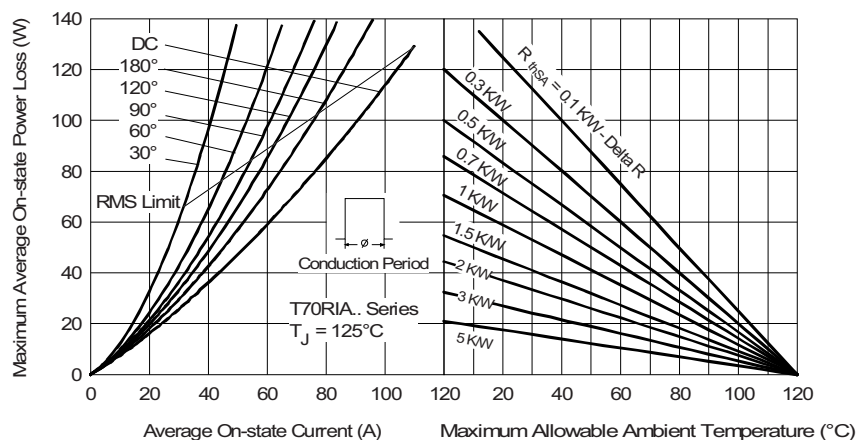


Fig. 12 - On-State Power Loss Characteristics

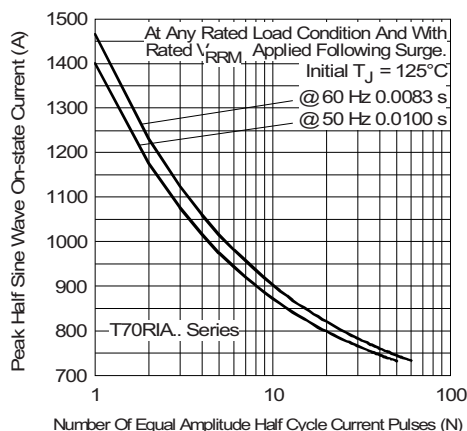


Fig. 13 - Maximum Non-Repetitive Surge Current

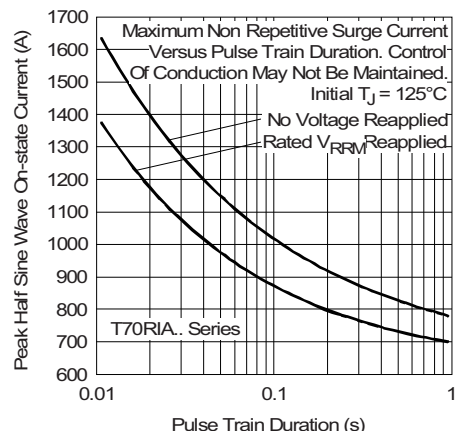


Fig. 14 - Maximum Non-Repetitive Surge Current

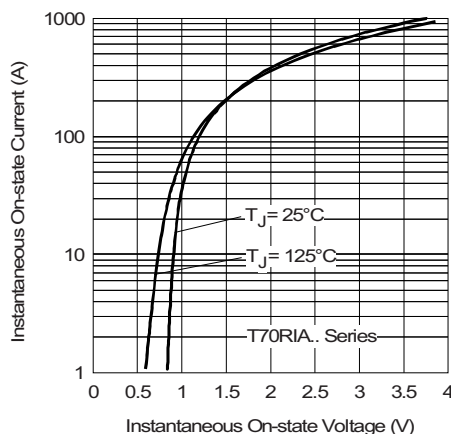


Fig. 15 - On-State Voltage Drop Characteristics

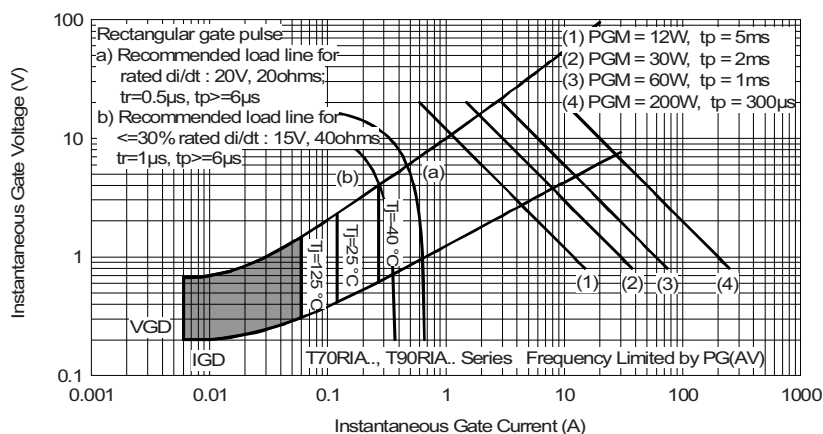


Fig. 16 - Gate Characteristics

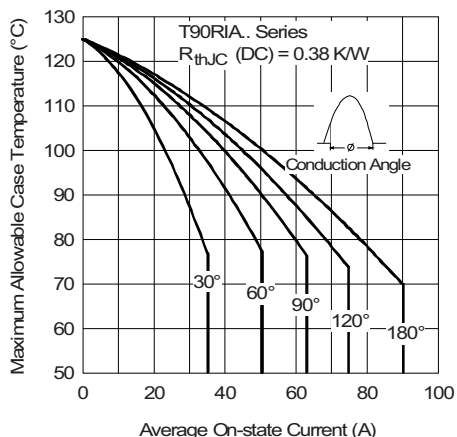


Fig. 17 - Current Ratings Characteristics

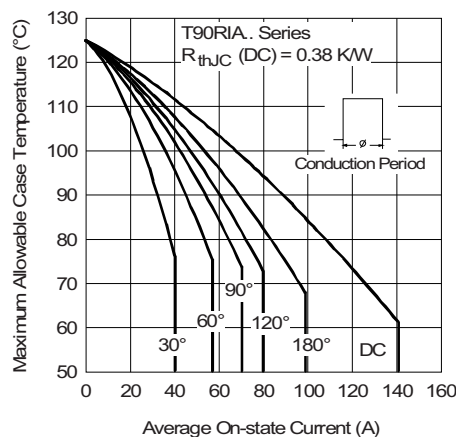


Fig. 18 - Current Ratings Characteristics

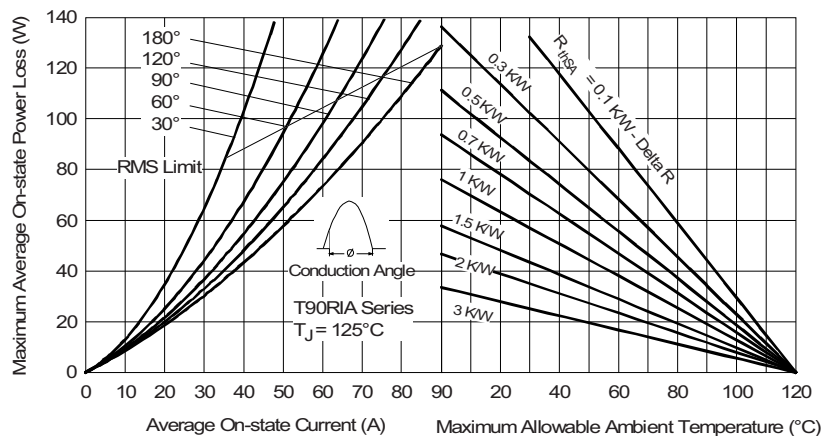


Fig. 19 - On-State Power Loss Characteristics

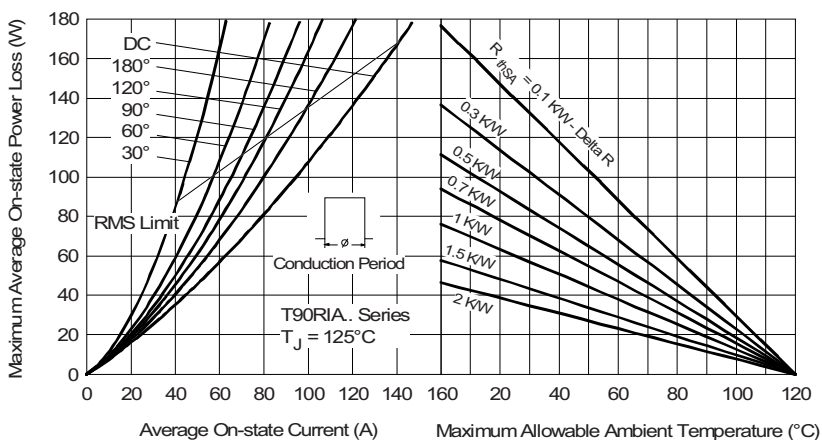


Fig. 20 - On-State Power Loss Characteristics

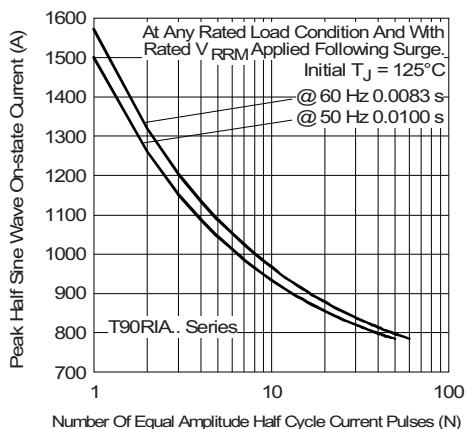


Fig. 21 - Maximum Non-Repetitive Surge Current

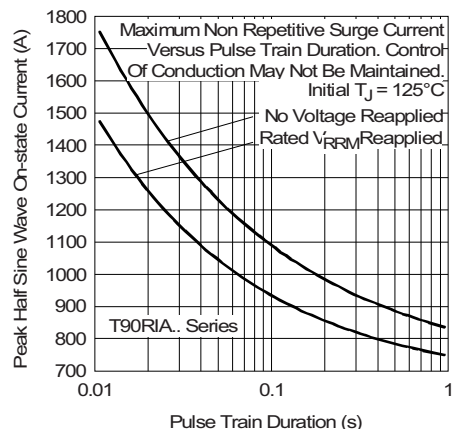


Fig. 22 - Maximum Non-Repetitive Surge Current

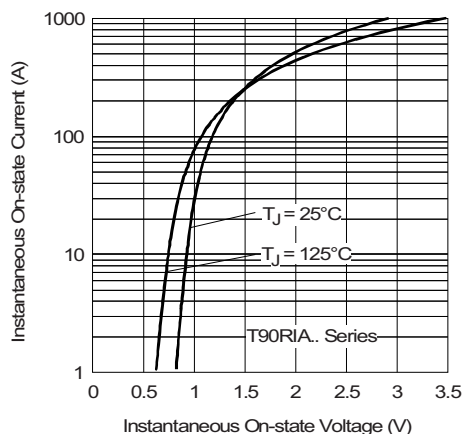


Fig. 23 - On-State Voltage Drop Characteristics

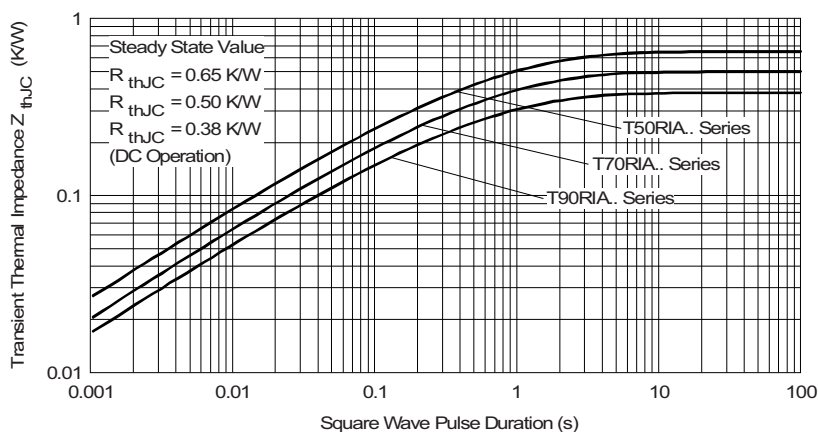


Fig. 24 - Thermal Impedance Z_{thJC} Characteristics



ORDERING INFORMATION TABLE

Device code	VS-	T	50	RIA	120
	1	2	3	4	5

1	-	Vishay Semiconductors product
2	-	Module type
3	-	Current rating
4	-	Circuit configuration
5	-	Voltage code x 10 = V_{RRM}

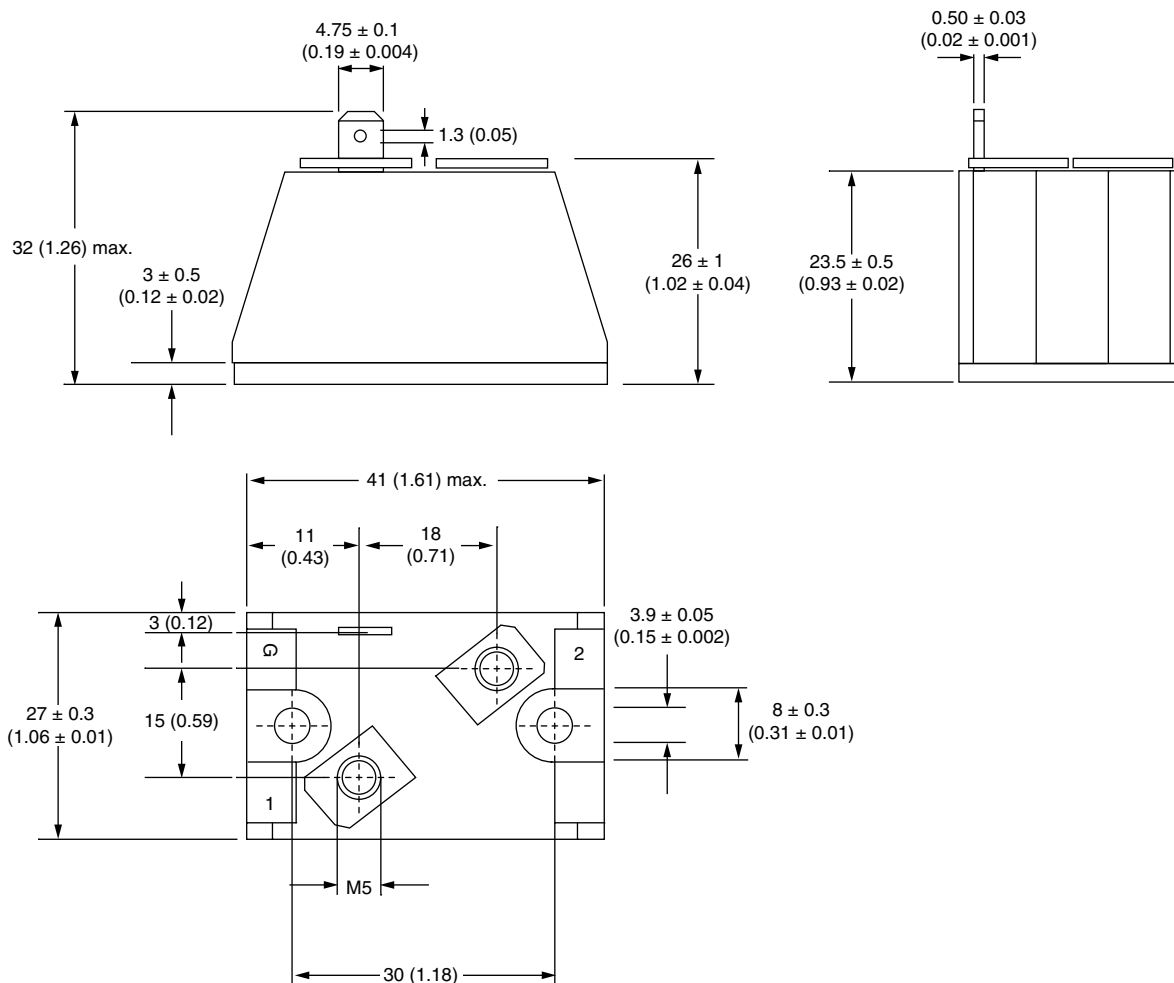
CIRCUIT CONFIGURATION	
CIRCUIT DESCRIPTION	CIRCUIT DRAWING
Single SCR	

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95336



D-55 (T-Module) Thyristor Standard

DIMENSIONS in millimeters (inches)



Note

- 1 = anode
- 2 = cathode



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