# Enpirion® Power Datasheet
# ER3125QI 2.5 A Regulator with Integrated High-Side MOSFET for Synchronous Buck or Boost Buck Converter



The ER3125QI is a 36V, 2.5A synchronous buck or boost buck controller with a high-side MOSFET and low-side driver integrated. In buck mode, the ER3125QI supports a wide input range of 3V to 36V. In boost-buck mode, the input range can be extended down to 2.5V and output regulation can be maintained when $V_{PVIN}$ drops below $V_{OUT}$, enabling sensitive electronics to remain on in low input voltage conditions.

The ER3125QI has a flexible selection of operation modes of forced PWM mode and LLM mode. In LLM mode, the quiescent input current is as low as 180µA (AVIN connected to $V_{OUT}$). The load boundary between LLM and PWM can be programmed to cover wide applications.

The low-side driver can be either used to drive an external low-side MOSFET for a synchronous buck, or left unused for a standard non-synchronous buck. The low-side driver can also be used to drive a boost converter as a pre-regulator followed by a buck controlled by the same IC, which greatly expands the operating input voltage range down to 2.5V or lower (Refer to "Typical Application Schematic III - Boost Buck Converter" on page 4).

The ER3125QI offers the most robust current protections. It uses peak current mode control with cycle-by-cycle current limiting. It is implemented with frequency foldback under current limit condition; besides that, the hiccup overcurrent mode is also implemented to guarantee reliable operations under short circuit conditions.

The ER3125QI has comprehensive protections against various faults including overvoltage and over-temperature protections, etc.

## Features

- Buck mode: input voltage range 3V to 36V (refer to "Input Voltage" on page 16 for more details)
- Boost mode expands operating input voltage lower than 2.5V (refer to "Input Voltage" on page 16 for more details)
- Selectable forced PWM mode or LLM mode
- 300µA IC quiescent current (LLM, no load); 180µA input quiescent current (LLM, no load, $V_{OUT}$ tied to AVIN)
- Less than 5µA (MAX) shutdown input current (IC disabled)
- Operational topologies
  - Synchronous buck
  - Non-synchronous buck
  - Two-stage boost buck
  - Non-inverting single inductor buck boost
- Programmable frequency from 200kHz to 2.2MHz and frequency synchronization capability
- ±1% tight voltage regulation accuracy
- Reliable overcurrent protection
  - Temperature compensated current sense
  - Cycle-by-cycle current limiting with frequency foldback
  - Hiccup mode for worst case short condition
- 20 Ld 4x4 QFN package
- Pb-free (RoHS compliant)

## Applications

- FPGA Applications
- General purpose
- 24V bus power
- Battery power
- Point of load
- Embedded processor and I/O supplies

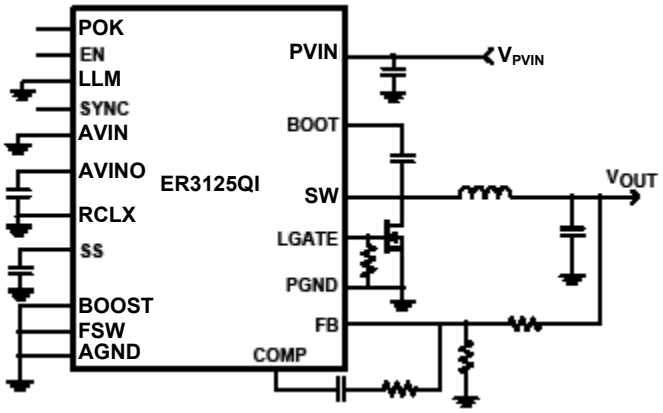



FIGURE 1. TYPICAL APPLICATION

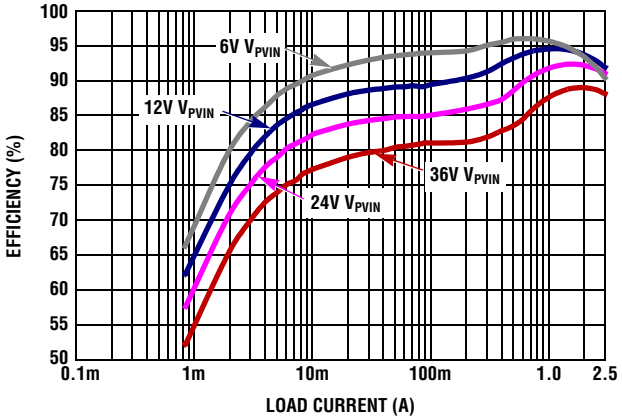



FIGURE 2. EFFICIENCY, SYNCHRONOUS BUCK, LLM MODE, $V_{OUT}$ 5V, $T_A$ = +25°C

101 Innovation Drive
San Jose, CA 95134
www.altera.com

# Ordering Information

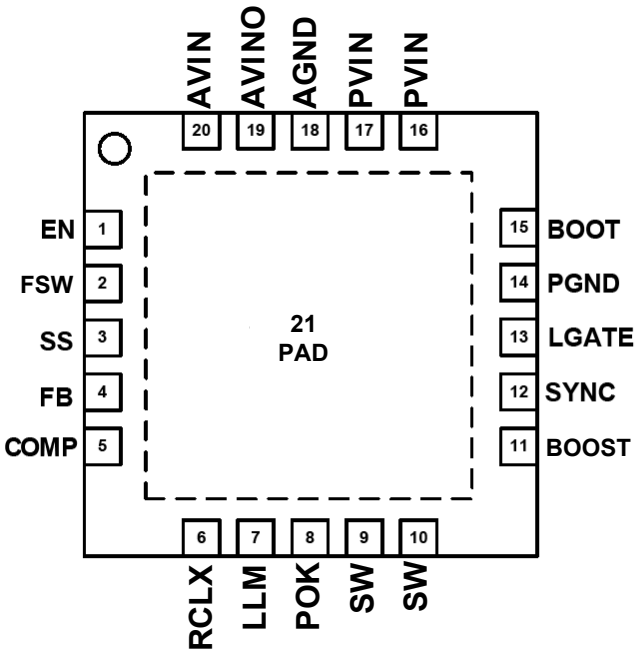
| PART NUMBER (Notes 1, 2) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (PB-Free) | PKG. DWG. # |
|---|---|---|---|---|
| ER3125QI | R3125 | -40 to +105 | 20 Ld 4x4 QFN | L20.4x4C |

NOTES:

1. Please refer to Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html
2. These Altera Enpirion Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Altera Enpirion Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

# Pin Configuration

ER3125QI
(20 LD QFN)
TOP VIEW




# Functional Pin Descriptions

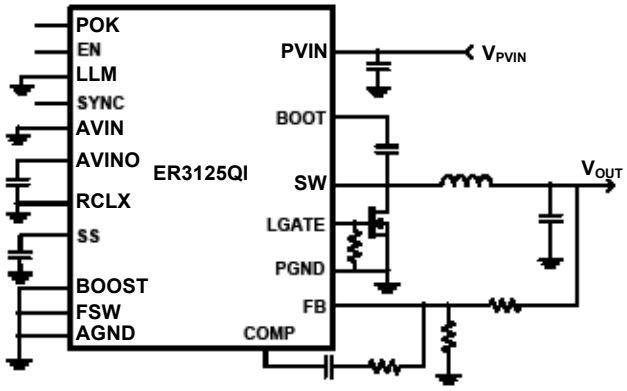
| PIN NAME | PIN # | DESCRIPTION |
|---|---|---|
| EN | 1 | The controller is enabled when this pin is left floating or pulled HIGH. The IC is disabled when this pin is pulled LOW. Range: 0V to 5.5V. |
| FSW | 2 | Connecting this pin to AVINO, or GND, or leaving it open will force the IC to have 500kHz switching frequency. The oscillator switching frequency can also be programmed by adjusting the resistor from this pin to GND. |
| SS | 3 | Connect a capacitor from this pin to ground. This capacitor, along with an internal 5µA current source, sets the soft-start interval of the converter. Also, this pin can be used to track a ramp on this pin. |
| FB | 4 | This pin is the inverting input of the voltage feedback error amplifier. With a properly selected resistor divider connected from $V_{OUT}$ to FB, the output voltage can be set to any voltage between the power rail (reduced by maximum duty cycle and voltage drop) and the 0.8V reference. Loop compensation is achieved by connecting an RC network across COMP and FB. The FB pin is also monitored for overvoltage events. |
| COMP | 5 | Output of the voltage feedback error amplifier. |
| RCLX | 6 | Programmable current limit pin. With this pin connected to the AVINO pin, or to GND, or left open, the current limiting threshold is set to default of 3.6A; the current limiting threshold can be programmed with a resistor from this pin to GND. |

# Functional Pin Descriptions (Continued)

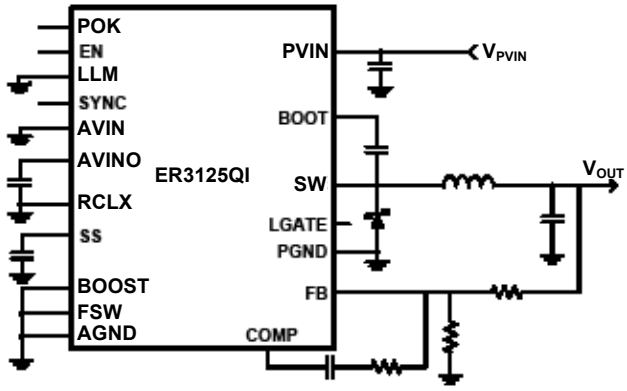
| PIN NAME | PIN # | DESCRIPTION |
|---|---|---|
| LLM | 7 | Light load mode selection pin. Pull this pin to GND for forced PWM mode; to have it floating or connected to AVINO will enable LLM mode when the peak inductor current is below the default threshold of 700mA. The current boundary threshold between LLM and PWM can also be programmed with a resistor at this pin to ground. Check for more details in the "LLM Mode Operation" on page 15. |
| POK | 8 | POK is an open drain output and pull-up pin with a resistor to AVINO for proper function. POK will be pulled low under the events when the output is out of regulation (OV or UV) or EN pin is pulled low. POK rising has a fixed 128 cycles delay. |
| SW | 9, 10 | These pins are the SW nodes that should be connected to the output inductor. These pins are connected to the source of the high-side N-channel MOSFET. |
| BOOST | 11 | This pin is used to set boost mode and monitor the battery voltage that is the input of the boost converter. After AVINO POR, the controller will detect the voltage on this pin; if voltage on this pin is below 200mV, the controller is set in synchronous/non-synchronous buck mode and will latch in this state unless AVINO is below POR falling threshold; if the voltage on this pin after AVINO POR is above 200mV, the controller is set in boost mode and latches in this state. In boost mode, the low-side driver output PWM with same duty cycle with upper-side driver to drive the boost switch.<br>In boost mode, this pin is used to monitor input voltage through a resistor divider. By setting the resistor divider, the high threshold and hysteresis can be programmed. When voltage on this pin is above 0.8V, the PWM output (LGATE) for the boost converter is disabled, and when voltage on this pin is below 0.8V minus the hysteresis, the boost PWM is enabled.<br>In boost mode operation, LLM is disabled when boost PWM is enabled. Check the "2-Stage Boost Buck Converter Operation" on page 17 for more details. |
| SYNC | 12 | This pin can be used to synchronize two or more ER3125QI controllers. Multiple ER3125QIs can be synchronized with their SYNC pins connected together. 180° phase shift is automatically generated between the master and slave ICs.<br>The internal oscillator can also lock to an external frequency source applied on this pin with square pulse waveform (with frequency 10% higher than the IC's local frequency, and pulse width higher than 150ns). Range: 0V to 5.5V.<br>This pin should be left floating if not used. |
| LGATE | 13 | In synchronous buck mode, this pin is used to drive the lower side MOSFET to improve efficiency. A 5.1k or smaller value resistor has to be added to connect LGATE to ground to avoid falsely turn-on of LGATE caused by coupling noise.<br>In non-synchronous buck when a diode is used as the bottom side power device, this pin should be connected to AVINO through a resistor (less than 5k) before IC start-up to have the low-side driver (LGATE) disabled.<br>In boost mode, it can be used to drive the boost power MOSFET. The boost control PWM is same with the buck control PWM. |
| PGND | 14 | This pin is used as the ground connection of the power flow including driver. Connect it to large ground plane. |
| BOOT | 15 | This pin provides bias voltage to the high-side MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive the internal N-channel MOSFET. The boot charge circuitries are integrated inside of the IC. No external boot diode is needed. A 1µF ceramic capacitor is recommended to be used between BOOT and SW pin. |
| PVIN | 16, 17 | Connect the input rail to these pins that are connected to the drain of the integrated high-side MOSFET as well as the source for the internal linear regulator that provides the bias of the IC. Range: 3V to 36V.<br>With the part switching, the operating input voltage applied to the PVIN pins must be under 36V. This recommendation allows for short voltage ringing spikes (within a couple of ns time range) due to switching while not exceeding "Absolute Maximum Ratings" on page 5. |
| AGND | 18 | This pin provides the return path for the control and monitor portions of the IC. Connect it to a quiet ground plane. |
| AVINO | 19 | This pin is the output of the internal linear regulator that supplies the bias for the IC including the driver. A minimum 4.7µF decoupling ceramic capacitor is recommended between AVINO to ground. |
| AVIN | 20 | This pin is the input of the auxiliary internal linear regulator, which can be supplied by the regulator output after power-up. With such configuration, the power dissipation inside of the IC is reduced. The input range for this LDO is 3V to 20V.<br>In boost mode operation, this pin works as boost output overvoltage detection pin. It detects the boost output through a resistor divider. When voltage on this pin is above 0.8V, the boost PWM is disabled; and when voltage on this pin is below 0.8V minus the hysteresis, the boost PWM is enabled.<br>Range: 0V to 20V. |
| PAD | 21 | Bottom thermal pad. It is not connected to any electrical potential of the IC. In layout it must be connected to PCB ground copper plane with area as large as possible to effectively reduce the thermal impedance. |

# Typical Application Schematics

## Typical Application Schematic I

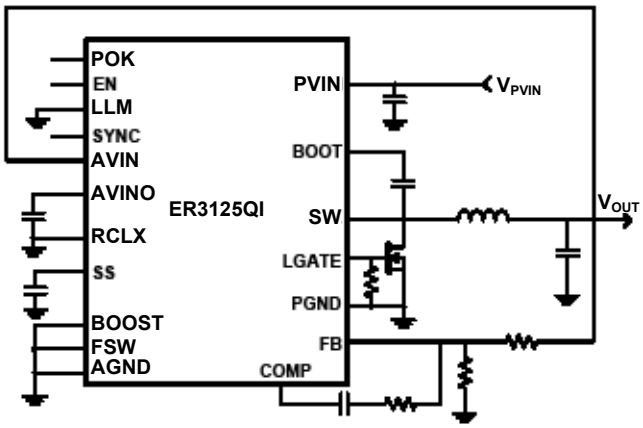



(a) SYNCHRONOUS BUCK

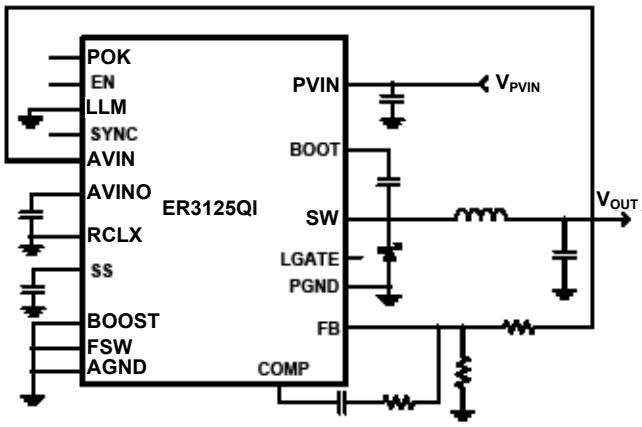



(b) NON-SYNCHRONOUS BUCK

## Typical Application Schematic II - AVINO Switch-Over to $V_{OUT}$

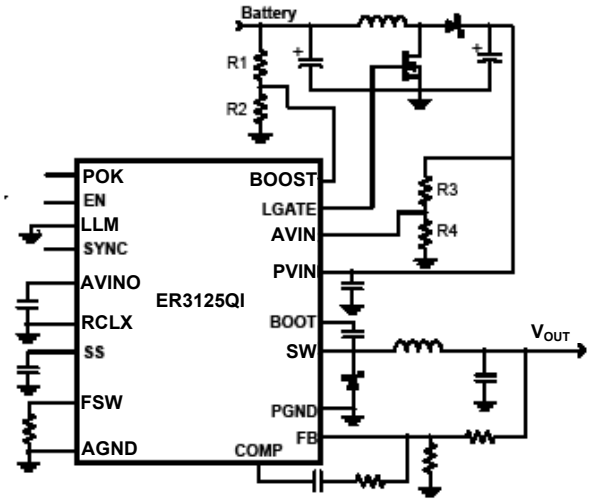



(a) SYNCHRONOUS BUCK

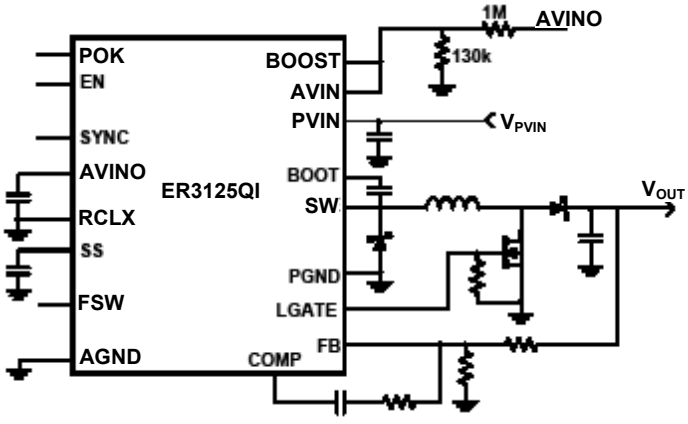



(b) NON-SYNCHRONOUS BUCK

## Typical Application Schematic III - Boost Buck Converter




(a) 2-STAGE BOOST BUCK




(b) NON-INVERTING SINGLE INDUCTOR BUCK BOOST

## Absolute Maximum Ratings

PVIN, SW . . . . . GND - 0.3V to +44V
AVINO . . . . . .GND - 0.3V to +6.0V
AVIN . . . . . GND - 0.3V to +22V
Absolute Boot Voltage, $V_{BOOT}$ . . . . . .+50.0V
Upper Driver Supply Voltage, $V_{BOOT}$ - $V_{SW}$ . . . . . .+6.0V
All Other Pins . . . . . GND - 0.3V to AVINO + 0.3V
ESD Rating
Human Body Model (Tested per JESD22-A114F) . . . . .2.5kV
Machine Model (Tested per JESD22-A115C) . . . . . 250V
Charged Device Model (Tested per JESD22-C101E) . . . . 1kV
Latchup Rating (Tested per JESD78B; Class II, Level A)100mA

## Thermal Information

| Thermal Resistance | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| QFN 4x4 Package (Notes 3, 4) . . . . . | 40 | 3.5 |

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C

## Recommended Operating Conditions

Supply Voltage on $V_{PVIN}$ . . . . . .3V to 36V
AVIN. . . . . .GND - 0.3V to +20V
Ambient Temperature Range . . . . . .-40°C to +105°C
Junction Temperature Range. . . . . .-40°C to +125°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

3. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.
4. For $\theta_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.

## Electrical Specifications

Refer to "Block Diagram" on page 14 and "Typical Application Schematics" on page 4. Operating Conditions Unless Otherwise Noted: $V_{PVIN}$ = 12V, or $V_{AVINO}$ = 4.5V ±10%, $T_A$ = -40°C to +105°C. Typicals are at $T_A$ = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C.**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 5) | TYP | MAX (Note 5) | UNITS |
|---|---|---|---|---|---|---|
| PVIN PIN SUPPLY | | | | | | |
| PVIN Pin Voltage Range | | PVIN Pin | **3.05** | | **36** | V |
| | | PVIN Pin connected to AVINO | **3.05** | | **5.5** | V |
| Operating Supply Current | $I_Q$ | LLM = AVINO/FLOATING, no load at the output | | 300 | | µA |
| | | LLM = GND (forced PWM), $V_{PVIN}$ = 12V, IC operating, not including driving current | | 1.3 | | mA |
| Shutdown Supply Current | $I_{IN\_SD}$ | EN connected to GND, $V_{PVIN}$ = 12V | | 2.8 | **4.5** | µA |
| INTERNAL MAIN LINEAR REGULATOR | | | | | | |
| MAIN LDO $V_{AVINO}$ Voltage | $V_{AVINO}$ | $V_{PVIN}$ > 5V | **4.2** | 4.5 | **4.8** | V |
| MAIN LDO Dropout Voltage | $V_{DROPOUT\_MAIN}$ | $V_{PVIN}$ = 4.2V, $I_{AVINO}$ = 35mA | | 0.3 | **0.52** | V |
| | | $V_{PVIN}$ = 3V, $I_{AVINO}$ = 25mA | | 0.25 | **0.42** | V |
| $V_{AVINO}$ Current Limit of MAIN LDO | | | | 60 | | mA |
| INTERNAL AUXILIARY LINEAR REGULATOR | | | | | | |
| AVIN Input Voltage Range | $V_{AVIN}$ | | **3** | | **20** | V |
| AUX LDO $V_{AVINO}$ Voltage | $V_{AVINO}$ | $V_{AVIN}$ > 5V | **4.2** | 4.5 | **4.8** | V |
| LDO Dropout Voltage | $V_{DROPOUT\_AUX}$ | $V_{AVIN}$ = 4.2V, $I_{AVINO}$ = 35mA | | 0.3 | **0.52** | V |
| | | $V_{AVIN}$ = 3V, $I_{AVINO}$ = 25mA | | 0.25 | **0.42** | V |
| Current Limit of AUX LDO | | | | 60 | | mA |
| AUX LDO Switch-over Rising Threshold | $V_{AVIN\_RISE}$ | AVIN voltage rise; Switch to auxiliary LDO | **3** | 3.1 | **3.2** | V |
| AUX LDO Switch-over Falling Threshold Voltage | $V_{AVIN\_FALL}$ | AVIN voltage fall; Switch back to main BIAS LDO | **2.73** | 2.87 | **2.97** | V |
| AUX LDO Switch-over Hysteresis | $V_{AVIN\_HYS}$ | AVIN switch-over hysteresis | | 0.2 | | V |

## Electrical Specifications

Refer to "Block Diagram" on page 14 and "Typical Application Schematics" on page 4. Operating Conditions Unless Otherwise Noted: $V_{PVIN}$ = 12V, or $V_{AVINO}$ = 4.5V ±10%, $T_A$ = -40°C to +105°C. Typicals are at $T_A$ = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 5) | TYP | MAX (Note 5) | UNITS |
|---|---|---|---|---|---|---|
| POWER-ON RESET | | | | | | |
| Rising $V_{AVINO}$ POR Threshold | $V_{PORH\_RISE}$ | | **2.82** | 2.9 | **3.05** | V |
| Falling $V_{AVINO}$ POR Threshold | $V_{PORL\_FALL}$ | | | 2.6 | **2.8** | V |
| $V_{AVINO}$ POR Hysteresis | $V_{PORL\_HYS}$ | | | 0.3 | | V |
| ENABLE | | | | | | |
| Enable On Voltage | $V_{ENH}$ | | **1.7** | | | V |
| Enable Off voltage | $V_{ENL}$ | | | | **1** | V |
| EN Pull-up Current | $I_{EN\_PULLUP}$ | $V_{EN}$ = 1.2V, $V_{PVIN}$ = 24V | | 1.5 | | µA |
| | | $V_{EN}$ = 1.2V, $V_{PVIN}$ = 12V | | 1.2 | | µA |
| | | $V_{EN}$ = 1.2V, $V_{PVIN}$ = 5V | | 0.9 | | µA |
| OSCILLATOR | | | | | | |
| PWM Frequency | $F_{OSC}$ | $R_T$ = 665kΩ | **160** | 200 | **240** | kHz |
| | | $R_T$ = 51.1kΩ | **1870** | 2200 | **2530** | kHz |
| | | FSW pin connected to AVINO or floating or GND | **450** | 500 | **550** | kHz |
| MIN ON Time | $t_{MIN\_ON}$ | | | 130 | **225** | ns |
| MIN OFF Time | $t_{MIN\_OFF}$ | | | 210 | **330** | ns |
| SYNCHRONIZATION | | | | | | |
| Input High Threshold | VIH | | | 2 | | V |
| Input Low Threshold | VIL | | | 0.5 | | V |
| Input Minimum Pulse Width | | | | 25 | | ns |
| Input Impedance | | | | 100 | | kΩ |
| Input Minimum Frequency Divided by Free Running Frequency | | | | 1.1 | | |
| Input Maximum Frequency Divided by Free Running Frequency | | | | 1.6 | | |
| Output Pulse Width | | $C_{SYNC}$ = 100pF | | 100 | | ns |
| Output Pulse High | VOH | $R_{LOAD}$ = 1kΩ | | AVINO-0.25 | | V |
| Output Pulse Low | VOL | | | GND | | V |
| REFERENCE VOLTAGE | | | | | | |
| Reference Voltage | $V_{REF}$ | | | 0.8 | | V |
| System Accuracy | | | **-1.0** | | **+1.0** | % |
| FB Pin Source Current | | | | 5 | | nA |
| Soft-start | | | | | | |
| Soft-Start Current | $I_{SS}$ | | **3** | 5 | **7** | µA |
| ERROR AMPLIFIER | | | | | | |
| Unity Gain-Bandwidth | | $C_{LOAD}$ = 50pF | | 10 | | MHz |
| DC Gain | | $C_{LOAD}$ = 50pF | | 88 | | dB |

## Electrical Specifications

Refer to "Block Diagram" on page 14 and "Typical Application Schematics" on page 4. Operating Conditions Unless Otherwise Noted: $V_{PVIN}$ = 12V, or $V_{AVINO}$ = 4.5V ±10%, $T_A$ = -40°C to +105°C. Typicals are at $T_A$ = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 5) | TYP | MAX (Note 5) | UNITS |
|---|---|---|---|---|---|---|
| Maximum Output Voltage | | | | 3.6 | | V |
| Minimum Output Voltage | | | | 0.5 | | V |
| Slew Rate | SR | $C_{LOAD}$ = 50pF | | 5 | | V/µs |
| LLM CONTROL | | | | | | |
| Default LLM Current Threshold | | LLM = AVINO or floating | | 700 | | mA |
| INTERNAL HIGH-SIDE MOSFET | | | | | | |
| Upper MOSFET $R_{DS(ON)}$ | $R_{DS(ON)\_UP}$ | Limits apply for +25°C only | | 127 | 140 | mΩ |
| LOW-SIDE MOSFET GATE DRIVER | | | | | | |
| LGate Source Resistance | | 100mA source current | | 3.5 | | Ω |
| LGATE Sink Resistance | | 100mA sink current | | 2.8 | | Ω |
| BOOST CONVERTER CONTROL | | | | | | |
| BOOST Boost_Off Threshold Voltage | | | **0.74** | 0.8 | **0.86** | V |
| BOOST Hysteresis Sink Current | $I_{BOOST\_HYS}$ | | **2.1** | 3.2 | **4.2** | µA |
| AVIN Boost Turn-Off Threshold Voltage | | | **0.74** | 0.8 | **0.86** | V |
| AVIN Hysteresis Sink Current | $I_{AVIN\_HYS}$ | | **2.1** | 3.2 | **4.2** | µA |
| POWER-GOOD MONITOR | | | | | | |
| Overvoltage Rising Trip Point | $V_{FB}/V_{REF}$ | Percentage of reference point | **104** | 110 | **116** | % |
| Overvoltage Rising Hysteresis | $V_{FB}/V_{OVTRIP}$ | Percentage below OV trip point | | 3 | | % |
| Undervoltage Falling Trip Point | $V_{FB}/V_{REF}$ | Percentage of reference point | **84** | 90 | **96** | % |
| Undervoltage Falling Hysteresis | $V_{FB}/V_{UVTRIP}$ | Percentage above UV trip point | | 3 | | % |
| POK Rising Delay | $t_{POK\_R\_DELAY}$ | | | 128 | | cycle |
| POK Leakage Current | | POK HIGH, $V_{POK}$ = 4.5V | | 10 | | nA |
| POK Low Voltage | $V_{POK}$ | POK LOW, IPOK = 0.2mA | | 0.10 | | V |
| OVERCURRENT PROTECTION | | | | | | |
| Default Cycle-by-Cycle Current Limit Threshold | $I_{OC\_1}$ | $I_{RCLX}$ = GND or AVINO or floating | **3** | 3.6 | **4.2** | A |
| Hiccup Current Limit Threshold | $I_{OC\_2}$ | Hiccup, $I_{OC\_2}/I_{OC\_1}$ | | 115 | | % |
| OVERVOLTAGE PROTECTION | | | | | | |
| OV 120% Trip Point | | Active in and after soft-start.<br>Percentage of reference point<br>LG = UG = LOW | | 120 | | % |
| OV 120% Release Point | | Active in and after soft-start.<br>Percentage of reference point | | 102.5 | | % |
| OV 110% Trip Point | | Active after soft-start done.<br>Percentage of reference point<br>LG = UG = LOW | | 110 | | % |
| OV 110% Release Point | | Active after soft-start done.<br>Percentage of reference point | | 102.5 | | % |
| OVER-TEMPERATURE PROTECTION | | | | | | |
| Over-Temperature Trip Point | | | | 160 | | °C |

## Electrical Specifications

Refer to "Block Diagram" on page 14 and "Typical Application Schematics" on page 4. Operating Conditions Unless Otherwise Noted: $V_{PVIN}$ = 12V, or $V_{AVINO}$ = 4.5V ±10%, $T_A$ = -40°C to +105°C. Typicals are at $T_A$ = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 5) | TYP | MAX (Note 5) | UNITS |
|---|---|---|---|---|---|---|
| Over-Temperature Recovery Threshold | | | | 140 | | °C |

NOTE:

5. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

# Typical Performance Curves

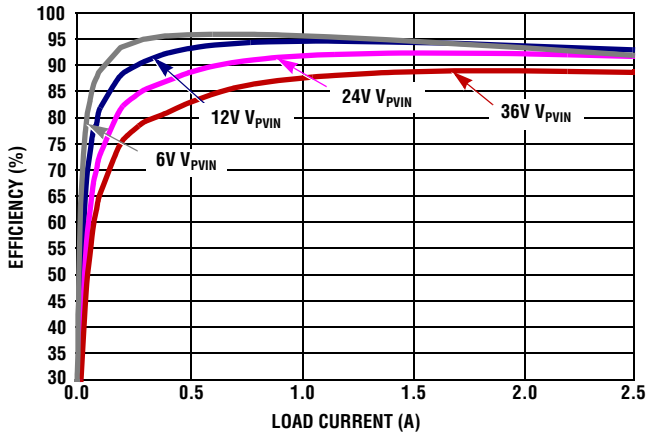



FIGURE 3. EFFICIENCY, SYNCHRONOUS BUCK, FORCED PWM MODE, 500kHz, $V_{OUT}$ 5V, $T_A$ = +25°C

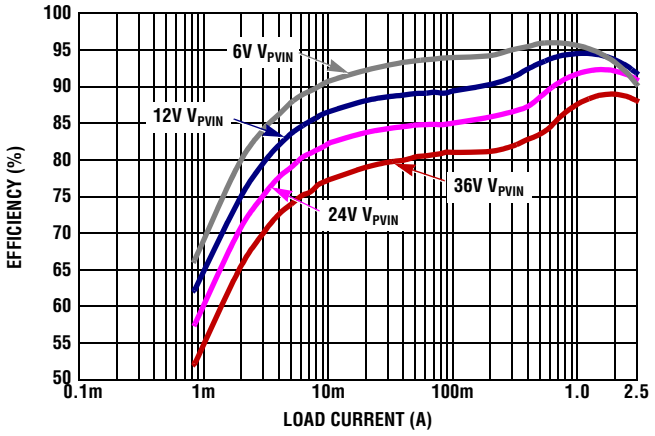



FIGURE 4. EFFICIENCY, SYNCHRONOUS BUCK, LLM MODE, $V_{OUT}$ 5V, $T_A$ = +25°C

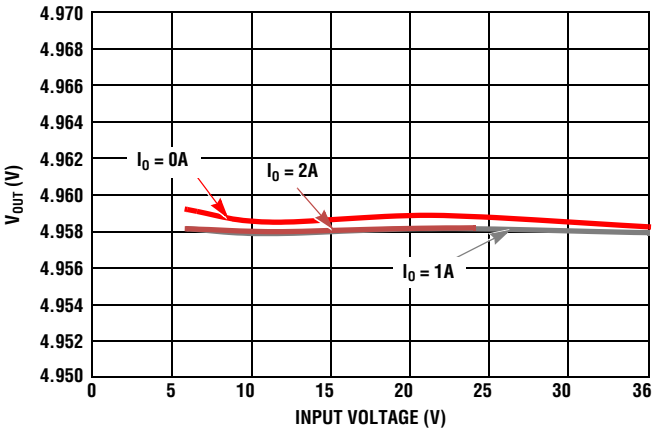



FIGURE 5. LINE REGULATION, $V_{OUT}$ 5V, $T_A$ = +25°C

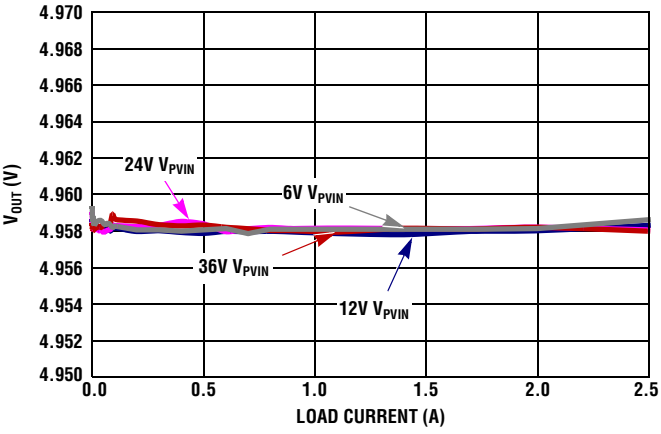



FIGURE 6. LOAD REGULATION, $V_{OUT}$ 5V, $T_A$ = +25°C

# Typical Performance Curves (Continued)

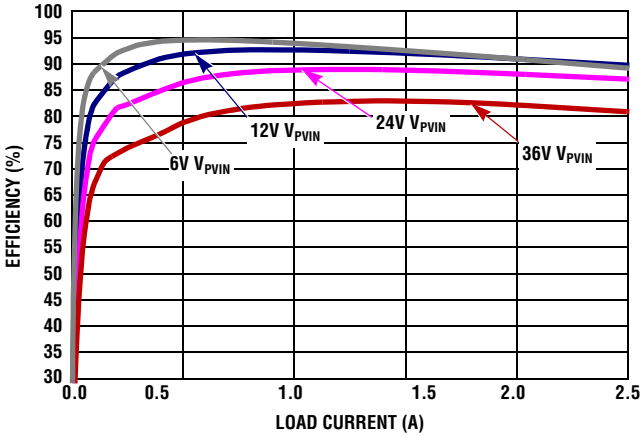



FIGURE 7. EFFICIENCY, SYNCHRONOUS BUCK, FORCED PWM MODE, 500KHZ, $V_{OUT}$ 3.3V, $T_A$ = +25°C

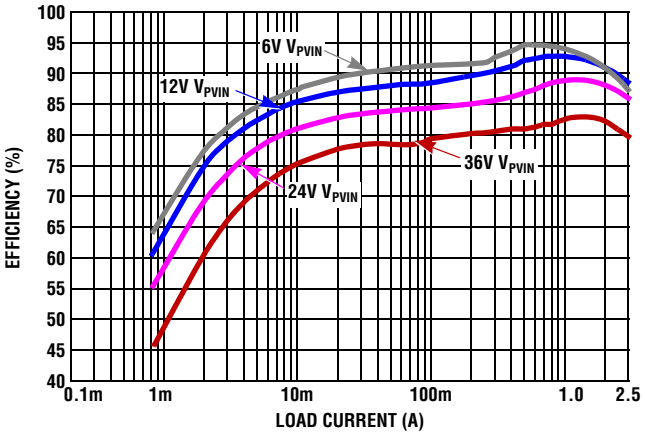



FIGURE 8. EFFICIENCY, SYNCHRONOUS BUCK, LLM MODE, $V_{OUT}$ 3.3V, $T_A$ = +25°C

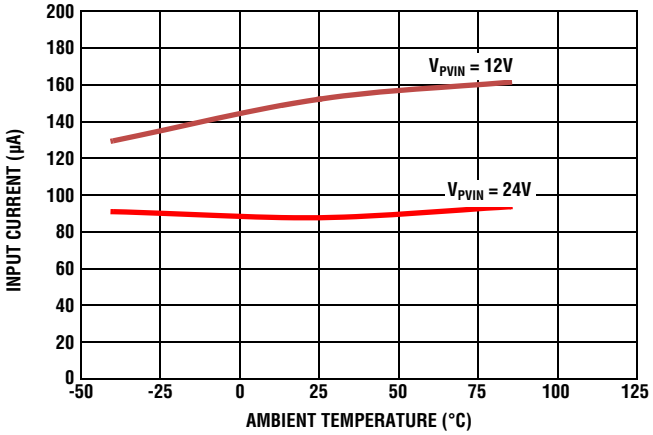



FIGURE 9. INPUT QUIESCENT CURRENT UNDER NO LOAD, LLM MODE, $V_{OUT}$ = 5V

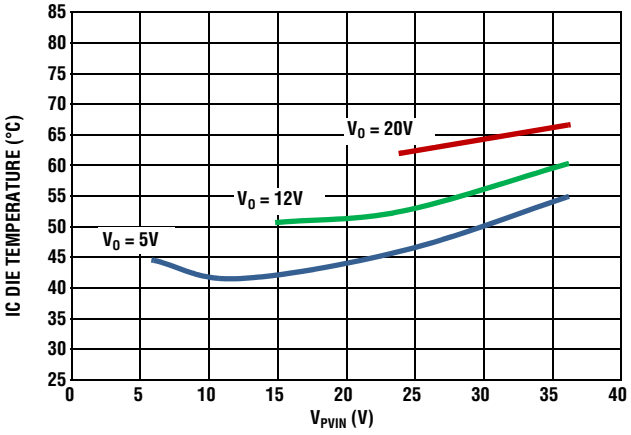



FIGURE 10. IC DIE TEMPERATURE UNDER +25°C AMBIENT TEMPERATURE, STILL AIR, 500KHZ, $I_O$ = 2A

# Typical Performance Curves (Continued)

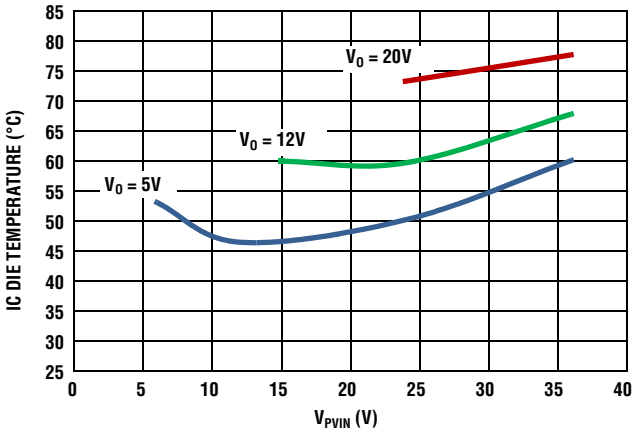



FIGURE 11. IC DIE TEMPERATURE UNDER +25°C AMBIENT TEMPERATURE, STILL AIR, 500KHZ, $I_O$ = 2.5A

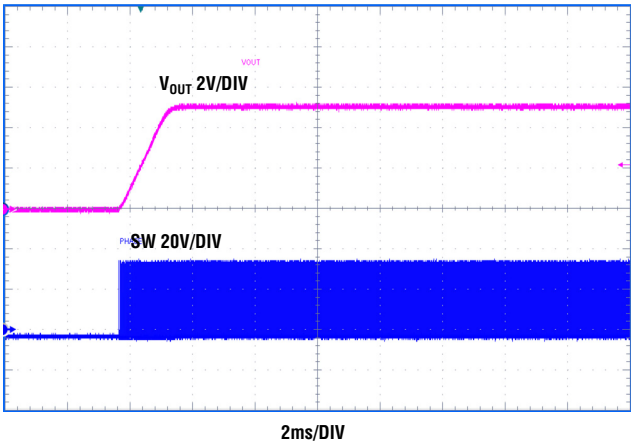



FIGURE 12. SYNCHRONOUS BUCK MODE, $V_{PVIN}$ 36V, $I_O$ 2A, ENABLE ON

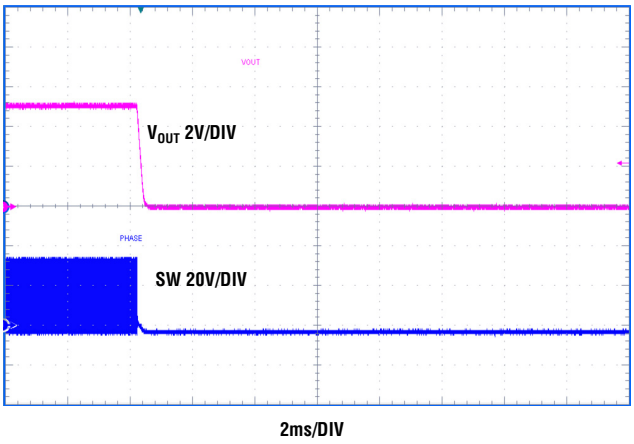



FIGURE 13. SYNCHRONOUS BUCK MODE, $V_{PVIN}$ 36V, $I_O$ 2A, ENABLE OFF

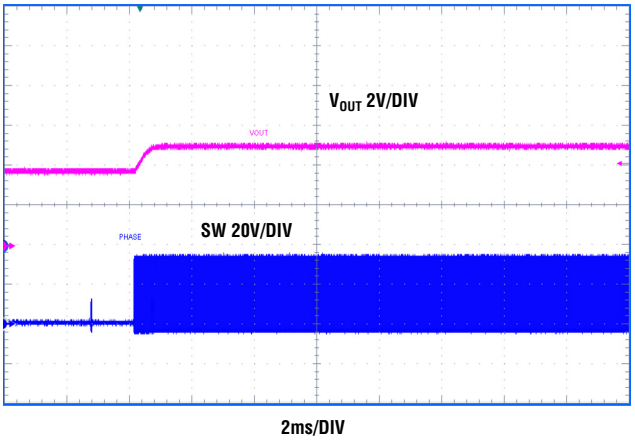



FIGURE 14. $V_{PVIN}$ 36V, PREBIASED START-UP

# Typical Performance Curves (Continued)

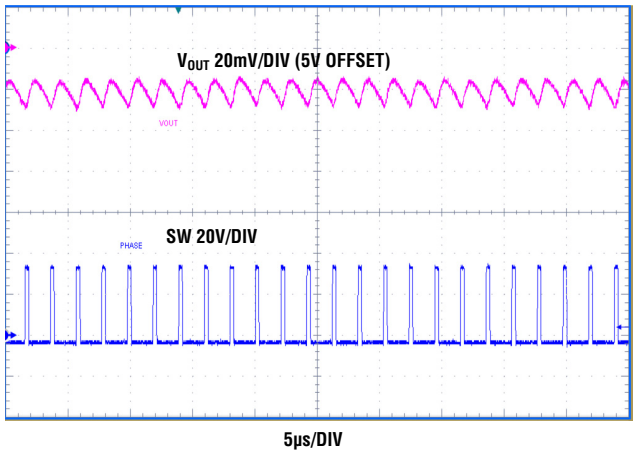



FIGURE 15. SYNCHRONOUS BUCK WITH FORCE PWM MODE, $V_{PVIN}$ 36V, $I_O$ 2A

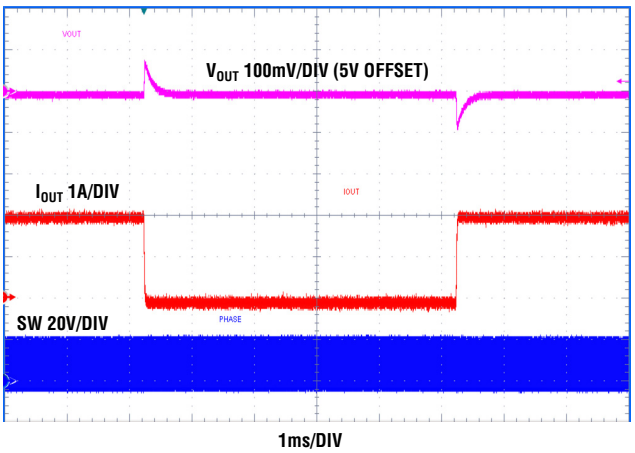



FIGURE 16. $V_{PVIN}$ 24V, 0 TO 2A STEP LOAD, FORCE PWM MODE

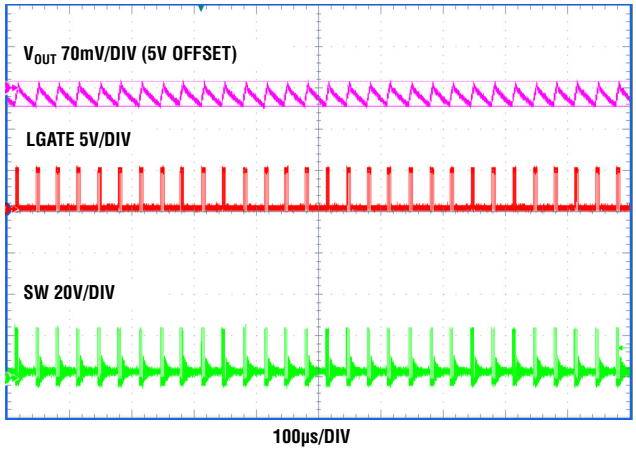



FIGURE 17. $V_{PVIN}$ 24V, 80mA LOAD, LLM MODE

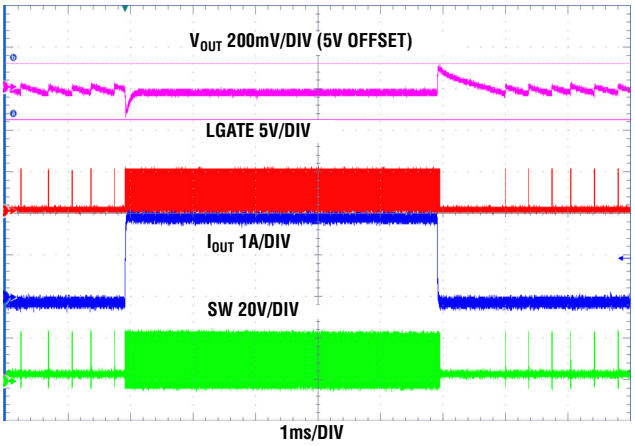



FIGURE 18. $V_{PVIN}$ 24V, 0 TO 2A STEP LOAD, LLM MODE

# Typical Performance Curves (Continued)

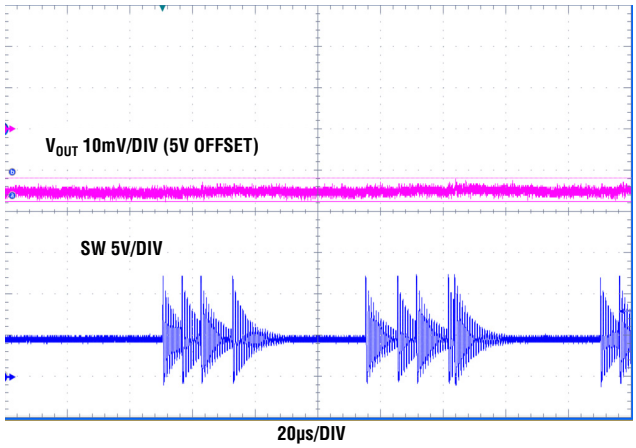



FIGURE 19. NON-SYNCHRONOUS BUCK, FORCE PWM MODE, $V_{PVIN}$ 12V, NO LOAD

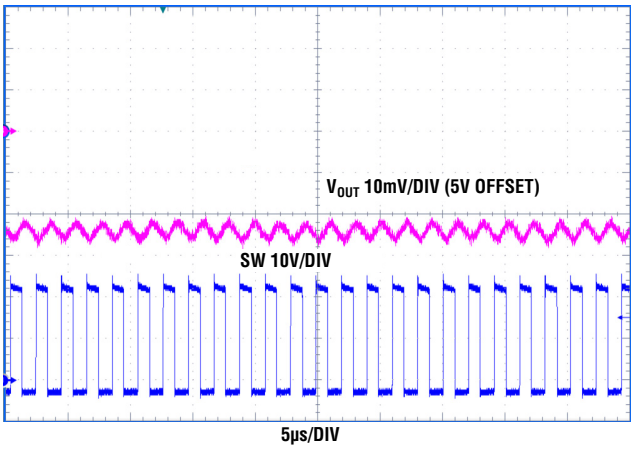



FIGURE 20. NON-SYNCHRONOUS BUCK, FORCE PWM MODE, $V_{PVIN}$ 12V, 2A

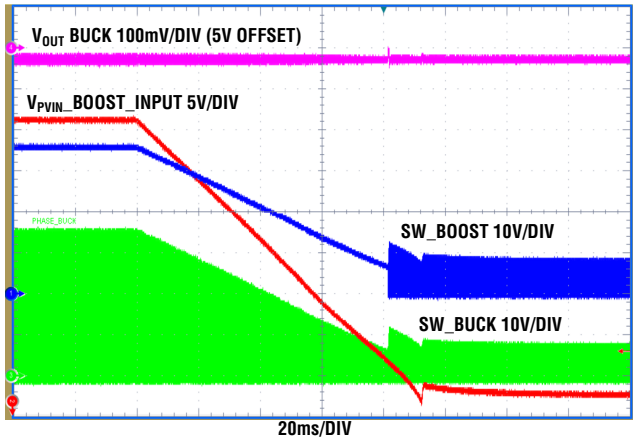



FIGURE 21. BOOST BUCK MODE, BOOST INPUT STEP FROM 36V TO 3V, $V_{OUT}$ BUCK = 5V, $I_{OUT}$_BUCK = 1A

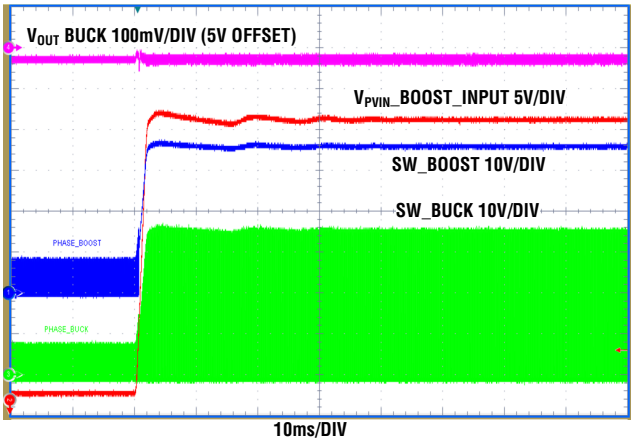



FIGURE 22. BOOST BUCK MODE, BOOST INPUT STEP FROM 3V TO 36V, $V_{OUT}$ BUCK = 5V, $I_{OUT}$_BUCK = 1A

# Typical Performance Curves (Continued)

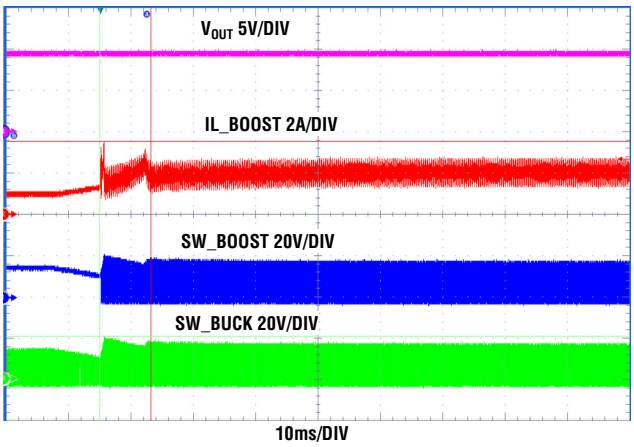



FIGURE 23. BOOST BUCK MODE, $V_O$ = 9V, $I_O$ = 1.8A, BOOST INPUT DROPS FROM 16V TO 9V DC

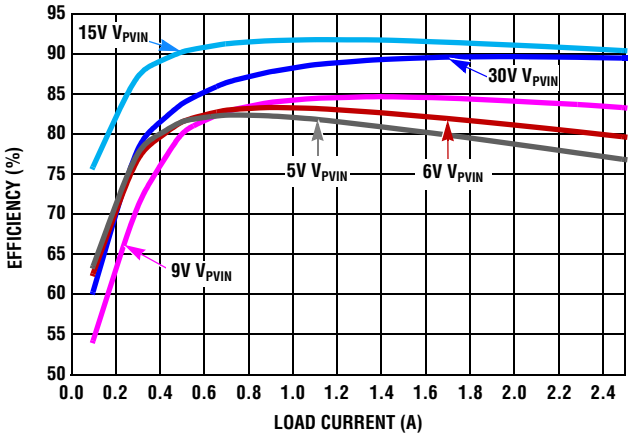



FIGURE 24. EFFICIENCY, BOOST BUCK, 500KHZ, $V_{OUT}$ 12V, $T_A$ = +25°C

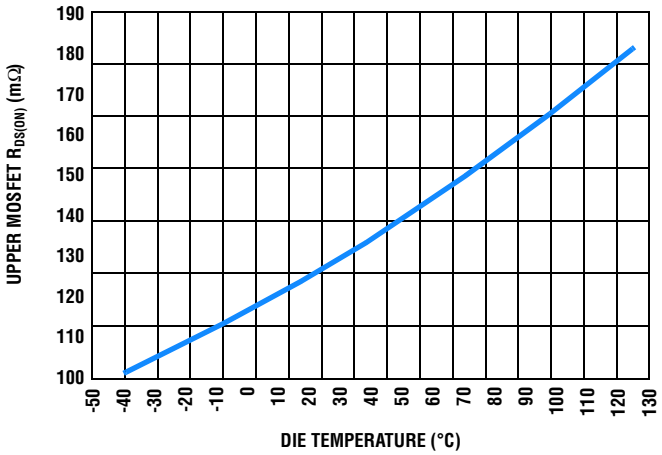
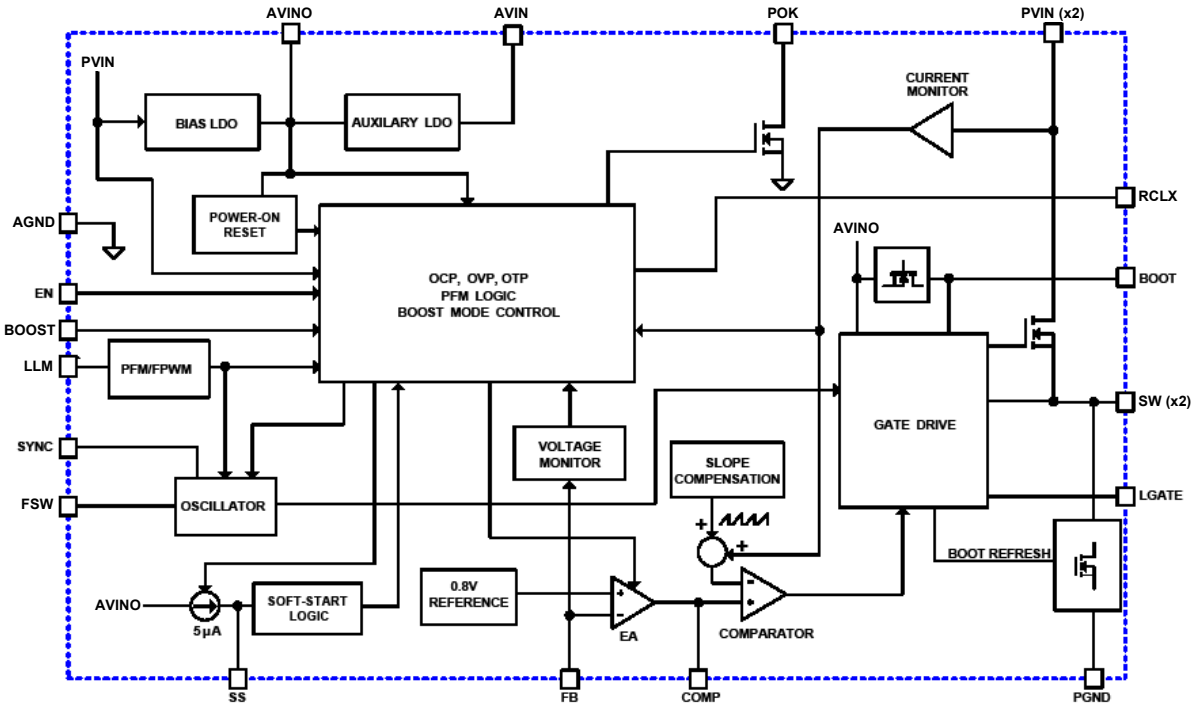



FIGURE 25. UPPER MOSFET $R_{DS(ON)}$ (mΩ) OVER-TEMPERATURE

# Block Diagram




# Functional Description

## Initialization

Initially the ER3125QI continually monitors the voltage at the EN pin. When the voltage on the EN pin exceeds its rising ON threshold, the internal LDO will start-up to build up AVINO. After Power-On Reset (POR) circuits detect that AVINO voltage has exceeded the POR threshold, the soft-start will be initiated.

## Soft-Start

The soft-start (SS) ramp is built up in the external capacitor on the SS pin that is charged by an internal 5µA current source.

$$C_{SS}[\mu F] = 6.5 \cdot t_{SS}[S] \qquad \text{(EQ. 1)}$$

The SS ramp starts from 0 to a voltage above 0.8V. Once SS reaches 0.8V, the bandgap reference takes over and IC gets into steady state operation. The soft-start time is referring to the duration for SS pin ramps from 0 to 0.8V while output voltage ramps up with the same rate from 0 to target regulated voltage. The required capacitance at SS pin can be calculated from Equation 1.

The SS plays a vital role in the hiccup mode of operation. The IC works as cycle-by-cycle peak current limiting at over load condition. When a harsh condition occurs and the current in the upper side MOSFET reaches the second overcurrent threshold, the SS pin is pulled to ground and a dummy soft-start cycle is initiated. At dummy SS cycle, the current to charge soft-start cap is cut down to 1/5 of its normal value. So a dummy SS cycle takes 5x of the regular SS cycle. During the dummy SS period, the control loop is disabled and no PWM output. At the end of this cycle, it will start the normal SS. The hiccup mode persist until the second overcurrent threshold is no longer reached.

The ER3125QI is capable of starting up with prebiased output.

## PWM Control

Pulling the LLM pin to GND will set the IC in forced PWM mode. The ER3125QI employs the peak current mode PWM control for fast transient response and cycle-by-cycle current limiting. See "Block Diagram" on page 14.

The PWM operation is initialized by the clock from the oscillator. The upper MOSFET is turned on by the clock at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current sense signal and the slope compensation signal reaches the error amplifier output voltage level, the PWM comparator is trigger to shutdown the PWM logic to turn off the high-side MOSFET. The high-side MOSFET stays off until the next clock signal comes for next cycle.

The output voltage is sensed by a resistor divider from $V_{OUT}$ to the FB pin. The difference between the FB voltage and 0.8V reference is amplified and compensated to generate the error voltage signal at the COMP pin. Then the COMP pin signal is compared with the current ramp signal to shutdown the PWM.

## LLM Mode Operation

To pull the LLM pin HIGH (>2.5V) or leave the LLM pin floating will set the IC to have PFM (Pulse Frequency Modulation) operation in light load. In LLM mode, the switching frequency is dramatically reduced to minimize the switching loss. The ER3125QI enters LLM mode when the MOSFET peak current is lower than the PWM/LLM boundary current threshold. The default threshold is 700mA when there is no programming resistor at the LLM pin.

The current threshold for PWM/LLM boundary can be programmed by choosing the LLM pin resistor value calculated from Equation 2.

$$R_{LLM} = \frac{118500}{I_{LLM} + 0.2} \qquad \text{(EQ. 2)}$$

where $I_{LLM}$ is the desired PWM/LLM boundary current threshold and $R_{LLM}$ is the programming resistor. The usable resistor value range to program LLM current threshold is 150kΩ to 200kΩ $R_{LLM}$ value out of this range is not recommended.

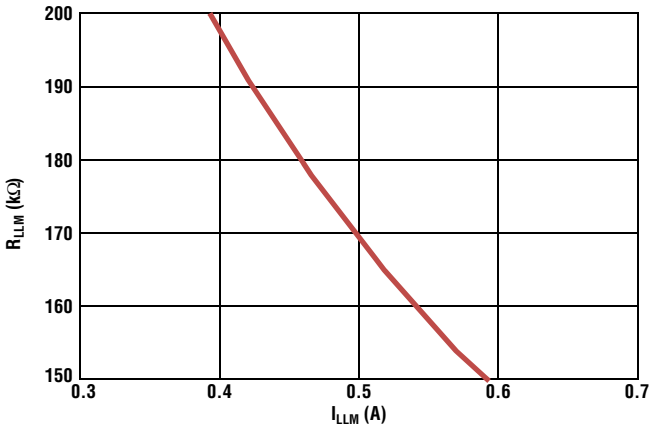



FIGURE 26. $R_{LLM}$ vs $I_{LLM}$

## Synchronous and Non-Synchronous Buck

The ER3125QI supports both Synchronous and non-synchronous buck operations.

In synchronous buck configuration, a 5.1k or smaller value resistor has to be added to connect LGATE to ground to avoid falsely turn-on of LGATE caused by coupling noise.

For a non-synchronous buck operation when a power diode is used as the low-side power device, the LGATE driver can be disabled with LGATE connected to AVINO (before IC start-up). For non-synchronous buck, the switch node will show oscillations after high-side turns off (as shown in Figure 19 - blue trace). This is normal due to the oscillations among the parasitic capacitors at switch node and output inductor. A RC snubber (suggesting 200Ω and 2.2nF as typical) at switch node can reduce this ringing.

## AVIN Switch-Over

The ER3125QI has an auxiliary LDO integrated as shown in the "Block Diagram" on page 14. It is used to replace the internal MAIN LDO function after the IC start-up. "Typical Application Schematic II - AVINO Switch-Over to $V_{OUT}$" on page 4 shows its basic application setup with output voltage connected to AVIN. After IC soft-start is done and the output voltage is built up to steady state, and once the AVIN pin voltage is over the AUX LDO Switch-over Rising Threshold, the MAIN LDO is shut off and the AUXILIARY LDO is activated to bias AVINO. Since the AVIN pin voltage is lower than the input voltage $V_{PVIN}$, the internal LDO dropout voltage and the consequent power loss is reduced. This feature brings substantial efficiency improvements in light load range, especially at high input voltage applications.

When the voltage at AVIN falls below the AUX LDO Switch-over Falling Threshold, the AUXILIARY LDO is shut off and the MAIN LDO is re-activated to bias AVINO. At the OV/UV fault events, the IC also switches back over from AUXILIARY LDO to MAIN LDO.

The AVIN switchover function is offered in buck configuration. It is not offered in boost configuration when the AVIN pin is used to monitor the boost output voltage for OVP.

## Input Voltage

With the part switching, the operating ER3125QI input voltage must be under 36V. This recommendation allows for short voltage ringing spikes (within a couple of ns time range) due to part switching while not exceeding the 44V, as stated in the Absolute Maximum Ratings.

The lowest IC operating input voltage (PVIN pin) depends on AVINO voltage and the Rising and Falling $V_{AVINO}$ POR Threshold in the Electrical Specifications table on page 6. At IC start-up when AVINO is just over rising POR threshold, there is no switching before the soft-start starts. Therefore, the IC minimum start-up voltage on the PVIN pin is 3.05V (MAX of Rising $V_{AVINO}$ POR). When the soft-start is initiated, the regulator is switching and the dropout voltage across the internal LDO increases due to driving current. Thus, the IC PVIN pin shutdown voltage is related to driving current and AVINO POR falling threshold. The internal upper side MOSFET has typical 10nC gate drive. For a typical example of synchronous buck with 4nC lower MOSFET gate drive and 500kHz switching frequency, the driving current is 7mA total causing 70mV drop across internal LDO under 3V $V_{PVIN}$. Then the IC shutdown voltage on the PVIN pin is 2.87V (2.8V + 0.07V). In practical design, extra room should be taken into account with concern to voltage spikes at PVIN.

With boost buck configuration, the input voltage range can be expanded further down to 2.5V or lower depending on the boost stage voltage drop upon maximum duty cycle. Since the boost output voltage is connected to the PVIN pin as the buck inputs, after the IC starts up, the IC will keep operating and switching as long as the boost output voltage can keep the AVINO voltage higher than falling threshold. Refer to "2-Stage Boost Buck Converter Operation" on page 17 for more details.

## Output Voltage

The output voltage can be programmed down to 0.8V by a resistor divider from $V_{OUT}$ to FB. For Buck, the maximum achievable voltage is ($V_{PVIN}$*$D_{MAX}$ - $V_{DROP}$), where $V_{DROP}$ is the voltage drop in the power path including mainly the MOSFET $R_{DS(ON)}$ and inductor DCR. The maximum duty cycle $D_{MAX}$ is decided by (1 - $f_{SW}$ * $t_{MIN(OFF)}$).

## Output Current

With the high-side MOSFET integrated, the maximum output current, which the ER3125QI can support is decided by the package and many operating conditions including input voltage, output voltage, duty cycle, switching frequency and temperature, etc. From the thermal perspective, the die temperature shouldn't exceed +125°C with the power loss dissipated inside of the IC. Figures 10 and 11 show the thermal performance of this part operating at different conditions.

Figures 10 and 11 show 2A and 2.5A buck applications under +25°C still air conditions over $V_{PVIN}$ range. The temperature rise data in these figures can be used to estimate the die temperature at different ambient temperatures under various operating conditions. Note that more temperature rise is expected at higher ambient temperature due to more conduction loss caused by $R_{DS(ON)}$ increase.

Generally, the part can output 2.5A in typical buck application conditions ($V_{PVIN}$ 8~30V, $V_O$ 5V, 500kHz, still air and +85°C ambient conditions). For any other operating conditions, refer to the previous mentioned thermal curves to estimate the maximum output current. The output current should be derated under any conditions causing the die temperature to exceed +125°C.

The die temperature is equal to the sum of ambient temperature and the temperature rise resulting from the power dissipated by the IC package with a certain junction to ambient thermal impedance $\theta_{JA}$. The power dissipated in the IC is related to the MOSFET switching loss, conduction loss and the internal LDO loss. Besides the load, these losses are also related to input voltage, output voltage, duty cycle, switching frequency and temperature. With the exposed pad at the bottom, the heat of the IC mainly goes through the bottom pad and $\theta_{JA}$ is greatly reduced. The $\theta_{JA}$ is highly related to layout and air flow conditions. In layout, multiple vias (≥9) are strongly recommended in the IC bottom pad. The bottom pad with its vias should be placed in the ground copper plane with an area as large as possible across multiple layers. The $\theta_{JA}$ can be reduced further with air flow. Refer to Figures 8 and 9 for the thermal performance with 100 CFM air flow.

For applications with high output current and extreme operating conditions (compact board size, high ambient temperature, etc.), synchronous buck is highly recommended since the external low-side MOSFET generates smaller heat than external low-side power diode. This helps to reduce PCB temperature rise around the ER3125QI and reduce junction temperature rise.

## 2-Stage Boost Buck Converter Operation

The "Typical Application Schematic III - Boost Buck Converter" on page 4, shows the circuits of boost function. Schematic (a) shows a boost working as a pre-stage to provide input to the following Buck stage. This is for applications when the input voltage could drop to a very low voltage in some constants (in some battery powered systems as for example), causing the output voltage to drop out of regulation. The boost converter can be enabled to boost the input voltage up to keep the output voltage in regulation. When system input voltage recovers back to normal, the boost stage is disabled while only the buck stage is switching.

The BOOST pin is used to set boost mode and monitor the boost input voltage. At IC start-up before soft-start, the controller will be latched in boost mode when the voltage is at or above 200mV; it will latch in synchronous buck mode if voltage on this pin is below 200mV. In boost mode the low-side driver output PWM has the same PWM signal with the buck regulator.

In boost mode, the BOOST pin is used to monitor boost input voltage to turn on and turn off the boost PWM. The AVIN pin is used to monitor the boost output voltage to turn on and turn off the boost PWM.

Referring to Figure 27 on page 18, a resistor divider from boost input voltage to the BOOST pin is used to detect the boost input voltage. When the voltage on BOOST pin is below 0.8V, the boost PWM is enabled with a fixed 500µs soft-start and the boost duty cycle increases linearly from $t_{MIN(ON)}*f_{SW}$ to ~50%. A 3µA sinking current is enabled at the BOOST pin for hysteresis purposes. When the voltage on the BOOST pin recovers to be above 0.8V, the boost PWM is disabled immediately. Use Equation 3 to calculate the upper resistor $R_{UP}$ (R1 in Figure 27) for a desired hysteresis $V_{HYS}$ at boost input voltage.

$$R_{UP}[M\Omega] = \frac{V_{HYS}}{3[\mu A]} \quad \text{(EQ. 3)}$$

Use Equation 4 to calculate the lower resistor $R_{LOW}$ (R2 in Figure 27) according to a desired boost enable threshold.

$$R_{LOW} = \frac{R_{UP} \cdot 0.8}{VFTH - 0.8} \quad \text{(EQ. 4)}$$

Where VFTH is the desired falling threshold on boost input voltage to turn on the boost, 3µA is the hysteresis current, and 0.8V is the reference voltage to be compared with.

Note that the boost start-up threshold has to be selected in a way that the buck is operating working well and kept in close loop regulation before boost start-up. Otherwise, large in-rush current at boost start-up could occur at boost input due to the buck open loop saturation. The boost start-up input voltage threshold should be set high enough to cover the DC voltage drop of boost inductor and diode, also the buck's maximum duty cycle and voltage conduction drop. This ensures buck is not reaching maximum duty cycle before boost start-up.

Similarly, a resistor divider from the boost output voltage to the AVIN pin is used to detect the boost output voltage. When the voltage on the AVIN pin is below 0.8V, the boost PWM is enabled with a fixed 500µs soft-start, and a 3µA

sinking current is enabled at AVIN pin for hysteresis purposes. When the voltage on the AVIN pin recovers to be above 0.8V, the boost PWM is disabled immediately. Use Equation 3 to calculate the upper resistor $R_{UP}$ ($R_3$ in Figure 27) according to a desired hysteresis $V_{HY}$ at boost output voltage. Use Equation 4 to calculate the lower resistor $R_{LOW}$ ($R_4$ in Figure 27) according to a desired boost enable threshold at boost output.

Assuming $V_{BAT}$ is the boost input voltage, $V_{OUT\_BST}$ is the boost output voltage and $V_{OUT}$ is the buck output voltage, the steady state DC transfer function are:

$$V_{OUTBST} = \frac{1}{1-D} \cdot V_{BAT} \quad \text{(EQ. 5)}$$

$$V_{OUT} = D \cdot V_{OUTBST} = \frac{D}{1-D} \cdot V_{BAT} \quad \text{(EQ. 6)}$$

From Equations 5 and 6, Equation 7 can be derived to estimate the steady state boost output voltage as function of $V_{BAT}$ and $V_{OUT}$:

$$V_{OUTBST} = V_{BAT} + V_{OUT} \quad \text{(EQ. 7)}$$

After the IC starts up, the boost buck converters can keep working when the battery voltage drops extremely low because the IC's bias (AVINO) LDO is powered by the boost output. For example, a 3.3V output application battery drops to 2V, and the PVIN pin voltage is powered by the boost output voltage that is 5.2V (Equation 7), meaning that the PVIN pin (buck input) still sees 5.2V to keep the IC working.

Note that in the previously mentioned case, the boost input current could be high because the input voltage is very low ($V_{PVIN}$*$I_{IN}$ = $V_{OUT}$*$I_{OUT}$/Efficiency). If the design is to achieve the low input operation with full load, the inductor and MOSFET have to be selected with enough current ratings to handle the high current appearing at boost input. The boost inductor current are the same with the boost input current, which can be estimated as Equation 8, where $P_{OUT}$ is the output power, $V_{BAT}$ is the boost input voltage, and EFF is the estimated efficiency of the whole boost and buck stages.

$$IL_{IN} = \frac{P_{OUT}}{V_{BAT} \cdot EFF} \quad \text{(EQ. 8)}$$

Based on the same concerns of boost input current, the start-up sequence must follow the rule that the IC is enabled after the boost input voltage rise above a certain level. The shutdown sequence must follow the rule that the IC is disabled first before the boost input power source is turned off. At boost mode applications where there is no external control signal to enable/disable the IC, an external input UVLO circuit must be implemented for the start-up and shutdown sequence.

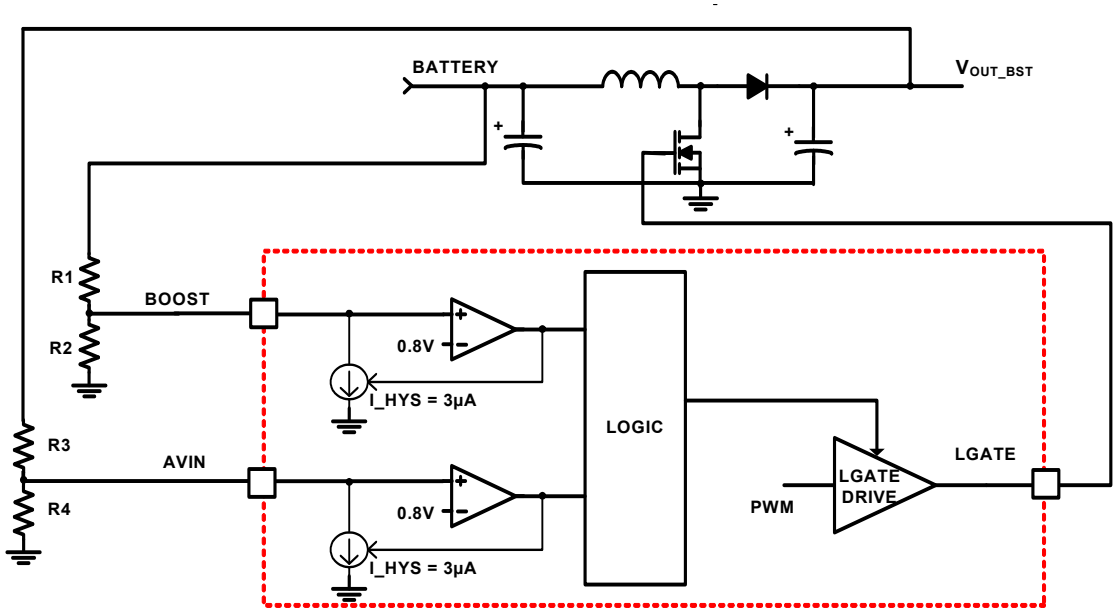



FIGURE 27. BOOST CONVERTER CONTROL

## Non-Inverting Single Inductor Buck Boost Converter Operation

In “Typical Application Schematic III - Boost Buck Converter” on page 4, schematic (b) shows non-inverting single inductor buck boost configuration. The recommended setting is to use resistor divider 1MΩ and 130kΩ (as shown in TYP Schematic III b) connecting from AVINO to both BOOST and AVIN pins (BOOST and AVIN pin are directly connected). In this way, the BOOST pin voltage is a fixed voltage 0.52V that is higher than the boost mode detection threshold 0.2V to set IC in boost mode and lower than the boost switching threshold 800mV to have boost being constantly switching (during and after soft-start).

As the same in 2-stage boost buck mode, LGATE is switching ON with the same phase of upper FETs switching ON, meaning both upper and lower side FETs are ON and OFF at the same time with the same duty cycle. When both FETs ON, input voltage charges inductor current ramping up for duration of DT; when both FETs OFF, inductor current is free wheeling through the 2 power diodes to output, and output voltage discharge the inductor current ramping down for (1-D)T (in CCM mode). The steady state DC transfer function is:

$$V_{OUT} = \frac{D}{1-D} \cdot V_{PVIN} \quad \text{(EQ. 9)}$$

where $V_{PVIN}$ is the input voltage, $V_{OUT}$ is the buck boost output voltage, D is duty cycle.

Another useful equation is to calculate the inductor DC current as below:

$$IL_{DC} = \frac{1}{1-D} \cdot I_{OUT} \quad \text{(EQ. 10)}$$

where $IL_{DC}$ is the inductor DC current and $I_{OUT}$ is the output DC current.

Equation 10 shows the inductor current is charging output only during (1-D)T, which means inductor current has larger DC current than output load current. Thus, for this part with high-side FET integrated, the non-inverting buck boost configuration has less load current capability compared with buck and 2-stage boost buck configurations. Its load current capability depends mainly on the duty cycle and inductor current.

Inductor ripple current can be calculated below:

$$IL_{RIPPLE} = \frac{V_{OUT}(1-D)T}{L} \quad \text{(EQ. 11)}$$

The inductor peak current is,

$$IL_{PEAK} = IL_{DC} + \frac{1}{2} \cdot IL_{RIPPLE} \quad \text{(EQ. 12)}$$

In power stage DC calculations, use Equation 9 to calculate D, then use Equation 10 to calculate $IL_{DC}$. D and $IL_{DC}$ are useful information to estimate the high-side FET’s power losses and check if the part can meet the load current requirements.

## Oscillator and Synchronization

The oscillator has a default frequency of 500kHz with the $f_{SW}$ pin connected to AVINO, or ground, or floating. The frequency can be programmed to any frequency between 200kHz and 2.2MHz with a resistor from $f_{SW}$ pin to GND.

$$R_{FSW[k\Omega]} = \frac{145000 - 16 \cdot f_{SW[kHz]}}{f_{SW[kHz]}} \quad \text{(EQ. 13)}$$

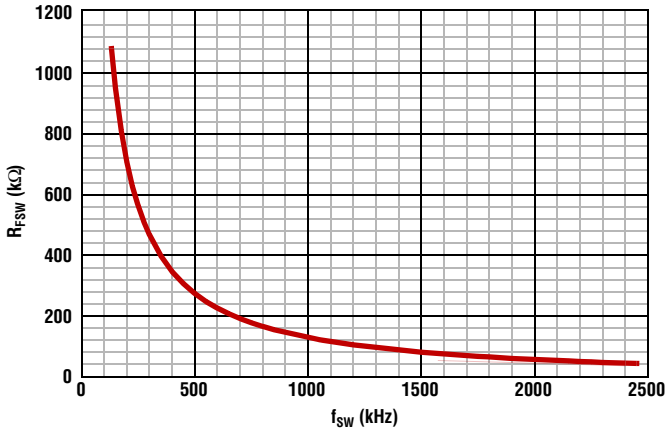



FIGURE 28. $R_{FSW}$ vs FREQUENCY

The SYNC pin is bi-directional and it outputs the IC's default or programmed local clock signal when it's free running. The IC locks to an external clock injected to the SYNC pin (external clock frequency recommended to be 10% higher than the free running frequency). The delay from the rising edge of the external clock signal to the SW rising edge is half of the free running switching period pulse 220ns, (0.5Tsw+220ns). The maximum external clock frequency is recommended to be 1.6 of the free running frequency.

When the part enters LLM pulse skipping mode, the synchronization function is shut off and also no clock signal output in SYNC pin.

With the SYNC pins simply connected together, multiple ER3125QIs can be synchronized. The slave ICs automatically have 180° phase shift with respective to the master IC.

### POK

The POK pin is output of an open drain transistor (refer to at "Block Diagram" on page 14). An external resistor is required to be pulled up to AVINO for proper POK function. At start-up, POK will be turned HIGH (internal POK open drain transistor is turned off) with 128 cycles delay after soft-start is finished (soft-start ramp reaches 1.02V) and FB voltage is within OV/UV window (90%REF < FB < 110%REF).

At normal operation, POK will be pulled low with 1 cycle (minimum) and 6 cycles (maximum) delay if any of the OV (110%) or UV (90%) comparator is tripped. The POK will be released HIGH with 128 cycles delay after FB recovers to be within OV/UV window (90%REF < FB < 110%REF). When EN is pulled low or AVINO is below POR, POK is pulled low with no delay.

In the case when the POK pin is pulled up by external bias supply instead of AVINO of itself, when the part is disabled, the internal POK open drain transistor is off, the external bias supply can charge POK pin HIGH. This should be known as false POK reporting. At start-up when AVINO rise from 0, POK will be pulled low when AVINO reaches 1V. After EN is pulled low and AVINO is falling, the POK internal open drain transistor will open with high impedance when AVINO falls below 1V. The time between EN pulled low and POK OPEN depends on the AVINO falling time to 1V.

## Fault Protection

### Overcurrent Protection

The overcurrent function protects against any overload condition and output short at worst case, by monitoring the current flowing through the upper MOSFET.

There are 2 current limiting thresholds. The first one $I_{OC1}$ is to limit the high-side MOSFET peak current cycle-by-cycle. The current limit threshold is set to default at 3.6A with RCLX pin connected to GND or AVINO, or left open. The current limit threshold can also be programmed by a resistor $R_{CLX}$ at RCLX pin to ground. Use Equation 14 to calculate the resistor.

$$R_{CLX} = \frac{300000}{I_{OC}[A] + 0.018} \quad \text{(EQ. 14)}$$

Note that $I_{OC1}$ is higher with lower $R_{CLX}$. The usable resistor value range to program OC1 peak current threshold is 40kΩ to 330kΩ $R_{CLX}$ value out of this range is not recommended.

The second current protection threshold $I_{OC2}$ is 15% higher than $I_{OC1}$ mentioned previously. Instantly after the high-side MOSFET current reaches $I_{OC2}$, the PWM is shut off after 2-cycle delay and the IC enters hiccup mode. In hiccup mode, the PWM is disabled for dummy soft-start duration equaling to 5 regular soft-start periods. After this dummy soft-start cycle, the true soft-start cycle is attempted again. The $I_{OC2}$ offers a robust and reliable protections against the worst case conditions.

The frequency foldback is implemented for the ER3125QI. When overcurrent limiting, the switching frequency is reduced to be proportional to output voltage in order to keep the inductor current under limit threshold during overload condition. The low limit of frequency under frequency foldback operation is 40kHz.

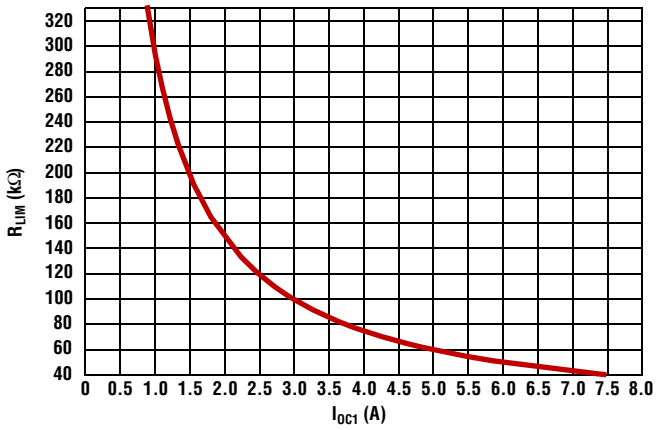



FIGURE 29. $R_{LIM}$ vs $I_{OC1}$

## Overvoltage Protection

If the voltage detected on the FB pin is over 110% or 120% of reference, the high-side and low-side driver shuts down immediately and keep off until FB voltage drops to 0.8V. When the FB voltage drops to 0.8V, the drivers are released ON. 110% OVP is off during soft-start and active after soft-start is done. 120% OVP is active during and after soft-start.

## Thermal Protection

The ER3125QI PWM will be disabled if the junction temperature reaches +160°C. There is +20°C hysteresis for OTP. The part will restart after the junction temperature drops below +140°C.

## Output Capacitors - Buck

An output capacitor is required to filter the inductor current. Output ripple voltage and transient response are 2 critical factors when considering output capacitance choice. The current mode control loop allows for the usage of low ESR ceramic capacitors and thus smaller board layout. Electrolytic and polymer capacitors may also be used.

Additional consideration applies to ceramic capacitors. While they offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the manufacturers data sheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published, but an assumption of ~20% further reduction will generally suffice. The result of these considerations can easily result in an effective capacitance 50% lower than the rated value. Nonetheless, they are a very good choice in many applications due to their reliability and extremely low ESR.

In buck topology, the following equations allow calculation of the required capacitance to meet a desired ripple voltage level. Additional capacitance may be used.

For the ceramic capacitors (low ESR):

$$V_{OUTripple} = \frac{\Delta I}{8 * (f_{SW}) * C_{OUT}} \quad \text{(EQ. 15)}$$

where ΔI is the inductor's peak to peak ripple current, $f_{SW}$ is the switching frequency and $C_{OUT}$ is the output capacitor.

If using electrolytic capacitors then:

$$V_{OUTripple} = \Delta I * ESR \quad \text{(EQ. 16)}$$

Regarding transient response needs, a good starting point is to determine the allowable overshoot in $V_{OUT}$ if the load is suddenly removed. In this case, energy stored in the inductor will be transferred to $C_{OUT}$ causing its voltage to rise. After calculating capacitance required for both ripple and transient needs, choose the larger of the calculated values. The Equation 17 determines the required output capacitor value in order to achieve a desired overshoot relative to the regulated voltage.

$$C_{OUT} = \frac{I_{OUT}^2 * L}{V_{OUT}^2 * (V_{OUTMAX} / V_{OUT})^2 - 1)} \quad \text{(EQ. 17)}$$

where $V_{OUTMAX}/V_{OUT}$ is the relative maximum overshoot allowed during the removal of the load.

## Input Capacitors - Buck

Depending on the system input power rail conditions, the aluminum electrolytic type capacitor is normally needed to provide the stable input voltage. Thus, restrict the switching frequency pulse current in a small area over the input traces for better EMC performance. The input capacitor should be able to handle the RMS current from the switching power devices.

Ceramic capacitors must be used at PVIN pin of the IC and multiple capacitors including 1µF and 0.1µF are recommended. Place these capacitors as closely as possible to the IC.

## Output Inductor - Buck

The inductor value determines the converter's ripple current. Choosing an inductor current requires a somewhat arbitrary choice of ripple current, ΔI. A reasonable starting point is 30% to 40% of total load current. The inductor value is calculated using Equation 18:

$$L = \frac{V_{PVIN} - V_{OUT}}{f_{SW} \times \Delta I} \times \frac{V_{OUT}}{V_{PVIN}} \quad \text{(EQ. 18)}$$

Increasing the value of inductance reduces the ripple current and thus ripple voltage. However, the larger inductance value may reduce the converter's response time to a load transient. The inductor current rating should be as such that it will not saturate in overcurrent conditions.

## Low-Side Power MOSFET

In synchronous buck application, a power N MOSFET is needed as the synchronous low-side MOSFET and a good one should have low Qgd, low $R_{DS(ON)}$ and small Rg (Rg_typ < 1.5Ωrecommended). The Vgth_min is recommended to be or higher than 1.2V. A good example is SQS462EN.

A 5.1k or smaller value resistor has to be added to connect LGATE to ground to avoid falsely turn-on of LGATE caused by coupling noise.

## Output Voltage Feedback Resistor Divider

The output voltage can be programmed down to 0.8V by a resistor divider from $V_{OUT}$ to FB according to Equation 19.

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R_{UP}}{R_{LOW}}\right) \quad \text{(EQ. 19)}$$

In an application requiring least input quiescent current, large resistors should be used for the divider. Generally, a resistor value of 10k to 300k can be used for the upper resistor.

## Boost Inductor (2-Stage Boost Buck)

Besides the need to sustain the current ripple to be within a certain range (30% to 50%), the boost inductor current at its soft-start is a more important perspective to be considered in selection of the boost inductor. Each time the boost starts up, there is a fixed 500µs soft-start time when the duty cycle increases linearly from $t_{MIN(ON)}$*$f_{SW}$ to ~50%. Before and after boost start-up, the boost output voltage will jump from $V_{PVIN\_BOOST}$ to voltage ($V_{PVIN\_BOOST}$ + $V_{OUT\_BUCK}$). The design target in boost soft-start is to ensure the boost input current is sustained to minimum but capable to charge the boost output voltage to have a voltage step equaling to $V_{OUT\_BUCK}$. A big inductor will block the inductor current to increase and not high enough to be able to charge the output capacitor to the final steady state value ($V_{PVIN\_BOOST}$ + $V_{OUT\_BUCK}$) within 500µs. A 6.8µH inductor is a good starting point for its selection in design. The boost inductor current at start-up must be checked by oscilloscope to ensure it is under acceptable range.

## Boost Output Capacitor (2-Stage Boost Buck)

Based on the same theory in boost start-up previously described in the boost inductor selection, a large capacitor at boost output will cause high in-rush current at boost PWM start-up. 22µF is a good choice for applications with a buck output voltage less than 10V. Also some minimum amount of capacitance has to be used in boost output to keep the system stable.

# Loop Compensation Design - Buck

The ER3125QI uses constant frequency peak current mode control architecture to achieve fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable since its peak current is constant, and the system becomes single order system. It is much easier to design the compensator to stabilize the loop compared with voltage mode control. Peak current mode control has inherent input voltage feed-forward function to achieve good line regulation. Figure 30 shows the small signal model of a buck regulator.

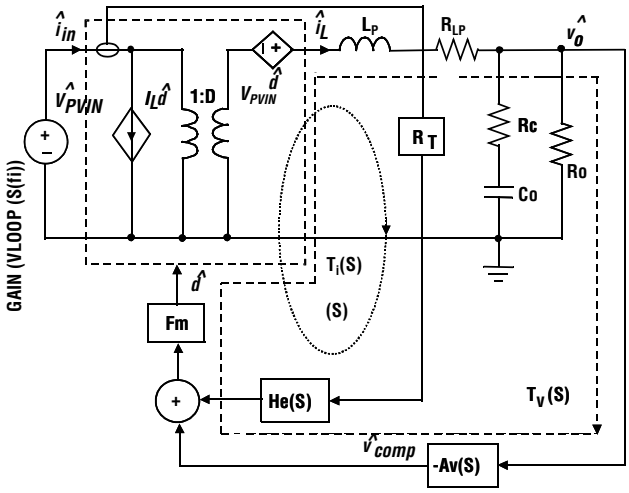



FIGURE 30. SMALL SIGNAL MODEL OF BUCK REGULATOR

## PWM Comparator Gain $F_m$

The PWM comparator gain $F_m$ for peak current mode control is given by Equation 20:

$$F_m = \frac{\hat{d}}{\hat{v}_{comp}} = \frac{1}{(S_e + S_n)T_s} \quad \text{(EQ. 20)}$$

Where, $S_e$ is the slew rate of the slope compensation and $S_n$ is given by Equation 21:

$$S_n = R_t \frac{V_{PVIN}(-V_o)}{L_P} \quad \text{(EQ. 21)}$$

where, $R_t$ is the gain of the current amplifier.

## Current Sampling Transfer Function $H_e(S)$

In current loop, the current signal is sampled every switching cycle. It has the following transfer function in Equation 22:

$$H_e(S) = \frac{S^2}{\omega_h^2} + \frac{S}{\omega_h Q_n} + 1 \quad \text{(EQ. 22)}$$

where, $Q_n$ and $\omega_h$ are given by $Q_n = -\frac{2}{\pi}$, $\omega_h = \pi f_{SW}$

## Power Stage Transfer Functions

Transfer function $F_1(S)$ from control to output voltage is:

$$F_1(S) = \frac{\hat{v}_o}{\hat{d}} = V_{in} \frac{1 + \frac{S}{\omega_{esr}}}{\frac{S^2}{\omega_0^2} + \frac{S}{\omega_0 Q_p} + 1} \quad \text{(EQ. 23)}$$

Where, $\omega_{esr} = \frac{1}{R_c C_o}$, $Q_p \approx R_o \sqrt{\frac{C_o}{L_P}}$, $\omega_0 = \frac{1}{\sqrt{L_P C_o}}$

Transfer function $F_2(S)$ from control to inductor current is given by Equation 24:

$$F_2(S) = \frac{\hat{i}_o}{\hat{d}} = \frac{V_{PVIN}}{R_o + R_{LP}} \frac{1 + \frac{S}{\omega_z}}{\frac{S^2}{\omega_0^2} + \frac{S}{\omega_0 Q_p} + 1} \quad \text{(EQ. 24)}$$

where $\omega_z = \frac{1}{R_o C_o}$ .

Current loop gain $T_i(S)$ is expressed as Equation 25:

$$T_i(S) = R_t F_m F_2(S) H_e(S) \quad \text{(EQ. 25)}$$

The voltage loop gain with open current loop is expressed in Equation 26:

$$T_v(S) = K F_m F_1(S) A_v(S) \quad \text{(EQ. 26)}$$

The Voltage loop gain with current loop closed is given by Equation 27:

$$L_v(S) = \frac{T_v(S)}{1 + T_i(S)} \quad \text{(EQ. 27)}$$

If $T_i(S) >> 1$, then Equation 27 can be simplified as Equation 28:

$$L_v(S) = \frac{R_o + R_{LP}}{R_t} \frac{1 + \frac{S}{\omega_{esr}}}{1 + \frac{S}{\omega_p}} \frac{A_v(S)}{H_e(S)}, \ \omega_p \approx \frac{1}{R_o C_o} \quad \text{(EQ. 28)}$$

Equation 28 shows that the system is a single order system. Therefore, a simple type II compensator can be easily used to stabilize the system. A type III compensator is needed to expand the bandwidth for current mode control in some cases.

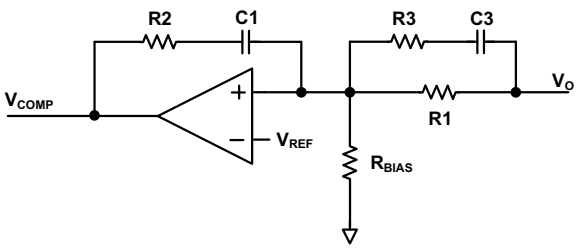



FIGURE 31. TYPE III COMPENSATOR

A compensator with 2 zeros and 1 pole is recommended for this part, as shown in Figure 31. Its transfer function is expressed as Equation 29:

$$A_v(S) = \frac{\hat{v}_{comp}}{\hat{v}_O} = \frac{1}{SR_1C_1} \frac{\left(1+\frac{S}{\omega_{tz1}}\right)\left(1+\frac{S}{\omega_{tz2}}\right)}{\left(1+\frac{S}{\omega_{tp}}\right)} \quad \text{(EQ. 29)}$$

where,

$$\omega_{tz1} = \frac{1}{R_2C_1},\ \omega_{tz2} = \frac{1}{(R_1+R_3)C_3},\ \omega_{tp} = \frac{1}{R_3C_3}$$

Compensator design goal:

Loop bandwidth $f_c$: $\left(\frac{1}{4}\text{to}\frac{1}{10}\right)f_{sw}$

Gain margin: >10dB

Phase margin: 45°

The compensator design procedure is as follows:

1. Position $\omega_{CZ2}$ and $\omega_{CP}$ to derive $R_3$ and $C_3$.

   Put the compensator zero $\omega_{CZ2}$ at (1 to 3)/($R_0C_o$)

$$\omega_{CZ2} = \frac{3}{R_0 C_0} \quad \text{(EQ. 30)}$$

   Put the compensator pole $\omega_{CP}$ at ESR zero or 0.35 to 0.5 times of switching frequency, whichever is lower. In all-ceramic-cap design, the ESR zero is normally higher than half of the switching frequency. $R_3$ and $C_3$ can be derived as follows:

   Case A: ESR zero $\frac{1}{2\pi R_c C_0}$ less than (0.35 to 0.5)$f_{SW}$

$$C_3 = \frac{R_0 C_0 - 3R_c C_0}{3R_1} \quad \text{(EQ. 31)}$$

$$R_3 = \frac{3R_c R_1}{R_0 - 3R_c} \quad \text{(EQ. 32)}$$

   Case B: ESR zero $\frac{1}{2\pi R_c C_0}$ larger than (0.35 to 0.5)$f_{SW}$

$$C_3 = \frac{0.33 R_0 C_0 f_{SW} - 0.46}{f_{SW} R_1} \quad \text{(EQ. 33)}$$

$$R_3 = \frac{R_1}{0.73 R_0 C_0 f_{SW} - 1} \quad \text{(EQ. 34)}$$

2. Derive $R_2$ and $C_1$.

   The loop gain $L_v(S)$ at cross over frequency of $f_c$ has unity gain. Therefore, $C_1$ is determined by Equation 35.

$$C_1 = \frac{(R_1 + R_3)C_3}{2\pi f_c R_t R_1 C_0} \quad \text{(EQ. 35)}$$

   The compensator zero $\omega_{CZ1}$ can boost the phase margin and bandwidth. To put $\omega_{CZ1}$ at 2 times of cross cover frequency $f_c$ is a good start point. It can be adjusted according to specific design. $R_1$ can be derived from Equation 36.

$$R_2 = \frac{1}{4\pi f_c C_1} \quad \text{(EQ. 36)}$$

   Example: $V_{PVIN}$ = 12V, $V_o$ = 5V, $I_o$ = 2A, $f_{SW}$ = 500kHz, $C_o$ = 60µF/3mΩ, L = 10µH, $R_t$ = 0.20V/A, $f_c$ = 50kHz, $R_1$ = 105k, $R_{BIAS}$ = 20kΩ

   Select the crossover frequency to be 35kHz. Since the output capacitors are all ceramic, use Equations 33 and 34 to derive $R_3$ to be 20k and $C_3$ to be 470pF.

   Then use Equations 35 and 36 to calculate C1 to be 180pF and $R_2$ to be 12.7k. Select 150pF for $C_1$ and 15k for $R_2$.

   There is approximately 30pF parasitic capacitance between COMP to FB pins that contributes to a high frequency pole. Any extra external capacitor is not recommended between COMP and FB.

   Figure 32 shows the simulated bode plot of the loop. It is shown that it has 26kHz loop bandwidth with 70° phase margin and -28 dB gain margin.

Note in applications where the LLM mode is desired especially when type III compensation network is used, the value of the capacitor between the COMP pin and the FB pin (not the capacitor in series with the resistor between COMP and FB) should be minimal to reduce the noise coupling for proper LLM operation. No external capacitor between COMP and FB is recommended at LLM applications.

In LLM mode operations, a RC filter from FB to ground (R in series with C, connecting from FB to ground) may help to reduce the noise effects injected to FB pin. The recommended values for the filter is 499Ω to 1k for the R and 470pF for the C.

# Loop Compensation Design for 2-Stage Boost Buck and Single-Stage Buck Boost

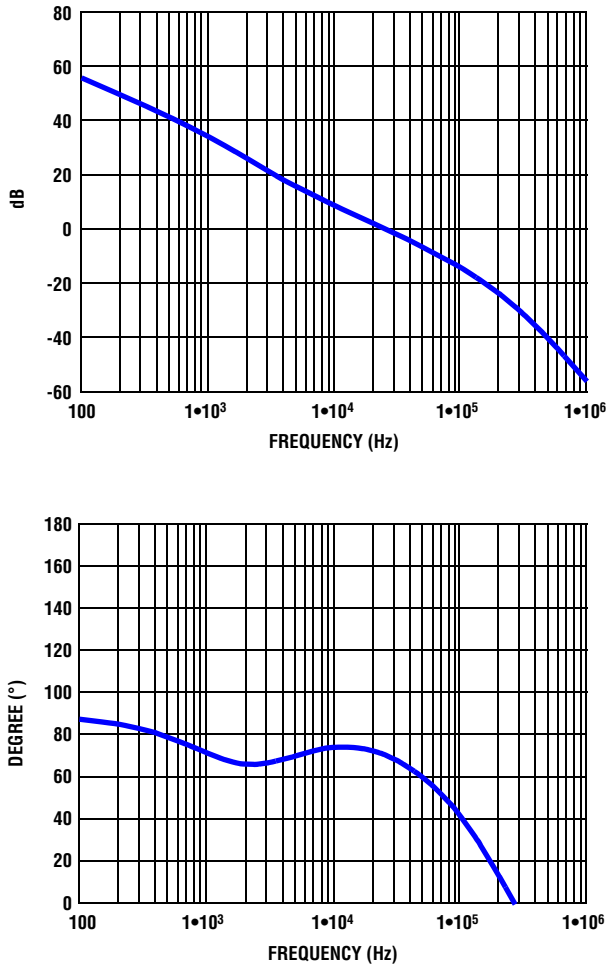



FIGURE 32. SIMULATED LOOP BODE PLOT

# Layout Suggestions

1. Place the input ceramic capacitors as closely as possible to the IC PVIN pin and power ground connecting to the power MOSFET or Diode. Keep this loop (input ceramic capacitor, IC PVIN pin and MOSFET/Diode) as tiny as possible to achieve the least voltage spikes induced by the trace parasitic inductance.
2. Place the input aluminum capacitors closely as possible to the IC PVIN pin.
3. Keep the switch node copper area small but large enough to handle the load current.
4. Place the output ceramic and aluminum capacitors close to the power stage components as well.
5. Place vias (≥9) in the bottom pad of the IC. The bottom pad should be placed in ground copper plane with an area as large as possible in multiple layers to effectively reduce the thermal impedance.
6. Place the 4.7µF ceramic decoupling capacitor at the AVINO pin (the closest place to the IC). Put multiple vias (≥3) close to the ground pad of this capacitor.
7. Keep the bootstrap capacitor close to the IC.
8. Keep the LGATE drive trace as short as possible and try to avoid using via in the LGATE drive path to achieve the lowest impedance.
9. Place the positive voltage sense trace close to the place to be strictly regulated.
10. Place all the peripheral control components close to the IC.

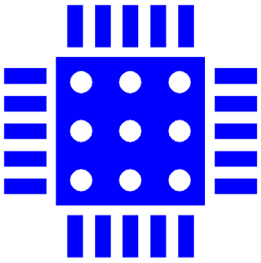


FIGURE 33. PCB VIA PATTERN

# Revision History

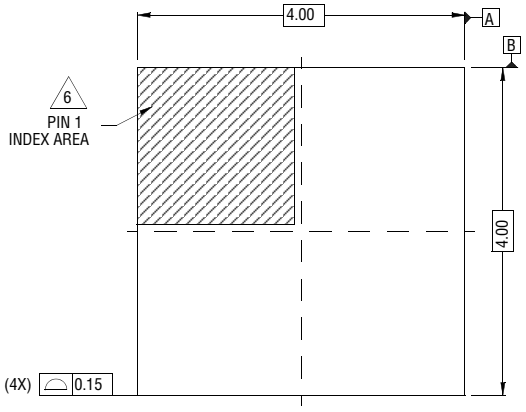
The table lists the revision history for this document.

| DATE | REVISION | CHANGE |
|---|---|---|
| May, 2014 | 1.0 | Initial Release. |

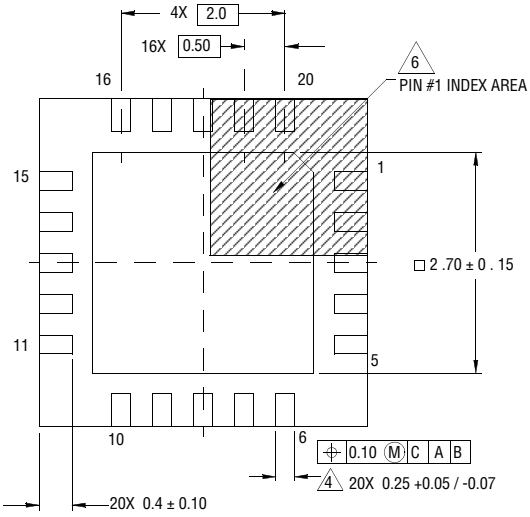
# Package Outline Drawing

## L20.4x4C

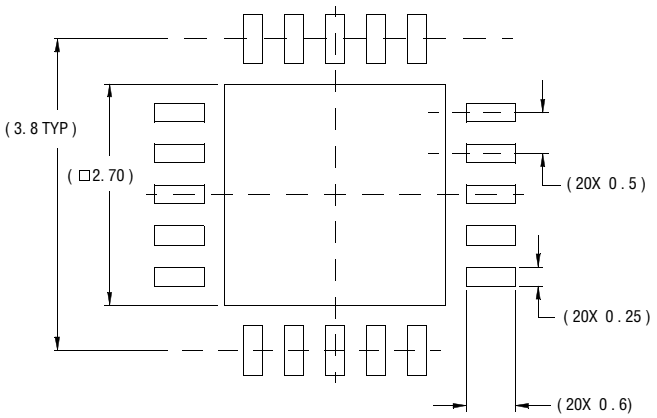
20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 11/06



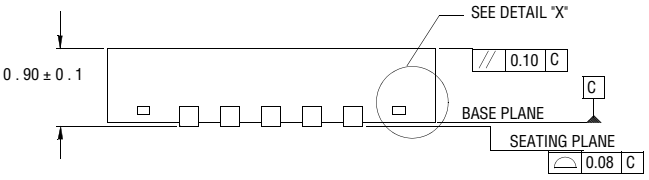

TOP VIEW



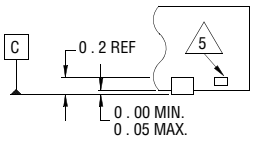

BOTTOM VIEW




TYPICAL RECOMMENDED LAND PATTERN




SIDE VIEW




DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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