315-W Mono BTL Digital Amplifier Power Stage

FEATURES

- **Total Output Power**
  - **125 W Into 8 Ω at <0.09% THD+N**
  - **220 W Into 6 Ω at 10% THD+N**
  - **315 W Into 4 Ω at 10% THD+N**
- **110-dB SNR (A-Weighted with TAS5518 modulator)**
- **Supports Pulse-Width Modulation (PWM) Frame Rates of 192 kHz to 384 kHz**
- **Resistor-Programmable Current Limit**
- **Integrated Self-Protection Circuit Including:**
  - **Under Voltage Protection**
  - **Over Temperature Warning and Error**
  - **Over Load Protection**
  - **Short Circuit (OC) Protection**
  - **PWM Activity Dectector**
- **Power-On Reset (POR) to Eliminate System Power-Supply Sequencing**
- **Thermally-Enhanced Package DKD (36-pin PSOP3)**
- **EMI Compliant When Used With Recommended System Design**
- **Error Reporting 3.3-V and 5-V Compliant**

APPLICATIONS

- **AV Receivers**
- **DVD Receivers**
- **Mini/Micro Component Systems**
- **Home Theater Systems**

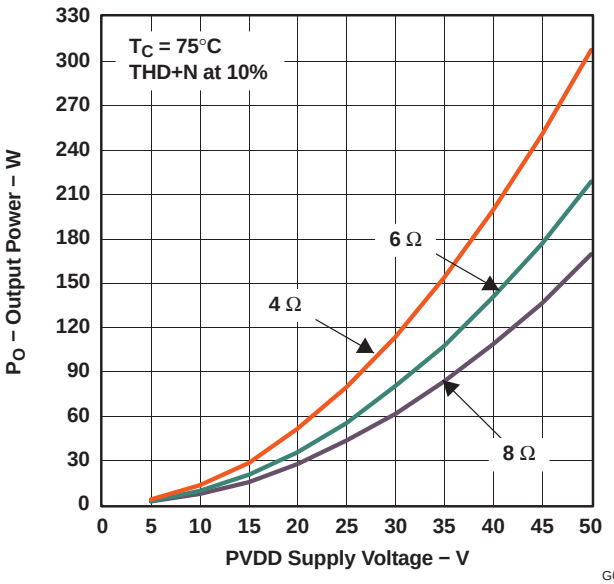
DESCRIPTION

The TAS5261 is a high-performance, integrated mono digital amplifier power stage designed to drive 4-Ω to 8-Ω speakers with low harmonic distortion. This system requires only a simple, passive demodulation filter to deliver high-quality, high-efficiency audio amplification.

The TAS5261 has complete protection circuitry integrated on chip, safeguarding the device and speakers against fault conditions that could damage the system. These protection features are short-circuit protection, overcurrent protection, undervoltage protection, and a loss of pulse-width modulation (PWM) input signal (PWM Activity Detector).

A power-on reset (POR) circuit is used to eliminate power-supply sequencing that is normally required for most H-bridge designs.

OUTPUT POWER
vs
PVDD_x SUPPLY VOLTAGE



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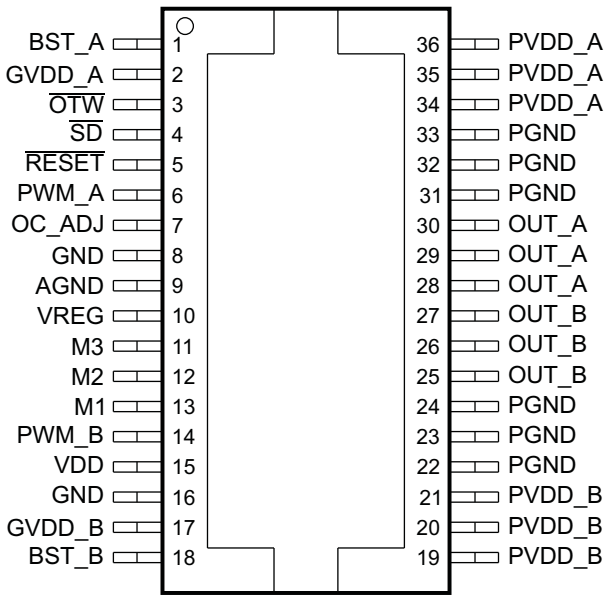
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

DEVICE INFORMATION

The TAS5261 is available in a thermally-enhanced 36-pin PSOP3 PowerPAD™ package. The heat slug is located on the top side of the device for convenient thermal coupling to a heat sink.

DKD PACKAGE
(TOP VIEW)



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DISSIPATION RATINGS

PARAMETER	CONDITION	TYPICAL (DKD)
$R_{\theta JC}$	BTL channel (four transistors)	0.6°C/W
$R_{\theta JC}$	One transistor	2.38°C/W
Pad area		80 mm^2

Protection Mode

Protection modes are selected by shorting M1, M2, and M3 to VREG or GND.

Table 1. Protection Modes

MODE PINS			PROTECTION MODE
M3(1)	M2	M1	
0	0	0	Full protection (default)
0	0	1	Reserved
0	1	0	OC latching mode
0	1	1	Reserved

(1) M3 is reserved and always should be connected to board GND.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
AGND	9	I	Analog ground
BST_A	1	P	Bootstrap, A side
BST_B	18	I	Bootstrap, B side
GND	8, 16	I	Power ground
GVDD_A	2	P	Gate-drive voltage supply, A side
GVDD_B	17	I	Gate-drive voltage supply, B side
M1	13	I	Mode-selection 1 (LSB)
M2	12	I	Mode-selection 2 (MSB)
M3	11	I	Reserved
OC_ADJ	7	I	Overcurrent threshold programming
$\overline{\text{OTW}}$	3	O	Overtemperature warning. Open drain, active low.
OUT_A	28, 29, 30	O	Output, half-bridge A
OUT_B	25, 26, 27	O	Output, half-bridge B
PGND	22, 23, 24, 31, 32, 33	P	Power ground
PWM_A	6	I	PWM for half-bridge A
PWM_B	14	I	PWM Input for half-bridge B
PVDD_A	34, 35, 36	P	PVDD supply for half-bridge A
PVDD_B	19, 20, 21	P	PVDD supply for half-bridge B
$\overline{\text{RESET}}$	5	I	Reset. Active low.
$\overline{\text{SD}}$	4	O	Shutdown. Open drain, active low.
VDD	15	I	Input power supply
VREG	10	O	Internal voltage regulator

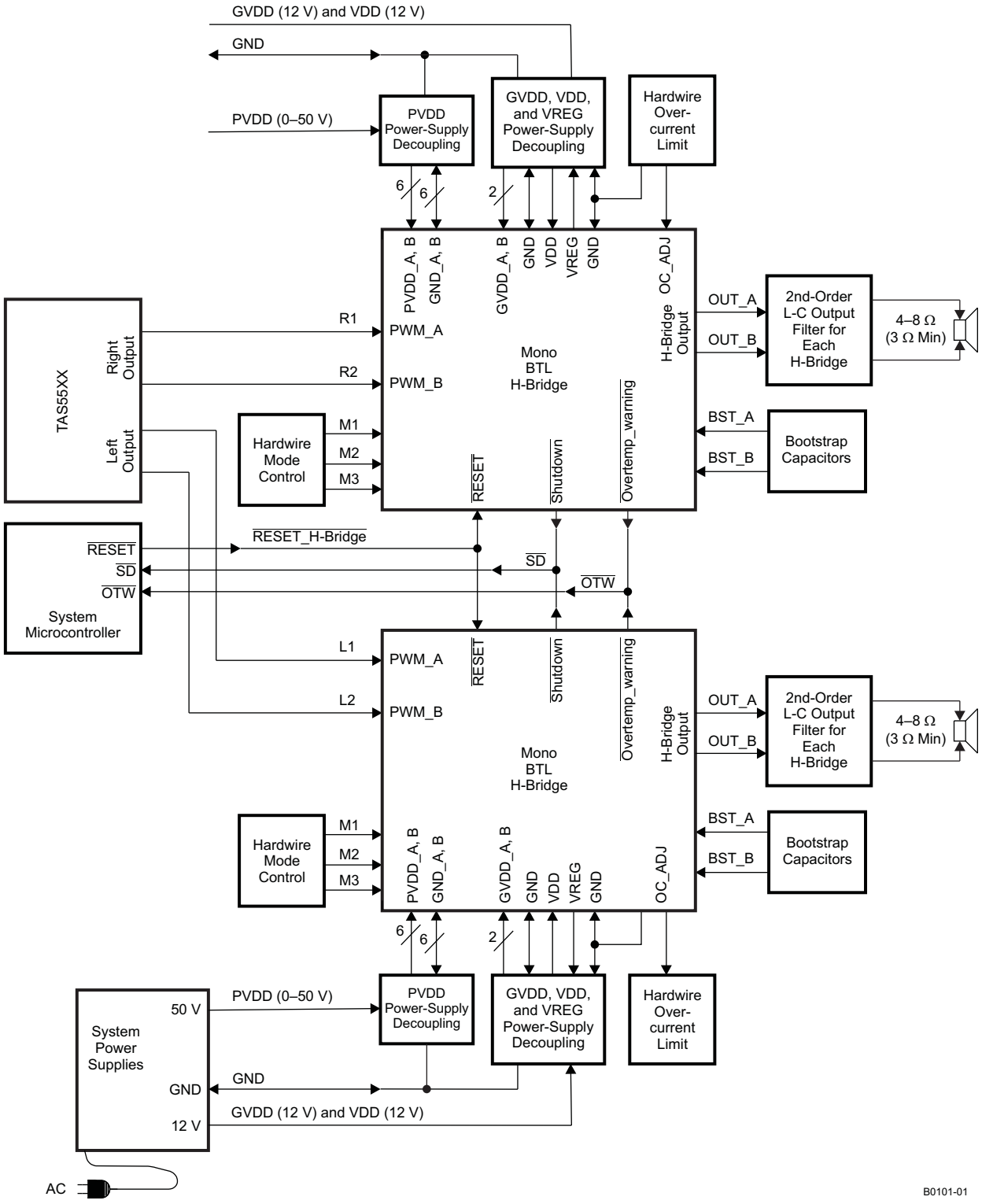


Figure 1. Typical System Block Diagram

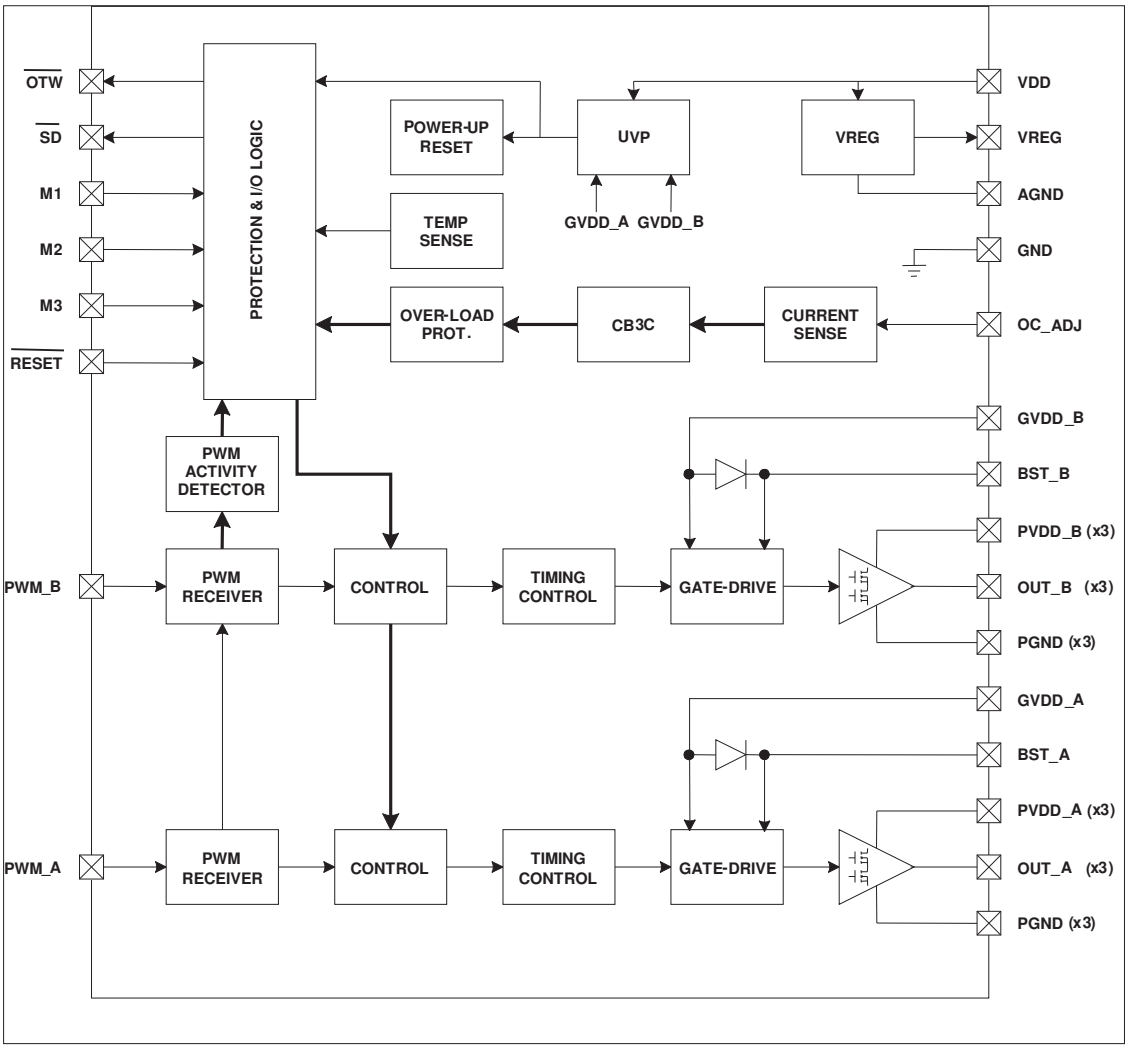


Figure 2. Functional Block Diagram

ORDERING INFORMATION

T_A	PACKAGE	DESCRIPTION
0°C to 70°C	TAS5261DKD	36-pin PSOP3

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VDD to AGND	–0.3	13.2	V
GVDD_x to AGND	–0.3	13.2	V
PVDD_x to PGND_x(2)	–0.3	71	V
OUT_x to PGND_x(2)	–0.3	71	V
BST_x to PGND_x(2)	–0.3	79.7	V
BST_x to GVDD_x(2)	–0.3	66.5	V
VREG to AGND	–0.3	4.2	V
PGND_x to GND	–0.3	0.3	V
PGND_x to AGND	–0.3	0.3	V
GND to AGND	–0.3	0.3	V
PWM_x, OC_ADJ, M1, M2, M3 to AGND	–0.3	4.2	V
$\overline{\text{RESET}}$, $\overline{\text{SD}}$, $\overline{\text{OTW}}$ to AGND	–0.3	7	V
Maximum continuous sink current ($\overline{\text{SD}}$, $\overline{\text{OTW}}$)		9	mA
Maximum operating junction temperature range, T_J	0	150	°C
Storage temperature range, T_{stg}	–65	150	°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s		260	°C
Minimum pulse duration, low – minimum pulse width must be ensured by the PWM processor	50		ns

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are only stress ratings, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represent the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
PVDD_x	Half-bridge supply voltage	0	50	52.5	V
GVDD_x	Gate-drive power supply	10.8(1)	12	13.2	V
VDD	Digital regulator supply voltage	10.8(1)	12	13.2	V
R_L	Resistive load impedance, bridge-tied load (BTL)		4-16		Ω
R_L	Resistive load impedance, BTL, R_{OC} = 22kΩ, PVDD = 50V, (no current limiting)	3			Ω
L_{DEM}	Minimum output filter inductance under both operating and short-circuit conditions, with appropriate OC_ADJ resistor value	5	10		µH
f_S	PWM frame rate	192		384	kHz
$t_{(low)}$	Minimum low-state pulse duration per PWM frame, noise shaper enabled	50			ns
C_{BS}	Bootstrap capacitor, selected value supports f_s = 192 kHz to 384 kHz		33		nF
R_{BS}	Bootstrap series resistor - 1/4 W		1.5		Ω
RC_{BS}	Bootstrap snubber - 1/4 W		4.7		Ω
			470		pF
D_{CLMP}	Ultra-Fast Recovery Clamping Diode, Average forward current = 1A, Maximum repetitive reverse voltage = 200V (ES1D, mfg:Fairchild)		15		nS
D_{TVS}	Transient Voltage Suppressor, 600W @ 1mS (P6SMB62AT3, mfg: ON Semiconductor)		62		V
C_{PVDD}	PVDD Close Decoupling Capacitor, two capacitors		100		nF
R_{AGND}	AGND resistor - 1/4 W		3.3		Ω
R	Optional external pullup resistor to +3.3V or +5 V for $\overline{SD}$ and $\overline{OTW}$	3.3	4.7		kΩ
T_J	Junction temperature	0		125	°C

(1) GVDD operation below 10.8 V significantly reduces efficiency of the output MOSFET stage and requires a larger heatsink. For the purpose of noise margin, the UVP level is set lower to provide an increased noise margin, however, TI recommends a nominal dc voltage of 12 V for GVDD.

AUDIO CHARACTERISTICS

Audio frequency = 1 kHz, PVDD_x = 50 V, GVDD_x = 12 V, VDD = 12 V, R_L = 8 Ω , f_s = 384 kHz, OC_ADJ = 22 kΩ, T_C= 75°C, output filter is L_{DEM} = 10 µH, C_L = 1 µF (unless otherwise noted). Audio performance is recorded as a chipset, TAS5518 as front end with an effective modulation index of 96.1% and TAS5261 as the power stage. PCB and system configuration are in accordance with recommended design guidelines.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Unclipped power output	R_L = 8 Ω, f = 1 kHz		125		W
		R_L = 6 Ω, f = 1 kHz		165		
		R_L = 4 Ω, f = 1 kHz		235		
P_O	Maximum power output	R_L = 8 Ω, f = 1 kHz, THD = 10%		165		W
		R_L = 6 Ω, f = 1 kHz, THD = 10%		220		
		R_L = 4 Ω, f = 1 kHz, THD = 10%		315		
		R_L = 3 Ω, f = 1 kHz, CBC allowed		400		
THD+N	Total harmonic distortion + noise, AES 17 filter	1 W to 125 W, RL=8 Ω, AES17 filter, Unclipped		0.09		%
SNR	Signal-to-noise ratio(1)	Ratio of 1-FFS to 0-FFS input, A-weighted filter		110		dB
DNR	Dynamic range	–60-dBFS input, A-weighted filter		110		dB
VOO	Output offset voltage	PWM switching frequency 384 kHz, Measured on speaker terminals	–15		15	mV
P_{idle}	Power dissipation due to idle losses (I_{PVDD_X})	P_O = 0 W, Output switching(2)		2		W

(1) SNR is calculated relative to the 0 dBFS input level.
(2) Actual system idle losses are also affected by core losses of output inductors.

ELECTRICAL CHARACTERISTICS

Audio frequency = 1 kHz, PVDD_x = 50 V, GVDDx = 12 V, VDD = 12 V, R_L = 8 Ω , f_s = 384 kHz, OC_ADJ = 22 kΩ, T_C = 75°C, output filter is L_{DEM} = 10 µH, C_L = 1 µF (unless otherwise noted). AC performance is recorded as a chipset, TAS5518 as front end with an effective modulation index of 96.1% and TAS5261 as the power stage. PCB and system configuration are in accordance with recommended design guidelines.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Internal Voltage Regulator and Current Consumption						
VREG	Voltage regulator, only used as reference node			3.3		V
I_{VDD}	VDD supply current	Operating, 50% duty cycle		7.7		mA
		Idle, reset mode		6.7		
I_{GVDD_x}	GVDD_x gate-supply current per half bridge	50% duty cycle		15		mA
		Idle, reset mode		1.5		
I_{PVDD_x}	Half-bridge idle current	50% duty cycle		23		mA
		Reset mode ($\overline{RESET}$ = 1), No switching		100		µA
Output-Stage MOSFETs						
$R_{DSON,LS}$	Drain-to-source resistance, low side	T_J = 25°C, LDMOS only		40		mΩ
$R_{DSON,HS}$	Drain-to-source resistance, high side	T_J = 25°C, LDMOS only		40		mΩ
I/O Protection						
$V_{UVP,POS}$	Undervoltage protection limit, GVDD_x			8.5		V
OTW	Overtemperature warning			125		°C
OTW_{hys}	OTW hysteresis			25		°C
OTE	Overtemperature error threshold			155		°C
OTE_{hys}	OTE hysteresis			30		°C
OTE-OTW differential	Temperature delta between OTW and OTE			30		°C
OLPC	Overload protection time constant	f_{PWM} = 384 kHz	20			ms
I_{OC}	Overcurrent limit response (1)	Resistor programmable high end with OC_ADJ = 22 kΩ(1)	15	16	17	A
R_{OC}	Programming resistor		22		100	kΩ
R_{PD}	Pulldown resistor at the output of each half-bridge	Connected when $\overline{RESET}$ is high to provide a charge path for the bootstrap capacitor		2.5		kΩ
PWM	PWM Activity Detector	Lack of transition of any PWM input		13		µs

(1) DC measurement with 1-ms pulse

ELECTRICAL CHARACTERISTICS

GVDD_x = 12 V ± 10%, VDD = 12 V ± 10%, T_J = 25°C (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Logic-Level and Open-Drain Outputs						
V_{IH}	High-level input voltage	Static	2			V
V_{IL}	Low-level input voltage	Static			0.8	V
I_{lkg} (1)	Input leakage current	Static, High PWM_A, High PWM_B, High M1, High M2, High M3	45		65	µA
		Static, Low PWM_A, Low PWM_B, Low M1, Low M2, Low M3	–10		10	
		Static, High $\overline{\text{RESET}}$	20		40	
		Static, Low $\overline{\text{RESET}}$	–70		–50	
R_{INT-PD}	Internal pulldown to AGND for PWM_A and PWM_B inputs			50		kΩ
R_{INT-PU}	Internal pullup resistance on $\overline{\text{OTW}}$ and $\overline{\text{SD}}$	Resistor to VREG	20	28	33	kΩ
V_{OH}	High-level output voltage	Internal pullup resistor	2.4		VREG	V
		External pullup of 3.3 kΩ to 5 V	2.5		4.9	
V_{OL}	Low-level output voltage	I_O = 4 mA			0.4	V
FANOUT	Device fanout ($\overline{\text{OTW}}$, $\overline{\text{SD}}$)	External pullup to 5 V	10			Devices

(1) Pullup and pulldown resistors affect the leakage current.

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

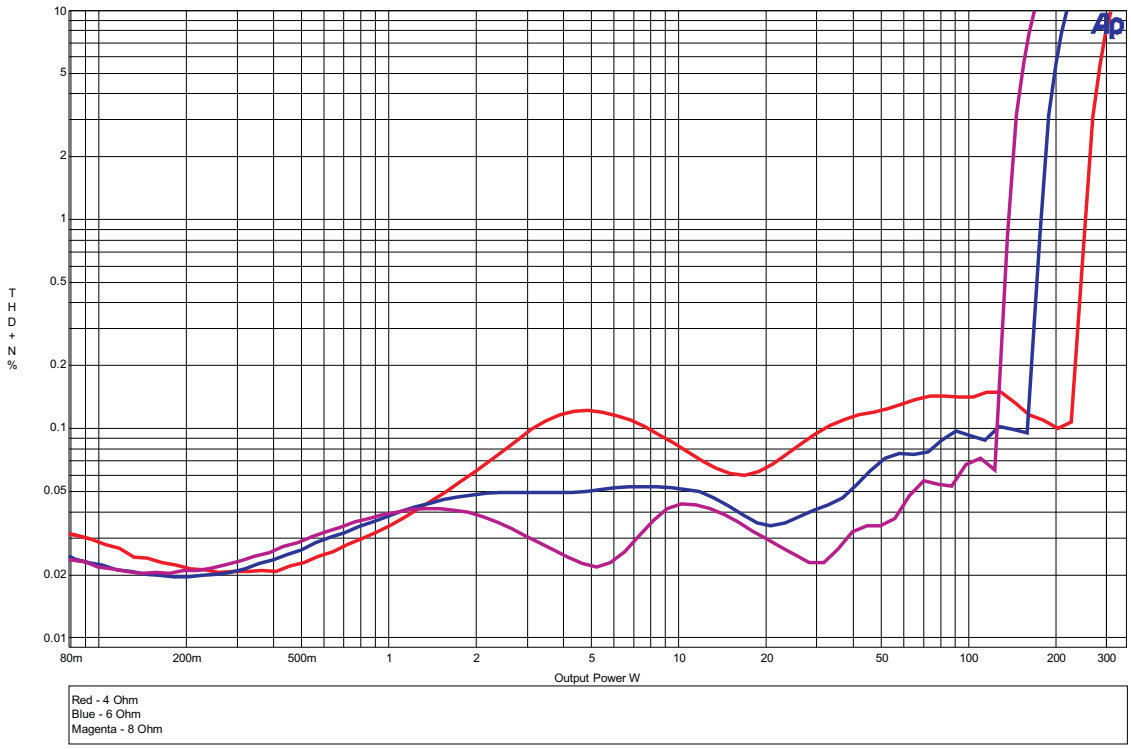


Figure 3.

OUTPUT POWER
vs
PVDD_x SUPPLY VOLTAGE

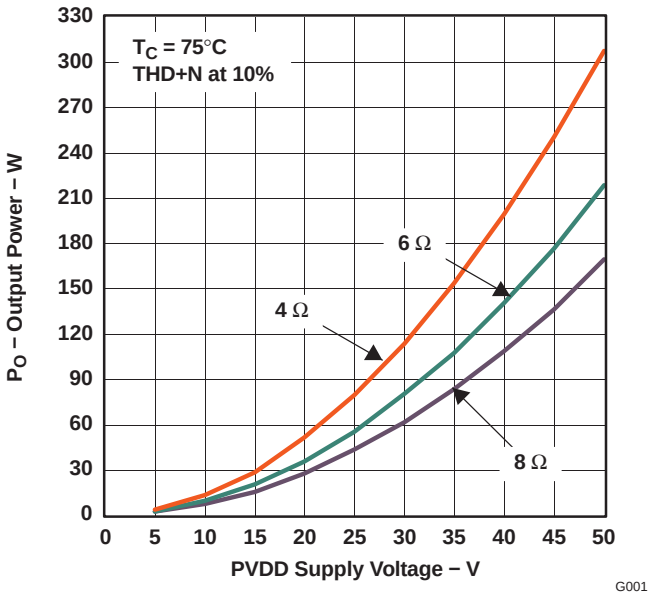


Figure 4.

UNCLIPPED OUTPUT POWER
vs
PVDD_x SUPPLY VOLTAGE

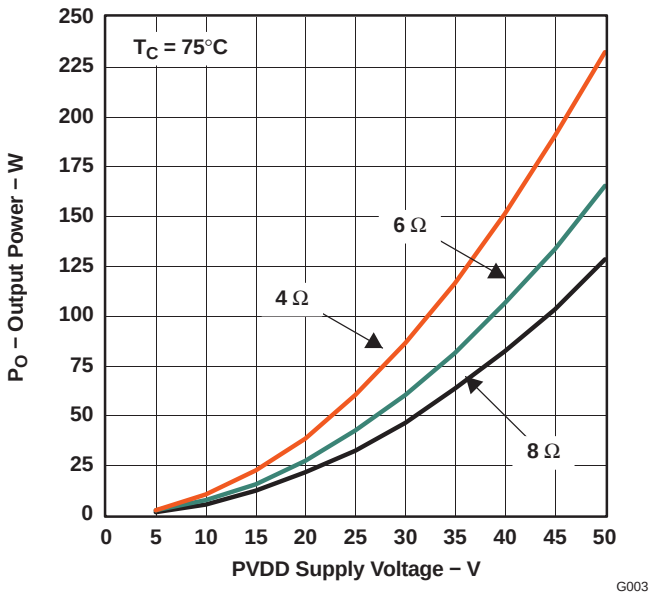


Figure 5.

TYPICAL CHARACTERISTICS (continued)

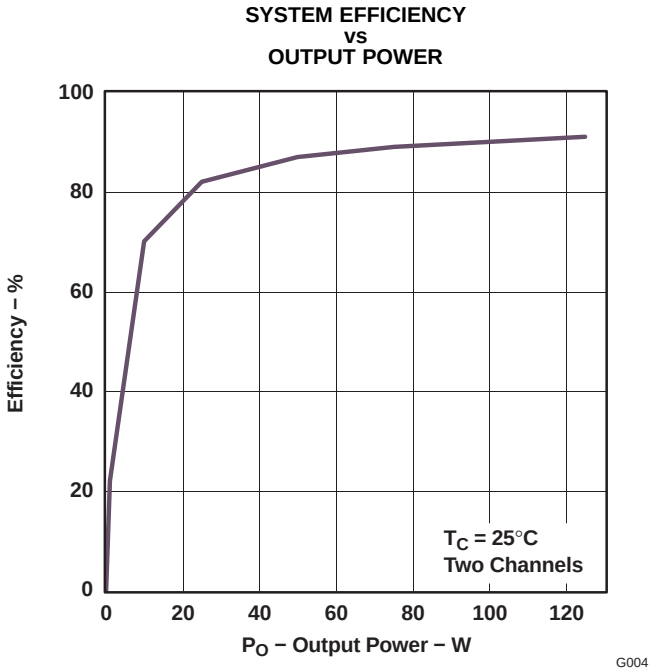


Figure 6.

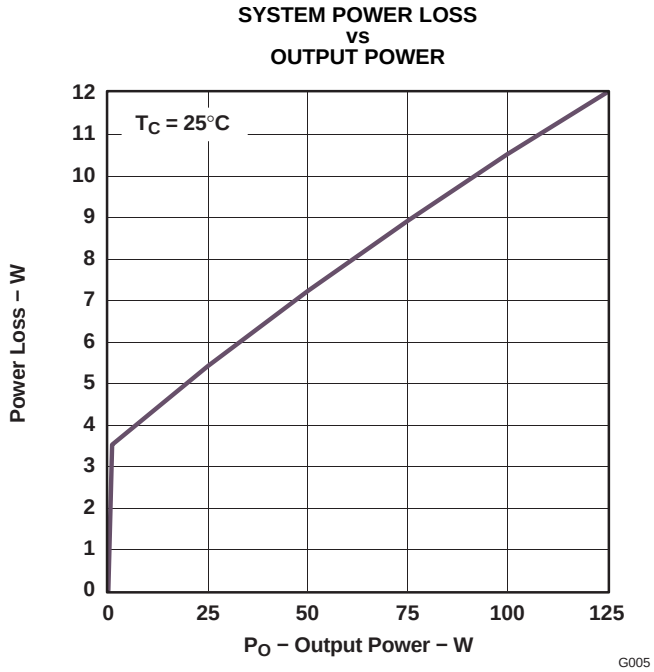


Figure 7.

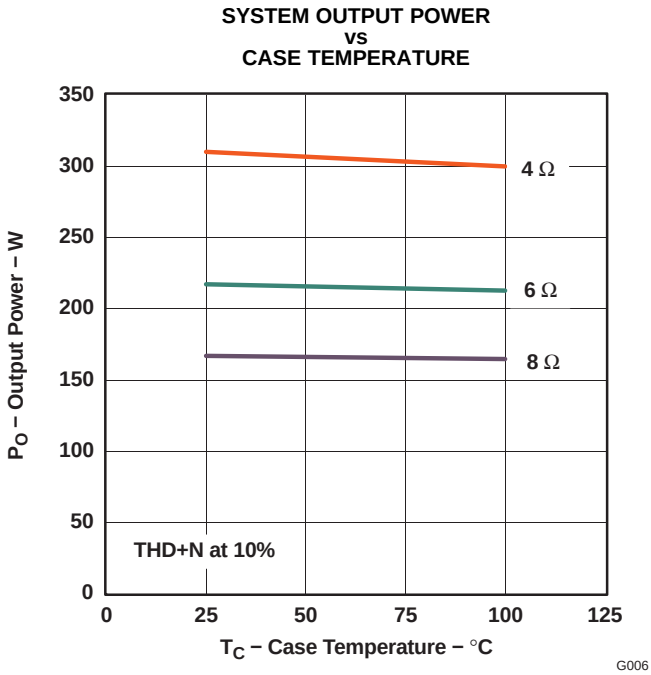


Figure 8.

TYPICAL CHARACTERISTICS (continued)

NOISE AMPLITUDE vs FREQUENCY

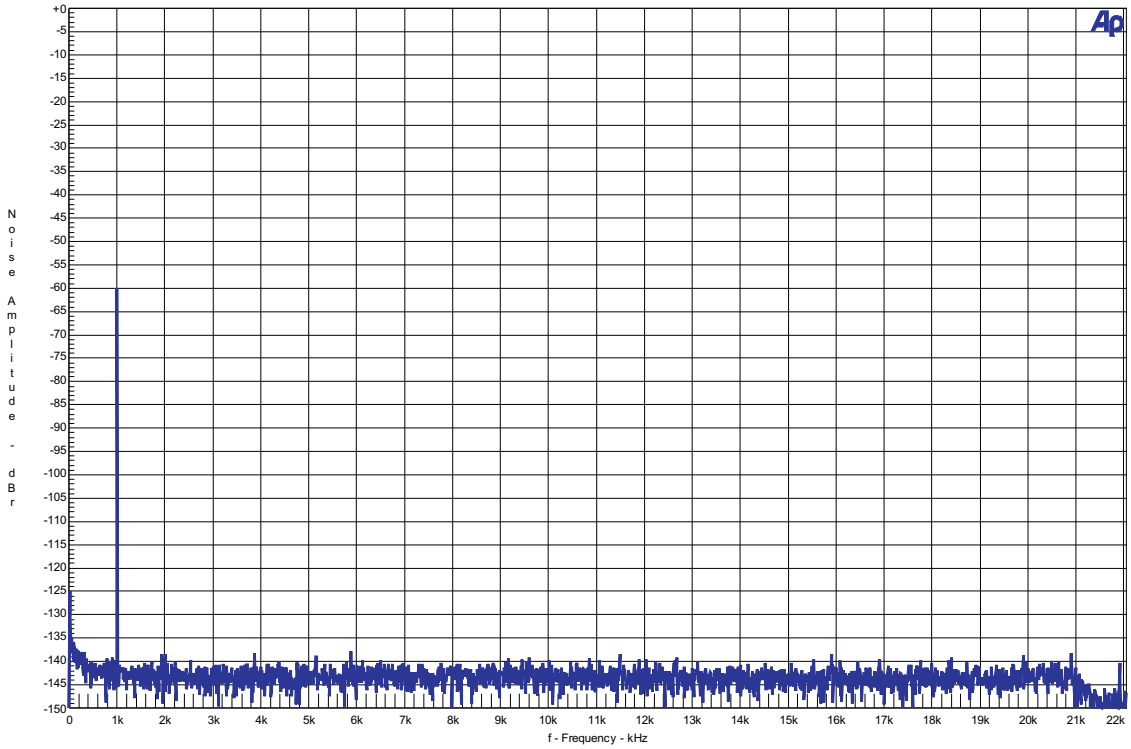
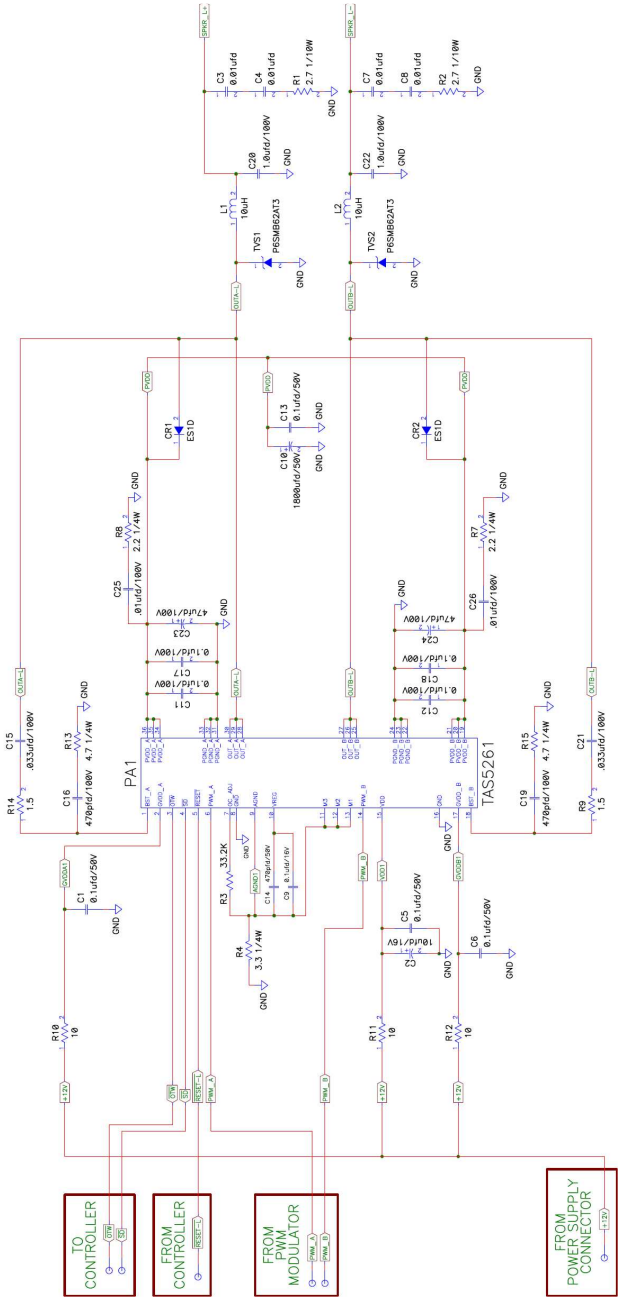


Figure 9.

APPLICATION INFORMATION

Typical Application Schematic



APPLICATION INFORMATION (continued)

Recommended Printed Circuit Board (PCB) Layout

PCB Requirements

- 2-oz copper (FR-4) recommended
- PVDD voltage and capacitor selection in accordance with the data sheet

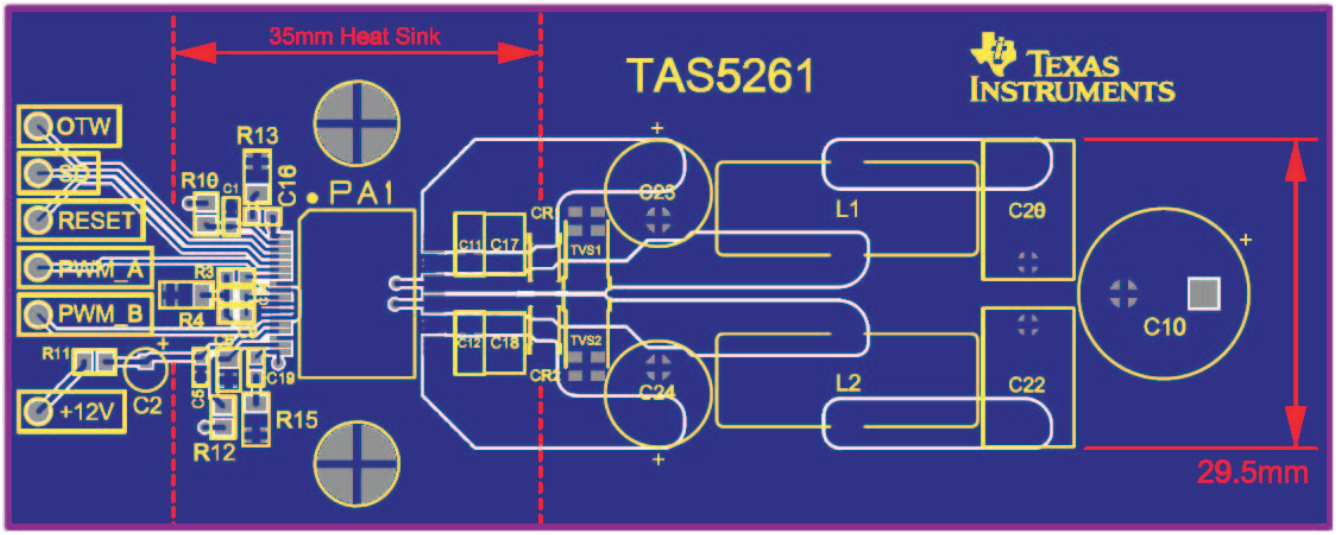


Figure 10. PCB (Top Layer)

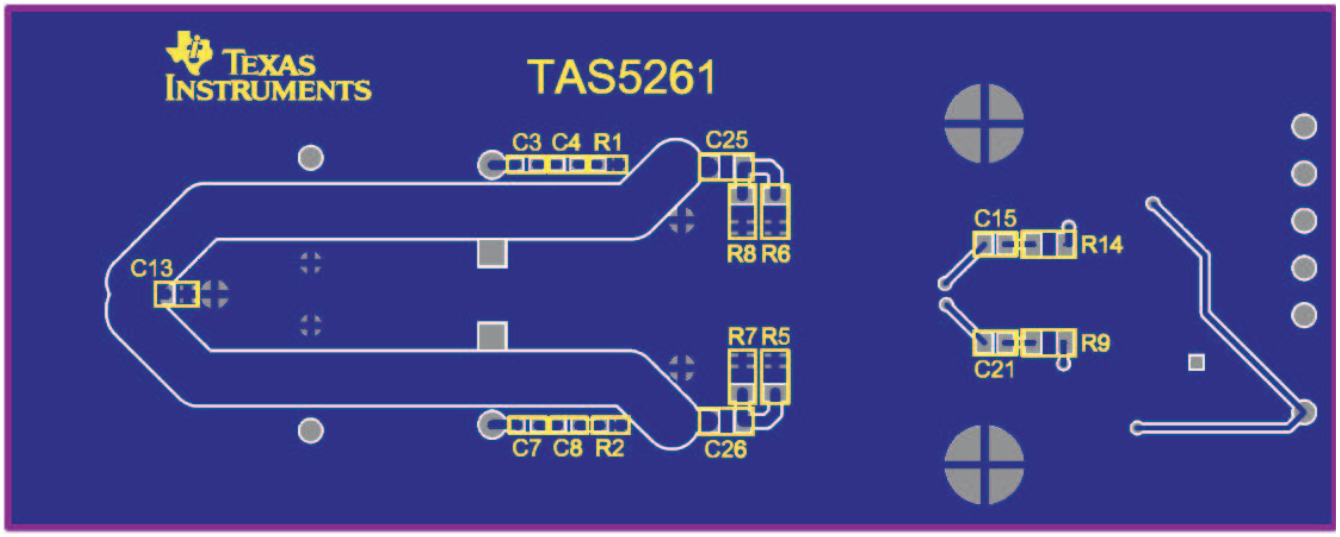


Figure 11. PCB (Bottom Layer)

THEORY OF OPERATION

Power Supplies

To facilitate system design, the TAS5261 needs only a 12-V supply in addition to a typical 50-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

To provide outstanding electrical and acoustic characteristics, the PWM signal path, including gate drive and output stage, is designed as identical, independent half bridges. For this reason, each half bridge has separated gate-drive supply (GVDD_x), bootstrap pins (BST_x) and power-stage supply pins (PVDD_x). Furthermore, an additional pin (VDD) is provided as power supply for all common circuits. Although supplied from the same 12-V source, it is highly recommended to separate GVDD_x and VDD on the printed circuit board (PCB) by RC filters (see application diagram for details). These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power-supply pins and decoupling capacitors must be avoided. (See reference board documentation for additional information.)

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_x) to the power-stage output pin (OUT_x). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_x) and the bootstrap pin. When the power-stage output voltage is high, the bootstrap capacitor voltage is shifted above the output voltage potential and, thus, provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range of 352 kHz to 384 kHz, it is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap capacitor. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power-stage FET (LDMOS) fully started during all of the remaining part of the PWM cycle. In an application running at a reduced switching frequency, generally 250 kHz to 192 kHz, the bootstrap capacitor might need to be increased in value. Special attention should be paid to the power-stage power supply – this includes component selection, PCB placement, and routing. As indicated, each half bridge has independent power-stage supply pins (PVDD_x). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_x pin is decoupled with two 100-nF ceramic capacitors placed as close as possible to each supply pin on the same side of the PCB as the TAS5261 location. It is recommended to follow the PCB layout of the TAS5261 reference design. For additional information on the recommended power supply and required components, see the application diagrams given in this data sheet.

The 12-V supply should be powered from a low-noise, low-output-impedance voltage regulator. Likewise, the 50-V power-stage supply is assumed to have low output impedance and low noise. The internal POR circuit eliminates the need for power-supply sequencing. Moreover, the TAS5261 is fully protected against erroneous power-stage turn on due to parasitic gate charging. Thus, voltage-supply ramp rates (dv/dt) are noncritical within the specified range (see the *Recommended Operating Conditions* section of this data sheet).

System Power-Up/Power-Down Sequence

Powering Up

There is no power-up sequence is required for the TAS5261. The outputs of the H-bridge remain in a high-impedance state until the gate-drive supply voltage (GVDD_x) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is recommended to hold $\overline{\text{RESET}}$ in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

While powering up the TAS5261, $\overline{\text{RESET}}$ should be held low.

Powering Down

There is no power-down sequence is required for the TAS5261. The device remains fully operational as long as the gate-drive supply (GVDD_x) voltage and VDD voltage are above the undervoltage protection (UVP) threshold level (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is a good practice to hold $\overline{\text{RESET}}$ low during power down, thus, preventing audible artifacts including pops and clicks.

Error Reporting

The $\overline{SD}$ and $\overline{OTW}$ pins are both active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device. Any fault resulting in device shutdown is signaled by the $\overline{SD}$ pin going low. Likewise, $\overline{OTW}$ goes low when the device junction temperature exceeds 115°C. (see Table 2).

Table 2. Error Reporting

$\overline{SD}$	$\overline{OTW}$	DESCRIPTION
0	0	Over Temperature (OTE) or Over Load (OLP) or Under Voltage (UVP)
0	1	Over Load (OLP), PWM Activity Dectector, or Under Voltage (UVP)
1	0	Over Temperature Warning. Junction temperature higher than 125°C.
1	1	Normal operation. Junction temperature lower than 125°C.

It should be noted that asserting $\overline{RESET}$ low forces the $\overline{SD}$ and $\overline{OTW}$ signals high, independent of faults being present. It is recommended to monitor the $\overline{OTW}$ signal using the system microcontroller and respond to an overtemperature warning signal by, for example, turning down the volume to prevent further heating of the device resulting in device shutdown ($\overline{OTW}$). To reduce external component count, an internal pullup resistor to 3.3 V is provided on both the $\overline{SD}$ and $\overline{OTW}$ outputs. Level compliance for 5-V logic can be obtained by adding external pullup resistors to 5 V (see the *Electrical Characteristics* section of this data sheet for further specifications).

Device Protection System

The TAS5261 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as safeguarding the device from permanent failure due to a wide range of fault conditions, such as short circuit, overload, and undervoltage. The TAS5261 responds to a fault by immediately setting the power stage in a high-impedance state (Hi-Z) and asserting the $\overline{SD}$ pin low. In situations other than overload, the device automatically recovers when the fault condition has been removed (e.g., the voltage supply has increased). For highest possible reliability, recovering from an overload fault requires external reset of the device no sooner than 1 s after the shutdown (see the *Device Reset* section of this data sheet).

Over Current (OC) Protection With Current Limiting and Overload Detection

The device has independent, fast-reacting current detectors with programmable trip threshold (OC threshold) on all high-side and low-side power-stage FETs. See Table 3 for OC-adjust resistor values. The detector outputs are closely monitored by two protection systems. The first protection system controls the power stage in order to prevent the output current from further increasing. For instance, it performs a current-limiting function rather than prematurely shutting down during combinations of high-level music transients and extreme speaker load impedance drops. If the high-current situation persists, i.e., the power stage is being overloaded, a second protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state.

Table 3. OC-Adjust Resistor Values

OC-ADJUST RESISTOR VALUES (kΩ) (1)	CURRENT BEFORE OC OCCURS (A)		
	MIN	TYP	MAX
22	15	16	17
27	12	13	14
47	7	8	8
68	5	5	6
100	3	4	4

(1) Resistor tolerance is ±5%.

For lowest-cost bill of materials in terms of component selection, the OC threshold current should be limited, considering the power output requirement and minimum load impedance. Higher-impedance loads require a lower OC threshold.

The demodulation filter inductor must retain a minimum of 5-H inductance at twice the selected OC threshold current.

Most inductors have decreasing inductance with increasing temperature and increasing current (saturation). To some degree, an increase in temperature naturally occurs when operating at high output currents, due to inductor core losses and the dc resistance of the inductor copper winding. A thorough analysis of inductor saturation and thermal properties is strongly recommended.

Setting the OC threshold too low might cause issues, such as lack of enough output power and/or unexpected shutdowns due to sensitive overload detection.

In general, it is recommended to follow closely the external component selection and PCB layout as given in the *Application Information* section of this data sheet.

For added flexibility, the OC threshold is programmable within a limited range using a single external resistor connected between the OC_ADJ pin and AGND. It should be noted that a properly functioning overcurrent detector assumes the presence of a properly designed demodulation filter at the power-stage output. Short-circuit protection is not provided directly at the output pins of the power stage but only on the speaker terminals (after the demodulation filter). It is required to follow certain guidelines when selecting the OC threshold and an appropriate demodulation inductor.

Over Temperature (OTE) Protection

The TAS5261 has a two-level, temperature-protection system that asserts an active-low warning signal ($\overline{\text{OTW}}$) when the device junction temperature exceeds the OTW level stated in the parametric table. If the device junction temperature exceeds the OTE level stated in the parametric table, the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance state (Hi-Z) and $\overline{\text{SD}}$ being asserted low. OTE is latched in this case. To clear the OTE latch, reset must be asserted. Thereafter, the device resumes normal operation.

Under Voltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the TAS5261 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_x and VDD supply voltages reach the UVP level stated in the parametric table. Although GVDD_x and VDD are independently monitored, a supply-voltage drop below the UVP threshold on any VDD or GVDD_x pin results in all half-bridge outputs immediately being set in the high-impedance state (Hi-Z) and $\overline{\text{SD}}$ being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

Device Reset

When $\overline{\text{RESET}}$ is asserted low, the output FETs in all half bridges are forced into a high-impedance state (Hi-Z). During this reset time, a resistor is connected between OUT_x and PGND pins, in order to charge the bootstrap capacitor.

Asserting $\overline{\text{RESET}}$ input low removes fault information. A rising-edge transition on the reset input allows the device to resume operation after an overload fault.

PWM Activity Detector

The PWM Activity Detector logic monitors individual PWM inputs. If one or more inputs are stuck in either a high state or a low state for more than a defined length of time, the entire device is shut down.

The PWM Activity Detector is not latched and normal operation resumes when PWM activity is present on the PWM inputs. When an invalid PWM frame is detected, the PWM Activity Detector responds immediately (no delay). The TAS5261 resumes operation as soon as valid PWM signals are present.

The PWM Activity Detector is reported as a low on the $\overline{\text{SD}}$ pin.

Modulation Index Setting

96.1% is the recommended setting for the modulation index limit of the PWM when driving the TAS5261. The following shows modulation index limit registers and setting value in hexadecimal for TI modulators.

TAS5508/TAS5518: 0x16h at 04h

TAS5086: 0x10h at 04h

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5261DKD	ACTIVE	HSSOP	DKD	36	29	Green (RoHS & no Sb/Br)	NIPDAU	Level-4-260C-72 HR	0 to 70	TAS5261	Samples
TAS5261DKDR	ACTIVE	HSSOP	DKD	36	500	Green (RoHS & no Sb/Br)	NIPDAU	Level-4-260C-72 HR	0 to 70	TAS5261	Samples
TAS5261DKDRG4	ACTIVE	HSSOP	DKD	36	500	Green (RoHS & no Sb/Br)	NIPDAU	Level-4-260C-72 HR	0 to 70	TAS5261	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

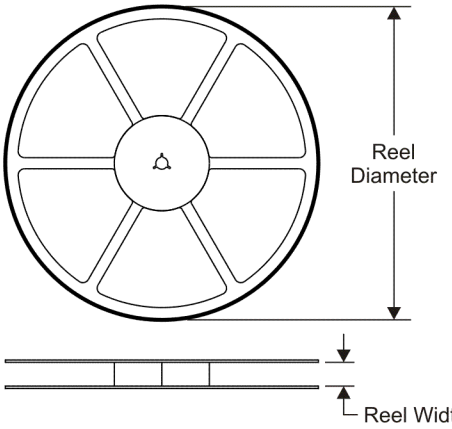
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

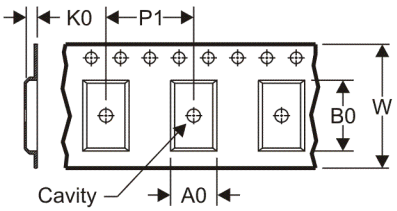
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

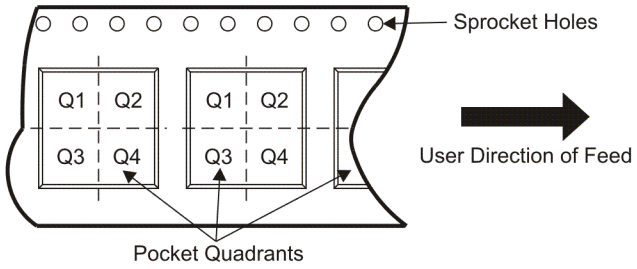


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

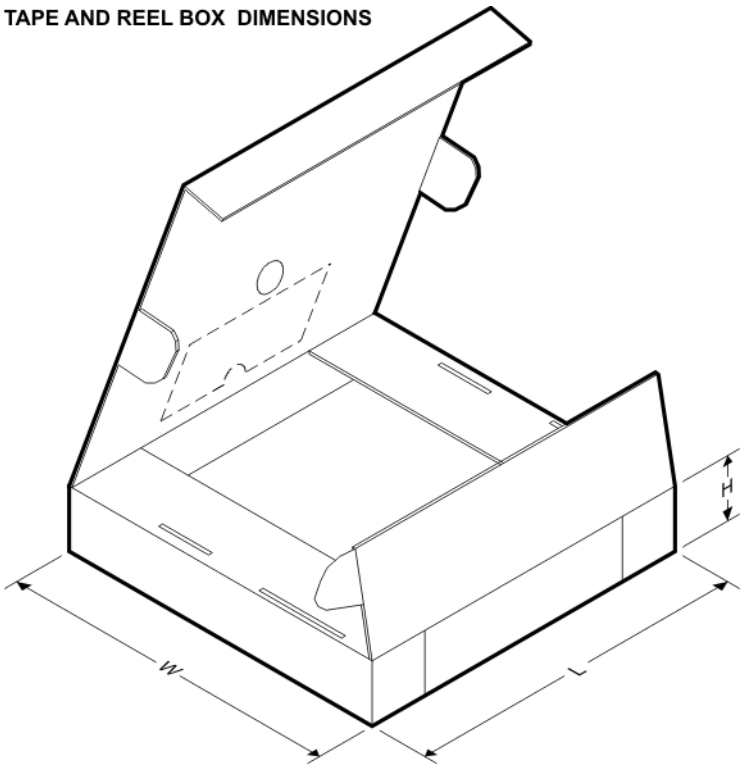
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5261DKDR	HSSOP	DKD	36	500	330.0	24.4	14.7	16.4	4.0	20.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



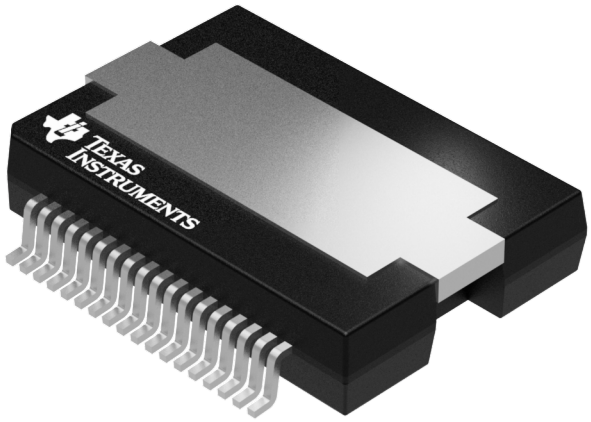
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5261DKDR	HSSOP	DKD	36	500	337.0	343.0	41.0

GENERIC PACKAGE VIEW

DKD 36 PowerPAD™ SSOP - 3.6 mm max height

PLASTIC SMALL OUTLINE

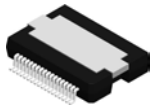


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204421-2/N

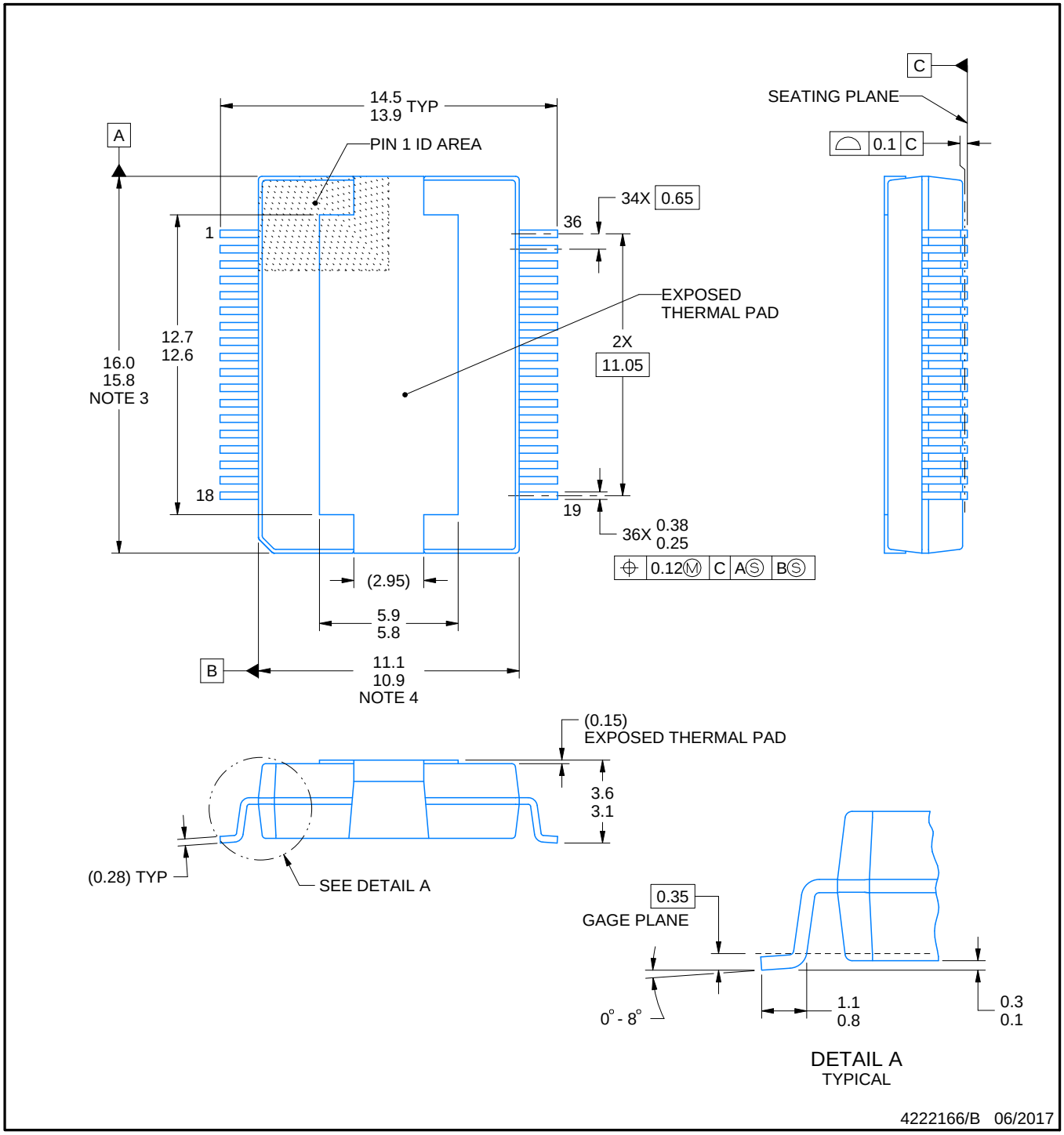
PACKAGE OUTLINE

DKD0036A



PowerPAD™ SSOP - 3.6 mm max height

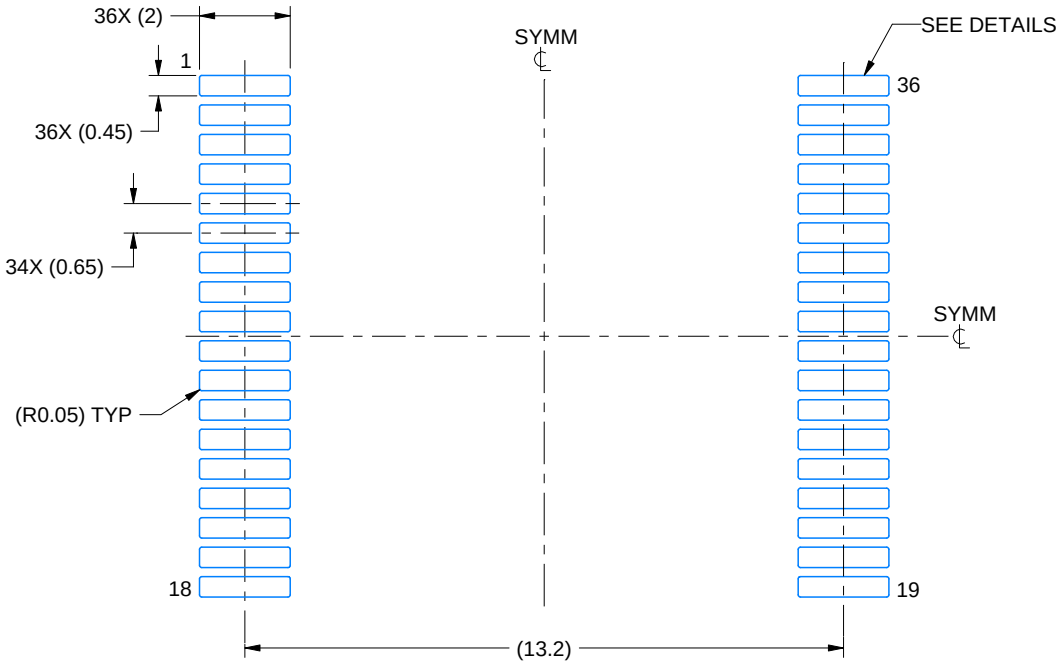
PLASTIC SMALL OUTLINE



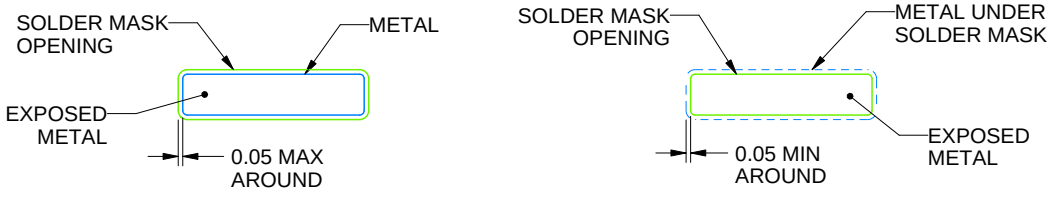
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. The exposed thermal pad is designed to be attached to an external heatsink.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

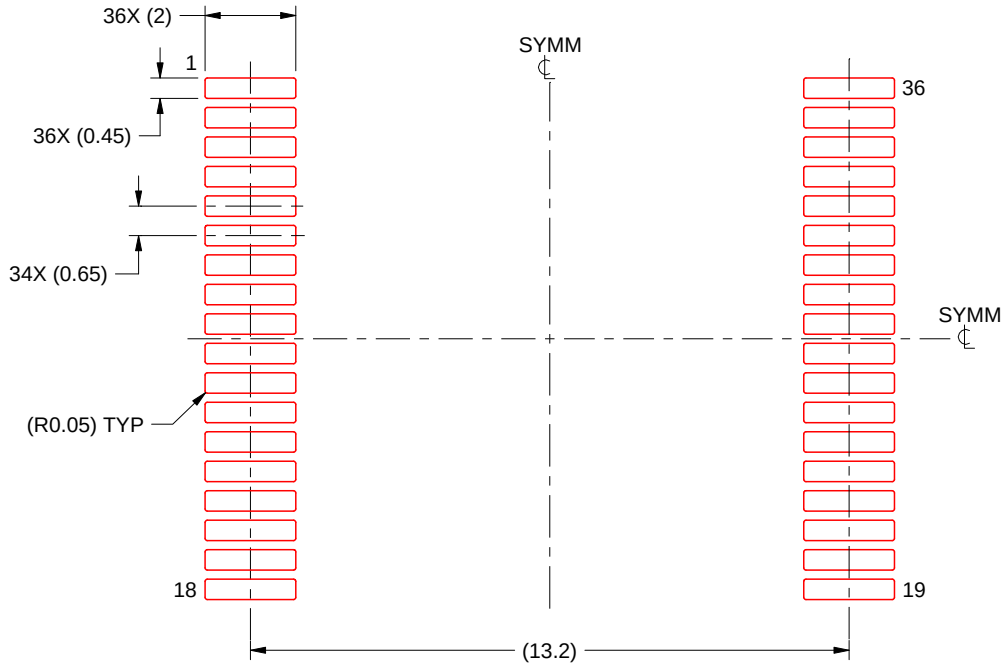


SOLDER MASK DETAILS
NOT TO SCALE

4222166/B 06/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE:6X

4222166/B 06/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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