Quad, 12-Bit, Parallel Input, Unipolar/Bipolar, Voltage Output DAC

Data Sheet

AD5725

FEATURES

+5 V to ±15 V operation
Unipolar or bipolar operation
±0.5 LSB max INL error, ±1 LSB max DNL error
Settling time: 10 µs max (10 V step)
Double-buffered inputs
Simultaneous updating via $\overline{\text{LDAC}}$
Asynchronous $\overline{\text{CLR}}$ to zero/mid scale
Readback
Operating temperature range: −40°C to +85°C
***i*CMOS® process technology**

APPLICATIONS

Industrial automation
Closed-loop servo control, process control
Automotive test and measurement
Programmable logic controllers

FUNCTIONAL BLOCK DIAGRAM

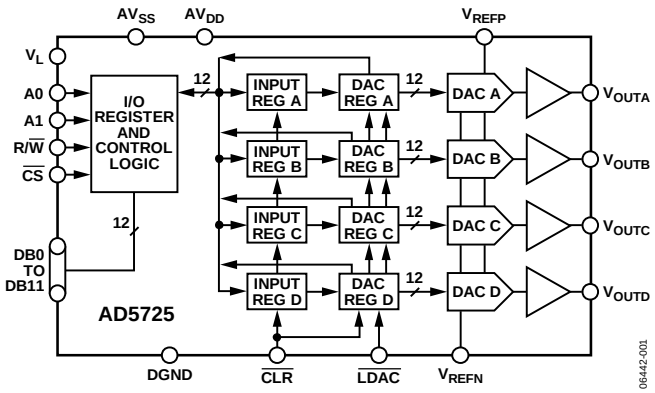

Figure 1.

GENERAL DESCRIPTION

The AD5725 is a quad, 12-bit, parallel input, voltage output digital-to-analog converter that offers guaranteed monotonicity, integral nonlinearity (INL) of ±0.5 LSB maximum and 10 µs maximum settling time.

Output voltage swing is set by two reference inputs, V_{REFP} and V_{REFN}. By setting the V_{REFN} input to 0 V and the V_{REFP} to a positive voltage, the DAC provides a unipolar positive output range. A similar configuration with V_{REFP} at 0 V and V_{REFN} at a negative voltage provides a unipolar negative output range. Bipolar outputs are configured by connecting both V_{REFP} and V_{REFN} to nonzero voltages. This method of setting output voltage ranges has advantages over the bipolar offsetting methods because it is not dependent on internal and external resistors with different temperature coefficients.

Digital controls allow the user to load or read back data from any DAC, load any DAC, and transfer data to all DACs at one time.

The AD5725 is available in a 28-lead SSOP package. It can be operated from a wide variety of supply and reference voltages, with supplies ranging from single +5 V to ±15 V, and references from +2.5 V to ±10 V. Power dissipation is less than 270 mW with ±15 V supplies and only 40 mW with a +5 V supply. Operation is specified over the temperature range of −40°C to +85°C.

*i*CMOS® Process Technology
For analog systems designers within industrial/instrumentation equipment OEMs who need high performance ICs at higher-voltage levels, *i*CMOS is a technology platform that enables the development of analog ICs capable of 30 V and operating at ±15 V supplies while allowing dramatic reductions in power consumption and package size, and increased ac and dc performance.

Rev. C **Document Feedback**

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REVISION HISTORY

8/13—Rev. B to Rev. C

Change Junction Temperature from 105°C to 150°C; Changed Power Dissipation Package Condition from Derate 10 mW/°C Above 70°C to Derate 10 mW/°C Above 60°C; Table 5 ... 8

4/13—Rev. A to Rev. B

Changes to V_{REFN} Input Current Parameter, Table 1 ... 3
Changes to Figure 27 and Figure 28 ... 17
Changes to Figure 29 and Figure 30 ... 18

12/08—Rev. 0 to Rev. A

Changes to Figure 26 ... 13

7/07—Revision 0: Initial Version

Power Dissipation Package (Derate 10 mW/°C Above 60°C)

SPECIFICATIONS

AV_{DD} = +15 V, AV_{SS} = −15 V, DGND = 0 V; V_{REFP} = +10 V; V_{REFN} = −10 V, V_L = 5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 1.

Parameter	Value	Unit	Test Conditions/Comments
ACCURACY			Outputs unloaded
Resolution	12	Bits	
Relative Accuracy (INL)	±0.5	LSB max	B grade
	±1	LSB max	A grade
Differential Nonlinearity (DNL)	±1	LSB max	Guaranteed monotonic
Zero-Scale Error	±2	LSB max	R_L = 2 kΩ
Zero-Scale TC[2]	±15	ppm FSR/°C typ	R_L = 2 kΩ
Full-Scale Error	±2	LSB max	R_L = 2 kΩ
Full-Scale TC[2]	±20	ppm FSR/°C typ	R_L = 2 kΩ
REFERENCE INPUT			
V_{REFP}			
Reference Input Range[3]	V_{REFN} + 2.5	V min	
	AV_{DD} − 2.5	V max	
Input Current	±2.75	mA max	Typically 1.5 mA
V_{REFN}			
Reference Input Range[3]	−10	V min	
	V_{REFP} − 2.5	V max	
Input Current[2]	0	mA max	Typically −2 mA
	−2.75	mA min	
Large Signal Bandwidth[2]	160	kHz typ	−3 dB, V_{REFP} = 0 V to 10 V p-p
OUTPUT CHARACTERISTICS[2]			
Output Current	±5	mA max	R_L = 2 kΩ, C_L = 100 pF
DIGITAL INPUTS			V_L = 2.7 V to 5.5 V, JEDEC compliant
V_{IH}, Input High Voltage	2.4	V min	T_A = 25°C
V_{IL}, Input Low Voltage	0.8	V max	T_A = 25°C
Input Current[2]	1	µA max	
Input Capacitance[2]	8	pF typ	
DIGITAL OUTPUTS (SDO)			
V_{OH}, Output High Voltage	4	V min	I_{OH} = 0.4 mA
V_{OL}, Output Low Voltage	0.4	V max	I_{OL} = −1.6 mA
POWER SUPPLY CHARACTERISTICS			
Power Supply Sensitivity[2]	30	ppm FSR/V max	14.25 V ≤ AV_{DD} ≤ 15.75 V
AI_{DD}	3	mA/channel max	Outputs unloaded, V_{REFP} = 2.5 V, typically 2.125 mA
AI_{SS}	2.5	mA/channel max	Outputs unloaded, typically 1.625 mA
Power Dissipation	270	mW max	

[1] All supplies can be varied ±5%, and operation is guaranteed. Device is tested with nominal supplies.
[2] Guaranteed by design and characterization, not production tested.
[3] Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.

AV_{DD} = +5 V, AV_{SS} = −5 V/0 V, DGND = 0 V; V_{REFP} = +2.5 V; V_{REFN} = −2.5 V/0 V, V_L = 5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Value	Unit	Test Conditions/Comments
ACCURACY			Outputs unloaded
Resolution	12	Bits	
Relative Accuracy (INL)	±0.5	LSB max	B grade
	±1	LSB max	A grade
	±1	LSB max	B grade, AV_{SS} = 0 V[1]
	±2	LSB max	A grade, AV_{SS} = 0 V[1]
Differential Nonlinearity (DNL)	±1	LSB max	Guaranteed monotonic
Zero-Scale Error	±5	LSB max	AV_{SS} = −5 V
	±10	LSB max	AV_{SS} = 0 V
Zero-Scale TC[2]	100	ppm FSR/°C typ	
Full-Scale Error	±5	LSB max	AV_{SS} = −5 V
	±10	LSB max	AV_{SS} = 0 V
Full-Scale TC[2]	100	ppm FSR/°C typ	
REFERENCE INPUT			
V_{REFP}			
Reference Input Range[3]	V_{REFN} + 2.5	V min	
	AV_{DD} − 2.5	V max	
Input Current[2]	±0.5	mA max	Code 0x0000
V_{REFN}			
Reference Input Range[3]	−2.5	V min	AV_{SS} = −5 V
	0	V min	AV_{SS} = 0 V
	V_{REFP} − 2.5	V max	
Large Signal Bandwidth[2]	450	kHz typ	−3 dB, V_{REFP} = 0 V to 2.5 V p-p
OUTPUT CHARACTERISTICS[2]			
Output Current	±1.25	mA max	R_L = 2 kΩ, C_L = 100 pF
DIGITAL INPUTS			V_L = 2.7 V to 5.5 V, JEDEC compliant
V_{IH}, Input High Voltage	2.4	V min	T_A = 25°C
V_{IL}, Input Low Voltage	0.8	V max	T_A = 25°C
Input Current[2]	1	µA max	
Input Capacitance[2]	8	pF typ	
DIGITAL OUTPUTS (SDO)			
V_{OH}, Output High Voltage	4	V min	I_{OH} = 0.4 mA
V_{OL}, Output Low Voltage	0.4	V max	I_{OL} = −1.6 mA
POWER SUPPLY CHARACTERISTICS			
Power Supply Sensitivity[2]	100	ppm FSR/V typ	
AI_{DD}	2	mA/channel max	Outputs unloaded.
AI_{SS}	1.5	mA/channel max	Outputs unloaded, A_{VSS} = −5 V
Power Dissipation	70	mW max	AV_{SS} = −5 V
	40	mW max	AV_{SS} = 0 V

[1] For single supply operation only (V_{REFN} = 0 V, AV_{SS} = 0 V): Due to internal offset errors, INL and DNL are measured beginning at code 0x005.
[2] Guaranteed by design and characterization, not production tested.
[3] Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.

AC PERFORMANCE CHARACTERISTICS[1]

AV_{DD} = +15 V/+5 V, AV_{SS} = −15 V/−5 V/0 V, DGND = 0 V; V_{REFP} = +10 V/+2.5 V; V_{REFN} = −10 V/−2.5 V/0 V, V_L = 5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	A Grade	B Grade	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Output Voltage Settling Time	10	10	µs typ	To 0.01%, 10 V step, R_L = 1 kΩ
	7	7	µs typ	To 0.01%, 2.5 V step, R_L = 1 kΩ
Slew Rate	2.2	2.2	V/µs typ	10% to 90%
Analog Crosstalk	72	72	dB typ	
Digital Feedthrough	5	5	nV-s typ	

[1] Guaranteed by design and characterization, not production tested.

TIMING CHARACTERISTICS[1, 2]

AV_{DD} = +5 V/+15 V, AV_{SS} = −5 V/0 V/−15 V, DGND = 0 V; V_{REFP} = +2.5 V/+10 V; V_{REFN} = −2.5 V/0 V/−10 V, V_L = 5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_{WCS}	10	ns min	Chip Select Write Pulse Width
t_{WS}	0	ns min	Write Setup, t_{WCS} = 10 ns
t_{WH}	0	ns min	Write Hold, t_{WCS} = 10 ns
t_{AS}	0	ns min	Address Setup
t_{AH}	0	ns min	Address Hold
t_{LS}	5	ns min	Load Setup
t_{LH}	5	ns min	Load Hold
t_{WDS}	5	ns min	Write Data Setup, t_{WCS} = 10 ns
t_{WDH}	0	ns min	Write Data Hold, t_{WCS} = 10 ns
t_{LDW}	10	ns min	Load Data Pulse Width
t_{RESET}	10	ns min	Reset Pulse Width
t_{RCS}	30	ns min	Chip Select Read Pulse Width
t_{RDH}	0	ns min	Read Data Hold, t_{RCS} = 30 ns
t_{RDS}	0	ns min	Read Data Setup, t_{RCS} = 30 ns
t_{DZ}	15	ns max	Data to High-Z, C_L = 10 pF
t_{CSD}	35	ns max	Chip Select to Data, C_L = 100 pF

[1] All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[2] Guaranteed by design and characterization, not production tested.

Timing Diagrams

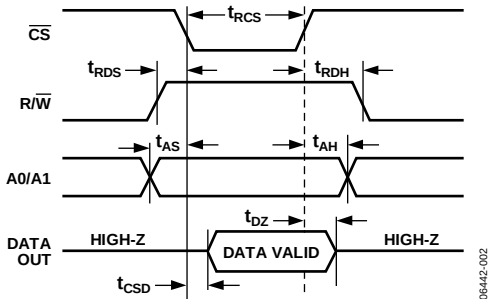

Figure 2. Data Read Timing

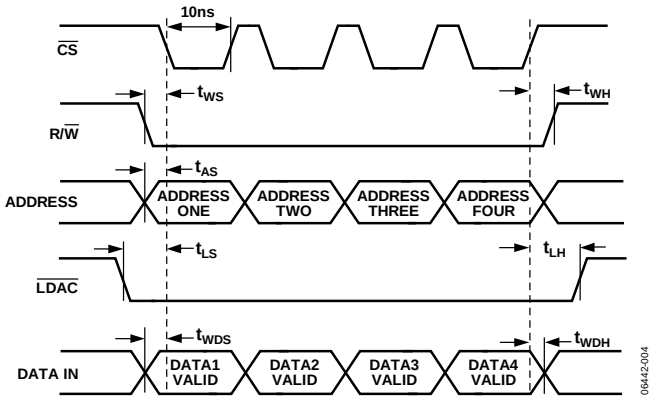

Figure 4. Single Buffer Mode Timing

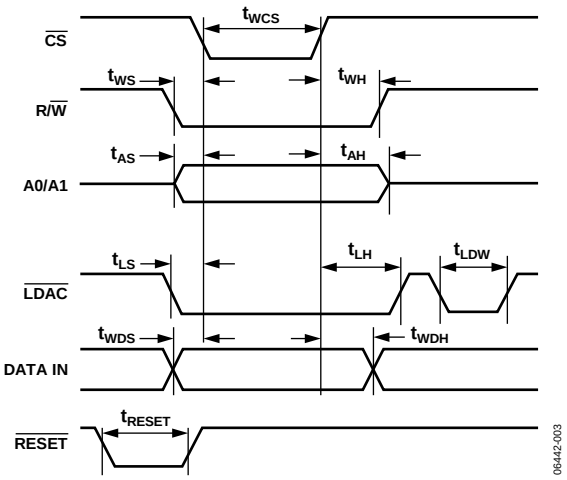

Figure 3. Data Write Timing

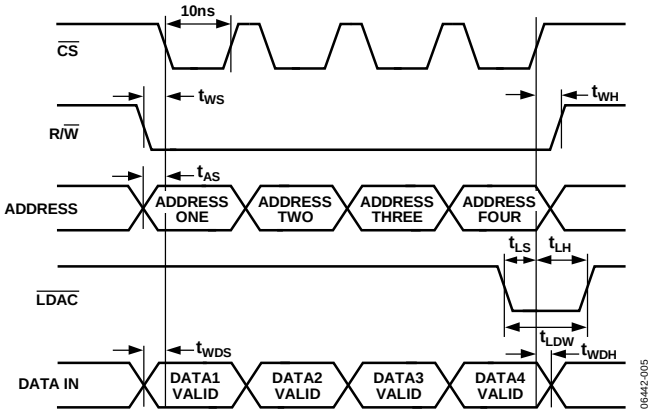

Figure 5. Double Buffer Mode Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
AV_{SS} to DGND	+0.3 V to −16.5 V
AV_{DD} to DGND	−0.3 V to +16.5 V
AV_{SS} to AV_{DD}	+0.3 V to −33 V
V_L to DGND	−0.3 V to +7 V
Current into Any Pin	±15 mA
Digital Pin Voltage to DGND	−0.3 V to +7 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
28-Lead SSOP Package	
θ_{JA} Thermal Impedance	100°C/W
θ_{JC} Thermal Impedance	39°C/W
Power Dissipation Package (Derate 10 mW/°C Above 60°C)	900 mW
Reflow Soldering	
Time at Peak Temperature	10 sec to 40 sec
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

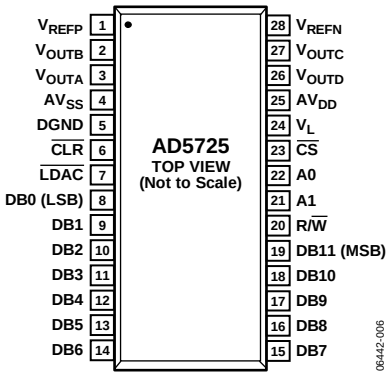

Figure 6. Pin Configuration Diagram

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{REFP}	Positive DAC Reference Input. The voltage applied to this pin defines the full-scale output voltage. Allowable range is AV_{DD} − 2.5 V to V_{REFN} + 2.5 V.
2	V_{OUTB}	Buffered Analog Output Voltage of DAC B.
3	V_{OUTA}	Buffered Analog Output Voltage of DAC A.
4	AV_{SS}	Negative Analog Supply Pin. Voltage ranges from 0 V to −15 V.
5	DGND	Digital Ground Pin.
6	$\overline{CLR}$	Active Low Input. Sets input registers and DAC registers to zero scale (0x000) for the AD5725-1 or midscale (0x800) for the AD5725.
7	$\overline{LDAC}$	Active Low Load DAC Input.
8	DB0	Data Bit 0 (LSB).
9	DB1	Data Bit 1.
10	DB2	Data Bit 2.
11	DB3	Data Bit 3.
12	DB4	Data Bit 4.
13	DB5	Data Bit 5.
14	DB6	Data Bit 6.
15	DB7	Data Bit 7.
16	DB8	Data Bit 8.
17	DB9	Data Bit 9.
18	DB10	Data Bit 10.
19	DB11	Data Bit 11 (MSB).
20	R/$\overline{W}$	Read/Write Pin. Active low to write data to DAC; Active high to read back previous data at data bit pins with V_L connected to +5 V.
21	A1	Address Bit 1.
22	A0	Address Bit 0.
23	$\overline{CS}$	Active Low Chip Select Pin.
24	V_L	Voltage Supply for Readback Function. Can be left open circuit if not used.
25	AV_{DD}	Positive Analog Supply Pin. Voltage ranges from +5 V to +15 V.
26	V_{OUTD}	Buffered Analog Output Voltage of DAC D.
27	V_{OUTC}	Buffered Analog Output Voltage of DAC C.
28	V_{REFN}	Negative DAC Reference Input. The voltage applied to this pin defines the zero-scale output voltage. Allowable range is AV_{SS} to V_{REFP} − 2.5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

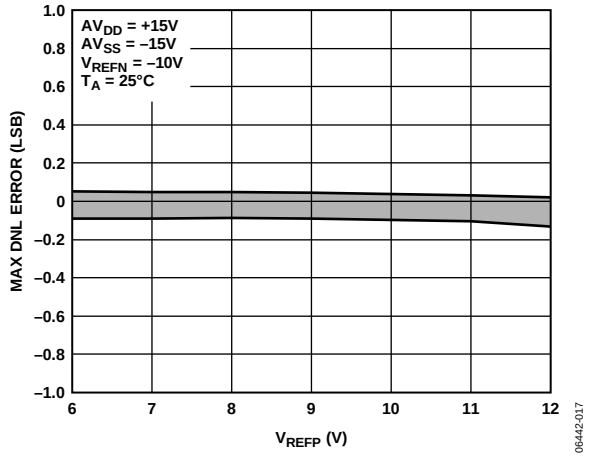

Figure 7. DNL vs. V_{REFP} (V_{SUPPLY} = ±15 V)

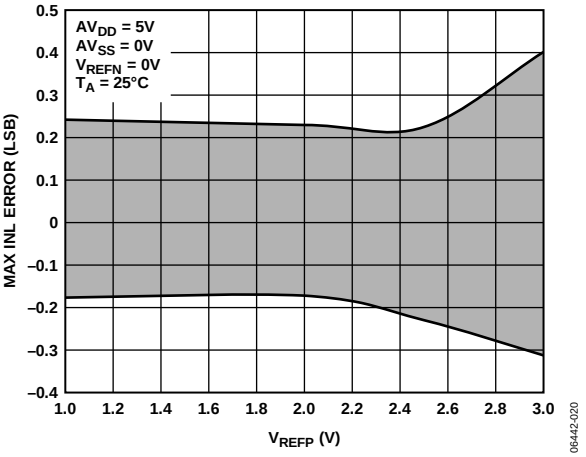

Figure 10. INL vs. V_{REFP} (V_{SUPPLY} = +5 V)

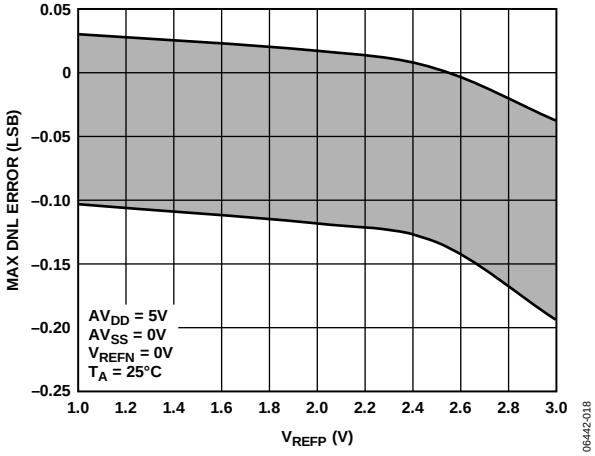

Figure 8. DNL vs. V_{REFP} (V_{SUPPLY} = +5 V)

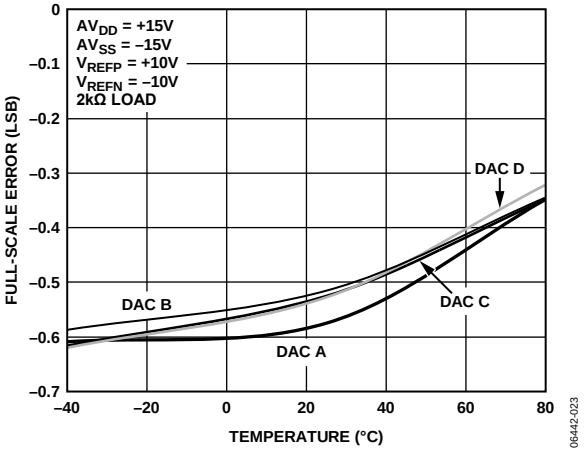

Figure 11. Full-Scale Error vs. Temperature

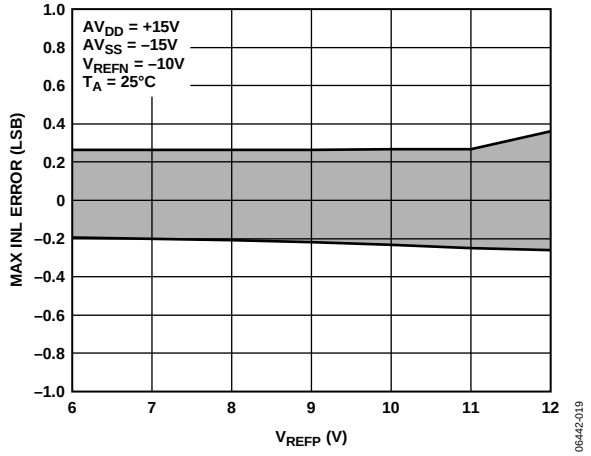

Figure 9. INL vs. V_{REFP} (V_{SUPPLY} = ±15 V)

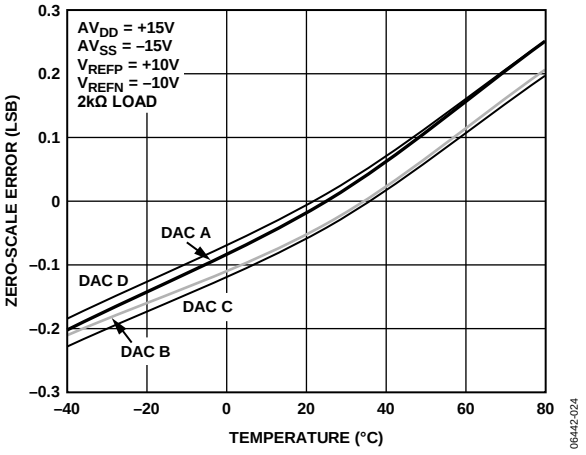

Figure 12. Zero-Scale Error vs. Temperature

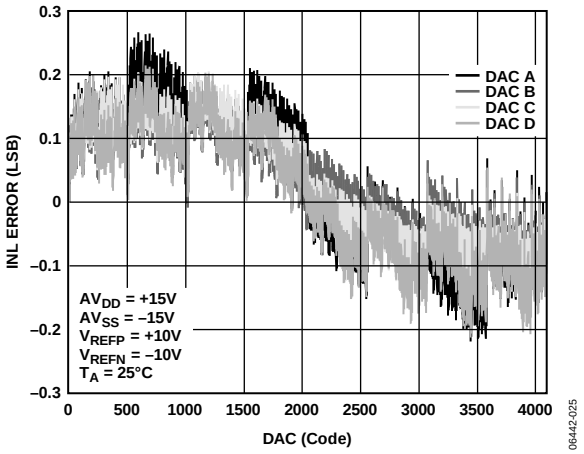

Figure 13. Channel-to-Channel Matching (V_{SUPPLY} = ±15 V)

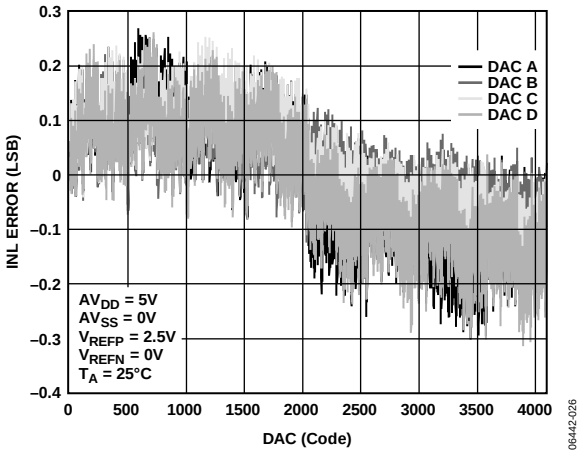

Figure 14. Channel-to-Channel Matching (V_{SUPPLY} = +5 V)

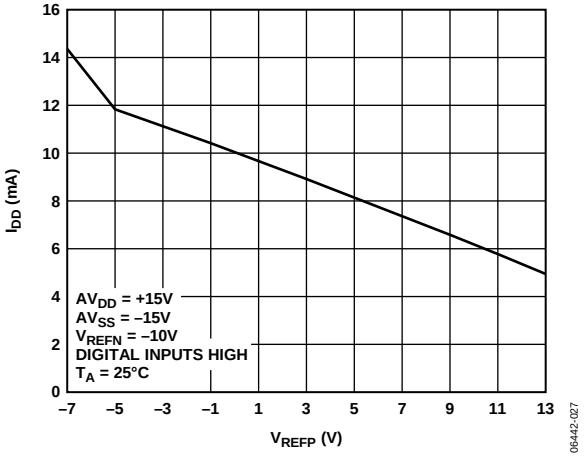

Figure 15. I_{DD} vs. V_{REFP}

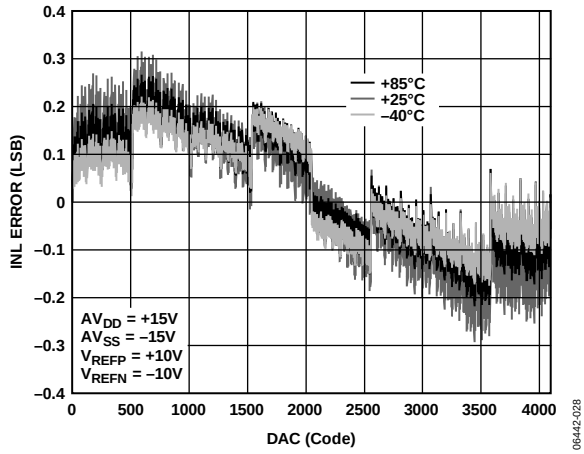

Figure 16. INL vs. DAC Code

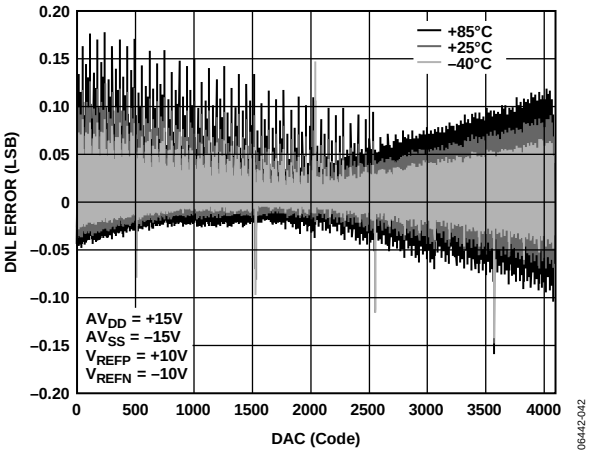

Figure 17. DNL vs. DAC Code

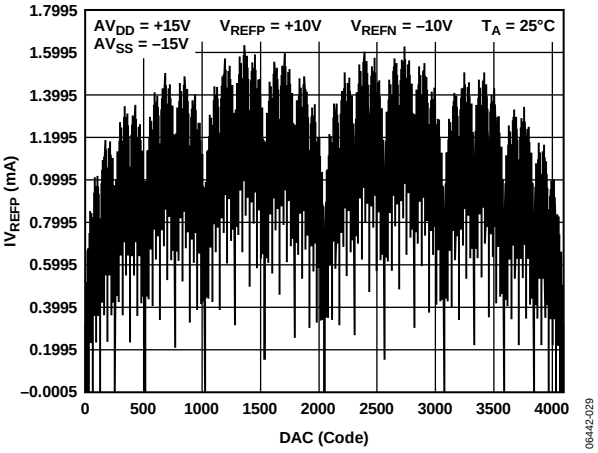

Figure 18. IV_{REFP} vs. DAC Code

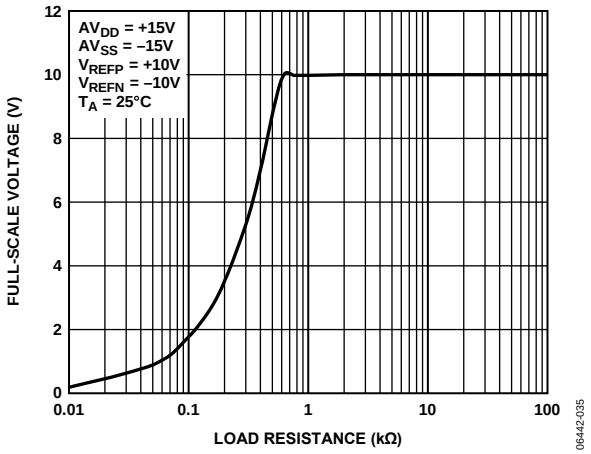

Figure 19. Output Voltage Swing vs. Resistive Load

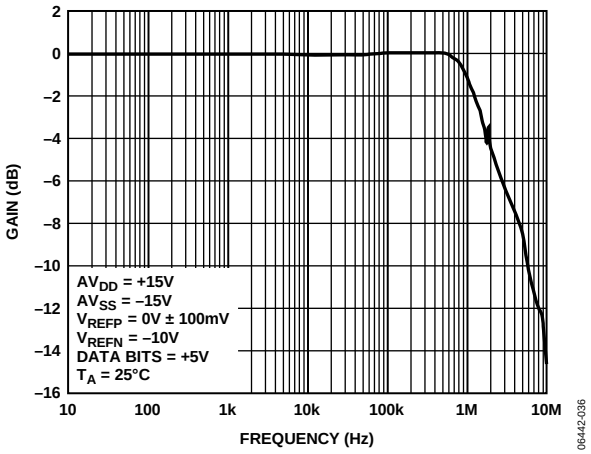

Figure 20. Small Signal Response

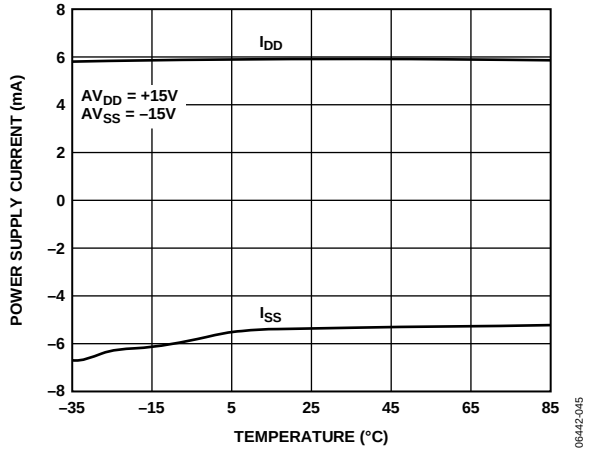

Figure 21. Power Supply Current vs. Temperature

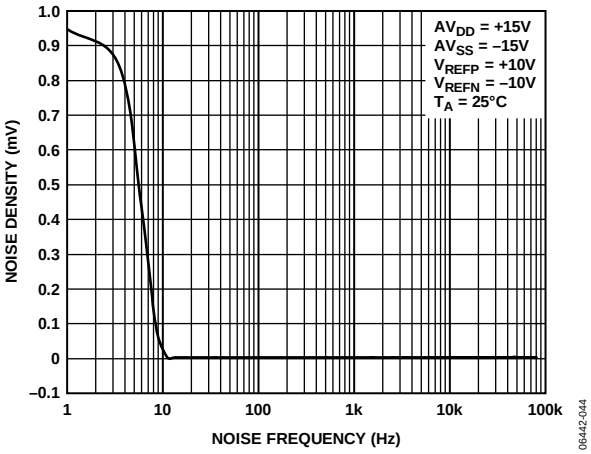

Figure 22. Output Noise Spectral Density vs. Frequency

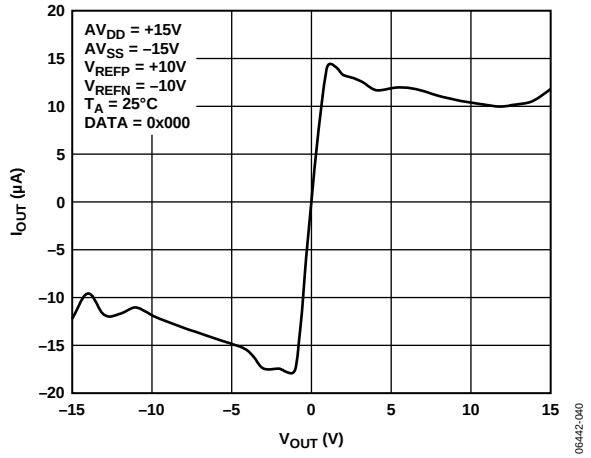

Figure 23. I_{OUT} vs. V_{OUT} (V_{SUPPLY} = ±15 V)

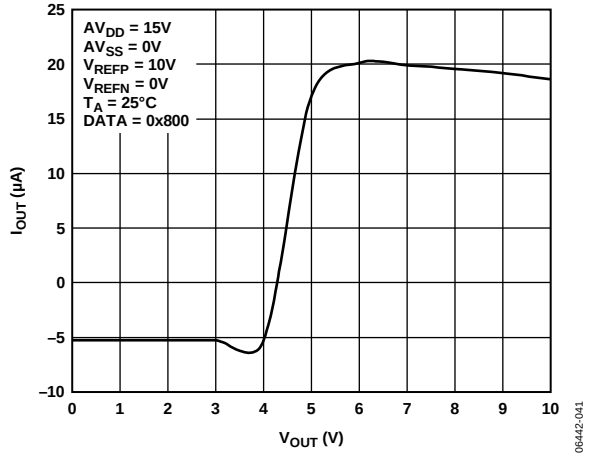

Figure 24. I_{OUT} vs. V_{OUT} (V_{SUPPLY} = +15 V)

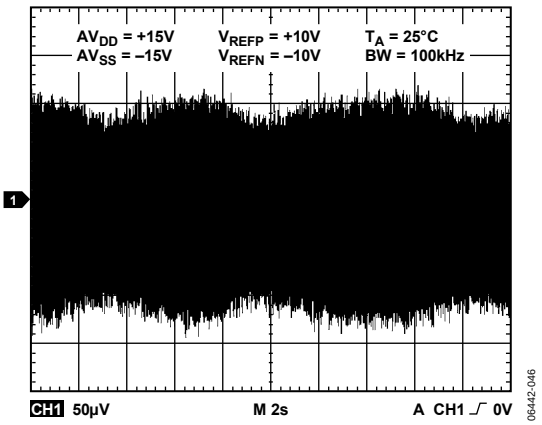

Figure 25. Broadband Noise

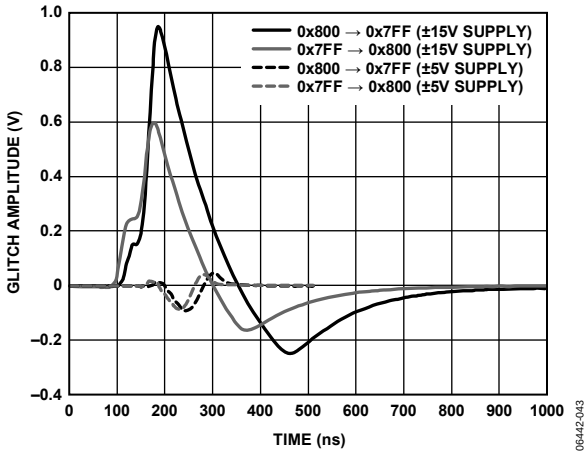

Figure 26. Output Glitch

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or integral nonlinearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 16.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 17.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5725 is monotonic over its full operating temperature range.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code is loaded to the DAC register. Ideally, the output should be V_{REFP} − 1 LSB. Full-scale error is expressed in LSBs. A plot of full-scale error vs. temperature can be seen in Figure 11.

Full-Scale Error TC
Full-scale error TC is a measure of the change in full-scale error with a change in temperature. Full-scale error TC is expressed in ppm FSR/°C.

Zero-Scale Error
Zero-scale error is the error in the DAC output voltage when 0x0000 (straight binary coding) is loaded to the DAC register. Ideally, the output voltage should be V_{REFN}. A plot of zero-scale error vs. temperature can be seen in Figure 12.

Zero-Scale Error TC
Zero-scale error TC is a measure of the change in zero-scale error with a change in temperature. Zero-scale error TC is expressed in ppm FSR/°C.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

Slew Rate
The slew rate of a device is a limitation in the rate of change of the output voltage. The output slewing speed of a voltage-output DAC is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is given in V/μs.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but it is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus.

Power Supply Sensitivity
Power supply sensitivity indicates how the output of the DAC is affected by changes in the power supply voltage.

Analog Crosstalk
Analog crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC. It is expressed in dB.

THEORY OF OPERATION

The AD5725 is a quad voltage output, 12-bit parallel input DAC featuring a 12-bit data bus with readback capability. The AD5725 operates from single or dual supplies ranging from +5 V up to ±15 V. The output voltage range is set by the reference voltages applied at the V_{REFP} and V_{REFN} pins.

DAC ARCHITECTURE

Each of the four DACs is a voltage switched, high impedance (50 kΩ), R-2R ladder configuration. Each 2R resistor is driven by a pair of switches that connect the resistor to either V_{REFH} or V_{REFL}.

OUTPUT AMPLIFIERS

The output amplifiers are capable of generating both unipolar and bipolar output voltages. They are capable of driving a load of 2 kΩ in parallel with 500 pF to DGND. The source and sink capabilities of the output amplifiers can be seen in Figure 23 and Figure 24. The slew rate is 2.2 V/µs with a full-scale settling time of 10 µs. The amplifiers are short-circuit protected.

Careful attention to grounding is important for accurate operation of the AD5725. With four outputs and two references there is potential for ground loops. Since the AD5725 has no analog ground, the ground must be specified with respect to the reference.

REFERENCE INPUTS

All four DACs share common positive reference (V_{REFP}) and negative reference (V_{REFN}) inputs. The voltages applied to these reference inputs set the output high and low voltage limits on all four of the DACs. Each reference input has voltage restrictions with respect to the other reference and to the power supplies. V_{REFN} can be any voltage between AV_{SS} and V_{REFP} − 2.5 V and V_{REFP} can be any value between AV_{DD} − 2.5 V and V_{REFN} + 2.5 V. Note that because of these restrictions, the AD5725 references cannot be inverted (V_{REFN} cannot be greater than V_{REFP}).

It is important to note that the AD5725 V_{REFP} input both sinks and sources current. Also, the input current of both V_{REFP} and V_{REFN} are code dependent. Many references have limited current sinking capability and must be buffered with an amplifier to drive V_{REFP}. The V_{REFN} reference input has no such special requirements.

It is recommended that the reference inputs be bypassed with 0.2 µF capacitors when operating with ±10 V references. This limits the reference bandwidth.

PARALLEL INTERFACE

See Table 7 for the digital control logic truth table. The parallel interface consists of a 12-bit bidirectional data bus, two register select inputs, A0 and A1, a R/$\overline{W}$ input, a chip select ($\overline{CS}$), and a load DAC ($\overline{LDAC}$) input. Control of the DACs and bus direction is determined by these inputs as shown in Table 7. Digital data bits are labeled with the MSB defined as Data Bit 11 and the LSB as Data Bit 0. All digital pins are TTL/CMOS compatible.

The register select inputs A0 and A1 select individual DAC Register A (Binary Code 00) through Register D (Binary Code 11). Decoding of the registers is enabled by the $\overline{CS}$ input. When $\overline{CS}$ is high, no decoding takes place, and neither the writing nor the reading of the input registers is enabled. The loading of the second bank of registers is controlled by the asynchronous $\overline{LDAC}$ input. By taking $\overline{LDAC}$ low while $\overline{CS}$ is high, all output registers can be updated simultaneously. Note that the t_{LDW} required pulse width for updating all DACs is a minimum of 10 ns. The R/$\overline{W}$ input, when enabled by $\overline{CS}$, controls the writing to and reading from the input register.

DATA CODING

The AD5725 uses binary coding. The output voltage can be calculated as follows:

$$V_{OUT} = V_{REFN} + \frac{(V_{REFP} - V_{REFN}) \times D}{4096}$$

where *D* is the digital code in decimal.

$\overline{CLR}$

The $\overline{CLR}$ function can be used either at power-up or at any time during the DACs operation. The $\overline{CLR}$ function is independent of $\overline{CS}$. This pin is active low and sets the DAC registers to either midscale code (0x800) for the AD5725 or zero code (0x000) for the AD5725-1. The $\overline{CLR}$ to midscale code is most useful when the DAC is configured for bipolar references and an output of 0 V is desired.

Table 7. AD5725 Logic Truth Table

A1	A0	R/$\overline{W}$	$\overline{CS}$	$\overline{CLR}$	$\overline{LDAC}$	INPUT REG	DAC REG	MODE	DAC
Low	Low	Low	Low	High	Low	Write	Write	Transparent	A
Low	High	Low	Low	High	Low	Write	Write	Transparent	B
High	Low	Low	Low	High	Low	Write	Write	Transparent	C
High	High	Low	Low	High	Low	Write	Write	Transparent	D
Low	Low	Low	Low	High	High	Write	Hold	Write Input	A
Low	High	Low	Low	High	High	Write	Hold	Write Input	B
High	Low	Low	Low	High	High	Write	Hold	Write Input	C
High	High	Low	Low	High	High	Write	Hold	Write Input	D
Low	Low	High	Low	High	High	Read	Hold	Read Input	A
Low	High	High	Low	High	High	Read	Hold	Read Input	B
High	Low	High	Low	High	High	Read	Hold	Read Input	C
High	High	High	Low	High	High	Read	Hold	Read Input	D
X	X	X	High	High	Low	Hold	Update all DAC registers		All
X	X	X	High	High	High	Hold	Hold	Hold	All
X	X	X	X	Low	X	All Registers set to mid/zero scale			All
X	X	X	High	↑	X	All Registers latched to mid/zero scale			All

POWER SUPPLIES

Power supplies required are AV_{SS}, AV_{DD}, and V_L. The AV_{SS} supply can be set between −15 V and 0 V. AV_{DD} is the positive supply; its operating range is between +5 V and +15 V.

V_L is the digital output supply voltage for the readback function. It is normally connected to +5 V. This pin is a logic reference input only. It does not supply current to the device. If the readback function is not used, V_L can be left open-circuit. While V_L does not supply current to the AD5725, it does supply current to the digital outputs when the readback function is used.

REFERENCE CONFIGURATION

Output voltage ranges can be configured as either unipolar or bipolar, and within these choices, a wide variety of options exists. The unipolar configuration can be either a positive or a negative voltage output, and the bipolar configuration can be either symmetrical or nonsymmetrical.

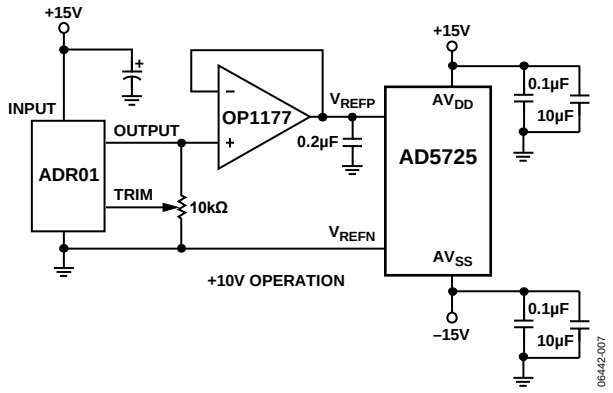

Figure 27. Unipolar +10 V Operation

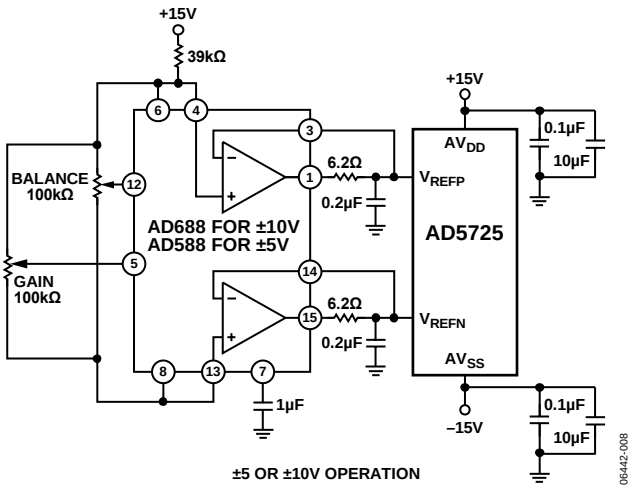

Figure 28. Symmetrical Bipolar Operation

Figure 28 (Symmetrical Bipolar Operation) shows the AD5725 configured for ±10 V operation. See the AD688 data sheet for a full explanation of reference operation. Adjustments may not be required for many applications since the AD688 is a very high accuracy reference. However, if additional adjustments are required, adjust the AD5725 full scale first. Begin by loading the digital full-scale code (0xFFF). Then, adjust the gain adjust potentiometer to attain a DAC output voltage of 9.9976 V. Then, adjust the balance adjust to set the mid-scale output voltage to 0.000 V.

The 0.2 µF bypass capacitors shown at the reference inputs in Figure 28 should be used whenever ±10 V references are used. Applications with single references or references to ±5 V may not require the 0.2 µF bypassing. The 6.2 Ω resistor in series with the output of the reference amplifier is to keep the amplifier from oscillating with the capacitive load. We have found that this is large enough to stabilize this circuit. Larger resistor values are acceptable, provided that the drop across the resistor does not exceed a V_{BE}. Assuming a minimum V_{BE} of 0.6 V and a maximum current of 2.75 mA, the resistor should be under 200 Ω for the loading of a single AD5725.

Using two separate references is not recommended. Having two references can cause different drifts with time and temperature, whereas with a single reference, most drifts will track.

Unipolar positive full-scale operation can usually be set with a reference with the correct output voltage. This is preferable to using a reference and dividing down to the required value. For a 10 V full-scale output, the circuit can be configured as shown in Figure 29. In this configuration, the full-scale value is set first by adjusting the 10 kΩ resistor for a full-scale output of 9.9976 V.

Figure 29 shows the AD5725 configured for −10 V to 0 V operation. An ADR01 and OP1177 are configured to produce a −10 V output, which is connected directly to V_{REFP} for the reference voltage.

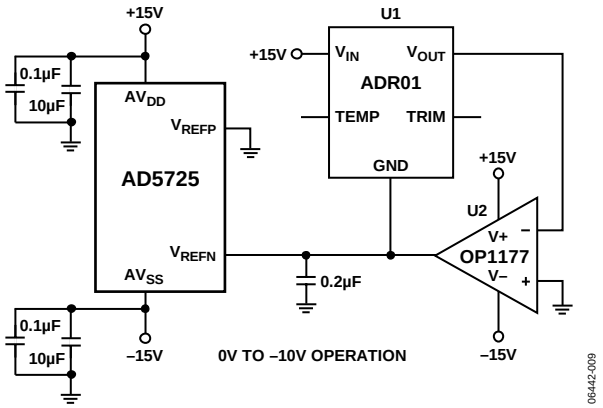

Figure 29. Unipolar −10 V Operation

SINGLE +5 V SUPPLY OPERATION

For operation with a +5 V supply, the reference voltage should be set between +1.0 V and +2.5 V for optimum linearity. Figure 30 shows an ADR03 used to supply a +2.5 V reference voltage. The headroom of the reference and DAC are both sufficient to support a +5 V supply with ±5 V tolerance. AV_{DD} and V_L should be connected to the same supply. Separate bypassing to each pin should be used.

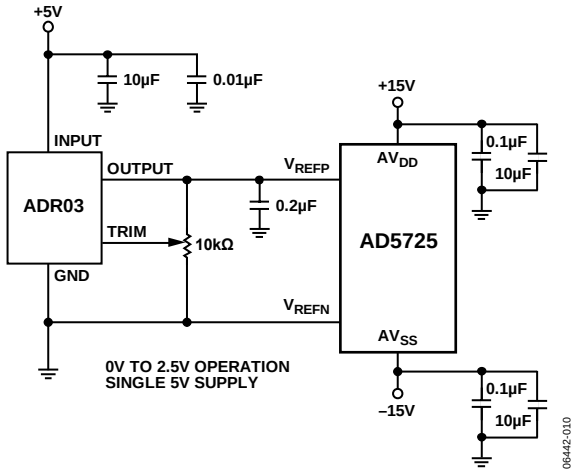

Figure 30. +5 V Single-Supply Operation

OUTLINE DIMENSIONS

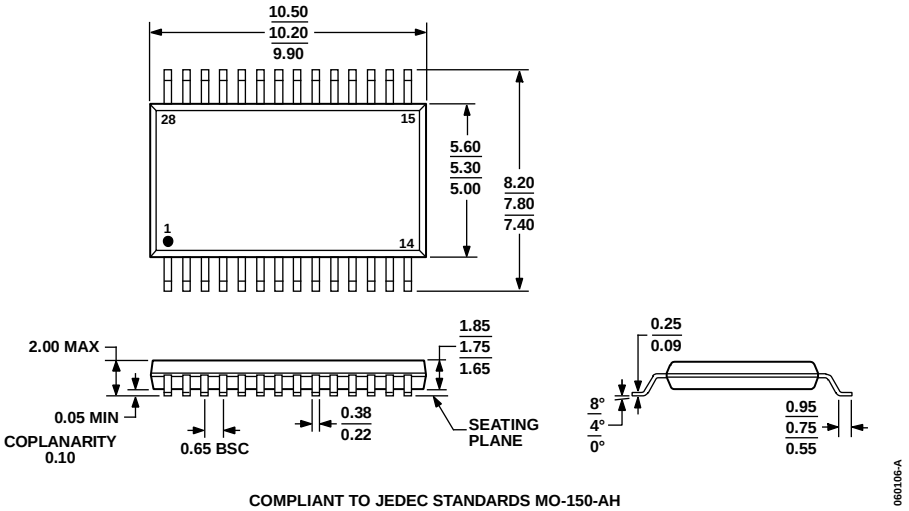

Figure 31. 28-Lead Shrink Small Outline Package [SSOP]
(RS-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	INL (LSB)	Clear Action	Package Description	Package Option
AD5725ARSZ-1500RL7	−40°C to +85°C	1	Clear to zero scale	28-Lead Shrink Small Outline Package [SSOP]	RS-28
AD5725ARSZ-1REEL	−40°C to +85°C	1	Clear to zero scale	28-Lead Shrink Small Outline Package [SSOP]	RS-28
AD5725ARSZ-500RL7	−40°C to +85°C	1	Clear to midscale	28-Lead Shrink Small Outline Package [SSOP]	RS-28
AD5725ARSZ-REEL	−40°C to +85°C	1	Clear to midscale	28-Lead Shrink Small Outline Package [SSOP]	RS-28
AD5725BRSZ-1500RL7	−40°C to +85°C	0.5	Clear to zero scale	28-Lead Shrink Small Outline Package [SSOP]	RS-28
AD5725BRSZ-1REEL	−40°C to +85°C	0.5	Clear to zero scale	28-Lead Shrink Small Outline Package [SSOP]	RS-28
AD5725BRSZ-500RL7	−40°C to +85°C	0.5	Clear to midscale	28-Lead Shrink Small Outline Package [SSOP]	RS-28
AD5725BRSZ-REEL	−40°C to +85°C	0.5	Clear to midscale	28-Lead Shrink Small Outline Package [SSOP]	RS-28

[1] Z = RoHS Compliant Part.

NOTES

D06442-0-8/13(C)

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