OPA177 0.1-µV/°C Offset Drift, 10-µV Offset, Low-Noise, Bipolar Operational Amplifier

1 Features

- Low offset voltage: 25 µV (max)
- Low offset voltage drift: 0.3 µV/°C (max)
- High open-loop gain: 134 dB (min)
- Low quiescent current: 1.3 mA (typ)
- Low input bias ±2 nA (max)
- Wide supply voltage range: 6 V to 36 V
- Replaces industry-standard op amps: OP-07, OP-77, OP-177, AD707, and more
- For improved performance with ±40-V overvoltage protection, see the OPA206

2 Applications

- Analog input module
- Data acquisition (DAQ)
- Battery test
- Lab and field instrumentation
- Temperature transmitter

3 Description

The OPA177 precision bipolar op amp feature very low offset voltage and drift. Laser-trimmed offset, drift and input bias current virtually eliminate the need for costly external trimming. High performance and low cost make these devices an excellent choice for a wide range of precision instrumentation.

The low quiescent current of the OPA177 dramatically reduces warm-up drift and errors due to thermoelectric effects in input interconnections. The OPA177 provides an effective alternative to chopper-stabilized amplifiers. The low noise of the OPA177 helps maintain maximum signal integrity.

OPA177 performance grade-outs are available. Packaging options include 8-pin plastic DIP and SO-8 surface-mount packages.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
OPA177	D (SOIC, 8)	4.9 mm × 6 mm
	P (PDIP, 8)	9.81 mm × 9.43 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

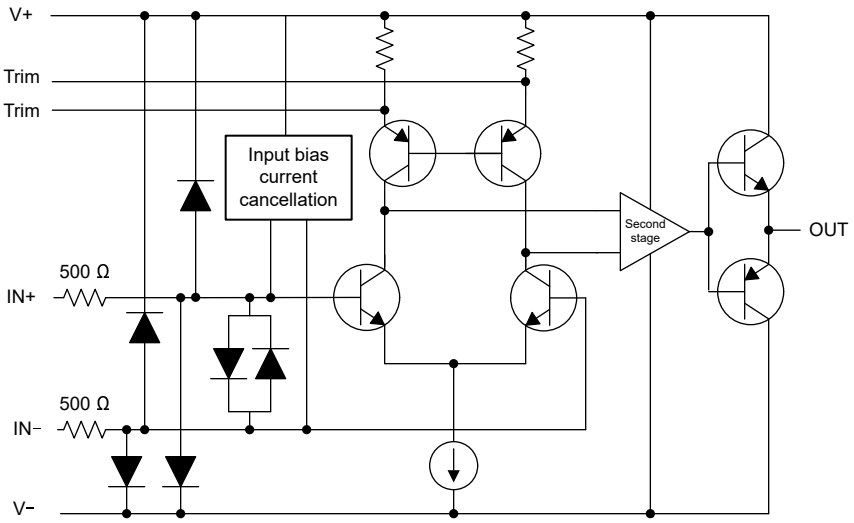


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2000) to Revision A (September 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed data sheet title for clarity	1
• Added *Package Information* table, and *Typical Application*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1
• Added additional Features bullets and updated several specifications to align with *Electrical Characteristics*	1
• Changed application bullets to show linked applications	1
• Changed *Description* text for clarity	1
• Updated front-page diagram	1
• Added pin functions table	3
• Changed supply voltage from ±22 V (44 V) to 40 V in *Absolute Maximum Ratings*	4
• Moved operating temperature from *Absolute Maximum Ratings* to *Recommended Operating Conditions*	4
• Deleted lead temperature from *Absolute Maximum Ratings*	4
• Moved junction to ambient thermal information from *Absolute Maximum Ratings* to *Thermal Information*	4
• Added *ESD Ratings* and *Thermal Information*	4
• Changed several parameter names for consistency with modern data sheets in *Electrical Characteristics*	5
• Updated the format of *Electircal Characteristics*	5
• Added test conditions to the header of *Electrical Characteristics*	5
• Moved test conditions from condition column to the header of *Electrical Characteristics*	5
• Changed open-loop voltage gain unit from V/mV to dB in *Electrical Characteristics*	5
• Changed large signal voltage gain to open-loop voltage gain in *Electrical Characteristics*	5
• Changed Power Supply parameters no load test condition to I_O = 0 A in *Electrical Characteristics*	5
• Updated quiescent current maximum over temperature specification value from 25 mA (typo) to ±2.5 mA	5
• Changed supply current to quiescent current in *Electrical Characteristics*	5
• Added information about integrated overvoltage protection including OPAx206 to Input Protection	10
• Updated Noise Performance with new products such as the OPAx828, OPAx140, and OPAx210	10
• Changed operational amplifier recommendations to reflect new product developments	10

5 Pin Configuration and Functions

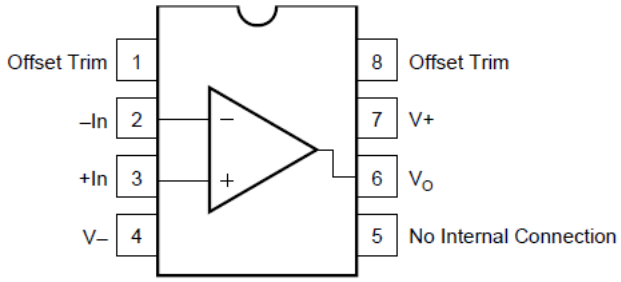


Figure 5-1. D Package, 8-Pin SOIC and P Package, 8-Pin PDIP (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
+In	3	Input	Noninverting input
−In	2	Input	Inverting input
No Internal Connection	5	—	No internal connection (can be left floating)
Offset Trim	1, 8	—	Input offset voltage trim (leave floating if not used)
V+	7	Power	Positive (highest) power supply
V−	4	Power	Negative (lowest) power supply
V_O	6	Output	Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)		40	V
	Input voltage	(V–)	(V+)	V
	Differential input voltage	–30	30	V
I_{SC}	Output short circuit(2)	Continuous		
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single supply	6	30	36	V
		Dual supply	±3	±15	±18	
T_A	Ambient temperature		–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA177		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160.0	100.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report

6.5 Electrical Characteristics

at T_A = 25°C, V_S = 30 V (±15 V), V_{CM} = V_{OUT} = V_S / 2, and R_L = 2 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
VOS	Input offset voltage	F grade			±10	±25	µV
		G grade			±20	±60	
		T_A = –40°C to +85°C	F grade		±15	±40	
			G grade		±20	±100	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C	F grade		±0.1	±0.3	µV/°C
			G grade		±0.7	±1.2	
	Offset adjustment range	R_P = 20 kΩ			±3		mV
	Long-term drift(1)	F grade			0.3		µV/mo
		G grade			0.4		
PSRR	Power-supply rejection ratio	V_S = ±3 V to ±18 V	F grade	115	125		dB
			G grade	110	120		
		V_S = ±3 V to ±18 V T_A = –40°C to +85°C	F grade	110	120		
			G grade	106	115		
INPUT BIAS CURRENT							
I_B	Input bias current	F grade			±0.5	±2	nA
		G grade			±0.5	±2.8	
		T_A = –40°C to +85°C	F grade		±0.5	±4	
			G grade		±0.5	±6	
	Input bias current drift(2)	T_A = –40°C to +85°C	F grade		±8	±40	pA/°C
			G grade		±15	±60	
I_{OS}	Input offset current	F grade			±0.3	±1.5	nA
		G grade			±0.3	±2.8	
		T_A = –40°C to +85°C	F grade		±0.5	±2.2	
			G grade		±0.5	±4.5	
NOISE							
	Input bias current drift(2)	F grade			±1.5	±40	pA/°C
		G grade			±1.5	±85	
	Input voltage noise	f =1 Hz to 100 Hz(3)			85	150	nV_{rms}
	Input current noise	f =1 Hz to 100 Hz			45		pA_{rms}
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range(4)			±13	±14		V
		T_A = –40°C to +85°C		±13	±13.5		
CMRR	Common-mode rejection ratio	V_{CM} = ±13 V	F grade	130	140		dB
			G grade	115	140		
		V_{CM} = ±13 V T_A = –40°C to +85°C	F grade	120	140		
			G grade	110	140		
INPUT IMPEDANCE							
R_{in}	Input resistance	Differential mode(5)	F grade	26	45		MΩ
			G grade	18.5	45		
		Common-mode			200		GΩ

6.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = 30 V (±15 V), V_{CM} = V_{OUT} = V_S / 2, and R_L = 2 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain(6)	–10 V ≤ V_O ≤ 10 V	F grade	134	141		dB
			G grade	126	135		
		–10 V ≤ V_O ≤ 10 V, T_A = –40°C to +85°C	F grade	126	135		
			G grade	120	132		
FREQUENCY RESPONSE							
BW_{CL}	Closed-loop bandwidth	G = 1		0.4	0.6		MHz
SR	Slew rate			0.1	0.3		V/µs
OUTPUT							
V_O	Voltage output swing	R_L ≥ 2 kΩ		±13.5	±14		V
			T_A = –40°C to +85°C	±12	±13		
		R_L ≥ 10 kΩ		±12.5	±13		
		R_L ≥ 1 kΩ		±12	±12.5		
I_{SC}	Short-circuit current				±35		mA
R_O	Open-loop output resistance				60		Ω
POWER SUPPLY							
	Power consumption	I_O = 0 A			40	60	mW
			T_A = –40°C to +85°C		60	75	
I_Q	Quiescent current	I_O = 0 A			1.3	2	mA
			T_A = –40°C to +85°C		2	2.5	

(1) Long-term input offset voltage stability refers to the averaged trend line of V_{OS} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than 2 µV.
(2) Specified by characterization.
(3) Sample tested.
(4) Specified CMRR test condition.
(5) Specified by design.
(6) To maintain high open-loop gain throughout the ±10-V output range, A_{OL} is tested at –10 V ≤ V_O ≤ 0 V, 0 V ≤ V_O ≤ +10 V, and –10 V ≤ V_O ≤ +10 V.

6.6 Typical Characteristics

at T_A = +25°C, V_S = ±15 V (unless otherwise noted)

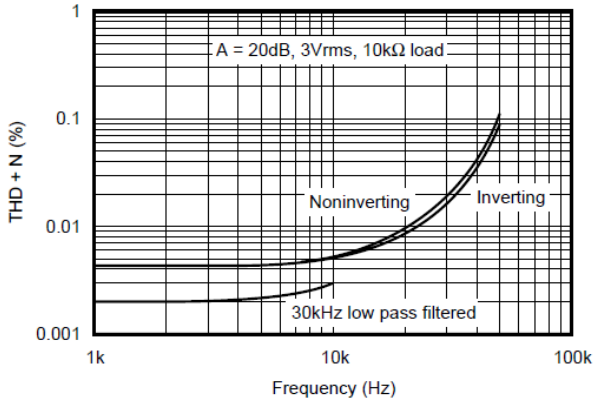


Figure 6-1. Total Harmonic Distortion and Noise vs Frequency

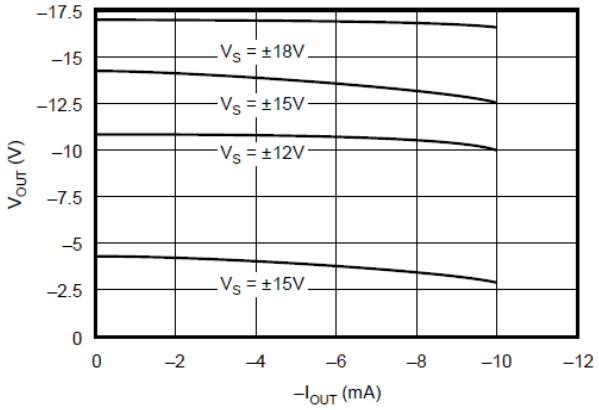


Figure 6-2. Maximum V_{OUT} vs I_{OUT} (Negative Swing)

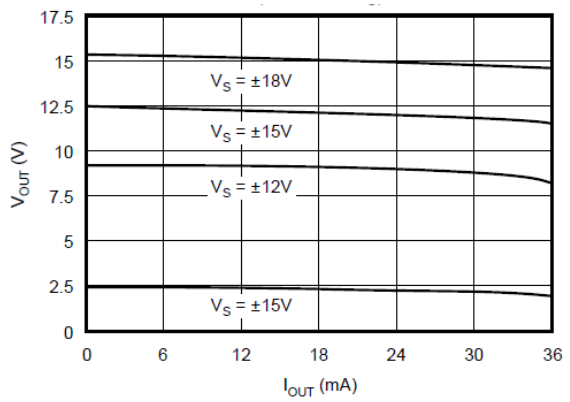


Figure 6-3. Maximum V_{OUT} vs I_{OUT} (Positive Swing)

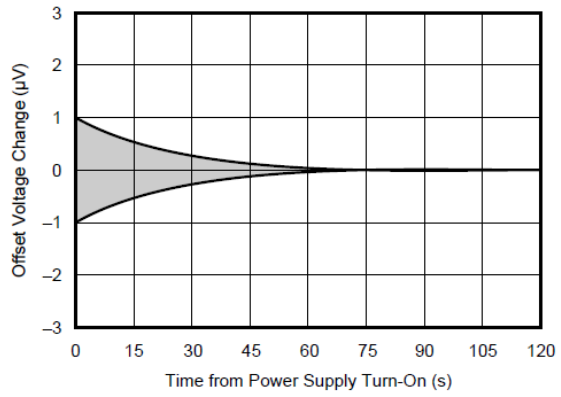


Figure 6-4. Warm-Up Offset Voltage Drift

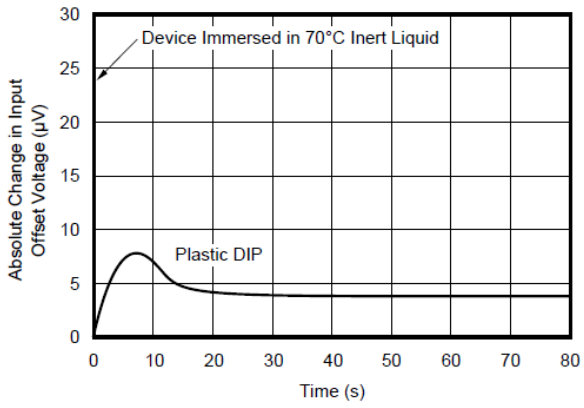


Figure 6-5. Offset Voltage Change Due To Thermal Shock

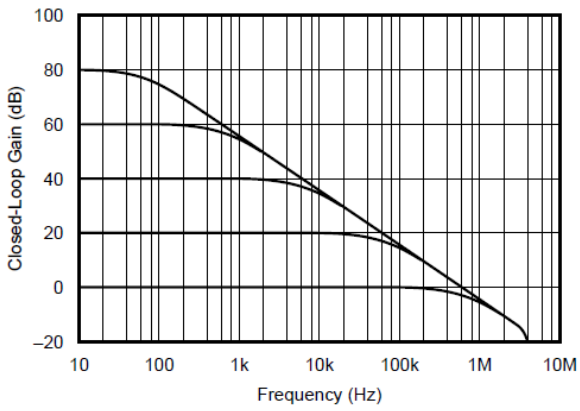


Figure 6-6. Closed-Loop Response vs Frequency

6.6 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15 V (unless otherwise noted)

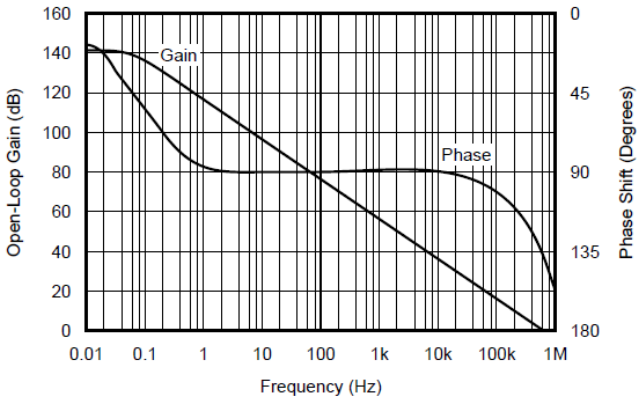


Figure 6-7. Open-Loop Gain/Phase vs Frequency

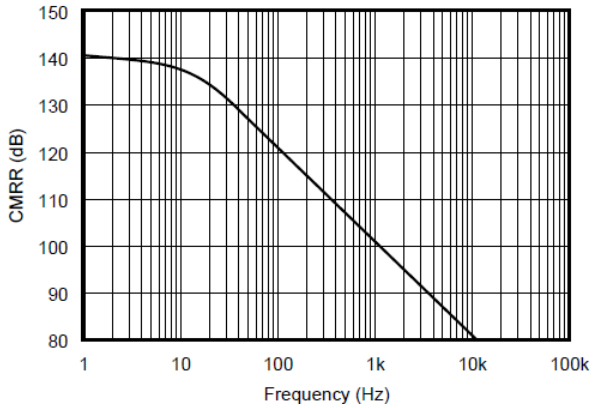


Figure 6-8. CMRR vs Frequency

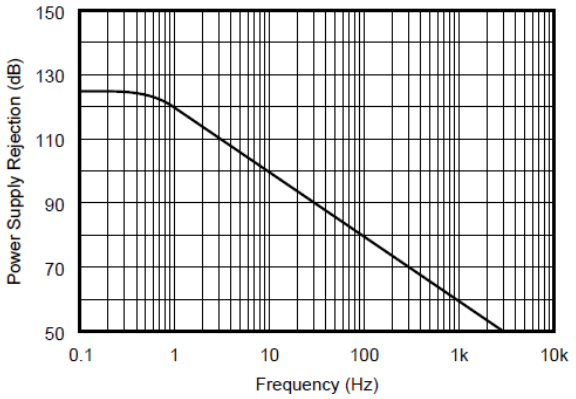


Figure 6-9. Power Supply Rejection vs Frequency

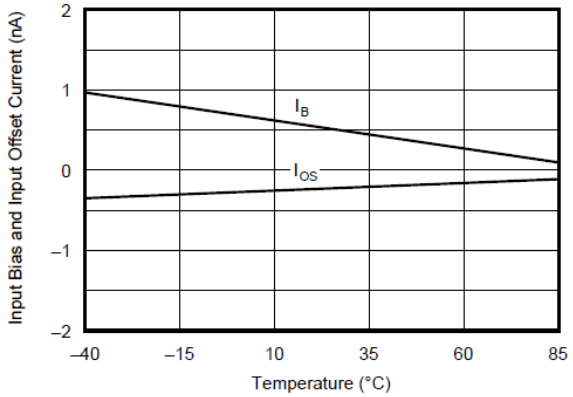


Figure 6-10. Input Bias and Input Offset Current vs Temperature

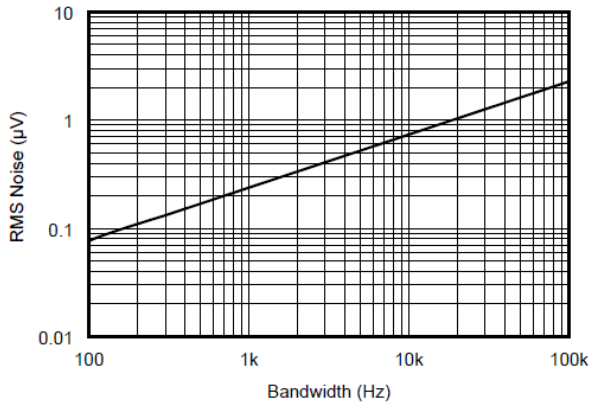


Figure 6-11. Total Noise vs Bandwidth (0.1Hz to Frequency Indicated)

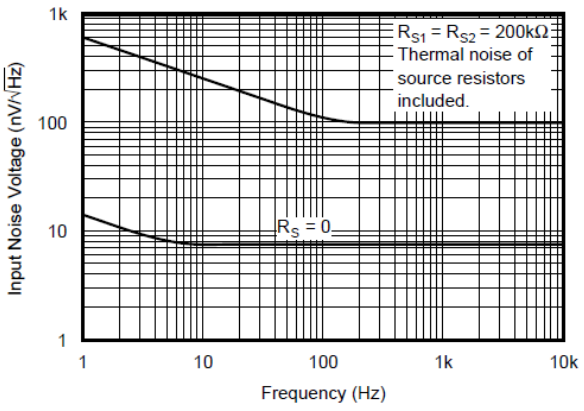


Figure 6-12. Input Noise Voltage Density vs frequency

6.6 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15 V (unless otherwise noted)

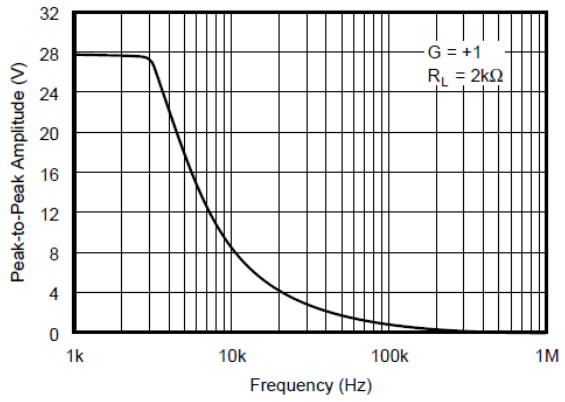


Figure 6-13. Maximum Output Swing vs Frequency

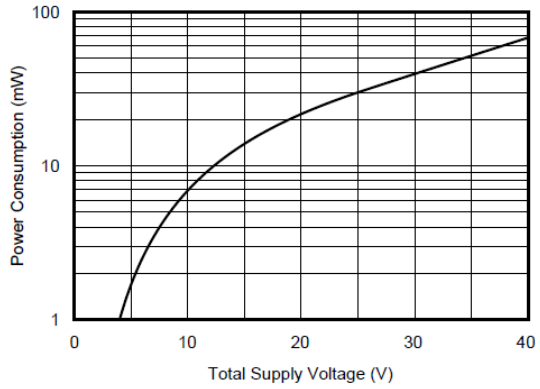


Figure 6-14. Power Consumption vs Power Supply

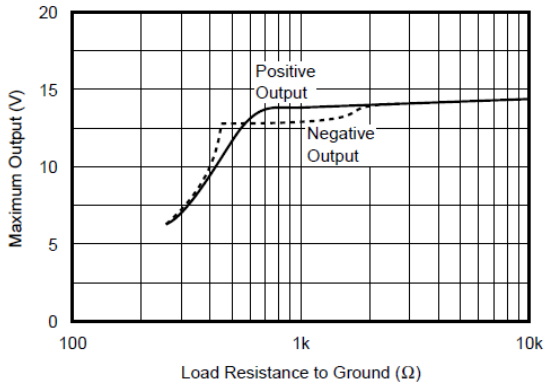


Figure 6-15. Maximum Output Voltage vs Load Resistance

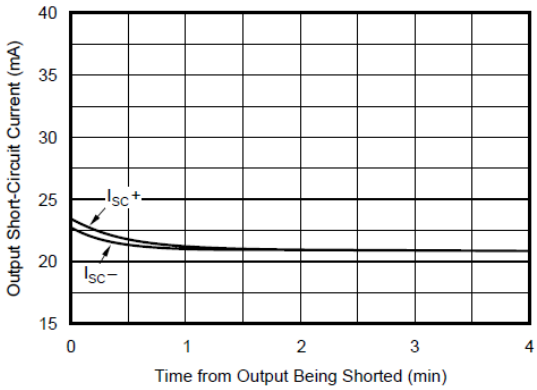


Figure 6-16. Output Short-Circuit Current vs Time

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPA177 is unity-gain stable, making this device easy to use and free from oscillations in the widest range of circuitry. Applications with noisy or high-impedance power-supply lines can require decoupling capacitors close to the device pins. In most cases, 0.1-µF ceramic capacitors are adequate.

The OPA177 has very low offset voltage and drift. To achieve highest performance, optimize circuit layout and mechanical conditions. Offset voltage and drift degrades because of small thermoelectric potentials at the op-amp inputs. Connections of dissimilar metals generate thermal potential that can degrade the ultimate performance of the OPA177. To cancel these thermal potentials, make sure the thermal potentials are equal in both input pins.

1. Keep connections made to the two input pins close together.
2. Locate heat sources as far as possible from the critical input circuitry.
3. Shield the op amp and input circuitry from air currents, such as cooling fans.

7.1.1 Offset Voltage Adjustment

The OPA177 has been laser-trimmed for low offset voltage and drift; therefore, most circuits do not require external adjustment. Figure 7-1 shows the optional connection of an external potentiometer to adjust offset voltage. Do not use this adjustment to compensate for offsets created elsewhere in a system because this adjustment can introduce excessive temperature drift.

7.1.2 Input Protection

The inputs of the OPA177 are protected with 500-Ω series input resistors and diode clamps as shown in the simplified circuit diagram on the front page. The inputs can withstand ±30-V differential inputs without damage. The protection diodes conduct current when the inputs are overdriven. This conducted current can disturb the slewing behavior of unity-gain follower applications, but does not damage the op amp. Some applications, such as programmable logic controllers (PLCs) require a robust input-protection design. An input-protection circuit can be implemented using four Schottky diodes; however, the temperature and voltage dependent leakage of the diodes can present undesirable nonlinear errors at the input. For applications requiring high precision and robust input protection, the OPAx206 family of op amps are an excellent choice, offering integrated input overvoltage protection that eliminates the need for external clamping circuits.

7.1.3 Noise Performance

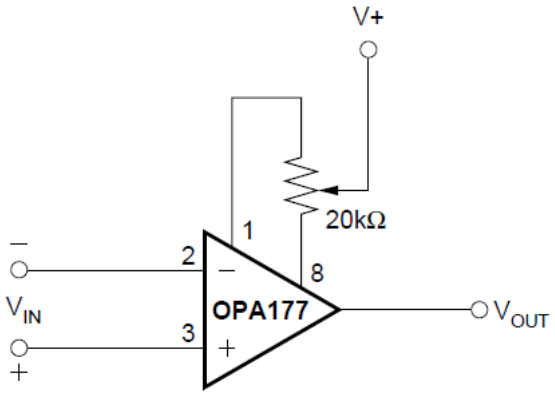
The OPA177 noise performance is optimized for a circuit impedance range of 2 kΩ to 50 kΩ. Total noise in an application is a combination of the op-amp input voltage noise and input bias current noise reacting with circuit impedance. For applications with higher source impedance, the OPAx828 and OPAx140 FET-input op amps generally provide lower noise due to the inherently low input current noise. For low-impedance, low-noise applications, the OPAx210 is an excellent choice because of the exceptionally low op-amp input-voltage noise.

7.1.4 Input Bias Current Cancellation

The input stage base current of the OPA177 is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

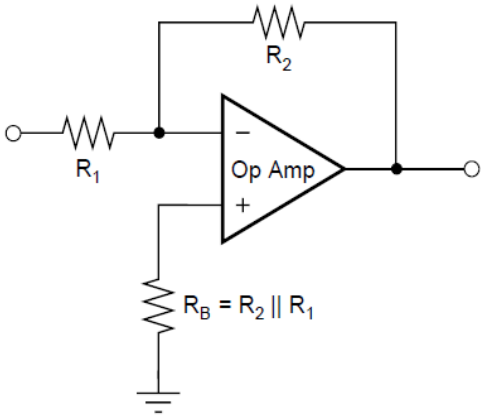
When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, there is no need to balance the dc resistance seen at the two input pins (Figure 7-2 and Figure 7-3). A resistor added to balance the input resistances can actually increase offset and noise.

7.2 Typical Application



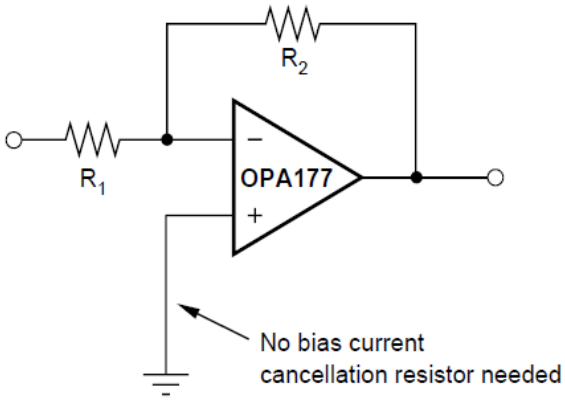
Trim range is approximately ±3.0 mV.

Figure 7-1. Optional Offset Nulling Circuit



Conventional op amp with external bias current cancellation resistor.

Figure 7-2. Input Bias Current Cancellation With Conventional Op Amp



OPA177 with no external bias current cancellation resistor.

Figure 7-3. Input Bias Current Cancellation With OPA177

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Support

8.1.1 Development Support

8.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

8.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

8.1.1.3 DIP-Adapter-EVM

Speed up your op amp prototyping and testing with the DIP-Adapter-EVM, which provides a fast, easy and inexpensive way to interface with small, surface-mount devices. Connect any supported op amp using the included Samtec terminal strips or wire them directly to existing circuits. The DIP-Adapter-EVM kit supports the following industry-standard packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT-23-6, SOT-23-5 and SOT-23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6).

8.1.1.4 DIYAMP-EVM

The DIYAMP-EVM is a unique evaluation module (EVM) that provides real-world amplifier circuits, enabling the user to quickly evaluate design concepts and verify simulations. This EVM is available in three industry-standard packages (SC70, SOT23, and SOIC) and 12 popular amplifier configurations, including amplifiers, filters, stability compensation, and comparator configurations for both single and dual supplies.

8.1.1.5 TI Reference Designs

TI reference designs are analog solutions created by TI's precision analog applications experts. TI reference designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI reference designs are available online at https://www.ti.com/reference-designs.

8.1.1.6 Filter Design Tool

The filter design tool is a simple, powerful, and easy-to-use active filter design program. The filter design tool allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the Design tools and simulation web page, the filter design tool allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA177FP	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		OPA177FP	
OPA177FPG4	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		OPA177FP	
OPA177GP	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA177GP	
OPA177GPG4	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA177GP	
OPA177GS	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR		OPA 177GS	Samples
OPA177GS/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR		OPA 177GS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

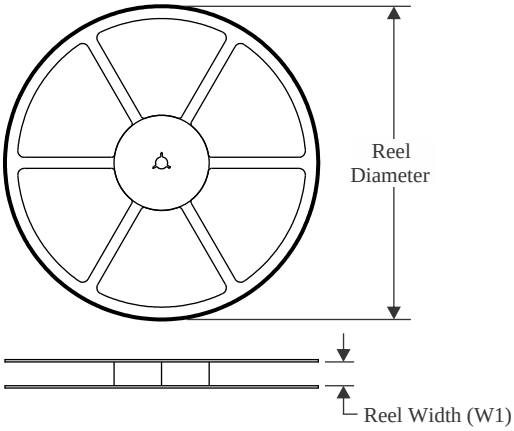
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

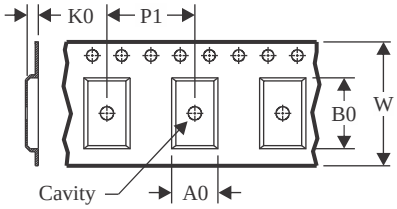
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

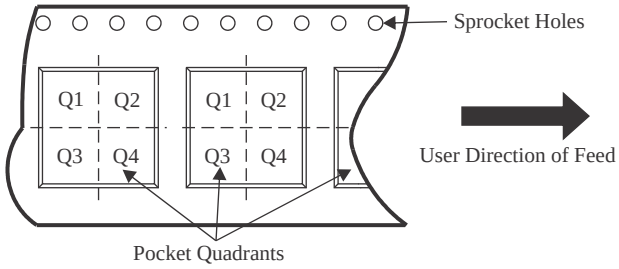


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

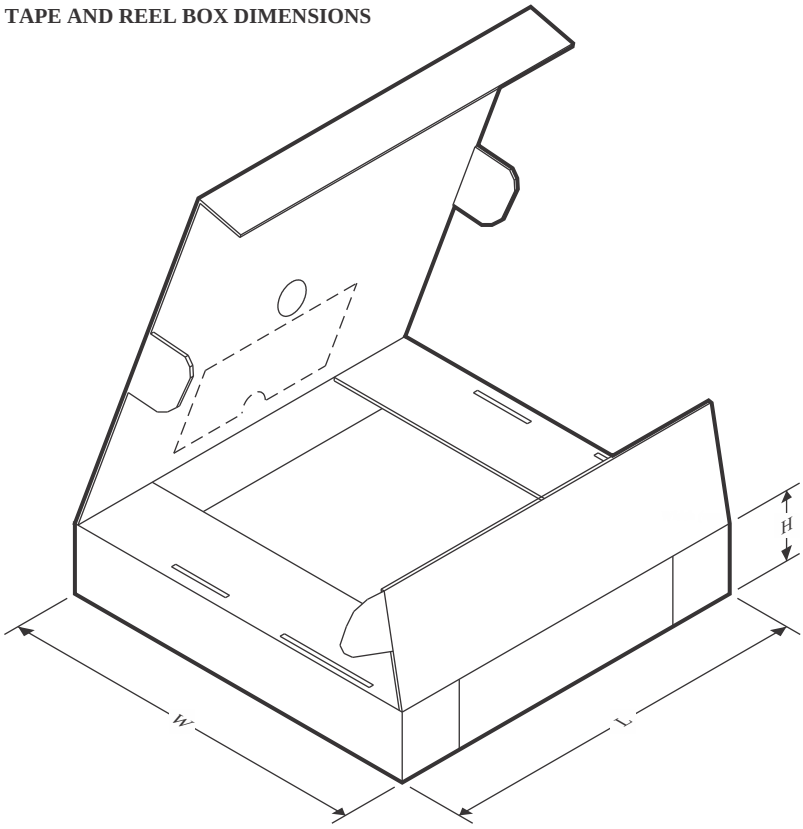
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA177GS/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA177GS/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

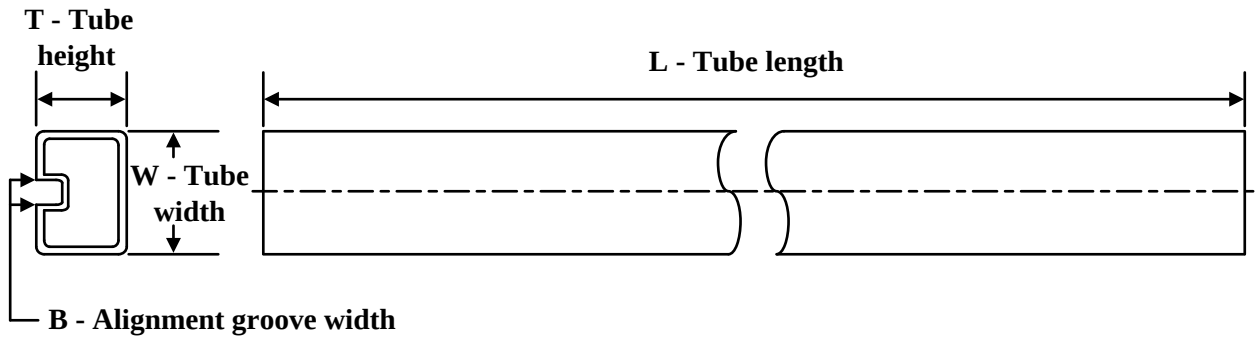
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA177GS/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA177GS/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA177FP	P	PDIP	8	50	506	13.97	11230	4.32
OPA177FPG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA177GP	P	PDIP	8	50	506	13.97	11230	4.32
OPA177GPG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA177GS	D	SOIC	8	75	506.6	8	3940	4.32

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